Study of Sb surface doping and borosilicate glass gate dielectric for 4H-SiC MOSFETs

by

Yongju Zheng

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Approved by

Sarit Dhar, Chair, Associate Professor of Physics
Minseo Park, Professor of Physics
Ayayi Claude Ahyi, Associate Research Professor of Physics
Guofu Niu, Alumni Professor of Electrical and Computer Engineering
Richard C. Jaeger, Professor Emeritus of Electrical and Computer Engineering

Abstract

Silicon carbide (SiC) is a compound material with a wide bandgap, high critical electric field strength, high saturation drift velocity and high thermal conductivity, which makes it an outstanding material among wide bandgap semiconductors for energy efficient power devices. In conjunction with development of high-voltage SiC Schottky barrier Diodes (SBDs), vertical 4H-SiC power metal-oxide-semiconductor field-effect transistors (MOSFETs) has been commercially available since 2010. However, one of the challenges for further development of 4H-SiC power MOSFETs is to improve low channel mobility (μ) and poor oxide reliability attributed to the poor quality SiO_2/SiC interface with high density of interface traps (D_{it}). Nitric oxide (NO) annealing, the standard post oxidation annealing approach for 4H-SiC MOS devices, has improved the channel mobility of 4H-SiC MOSFETs from single digit to ~35 $cm^2/V{\cdot}s$ by passivating interface traps and results in the most reliable gate oxide compared to other interface engineering processes. However, the passivation effect of NO annealing has been shown to be almost saturated due to the competing between nitridation and oxidation reactions during high temperature annealing. Also, a recent research proposed that high temperature NO annealing creates fast interface traps near the 4H-SiC conduction band edge, observed by C-ψ_s analysis. Theses fast traps can response to frequencies higher than the typical high frequencies (100 kHz-1 MHz) used in hi-lo C-V measurements and could be the main limiting factor for channel transport of 4H-SiC MOSFETs. Thus, more effective approaches have to be developed beyond NO annealing to improve the interface quality for next-generation SiC power MOSFETs.

In this work, shallow ion implantations in channel region with antimony (Sb) combined with NO annealing have been investigated on channel transport of 4H-SiC MOSFETs. We found that Sb doping in conjunction with NO annealing improves subthreshold slope (SS) as well as channel mobility (~1.5x) of 4H-SiC MOSFETs compared with standard NO annealing. Threshold voltage decreases with Sb doping due to the compensation of the p-type acceptors in the surface region by Sb donors. Electrical characterization shows the primary effect of Sb is counter-doping rather than trap passivation, which well explains why the improvement of channel mobility by Sb doping is only obvious at low oxide fields, where Coulomb scattering is dominant.

We also employed borosilicate glass (BSG) formed by planar diffusion source annealing and PECVD as the gate dielectric for 4H-SiC MOSFETs. We demonstrated an improved channel mobility over a wide range of transverse electric fields with a peak value of 140 $cm^2/V \cdot s$ (4x higher than by NO annealing) by using BSG due to the effective reduction of fast interface trap density. The correlation between B concentration at the interface of BSG/4H-SiC and electrical results indicates that D_{it} decreases with increasing B concentration. In return, higher B concentration results in higher channel mobility. We also observed a best μ-V_{th} trade-off by using the combination of Sb implantation with BSG gate dielectric, which is a promising process for utilizing on SiC power MOSFETs.

We have performed Hall effect measurements on 4H-SiC Hall bar MOSFETs to accurately estimate free carrier concentration and carrier mobility in the inversion layer of 4H-SiC MOSFETs. The results help better understand the mechanisms of different scattering effects on carrier mobility with various interfacial chemical configurations by NO annealing, combination of Sb doping and NO annealing, and BSG gate dielectric.

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Chapter 1

Introduction

1.1 Power electronics and wide bandgap semiconductors

Development of semiconductor materials and devices has been driving the innovations in modern society since the inventions of germanium (Ge)-based bipolar transistors in 1947-1948 [1, 2] and silicon (Si)-based metal-oxide-semiconductor field effect transistors (MOSFET) in 1959 [3]. With continuous technological advance on semiconductor devices, our society is increasingly dependent upon electrical appliances. From the energy efficiency's point of view, various demands for power electronics have been extremely extended, where Si-based power devices is relatively mature and hard to achieve further breakthroughs due to its physical properties [4]. The world average ratio of electrical energy consumption to total energy consumption is ~20% in 2010. Current technology has improved the efficiency to 85%-95% while ~10% of electric power is lost as heat [4]. Therefore, reduce power consumption and dissipation during power conversion is still a basic problem, which can be realized by power electronics by means of cost-effective and efficient delivery.

Power electronics is designed to regulate and convert electric power to supply in the form of voltage conversion (AC-DC, DC-DC, DC-AC) and frequency conversion (AC-AC) [5]. High-performance power devices can be realized by wide bandgap materials allowing devices to operate at much higher voltages, frequencies and temperatures as either bipolar power devices such as insulated gate bipolar transistor (IGBT) or unipolar power devices such as MOSFETs as inverters or converters. However, unipolar power devices are more and more commonly used than bipolar power devices due to the significant power losses during on and off-state switching on bipolar devices caused by minority carrier removal via electron-hole recombination [6].

Fig.1.1.1 (a) [6] shows the structure of commercially available D-MOSFETs with a "planar-gate", p-base region, n^+ source and drain regions and n-drift region. The n-type channel is defined as the junction difference between n^+ source and p-base region under gate electrode. The drift region is designed to block voltage across p-base/n-drift region junctions when the drain is

applied with positive voltage. The capability of voltage blocking is determined by the doping concentration and thickness of the n-drift region. Compared to SiC MOSFETs, the drift region resistance of Si power MOSFETs increases dramatically with increasing blocking voltage, which limits the performance of silicon power MOSFETs to block voltages below 200 V [6]. The resistance of an ideal drift region is related to the material properties of the semiconductor. In an ideal drift region with a uniform doping for MOSFETs, as shown in Fig.1.1.1 (b) [6], the distribution of electric field is a triangular based on the solution of Poisson's equation. The

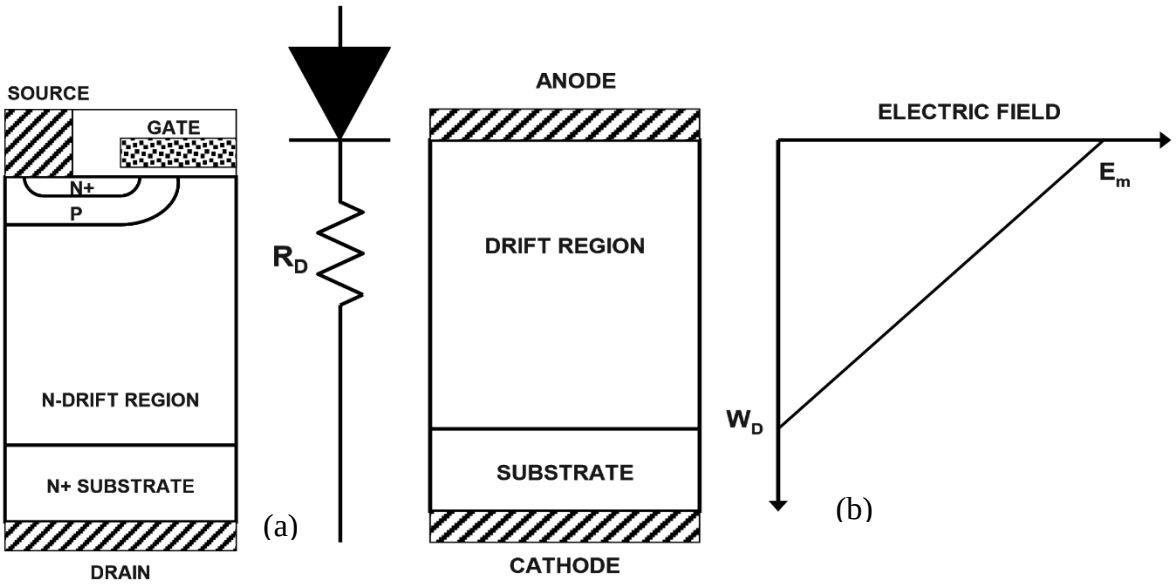

Fig.1.1.1. (a) Structure of commercially available D-MOSFETs; (b) The ideal drift region and its electric field distribution [6].

maximum voltage supported by the drift region is determined by the maximum electric field (E_m) when it reaches the critical electric field (E_c). Then the maximum depletion width (W_D) is determined by the E_c and the doping concentration of the drift region.

The specific resistance of the ideal drift region is given by:

$$R_{on.sp} = \frac{W_D}{q\mu_n N_D} \tag{1.1}$$

The depletion width under breakdown conditions is given by:

$$W_D = \frac{2BV}{E_c} \tag{1.2}$$

where BV is the breakdown voltage. Then the required doping concentration of the drift region to obtain BV is:

$$N_D = \frac{\varepsilon_s E_c^2}{2qBV} \tag{1.3}$$

Thus, the specific resistance of the ideal drift region is given by:

$$R_{on.sp} = \frac{4BV^2}{\varepsilon_s \mu_n E_c^3} \tag{1.4}$$

The denominator of this equation $\varepsilon_s \mu_n E_c^3$ refers to the well-known Baliga figure of merit (BFOM) for power field-effect transistors, derived by B. Baliga in 1982 [7] to define material properties for minimizing the conduction losses in power devices and achieve high efficiencies. The dependence of the drift region resistance on the mobility favors semiconductors with high mobilities such as GaAs. However, compared to Si, the strong dependence of the on-resistance on the critical electric field at the same breakdown voltage makes wide band gap semiconductors much more promising for power devices applications. Some material parameters of the candidate semiconductors for

Table 1-1. Material properties of candidate semiconductors for power devices

Properties	Si	4H-SiC	GaAs	GaN
Crystal Structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy Gap : E_G (eV)	1.12	3.26	1.43	3.5
Electron Mobility : μ_n (cm^2/Vs)	1400	900	8500	1250
Hole Mobility : μ_p (cm^2/Vs)	600	100	400	200
Breakdown Field : E_B (V/cm) X10^6	0.3	3	0.4	3
Thermal Conductivity (W/cm°C)	1.5	4.9	0.5	1.3
Saturation Drift Velocity : v_s (cm/s) X10^7	1	2.7	2	2.7
Relative Dielectric Constamt : ε_S	11.8	9.7	12.8	9.5

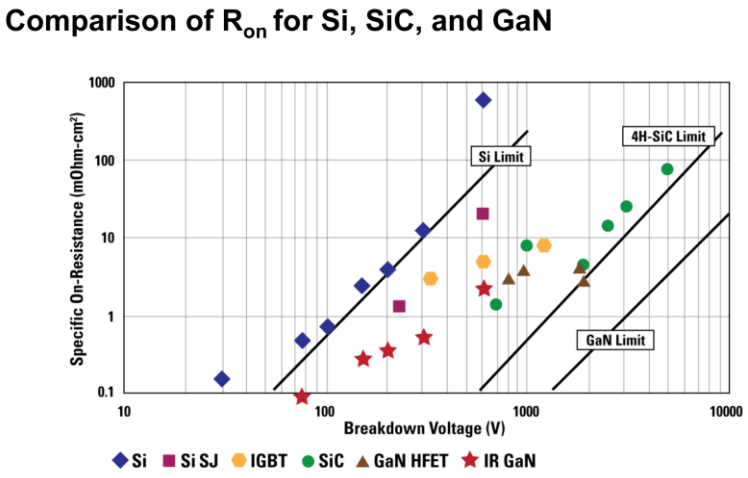

Fig.1.1.2. Comparison of the theoretical $R_{on.sp}$ as a function of breakdown voltage for Si, 4H-SiC and GaN [8].

power devices as well as the on-resistance as a function of breakdown voltage are shown in Table 1-1 and Fig.1.1.2 [8].

1.2 Physical properties of SiC and promise of SiC power devices

SiC is a compound semiconductor with 50% silicon (Si) and 50% carbon (C). Both Si and C atoms are tetravalent elements and have four valence electrons in their outermost shells. Si and C atoms are tetrahedrally bonded with covalent bonds by sharing electron pairs in sp^3-hybrid orbitals with a very high bond energy of 4.6 eV [9] to form a SiC crystal.

SiC is the best-known example of polytypism [9-12], where a material can adopt different crystal structures varying in stacking sequence without changes in chemical composition. In principle, only one stacking structure (often either the zincblende or wurtzite structure) is usually stable for most materials. However, SiC crystallizes in surprisingly more than 200 stable polytypes, each of which exhibits unique material properties. Polytypes are represented by the number of Si-C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal and R for rhombohedral). The structures of popular SiC polytypes of 3C-SiC, 4H-SiC and 6H-SiC are shown in Fig.1.2.1 [9]. Here, A, B, and C are the potentially occupied sites in a hexagonal close-packed structure. Thus, 3C-SiC is described by the repeating sequence of ABC, 4H- and 6H-SiC

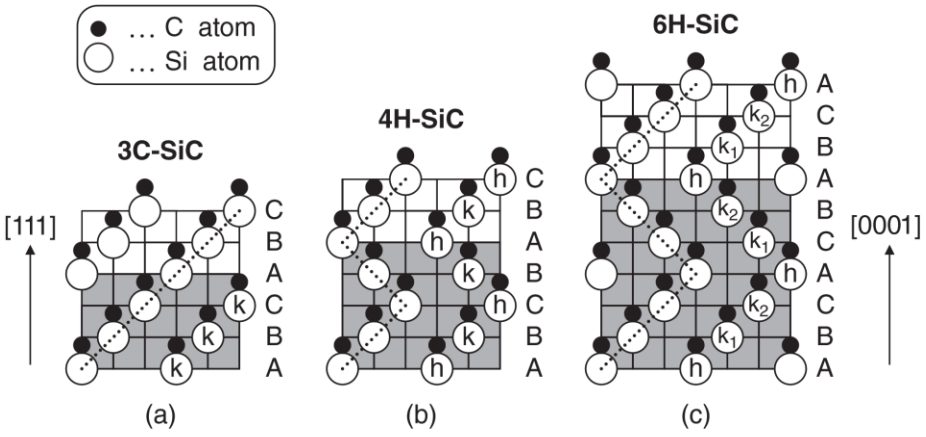

Fig.1.2.1. Schematic structures of popular SiC polytypes: (a) 3C-SiC, (b) 4H-SiC, and (c) 6H-SiC. Open and closed circles denote Si and C atoms, respectively [9].

can be described by ABCB and ABCACB, respectively. The primitive cells and fundamental translation vectors of cubic and hexagonal SiC are shown in Fig.1.2.2.

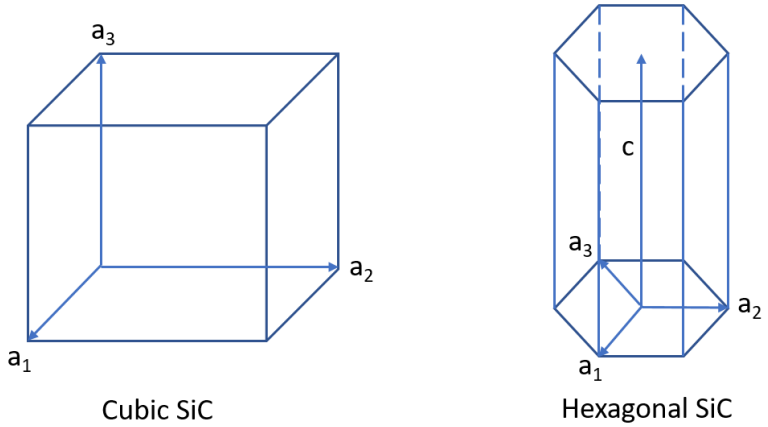

Fig.1.2.2. The primitive cells and fundamental translation vectors of cubic and hexagonal SiC.

The stability and nucleation probability of SiC polytypes depend strongly on temperature [13]. 3C-SiC can be transformed into hexagonal SiC polytypes such as 6H-SiC above 1900-2000°C [14]. Thus, 4H-SiC and 6H-SiC are the most popular polytypes due to their stability. 3C-SiC is another popular polytype even if it is not stable at very high temperature because 3C-SiC can be grown heteroepitaxially on Si substrates [15-17].

Table 1-2 summarizes the major physical properties of 3C-SiC, 4H-SiC and 6H-SiC polytypes. The bandgap at room temperature is 2.36 eV for 3C-SiC, 3.26 eV for 4H-SiC and 3.02 eV for 6H-SiC and it decreases with increasing temperature because of thermal expansion [18]. The electron mobility of 4H-SiC is almost double that of 6H-SiC at a given dopant density and the hole mobility is also slightly higher than 6H-SiC. Also, the mobility anisotropy is relatively small in 4H-SiC, where the electron mobility along the c-axis direction is ~20% higher than that perpendicular to the c-axis. This is one of the major reasons why 4H-SiC is the most attractive polytype for vertical power devices fabricated on Si-face (0001) of SiC wafers. The in-plane mobility anisotropy on various faces of 4H-SiC also has been studied [19-21]. The results demonstrated that mobility anisotropy on Si-face (0001) is negligible while mobility ratio of perpendicular/parallel to c-axis on a-face $(11\bar{2}0)$ is ~0.8 [19]. Although the critical electric field of 6H-SiC (0001) is slightly higher than that of 4H-SiC (0001), it exhibits strong anisotropy in carrier transport [22, 23] with low electron mobility along the (0001) and the critical field strength

of (1120) is only half that of (0001). Owing to the high critical field strength and high electron mobility along the c-axis, 4H-SiC exhibits a significantly higher BFOM than other SiC polytypes. Another advantage of 4H-SiC is that it has slightly smaller donor and acceptor ionization energies compared with those of other SiC polytypes [9]. Furthermore, the availability of single-crystalline 4H-SiC (0001) wafers with large diameters and good quality has driven development of 4H-SiC-based power devices. The characteristics of commercial 4H-SiC power devices have already outperformed the theoretical limits of 3C- and 6H-SiC unipolar devices. All the advantages above make 4H-SiC very attractive for power device applications [24].

Table 1-2. Major physical properties of 3C-, 4H-, and 6H-SiC polytypes at room temperature.

Properties/polytype	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	2.36	3.26	3.02
Electron mobility perpendicular to c-axis (cm^2/Vs)	1000	1020	450
Electron mobility parallel to c-axis (cm^2/Vs)	1000	1200	100
Hole mobility (cm^2/Vs)	100	120	100
Electron saturated drift velocity (cm/s)	~$2x10^7$	$2.2x10^7$	$1.9x10^7$
Hole saturated drift velocity (cm/s)	~$1.3x10^7$	~$1.3x10^7$	~$1.3x10^7$
Breakdown electric field perpendicular to c-axis (MV/cm)	1.4	2.2	1.7
Breakdown electric field parallel to c-axis (MV/cm)	1.4	2.8	3.0
Relative dielectric constant ε_s perpendicular to c-axis	9.72	9.76	9.66
Relative dielectric constant ε_s parallel to c-axis	9.72	10.32	10.03
BFOM (n-type, parallel to c-axis) normalized by that of Si	61	626	63
BFOM (p-type, parallel to c-axis) normalized by that of Si	2	25	19

1.3 SiC MOS interface challenges

A unique advantage of SiC is that it is the only compound semiconductor that can be thermally oxidized to give high-quality SiO_2 for the fabrication of power devices compared to other wide bandgap materials. However, in oxides grown on SiC, the release of excess carbon occurs during thermal oxidation, which is the limiting factor for obtaining good SiC/SiO_2

interfaces [25]. Although other high-κ dielectrics, such as Al_2O_3, AlN, Si_3N_4 and HfO_2 have been evaluated with better potential to reduce electric field in gate dielectric with equal thickness and also obtain a better threshold voltage stability [26], thermal oxides are still the most commonly utilized gate dielectrics in SiC MOS technology. In spite of continuous improvement of interface, the quality and the understanding of the factors controlling this quality are still far from a satisfactory level.

The thermal oxidation mechanisms of Si have been widely studied by Deal-Grove model [27]. The difference from Si oxidation to SiC oxidation is the carbon release process. The C emission process related to the SiC/SiO_2 interface has been studied with various models [25, 28-30] and it has been claimed that the release of excess carbon occurs during oxidation mainly as molecular CO [31]. Some other researches suggest the removal of C atoms is in form of CO_2 at the initial stage of oxidation and then CO as the SiO_2 layer grows [32]. In general form, the oxidation reaction on SiC is expressed as [33]

$$SiC + \frac{3}{2}O_2 \rightarrow SiO_2 + CO \qquad (1.5)$$

Taking into account the Si density in SiC, the amount consumed Si during thermal oxidation of SiC can be calculated as 46%, close to the value of thermal oxidation of Si. The oxidation process has also been demonstrated with ball-and-stick models at an abrupt SiC-oxide interface, as shown

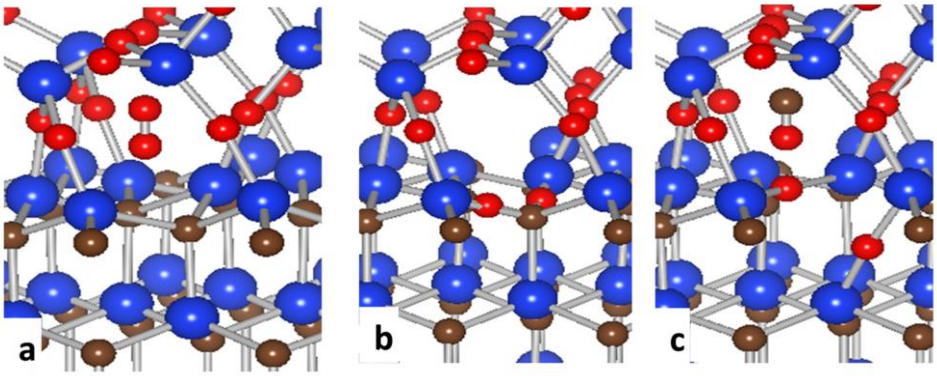

Fig.1.3.1. The oxidation of SiC with ball-and-stick models [31].

in Fig.1.3.1 [31]. The blue balls are Si atoms, brown balls are carbon atoms, and red balls are oxygen. O_2 molecule first inserts in the SiC/SiO_2 interface with O-O bonds and then breaks apart at interface to form stronger Si-O and C-O bonds with a CO molecule emitted leaving behind Si-

O-Si bonds. The computation of binding energies of CO in SiO_2 and CO in SiC suggests CO molecules are more likely to diffuse into the SiO_2 instead of into SiC and then be released from the surface, as is indeed observed [34].

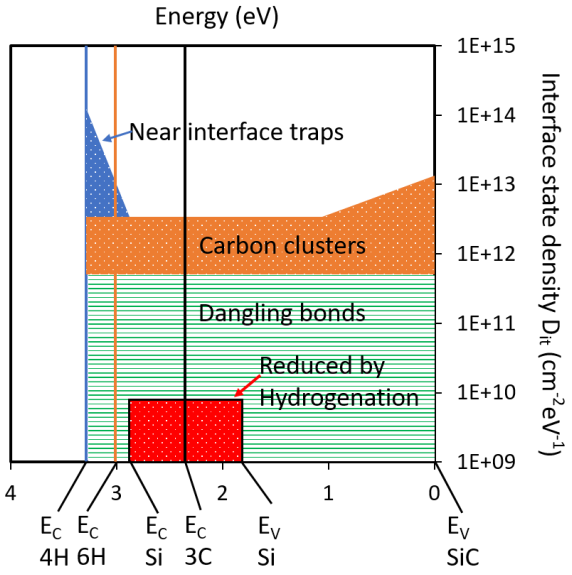

Fig.1.3.2. The distribution of D_{it} inside the bandgaps of various SiC polytypes compared to Si.

It is believed that the thermal oxide is not free of carbon due to incomplete CO ejection, which causes several types of defects in the form of C cluster and C interstitials near the interface of SiC/SiO_2 [26]. Oxygen vacancies, Si dangling bands and Si interstitials also exist after thermal oxidation. Although the exact origins of these defects are still not very well understood, a rough interface state distribution has been revealed [9]. Fig.1.3.2 shows the interface state distribution inside of the bandgaps of various SiC polytypes compared with Si. The D_{it} distribution seems to be common for all SiC polytypes. D_{it} distribution near the conduction band edge depends on the location of the conduction band bottom for each polytype. As discussed in chapter 2, the interface states near the conduction band edge are mostly acceptor-like and negatively charged when trapping electrons below the Fermi level. The trapped electrons act as negative fixed charges. The donor-like traps located in the lower half of the bandgap are positively charged by trapping holes above Fermi level. Holes trapped by donor-like traps, especially those located in the deep energy region, behave as positive fixed charges. For 4H-SiC, D_{it} increases almost exponentially toward the conduction band edge [35, 36]. In 4H-SiC n-channel MOSFETs, electrons are trapped in

inversion layer during on-state and act as Coulomb scattering centers, causing very low channel mobility, usually ~5-8 $cm^2/V \cdot s$ without any post oxidation treatments [9].

1.4 Processes of interface engineering

1.4.1. Interface nitridation

To obtain high-quality MOS interfaces of SiO_2/SiC, various interface engineering has been processed. Post-oxidation annealing (POA) is one of the crucial methods to passivate interface traps. In Si technology, the interface state density can be reduced to 10^9 cm^{-2} eV^{-1} by hydrogen passivation of dangling bonds [37, 38]. In the case of SiC, the essential problem at the interface is totally different since the effect of the same hydrogen annealing process on D_{it} is very small. One promising POA process to reduce D_{it} in SiC MOS interface is nitridation by using nitrogen-containing gas, such as nitric oxide (NO) [39-41], nitrous oxide (N_2O) [42, 43] or ammonia (NH_3) [44, 45].

NO annealing at high temperature (1100°C) was first reported by H. Li *et al*. on SiO_2/6H-SiC interface. It reveals that nitrogen only covers the interface during NO annealing, which reduces D_{it} by a factor of ~10. Then NO annealing was applied on SiO_2/4H-SiC, demonstrated by G. Y. Chung *et al*., showing an improvement of field-effect mobility from single digit to ~30-35 $cm^2/V \cdot s$. N_2O annealing is also found to be significantly effective on D_{it} reduction. However, it is not as efficient as NO due to the competing reactions between undesired byproducts created by the

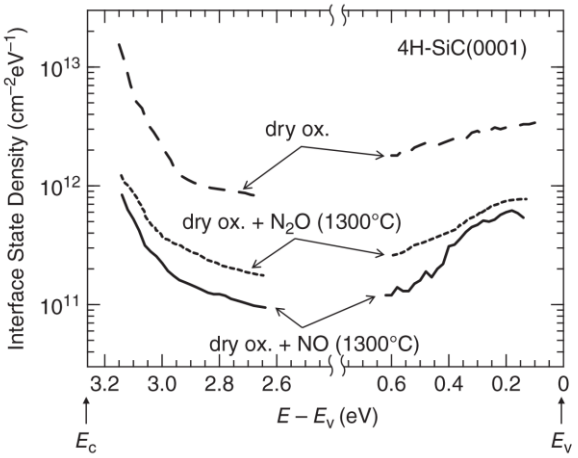

Fig.1.4.1. D_{it} distribution inside the bandgap of 4H-SiC by NO and N_2O annealing obtained from n- and p-type capacitors [9].

decomposition of N_2O in gas phase into NO, N_2 and O_2 at high temperature. Fig.1.4.1 [9] shows the comparison of D_{it} distribution inside the bandgap of 4H-SiC by NO and N_2O annealing obtained from n- and p-type capacitors. The results show that relatively high temperatures (1250-1300°C) are required to achieve effective nitridation effects by N_2O. Thus, the nitridation must be processed not by N_2O itself but by NO created by N_2O at high temperature.

NH_3 annealing was first demonstrated on MOS capacitors with deposited SiO_2 and it was found to be effective on the reduction of both effective oxide charges and interface states on n-type 4H-SiC capacitors with nitrogen distributing throughout the oxide layer. However, the oxide strength has been shown to be deteriorated by nitrogen distribution causing high leakage current. Nowadays, interface nitridation by NO annealing is still the most widely employed in industry for mass production of SiC power MOSFETs as well as in academic research.

Correlation between the nitrogen coverage at the interface, NO annealing time and interface trap density as well as the field-effect mobility has been studied by several groups [46-49]. Fig.1.4.2 (a) [48] shows the nitrogen density incorporated at the interface increase with NO annealing (1175°C) time and it reaches the maximum value of ~$6x10^{14}/cm^2$ with 2 hour NO annealing. The peak mobility increases as the charged interface trap density decreases with higher coverage of nitrogen, as shown in Fig.1.4.2 (b) [49].

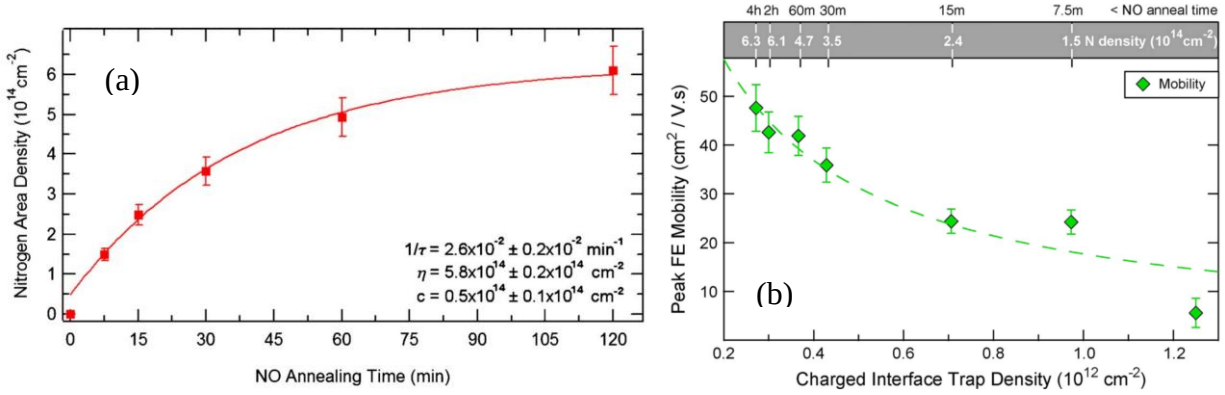

Fig.1.4.2. (a) N density as a function of NO annealing time [48]; (b) Peak field-effect mobility as a function of NO annealing time, yield various densities of interface states [49].

However, it has been reported that NO annealing at high temperature creates a high density of very fast interface states near the conduction band edge [50], as shown in Fig.1.4.3 [50]. Here the D_{it} was extracted by C-ψ_s analysis. Compared to high-low C-V characterization, C-ψ_s analysis allows the detection of very fast states with emission times shorter than typical practical

measurement frequencies (1 MHz). This method will be discussed in the following chapters. Fig.1.4.3 shows the D_{it} profiles at 0.3 eV as a function of nitrogen density near the interface of SiO_2/4H-SiC annealed by NO at different temperatures (1150°C-1350°C). It can be seen the density of very fast traps almost proportionally increases with nitrogen density. The lowest D_{it} is obtained by NO annealing at 1250°C for 70 mins. It has also been found that nitridation process causes not only reduction of D_{it} near the conduction band edge but also increases hole traps in deep energy level [48]. Therefore, excessive nitridation is not desirable.

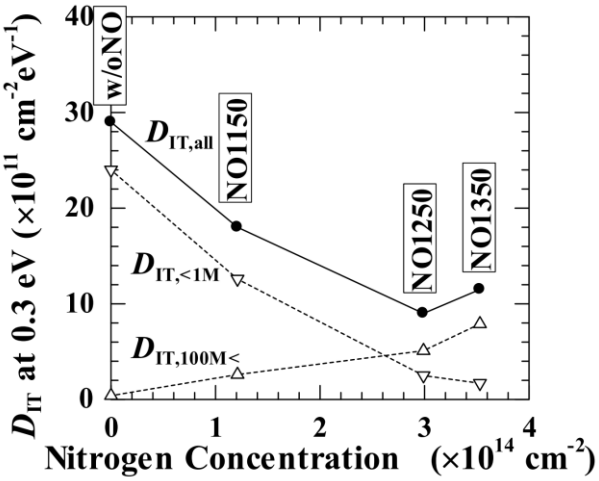

Fig.1.4.3. D_{it} distribution as a function of nitrogen density near the interface of SiO_2/4H-SiC annealed by NO at different temperatures [50].

1.4.2 Phosphosilicate glass (PSG) and borosilicate glass (BSG)

Significant reduction of interface state density and improvement of channel mobility can be also realized by post-oxidation annealing with phosphoryl chloride ($POCl_3$) [51, 52]. High channel mobility of 89 cm^2/V·s has been obtained by $POCl_3$ annealing at 1000°C for 10 mins and further improvement of mobility up to ~120 cm^2/V·s has been achieved by two-step annealing in $POCl_3$ for 4H-SiC (0001) MOSFETs [53, 54]. In the annealing process, SiO_2 is converted into phosphosilicate glass (PSG) and phosphorus are almost uniformly distributed inside the gate oxide after the annealing. The correlation of interface trap density and P coverage at the interface has been studied by changing annealing temperature. Fig.1.4.4 (a) [54] shows the Phosphorus coverage at the interface of SiC and in PSG bulk as a function of $POCl_3$ annealing temperature. The results indicate that the P incorporation both at the PSG/SiC interface and in the bulk decreases as

annealing temperature increases in the range of 900-1100°C. In return, similar to NO annealing, the lowest D_{it} occurs at annealing temperature of 900°C yield the highest P coverage, as shown in Fig.1.4.4 (b) [54].

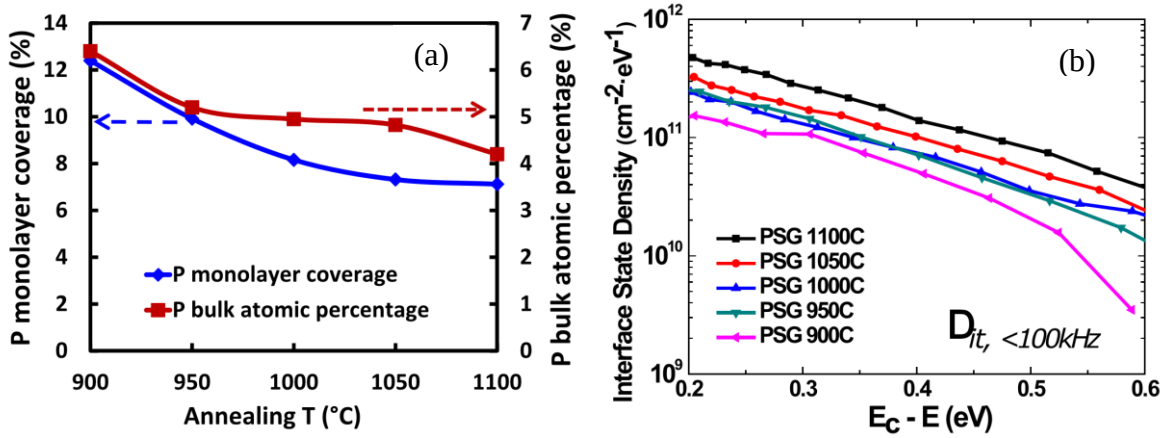

Fig.1.4.4. (a) Phosphorus coverage at the interface and in PSG bulk as a function of $POCl_3$ annealing temperature [54]; (b) Interface trap density (slower than 100kHz) of five MOS capacitors with different interface phosphorus coverage [54].

However, PSG has been proved to be a polarizable material and can therefore lead to threshold voltage instability. The threshold voltage shifts to left when applying positive bias temperature stress on PSG gated 4H-SiC n-channel MOSFETs due to the presence of polarization charges [54, 55]. It was found that the oxide traps in phosphorus-doped oxides are the main origin of the threshold voltage instability via the capture of electrons [55].

Borosilicate glass (BSG) as gate dielectric for 4H-SiC MOSFETs was first reported by Okamoto *et al*. [56, 57]. By post oxidation annealing using boron nitride (BN) planar diffusion source, a low interface trap density as well as a high channel mobility of ~100 $cm^2/V{\cdot}s$ has been obtained compared with NO annealing, as shown in Fig.1.4.5 [56, 57]. Similar to PSG, BSG is formed by the conversion of SiO_2 during B annealing. The B atoms were found to be distributed uniformly in the oxide at a concentration and then accumulated at the interface at a higher concentration by secondary ion mass spectrometry SIMS [56]. The mechanism of B annealing for low interface trap density and high channel mobility has been suggested to be stress relaxation of SiO_2 by B doping [56]. It also has been reported that a significant improvement of the electrical forward characteristics of VDMOS was realized by a stack oxide layer with thermal oxide treated by boron diffusion and deposited TEOS oxide [58]. Also, a relatively good threshold voltage

stability under both positive and negative bias stress at room temperature with B annealed oxide has been achieved by the same group [59]. However, threshold voltage stability with high temperature bias stress has not been widely studied.

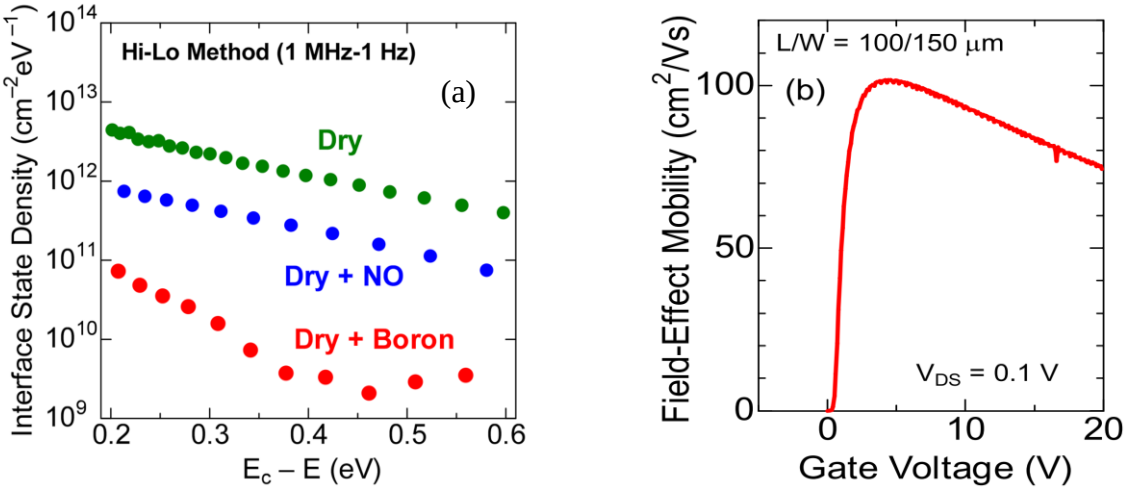

Fig.1.4.5. (a) D_{it} distributions of 4H-SiC n-type capacitors with dry, NO annealed, and B annealed oxides [57]; (b) Field-effect mobility of 4H-SiC MOSFETs fabricated with the B diffusion process [56].

1.4.3 Metals

Another technique to enhance the channel mobility is "sodium-contaminated" oxidation [60, 61]. A high channel mobility of 120-150 cm^2/V·s for 4H-SiC (0001) MOSFETs has been achieved by using an Al_2O_3 tube for gate oxidation, where the oxidation rate was accelerated in this Na-contaminated oxidation. Similar results were also realized by dipping SiC samples in Na-containing solutions prior to normal oxidation in a clean furnace, reported by Das *et al*. [62]. The mechanism of the mobility enhancement can be explained by that the presence of sodium during oxidation increases the oxidation rate and suppresses the formation of near interface traps. This technique cannot be employed for manufacturing of power MOSFETs due to the poor device stability from the mobile ion effect. The sodium ions can move in the gate oxide at typical operating temperatures and gate biases. Fig.1.4.6 [63] shows the change of device's mobilities before and after bias temperature stress. The change of the shape of mobility curves as well as the shift of the threshold voltage indicates very poor device stability. However, it is still worth investigating it to acquire important insights into mobility limiting factors.

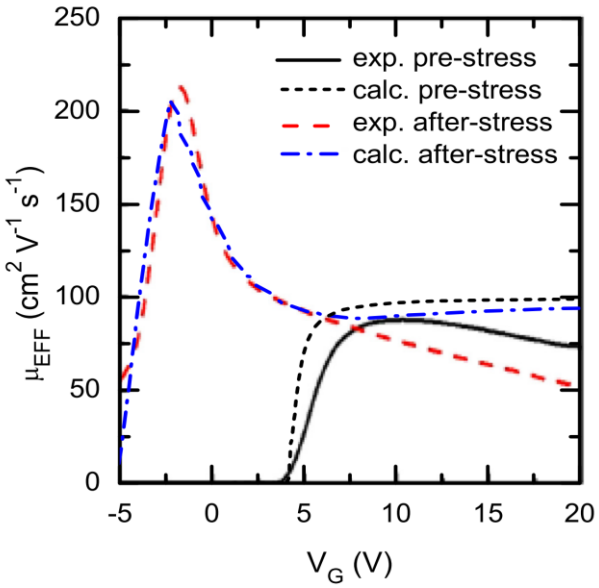

Fig.1.4.6. The change of mobility curves of the device with sodium incorporation pre- and after stress [63].

Recently, the effect of atoms in group I (alkali elements Rb and Cs) and group II (alkaline earth elements Ca, Sr, and Ba) on channel mobility of 4H-SiC MOSFETs was investigated by D. Lichtenwalner *et al.* [64]. They evaporated a very thin interface layer (~0.6-0.8 nm) of these metal materials by molecular beam epitaxy (MBE) in an ultra-high vacuum and then stack with ~30 nm

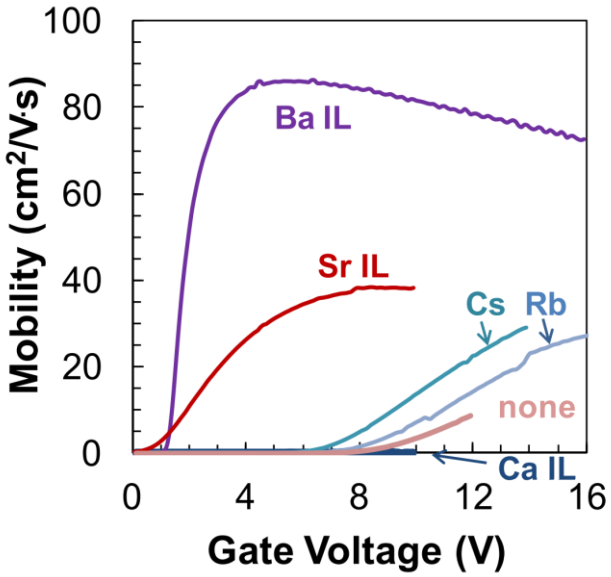

Fig.1.4.7. Field-effect mobility for 4H-SiC MOSFETs processed with Rb, Cs, Ca, Sr and Ba interface layers compared to an unpassivated thermal oxide [64].

deposited SiO_2 followed by a PDA in O_2 and N_2. Fig.1.4.7 [64] shows the field-effect mobility for 4H-SiC MOSFETs processed with Rb, Cs, Ca, Sr and Ba interface layers compared to an unpassivated thermal oxide. The peak mobility of devices with Rb and Cs is above 25 $cm^2/V{\cdot}s$ with stretched out curves indicating high D_{it}. A peak mobility of ~40 $cm^2/V{\cdot}s$ is obtained by Sr and with Ba the peak mobility is further improved to 85 $cm^2/V{\cdot}s$. The sharp turn-on with Ba interlayer indicates lower interface traps. This is consistent with the results of lower D_{it} extracted by high-low C-V on the companion n-type capacitors as well as the good threshold stability under positive and negative bias temperature stress of ± 2 MV/cm, as shown in Fig.1.4.8 [64]. The results demonstrate that Ba, as a larger ionic radii element, is likely less mobile and more strongly bonded. It is also possible that Ba acts like donor-like states.

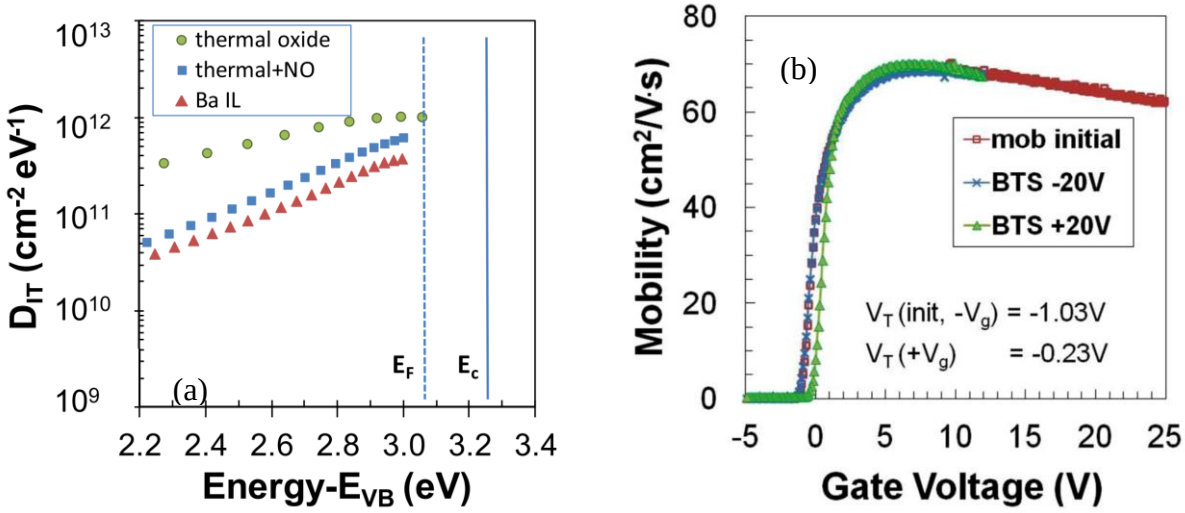

Fig.1.4.8. (a) D_{it} extracted from the high-low C-V of nMOS capacitors with Ba interlayer, without passivation and NO annealing [64]; (b) Field-effect mobility before and after BTS stress with ± 2 MV/cm at 175°C for 15 min [64].

1.4.4 Counter-doping

Counter-doping refers to carrier concentration enhancement for n-channel MOSFETs in strong inversion by n-type dopants. As group-V elements, nitrogen and phosphorous have been confirmed to have doping effect in addition to the passivation effect at the interface of SiO_2/4H-SiC, reported by P. Fiorenza *et al*. [65]. In their study, a nanoscale characterization approach using scanning capacitance microscopy (SCM) on the cross section of MOS structures was performed to determine the electrically active N and P concentration below the SiO_2 after N_2O or $POCl_3$

annealing. Fig.1.4.9 (a) and (b) [65] show the schematic SCM analysis on the MOS cross section. As can be seen in Fig.1.4.9 (c), compared to "as oxidized" sample, the active doping concentration increased from the value of the epilayer doping of the "as oxidized" ($5x10^{15}/cm^3$) up to $5x10^{17}/cm^3$ for the N_2O annealed sample and $4.5x10^{18}/cm^3$ for the $POCl_3$ annealed sample, respectively. The higher active doping concentration of P indicates that P is more likely acting as dopants than N.

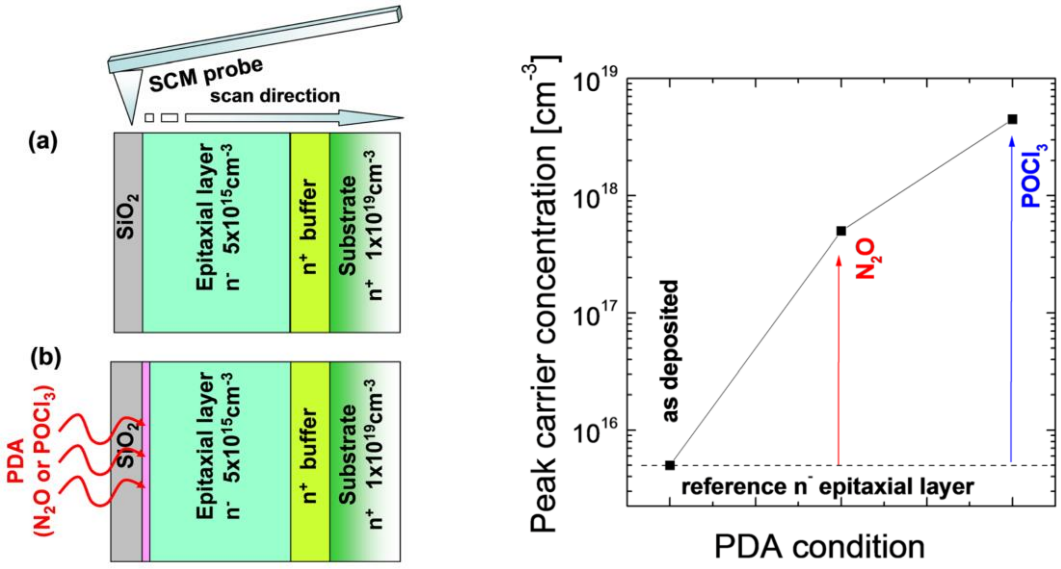

Fig.1.4.9. Schematic of the cross section of a MOS capacitor on 4H-SiC epitaxial samples, (a) before and (b) after the annealing [65]; (c) Peak carrier concentration below the SiO_2 layer for the as deposited sample in N_2O annealed and $POCl_3$ annealed samples [65].

Counter-doping effect by ion implantation of nitrogen in the SiC channel was first reported by K. Ueno *et al*. [66]. It was identified that the channel mobility increases as the interfacial nitrogen density increases and the threshold voltage decreases due to more free carriers in channel region.

Modic *et al*. [67] reported that a surface counter-doping layer around 10 nm deep in channel region by antimony (Sb) combining with NO annealing improves channel mobility to ~110 $cm^2/V{\cdot}s$. The n-type Sb dopants provide higher electron density in the channel, which results in higher transconductance as well as lower carrier scattering at low electric fields. Unlike N and P, interface trap passivation effects observed in the Sb surface counter-doping process are minimal and the primary effect of Sb is found to be counter-doping the p-type SiC surface [68]. The threshold voltage stability of Sb implanted device is as good as NO annealed device under the

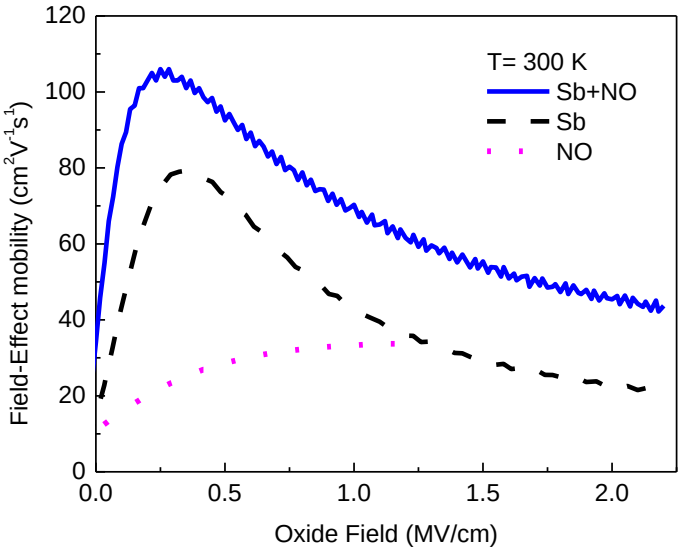

Fig.1.4.10. Field-effect mobility of 4H-SiC MOSFETs with NO annealing, Sb implantation and 'Sb+NO' processes [67].

same bias condition [68]. However, this process does not improve the field-effect mobility at high transverse fields compared to standard NO annealing, which was also observed in nitrogen implantation process [66], as depicted in Fig.1.4.10 [67]. At low electric fields, Coulomb scattering is the dominant limiting factor and it strongly depends on free carrier density. While it has little effect at high field due to the dominance of surface roughness scattering in this regime.

1.4.5 Oxidation process

The mobility enhancement methods discussed in previous sections all involve adding other elements to the SiO_2/SiC interface region. It has long been a goal to directly grow a defect-free interface by thermal oxidation without post-oxidation treatments. The oxidation condition has been proved to be critical to the oxidation kinetics as well as the distribution of interface states in SiC MOS structures [69] and therefore, the oxidation process is believed to be able to be optimized by changing oxidation condition (dry/wet, fast/slow, temperature) to achieve high-quality oxide and interface. In 2006, Kurimoto *et al*. reported that the interface trap density and the products generated during oxidation process depends on the thermal oxidation temperature [70]. Recently, Kikuchi and Kita observed a D_{it} lower than 10^{11} $cm^{-2}eV^{-1}$ for the energy range of 0.1-0.4 eV below the conduction band as well as a good device stability by raising the oxidation temperature to 1300°C with a short temperature rise/fall time followed by O_2 annealing [71], as shown in

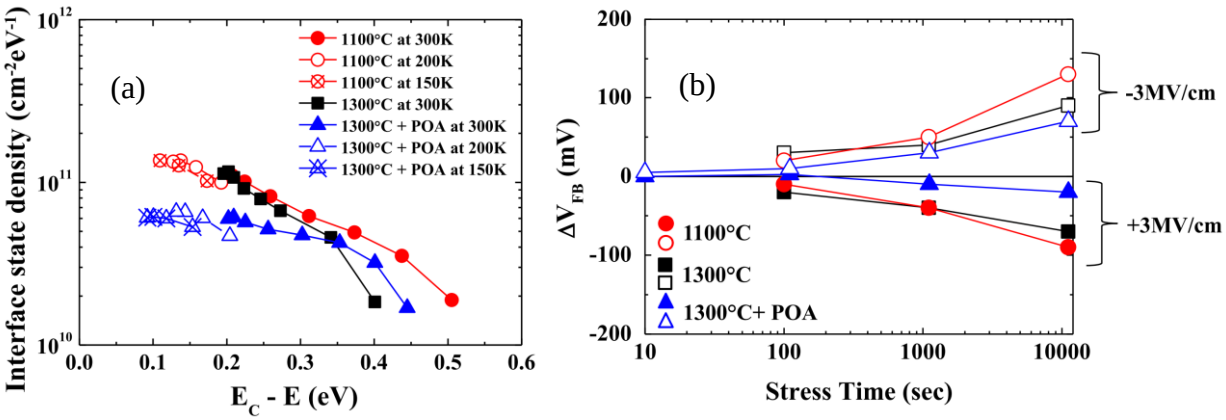

Fig.1.4.11. (a) Interface state density as a function of energy level below the conduction band [71]; (b) Flatband voltage shifts of C-V curves of MOS capacitors by the application of constant electrical stress ± 3 MV/cm at room temperature [71].

Fig.1.4.11 [71]. In another study, an improved channel mobility of 40 $cm^2/V{\cdot}s$ was reported by Thomas *et al*. [72] using an oxidation temperature of 1500°C without post oxidation annealing. However, the device was normally on. They suggest the improvement of channel mobility was caused by the reduction of carbon precipitation at high temperature [72]. Some other studies suggest that high temperature oxidation enhances interstitial C injection into SiC, which could potentially result in higher amount of scattering centers as well as traps in the SiC inversion channel [73]. More work is needed to understand mechanisms for mobility improvement by high temperature oxidation.

1.4.6 Crystal faces

The distributions and densities of interface states are very different when different crystal faces are employed in SiO_2/SiC interfaces. Other than (0001) Si-face of 4H-SiC, which has been commercially available due to the high critical field strength and high electron mobility, the polar $(000\bar{1})$ C-face and other non-polar faces, such as the $(11\bar{2}0)$ a-face and the $(1\bar{1}00)$ m-face also have been widely studied. Fig.1.4.12 shows the crystal faces in 4H-SiC. Due to the difference of surface atomic structure from face to face, the distribution of interface states near the conduction band edge is striking different under the same oxidation condition. Fig.1.4.13 [9] shows the D_{it} distribution obtained from n-type SiC capacitors with Si-face, C-face, a-face and m-face from dry and wet oxidation without POA. The results indicate D_{it} on Si-face is not very sensitive to the

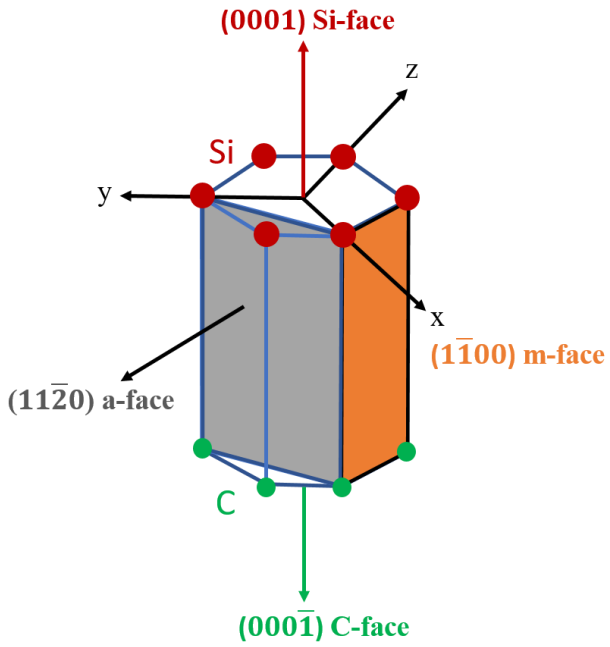

Fig.1.4.12. Crystal faces in 4H-SiC. The Si-face is terminated by Si atoms (large red balls) and C-face by C atoms (small green balls).

oxidation conditions (dry/wet) while D_{it} is much higher with dry oxidation than with wet oxidation on other faces. Also, D_{it} distribution is less sharp toward the conduction band edge on other faces than on Si-face. The dependence of D_{it} on crystal face has also been studied with pyrogenic

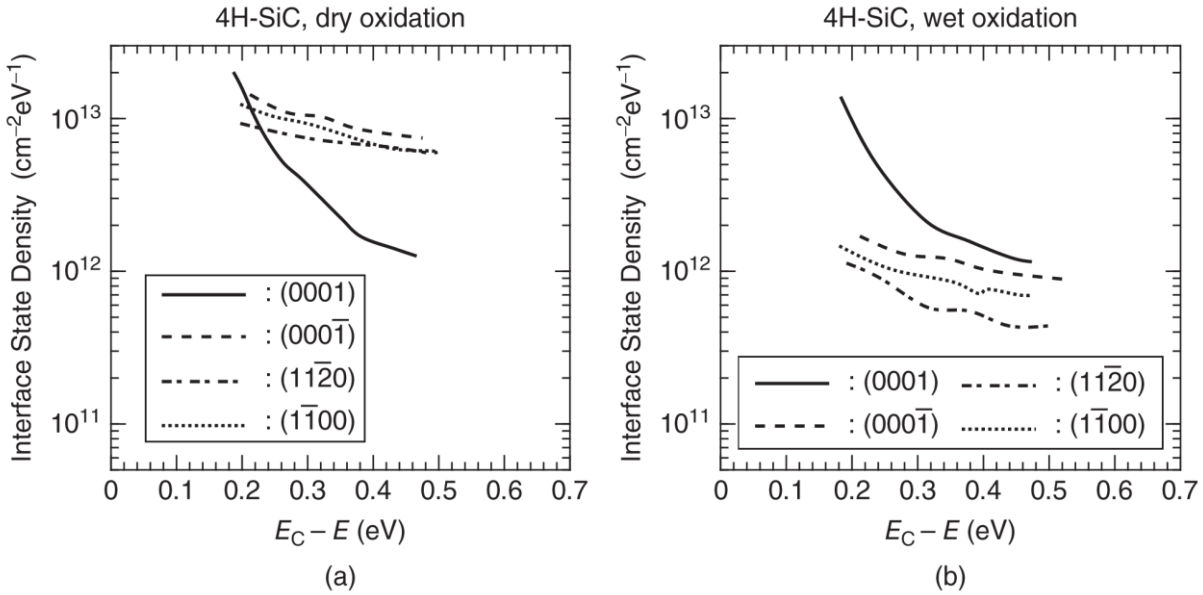

Fig.1.4.13. Interface state density distributions obtained from n-type 4H-SiC (0001), (000$\bar{1}$), (11$\bar{2}$0), and (1$\bar{1}$00) MOS structures prepared by (a) dry and (b) wet oxidation [9].

oxidation [74]. The result reveals a lower D_{it} on a-face and C-face than on Si face by pyrogenic oxidation. Liu *et al*. [75] reported that the oxides formed on a-face and C-face absorb more hydrogen at the interface than on Si-face after exposed to water, which is consistent with the lower D_{it} obtained by pyrogenic oxidation in [74].

The significantly improved high channel mobility has been achieved on non-Si face devices, which makes them an alternative solution to the low mobility on Si-face. Fig 1.4.14 [9] shows the field-effect mobility as a function of the gate voltage of n-channel MOSFETs fabricated on (0001), $(000\bar{1})$, $(11\bar{2}0)$, and $(1\bar{1}00)$ faces [9, 76]. All the devices were annealed in NO (10%)/N_2 (90%) atmosphere at 1250°C after dry oxidation. The channel mobility is 46 $cm^2/V{\cdot}s$ on C-face and ~115 $cm^2/V{\cdot}s$ on a-face and m-face. The high mobility obtained on a-face and m-face is very promising for development of SiC trench MOSFETs [77, 78]. It has been suggested that the reason for the higher mobility in the non-polar face MOSFETs is the significantly lower fast trap density compared to the Si-face [79].

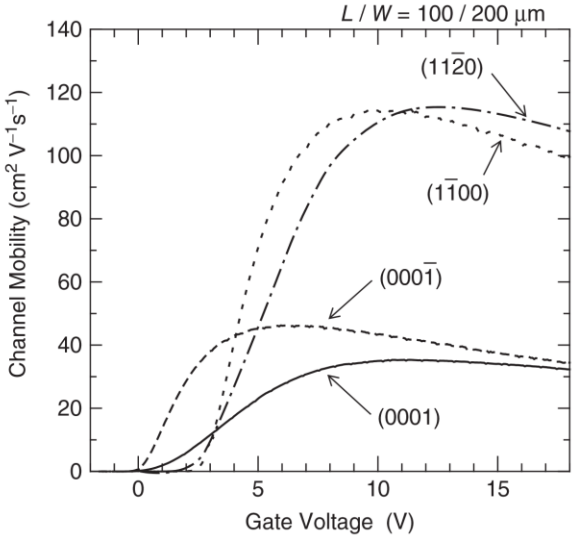

Fig.1.4.14. Field-effect mobility obtained from 4H-SiC MOSFETs on (0001), $(000\bar{1})$, $(11\bar{2}0)$, and $(1\bar{1}00)$ annealed in NO/N_2 [9].

1.5 Motivation of Sb doping and BSG gate dielectric for 4H-SiC MOSFETs in this study

As discussed above, channel mobility has been significantly improved by shallow Sb counter-doping in channel region combining with NO annealing on the lightly doped p-well

(~10^{16}/cm^3) 4H-SiC MOSFETs with good device stability. For SiC power MOSFETs with heavily doped p-wells (above 10^{17}/cm^3), low channel mobility and poor subthreshold slope are still challenges for further development. It is very promising to utilize this approach to improve the device performance of SiC power MOSFETs from the perspective of channel mobility and device stability.

A low interface trap density and a high channel mobility for a wide range of surface transverse electric fields have been reported by using BSG as gate dielectric for 4H-SiC MOSFETs. The mechanism of B diffusion for the improvement of interface and high channel mobility has been suggested to be stress relaxation of SiO_2 by B doping. But the exact mechanism is not clear. Also, the threshold voltage stability with high temperature bias stress has not been widely studied although a relatively good threshold voltage stability at room temperature has been reported. Thus, more study is needed to understand the mechanism of B treatment on thermal oxide to utilize the attractive properties of BSG on SiC power MOSFETs.

The main motivation of this thesis work is to: (1) Investigate the effect of Sb counter-doping with various doping doses combined with NO annealing on the electrical characteristics of 4H-SiC MOSFETs with heavily doped p-wells; (2) Study the impact of BSG gate dielectric on channel transport and understand the correlation between B concentration at the interface and electrical properties of 4H-SiC MOSFETs; (3) Better understand the channel mobility limiting factors with Sb counter-doping and BSG gate dielectric compared to NO annealing.

1.6 Thesis outline

In chapter 2, a broad introduction of the fundamentals of MOS devices and the several characterization methods to estimate interface traps as well as various channel mobilities used for channel transport will be described.

Chapter 3 describes the doping process for both Sb implantation and heavy p-well doping in channel region and provides detailed analysis of the impact of Sb counter-doping combining with NO annealing on channel transport of 4H-SiC MOSFETs.

Chapter 4 discusses the processes used for the BSG formation as well as the characterization on physical B concentration and the electrical properties on BSG-gated MOS devices.

Chapter 5 introduces Hall effect measurements to estimate the free carrier density and the true carrier mobility with various interface configurations. The discussion of carrier mobility limiting factors with various interface configurations is provided.

Chapter 6 is the conclusion and some suggestions on future work regarding this thesis work discussed in previous chapters.

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Chapter 2

MOS interface physics and characterization

2.1 MOS fundamentals

As the basic structure of metal-oxide-semiconductor field-effect transistor (MOSFET), which constitutes the important gate-channel-substrate structure of the MOSFET, two-terminal MOS structure has been extensively studied over years for detailed understanding of semiconductor surface [1]. Since most of the reliability and stability issues on MOS devices are intimately related to the surface conditions of semiconductors, it is critical to understand the physics of semiconductor surface for the development of better fabrication methods, which address these practical problems and make MOS transistors with high performance [2, 3].

The fabrication techniques have been focusing on n-channel (p-substrate) MOS field-effect transistor for years due to its advantages of higher electron mobility than hole mobility as well as lower cost, higher current capability and easier control characteristics [4]. In this chapter, we will discuss the operation principle of two-terminal p-type MOS capacitor and four-terminal n-channel MOSFET.

2.1.1 P-type MOS capacitor

A MOS capacitor structure and the equivalent circuit are shown in Fig.2.1.1 and Fig.2.1.2. The MOS capacitor is composed of a metal plate, an insulating layer and a semiconductor layer. The metal plate is either a metal layer or a heavily doped poly-silicon layer which behaves as a

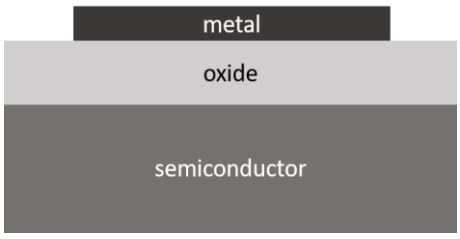

Fig.2.1.1. The schematic of MOS capacitor structure.

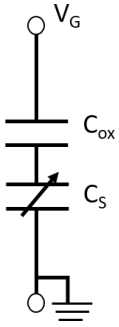

Fig.2.1.2. The equivalent circuit of total C of MOS capacitor.

metal as gate contact. The insulating layer is silicon dioxide and the semiconductor layer, in our case is uniformly doped p-type silicon as body. The total capacitance C of the MOS system is the series capacitance of oxide capacitance C_{ox} and semiconductor capacitance C_s. The field effect is implanted by a voltage applied on the gate, which controls the surface potential as well as the charge distribution and semiconductor capacitance in the semiconductor. Ideally, the oxide is a perfect insulator with zero current flowing under gate bias and no oxide charge centers near the interface between the oxide and semiconductor. The relationship between gate voltage (V_G), surface potential (ψ_s) and space charge density in semiconductor will be discussed in different regimes by energy band diagram and space charge diagram under the ideal case in this section.

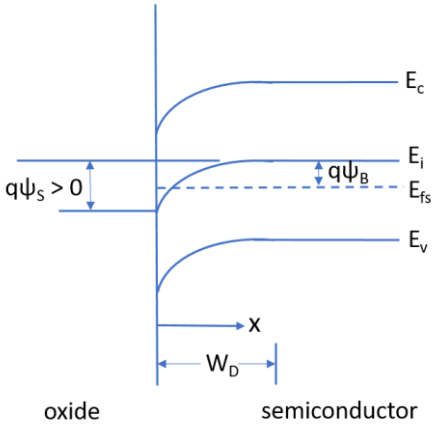

Fig.2.1.3. Energy band diagram at the surface of a p-type semiconductor.

Fig.2.1.3 shows the energy band diagram at the surface of a p-type semiconductor. The potential in the semiconductor is defined as

$$\psi(x) = -\frac{E_i(x) - E_i(\infty)}{q} \tag{2.1}$$

where $\psi(0) \equiv \psi_s$. The electron and hole concentration as a function of ψ are given by

$$n_p(x) = n_{p0} \exp\left(\frac{q\psi}{kT}\right) = n_{p0} \exp(\beta\psi) \tag{2.2}$$

$$p_p(x) = p_{p0} \exp\left(\frac{-q\psi}{kT}\right) = p_{p0} \exp(-\beta\psi) \tag{2.3}$$

where n_{p0} and p_{p0} are the equilibrium densities of electrons and holes, k is the Boltzmann constant. Therefore, the electron and hole densities at the surface can be written as

$$n_p(0) = n_{p0} \exp\left(\frac{q\psi_s}{kT}\right) = n_{p0} \exp(\beta\psi_s) \tag{2.4}$$

$$p_p(0) = p_{p0} \exp\left(\frac{-q\psi_s}{kT}\right) = p_{p0} \exp(-\beta\psi_s) \tag{2.5}$$

By applying one-dimensional Poisson equation,

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_s} \tag{2.6}$$

where ρ(x) is the total space charge density, ε_s is the dielectric permittivity of semiconductor, the electric field at the surface as a function of surface potential can be obtained as [2]

$$E_s = \pm\frac{\sqrt{2}kT}{qL_D}\sqrt{[\exp(-\beta\psi_s) + \beta\psi_s - 1] + \exp(-2\beta\psi_B)\,[\exp(\beta\psi_s) - \beta\psi_s - 1]} \tag{2.7}$$

where $L_D \equiv \sqrt{\frac{kT\varepsilon_s}{N_A q^2}}$, is the extrinsic Debye length of holes and ψ_B is the bulk potential. The space charge density Q_s as a function of surface potential ψ_s can be derived by Gauss' law [2],

$$Q_s = -\varepsilon_s E_s = \mp\frac{\sqrt{2}\varepsilon_s kT}{qL_D}\sqrt{[\exp(-\beta\psi_s) + \beta\psi_s - 1] + \exp(-2\beta\psi_B)\,[\exp(\beta\psi_s) - \beta\psi_s - 1]} \tag{2.8}$$

Fig.2.1.4 [2] shows the space charge density as a function of the surface potential for a p-type silicon with $N_A = 4\text{x}10^{15}$ cm^{-3}.

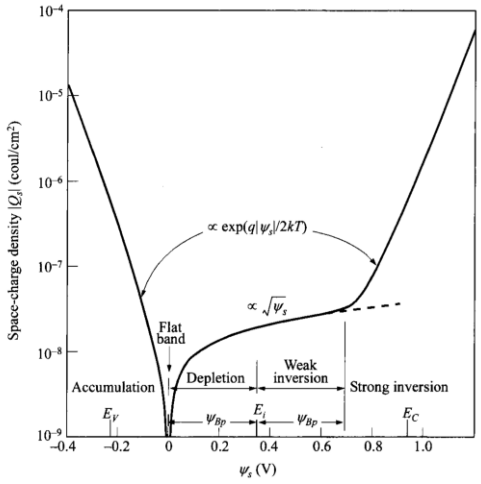

Fig.2.1.4. Space charge density in the semiconductor as a function of the surface potential, for a p-type silicon with $N_A = 4\text{x}10^{15}$ cm^{-3} at room temperature [2].

According Fig.2.1.2, the total capacitance and the semiconductor capacitance can be written as [2]

$$C = \frac{1}{1/C_{ox} + 1/C_s} \tag{2.9}$$

$$C_s = \frac{\varepsilon_s}{\sqrt{2}L_D} \frac{1 - \exp(-\beta\psi_s) + \exp(-2\beta\psi_B)[\exp(\beta\psi_s) - 1]}{\sqrt{[\exp(-\beta\psi_s) + \beta\psi_s - 1] + \exp(-2\beta\psi_B)\,[\exp(\beta\psi_s) - \beta\psi_s - 1]}} \tag{2.10}$$

Thermal equilibrium

In the MOS system, the Fermi energy is considered to be constant throughout the metal, the oxide and the silicon in thermal equilibrium. This is realized by the transfer of negative charge from the materials with higher Fermi level to the materials with lower Fermi level, which results in a thin sheet of positive charges at the surface of the metal and negative charges at the surface of semiconductor side as well as a voltage drop on two sides of oxide called built-in voltage. Fig.2.1.5 shows the energy levels of three separated materials and the energy band diagram at thermal equilibrium when they form a MOS system. The vacuum level is continuous with position when materials are separated. The electron affinities and work functions are defined by the difference of energy level between vacuum level and conduction band edge E_C and Fermi level, respectively.

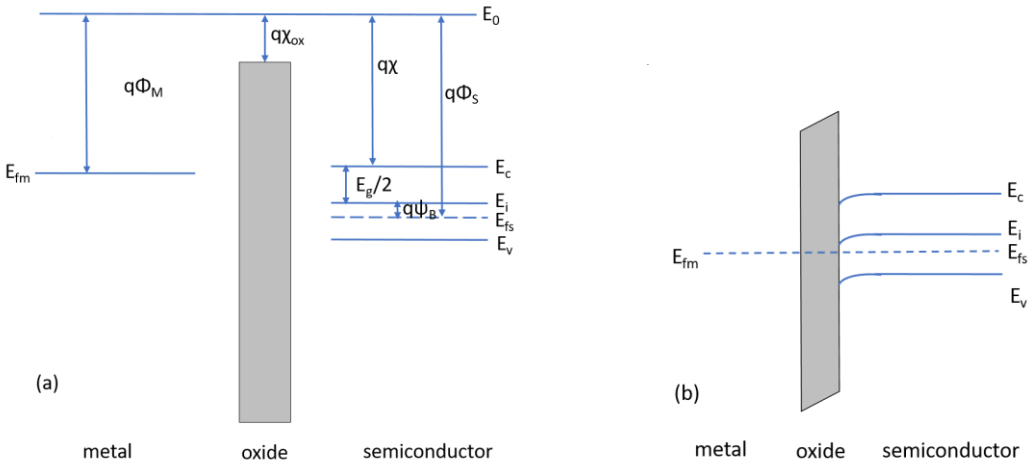

Fig.2.1.5. (a) Energy levels in three separated materials and (b) Energy band diagram at thermal equilibrium for an MOS system.

Flat-band

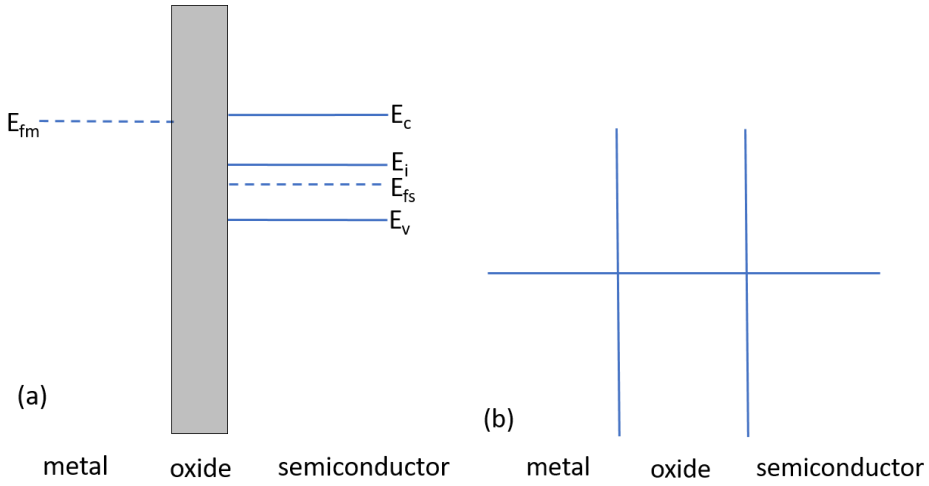

Fig.2.1.6. (a) Energy band diagram and (b) Charge distribution of MOS system at flat-band condition.

When the applied voltage that exactly compensates the built-in voltage, the energy band diagram in the semiconductor becomes flat, in return, the surface potential ψ_s is zero and the stored charge is reduced to zero as well. This applied voltage is called flat-band voltage V_{FB}, given by

$$V_{FB}^0 = \Phi_M - \Phi_S \equiv \Phi_{MS} \tag{2.11}$$

where Φ_M is the metal work function and Φ_S is the semiconductor work function. Fig.2.1.6 shows the energy band diagram and charge distribution at flat-band voltage V_{FB}. We have

$$V_G = V_{FB} \tag{2.12}$$

$$Q_s = 0 \tag{2.13}$$

$$\psi_s = 0 \tag{2.14}$$

At flat-band state, the system is not in equilibrium therefore the Fermi level is not constant in metal and semiconductor. Based on Eq.2.9 and Eq.2.10, the semiconductor capacitance and the total capacitance of the system can be obtained as

$$C_{s,FB} = \frac{\varepsilon_s}{L_D} = \sqrt{\frac{\varepsilon_s q^2 N_A}{kT}} \tag{2.15}$$

$$C_{FB} = \frac{1}{1/C_{ox} + L_D/\varepsilon_s} \tag{2.16}$$

The flat-band voltage is an important parameter since it influences the threshold voltage of a MOSFET. In addition, the variation between ideal case and the experimental value is a measure of defects, oxide traps and interface traps near the interface of oxide and semiconductor [2].

Accumulation

When the gate voltage decreases below V_{FB}, holes will accumulate at the surface of the semiconductor to produce a net positive charge Q_s with greater density than the doping concentration N_A. This will cause the same amount of negative charge $Q_G = -Q_s$ on the metal side to balance the system. This condition is called surface accumulation and is illustrated in Fig.2.1.7.

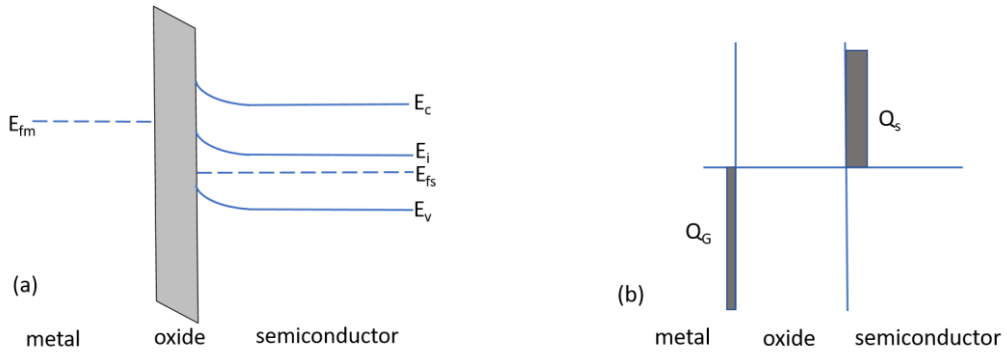

Fig.2.1.7. (a) Energy band diagram and (b) Charge distribution of MOS system at surface accumulation.

At accumulation, we have

$$V_G < V_{FB} \tag{2.17}$$

$$Q_s > 0 \tag{2.18}$$

$$\psi_s < 0 \tag{2.19}$$

Since Q_s is positive and ψ_s is negative, the surface charge density will be dominated by the first term in Eq.2.8, that is,

$$Q_s \approx \frac{\sqrt{2}\varepsilon_s kT}{qL_D}\sqrt{\exp(-\beta\psi_s)} \tag{2.20}$$

Depletion

When the gate voltage is above flat-band voltage, the positive charge at the surface of semiconductor will be moved away leaving behind the negative-charged acceptor core ions. Correspondingly, the positive charges on the metal side increases. This condition is called surface depletion due to the behavior of semiconductor surface charge. The energy band diagram and the

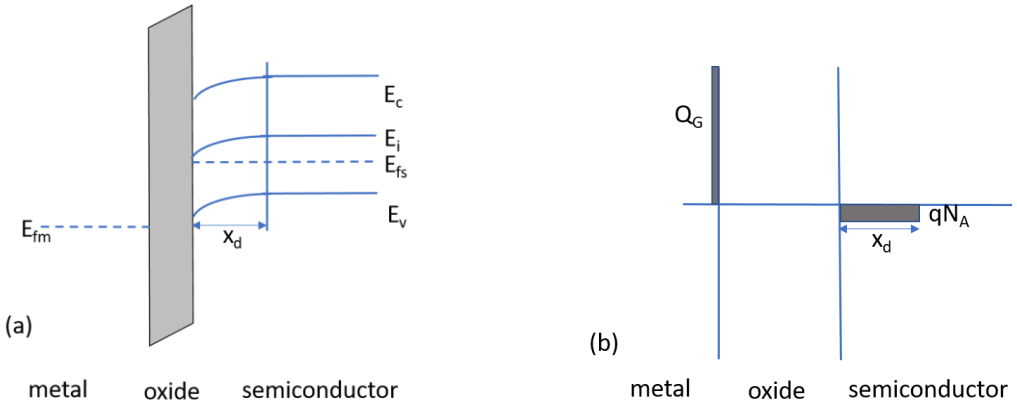

Fig.2.1.8. (a) Energy band diagram and (b) Charge distribution of MOS system at depletion.

charge configuration are sketched in Fig.2.1.8. The depletion layer width further increases with increasing gate voltage. At depletion, we have

$$V_G > V_{FB} \tag{2.21}$$

$$Q_s < 0 \tag{2.22}$$

$$\psi_B > \psi_s > 0 \tag{2.23}$$

The surface charge density now is dominated by the second term in Eq.2.8, that is,

$$Q_s \approx -\frac{\sqrt{2}\varepsilon_s kT}{qL_D}\sqrt{-\beta\psi_s} \tag{2.24}$$

and the total capacitance can be expressed by

$$C = \frac{1}{1/C_{ox} + x_d/\varepsilon_s} \tag{2.25}$$

where $x_d = \sqrt{\frac{2\varepsilon_s\psi_s}{qN_A}}$ is the depletion width. We see that the capacitance of the system decreases as the depletion region widens.

Inversion

As the applied voltage is increased further, the energy bands bend considerably away from their levels in the bulk of the semiconductor so that the intrinsic level E_i at the surface crosses over the Fermi level E_f. The conduction band edge at the surface is closer to the Fermi level than the valence band edge. The applied voltage has created an inversion layer at this point, so it is called inversion. When E_i is slightly below E_f, the system is said to be in the weak inversion region with a low electron density in the inversion layer. The depletion will reach to the maximum width x_{dmax}. When the surface potential passes $2\psi_B$, the electron density at the surface is higher than that of the

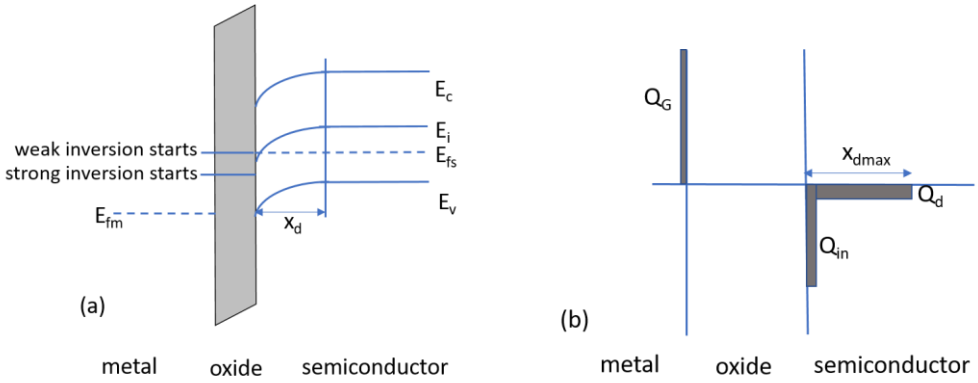

Fig.2.1.9. (a) Energy band diagram and (b) Charge distribution of MOS system at inversion.

hole density (majority carriers). The system is strong inversion region. Fig.2.1.9 shows the energy band diagram and charge distribution at inversion region. We have

$$V_G > V_{FB} \tag{2.26}$$

$$Q_s < 0 \tag{2.27}$$

$$2\psi_B > \psi_s > \psi_B \text{ (weak inversion)} \tag{2.28}$$

$$\psi_s > 2\psi_B \text{ (strong inversion)} \tag{2.29}$$

$$x_{dmax} = \sqrt{\frac{4\varepsilon_s \psi_B}{qN_A}} \tag{2.30}$$

In weak inversion, the depletion will reach to the maximum width and the surface charge density can be approximated as that under depletion region since the electron density is still low. Once strong inversion starts, the surface potential remains relatively constant due to the sensitivity

of electron density to surface potential. In strong inversion, the surface charge density will be dominated by the fourth term in Eq.2.8, that is,

$$Q_s \approx -\frac{\sqrt{2}\varepsilon_s kT}{qL_D}\sqrt{\beta\psi_s} \tag{2.31}$$

For n-type MOS capacitors, the condition for the surface potential is opposite to that for p-type as discussed above. The table below shows the summary of different regions distinguished by surface potential and electron concentrations on n-type MOS system.

$\psi_s > 0$	accumulation
$\psi_s = 0$	Flat-band
$\psi_B < \psi_s < 0$	depletion
$\psi_B = \psi_s$	Midgap with $p_s=n_s=n_i$
$2\psi_B < \psi_s < \psi_B$	Weak inversion $p_i < p_s < N_d$
$\psi_s = 2\psi_B$	Onset of strong inversion $p_s = N_d$
$\psi_s < 2\psi_B$	Strong inversion $p_s > N_d$

2.1.2 N-channel MOSFET

The principle of the surface field-effect transistor was first proposed in 1930s by Lilienfeld and Heil [5, 6] and the first MOSFET was reported by Kahng and Atalla in 1960s [7]. The MOSFET is the most important device for high density integrated circuits as well as the power devices [2]. In general, a MOSFET is a four-terminal device with gate, source, drain and body and both source and body are grounded as voltage reference. As shown in Fig.2.1.10, a n-channel MOSFET is composed of heavily doped source and drain regions by n^+ ion implantation (~10^{20}

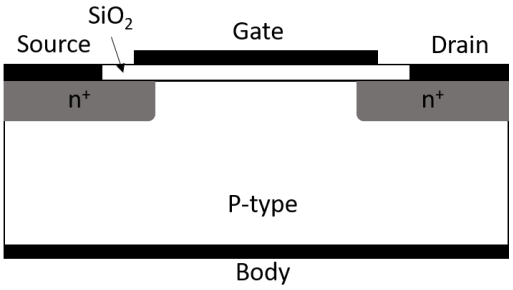

Fig.2.1.10. Structure of a n-channel MOSFET.

cm^{-3}) and p-type substrate. The channel is formed by applying a positive gate voltage and electrons starts flowing in the form of current when a voltage is applied between source and drain. The operation principle of a n-channel MOSFET in flat-band, accumulation, depletion and inversion is the same as p-type MOS capacitor discussed in section 2.1.1 due to its p-type substrate. The relationship between the drain current and gate voltage will be discussed.

To analyze conditions in MOSFETs when applied with a drain voltage V_D, the situation where the electron and hole quasi-Fermi levels are unequal should be considered [7]. Fig.2.1.11 shows the band diagram of a MOS system in inversion with the electron and hole quasi-Fermi levels split by an amount of qV_R. Therefore, the surface potential at onsite of strong inversion needed to be modified as

$$\psi_s = 2\psi_B + V_R \tag{2.32}$$

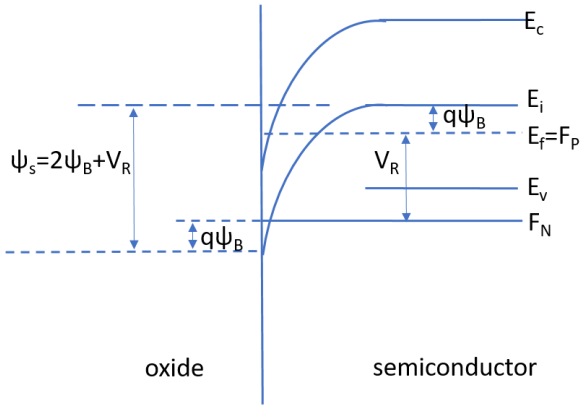

Fig.2.1.11. Band diagram of p-type MOS capacitor in inversion with the electron and hole quasi-Fermi levels split.

N-channel MOSFET current-voltage relationship

When a positive gate voltage is applied to produce n-channel, the current will flow between source and drain through channel region by applying drain voltage. We starts with applying a gate voltage V_G above threshold voltage V_T, the gate voltage at the onset of inversion so that an inversion layer exists at the oxide/semiconductor interface. Fig.2.1.12 shows the basic MOSFET under inversion. We assume that the potential in the channel gradually changes with y and can be evaluated by one-dimensional electrostatics based on the vertical slice at any y point. We neglect

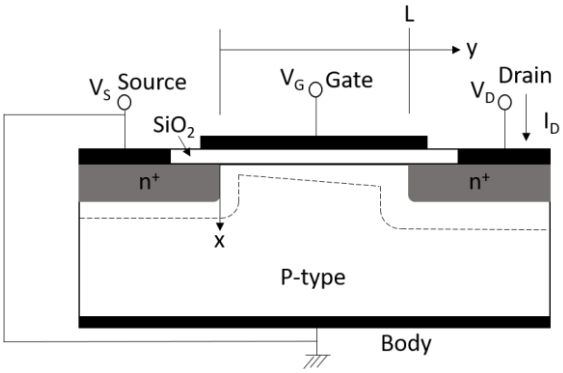

Fig.2.1.12. Structure of the basic MOSFET under inversion.

velocity saturation and the currents in x direction so that the electron drift velocity at point y is given by [7]

$$v_y = \mu_N^* E_y(y) \tag{2.33}$$

where μ_N^* is the electron mobility and $E_y(y)$ is the electric field in y direction in the channel. Consider a thin inversion layer with length of dy at y, the drain current can be written as [7]

$$I_D = -W\mu_N^* n_s \frac{dF_N}{dy} = W\mu_N^* Q_N \frac{d}{dy}\left(\frac{F_N}{q}\right) = -W\mu_N^* Q_N \frac{dV_R}{dy} = -\frac{W\mu_N^*}{L}\int_{V_S}^{V_D} Q_N d\,V_R \tag{2.34}$$

where W is the width of the channel perpendicular to the page in Fig.2.1.12, n_s is the electron density per unit area in the inversion layer, and F_N is the electron quasi-Fermi level. $Q_N = -qn_s$ is the charge per unit area. When $V_G > V_T$, the inversion charge can be written as

$$Q_N = -C_{ox}(V_G - V_T) \tag{2.35}$$

where the threshold voltage V_T is defined as

$$V_T = V_{FB} + (2\psi_B + V_R) + \frac{\sqrt{2q\varepsilon_s N_A(2\psi_B + V_R)}}{C_{ox}} \tag{2.36}$$

We insert Eq.2.36 and 2.35 into Eq.2.34 to obtain

$$I_D = \mu_N^* C_{ox}\frac{W}{L}\{(V_G - V_{FB} - 2\psi_B)V_D - \frac{1}{2}V_D^2 - \frac{2}{3}\frac{\sqrt{2q\varepsilon_s N_A}}{C_{ox}}\left[(2\psi_B + V_D)^{\frac{3}{2}} - (2\psi_B)^{\frac{3}{2}}\right]\} \tag{2.37}$$

Eq.2.36 is under the assumption of a continuous inversion layer from source to drain. As V_D increases, the pinch off occurs where the charge in inversion layer at drain is zero. At this moment, Eq.2.36 is no longer valid. The saturation drain voltage can be solved by setting $Q_N = 0$, y = L and $V_R = V_{D,sat}$, which is

$$V_{D,sat} = (V_G - V_{FB} - 2\psi_B) + \frac{q\varepsilon_s N_A}{C_{ox}^2} - \sqrt{(\frac{q\varepsilon_s N_A}{C_{ox}^2})^2 + 2\frac{q\varepsilon_s N_A}{C_{ox}^2}(V_G - V_{FB})} \quad (2.38)$$

2.2 Interface trap characterization

2.2.1 Physics of interface traps

The theory discussed in previous sections is under the assumption of an ideal oxide in which there are no fixed oxide or interface charges. In MOS system, especially for SiC, the presence of these two types of charges is unavoidable and non-negligible. In Si MOS system, interface traps can be produced by dangling silicon bonds and impurities during the high temperature processing and the density of these traps is typically reduced by annealing the oxidized silicon wafer in hydrogen or forming gas (a mixture of hydrogen and nitrogen) [8]. In the case of SiC, the interface of SiO_2/SiC is highly disordered due to the presence of C during thermal oxidation and the interface trap density is ~10^{13}/cm^2 eV near band edges of 4H-SiC. Fig.2.2.1 shows the energy band diagram of the charge contribution from interface traps in inversion in p-type MOS system. All interface traps with energy levels $E_T > E_i$ are treated as acceptor-like and those with $E_T < E_i$ are treated as donor-like based on the verified nature of traps by experiments [9,10]. Acceptor-like traps are neutral when empty and negatively charged when occupied by an electron while donor-like traps are positively charged when empty and neutral when occupied by

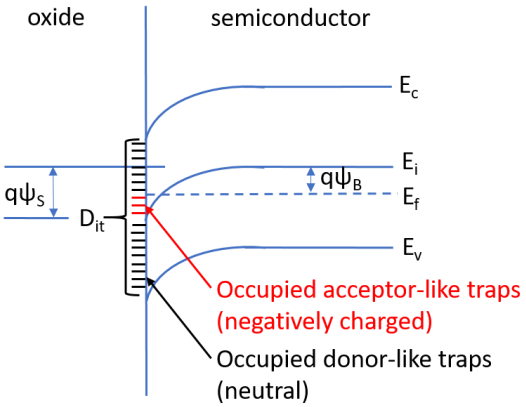

Fig.2.2.1. Energy band diagram of the charge contribution from interface traps in inversion in p-type MOS system.

an electron [11]. In the case of inversion, all donor-like traps are neutral and some acceptor-like traps are occupied and negatively charged.

It is essential to fully understand the nature of the interface charges and accurately determine their physical properties and behavior because they are likely to be directly linked to the device performance and reliability. As a part of this research, several techniques that have been applied to characterize interface traps on SiC MOS devices will be discussed in the following sections.

2.2.2 Simultaneous high-low frequency capacitance-voltage method

The high-low frequency C-V measurement is a common interface trapped charge measurement method [12]. This method assumes that the interface states fully respond to a low frequency (quasi-static) and do not respond at all to a high frequency applied in the measurement. Under this assumption, the low-frequency capacitance includes contributions from all the interface states, while the high-frequency capacitance does not include any interface state contributions [7]. Fig.2.2.2 shows the equivalent circuit in depletion mode when take interface traps into account. As the gate voltage is swept from accumulation to inversion, the gate charge is $Q_G = -(Q_s+Q_{it})$ assuming no oxide charge and both semiconductor and interface traps must be charged with gate voltage sweeping.

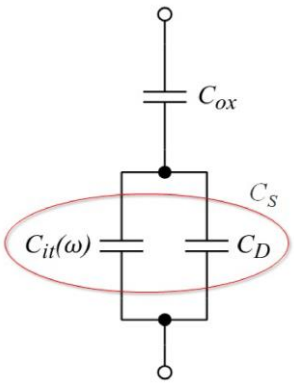

Fig.2.2.2. Equivalent circuit of overall capacitance in depletion when interface traps present.

At strong accumulation, C_D and C_{it} can be ignored. In depletion, the overall capacitance at low-frequency is given by

$$C_{LF} = \left(\frac{1}{C_{ox}} + \frac{1}{C_D + C_{it}}\right)^{-1} \tag{2.39}$$

where C_{LF} is the low-frequency capacitance and C_{it} is the interface trap capacitance. The high-frequency capacitance can be written as

$$C_{HF} = (\frac{1}{C_{ox}} + \frac{1}{C_D})^{-1} \tag{2.40}$$

where C_{HF} is the high-frequency capacitance and C_{it} is assumed to be zero. Therefore, the interface trap density D_{it} can be calculated as

$$D_{it} = \frac{C_{LF} - C_{HF}}{q^2 S} = \frac{C_{ox}}{q^2 S}(\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}}) = \frac{(C_D + C_{it})_{LF} - (C_D)_{HF}}{q^2 S} \tag{2.41}$$

where S is the device gate area.

It is important to accurately determine the surface potential ψ_s since it determines the energy position of interface traps. In addition, the surface potential is critical for SiC because the interface state density usually exhibits exponential distribution near the band edge [7]. According to a theory proposed by Berglund [13], the surface potential can be calculated from the low-frequency C-V curves using

$$\psi_s(V_G) = \int (1 - C_{LF}/C_{ox}) dV_G + A \tag{2.42}$$

where A is the integration constant, which is often determined based on the flat-band capacitance in high-frequency assuming $\psi_s = 0$ as shown in Fig.2.2.3 [7] with $1/(C_D+C_{it})^2$ vs. ψ_s. In Fig.2.2.3, a linear correlation is evident for sufficiently negative surface potential in the depletion region. At

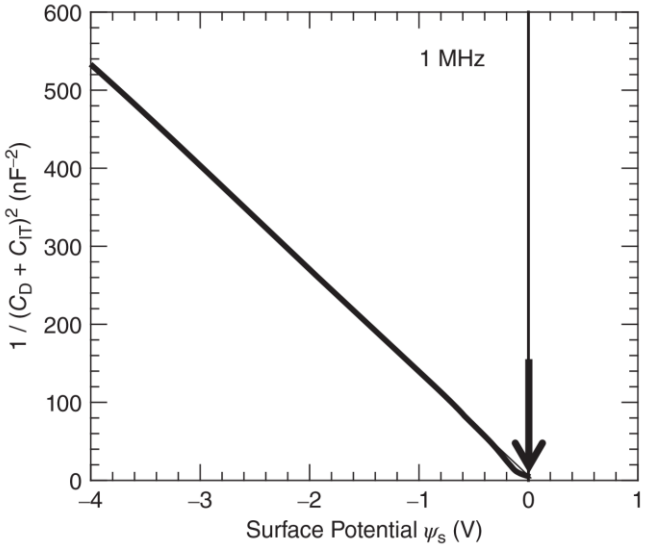

Fig.2.2.3. $1/(C_D+C_{it})^2$ vs. ψ_s. The integration constant A can be determined so that extrapolation of the straight line should intersect the origin of the plot [7].

a sufficiently high frequency, the interface states do not respond and no inversion carriers are generated at the interface. Therefore, a linear relationship can be established between $1/(C_D+C_{it})^2$ and ψ_s. The constant A can be determined so that extrapolation of the straight line should intersect the origin of the plot, as shown in Fig.2.2.3.

2.2.3 C-ψ_s method

The interface state density has been characterized by high-low C-V method with the maximum frequency of 1 MHz. However, the fast interface states that respond to the frequencies above 1 MHz are undetectable by the high-low C-V method. Higher frequencies than 1 MHz are not easily obtained to detect fast traps due to the series resistance and inductance. Therefore C-ψ_s method has been proposed by H. Yoshioka *et al.* [14,15] to extract interface traps in SiC MOS systems, where they are important. By using the theoretical capacitance, the high-frequency limit is considerably solved. This method requires a very accurate determination of surface potential and theoretical capacitance to extract interface states. By using Eq.2.41, the integration constant A can be calculated based on the flat-band capacitance in high-frequency measurement assuming $C_{it} = 0$. If the frequency is not high enough, the flat-band capacitance contains a component of the fast interface states, leading to an error in the surface potential [14]. By using the obtained surface potential, the theoretical semiconductor capacitance $C_{s,theory}$ and interface trap density can be calculated by

$$C_{D,theory}(\psi_s) = \frac{SqN_D \left|\exp\left(\frac{q\psi_s}{kT}\right) - 1\right|}{\sqrt{\frac{2kTN_D}{\varepsilon_{SiC}}\left[\exp\left(\frac{q\psi_s}{kT}\right) - \frac{q\psi_s}{kT} - 1\right]}} \tag{2.43}$$

$$D_{it} = \frac{(C_D + C_{it})_{LF} - C_{D,theory}}{q^2 S} \tag{2.44}$$

assuming n-type SiC, where N_D is the doping concentration. Fig.2.2.4 shows the comparison of semiconductor capacitance measured at different frequencies and theoretical calculation, indicating more accurate D_{it} extraction by C-ψ_s method.

The C-ψ_s method is superior to other methods from two points of view: (i) C-ψ_s can detect fast interface states without frequency limits; (ii) Simple measurement (similar to high-low C-V

measurement). The code of C-ψ_s analysis used in this work was developed by Purdue University in collaboration as detailed in [16].

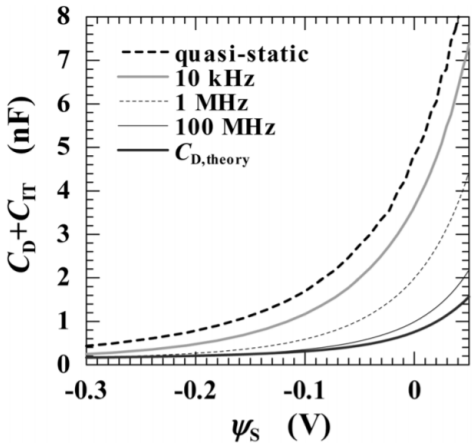

Fig.2.2.4. Semiconductor capacitance C_D+C_{it} versus surface potential ψ_s for a n-type SiC MOS capacitor [14].

2.2.4 Gray-Brown method

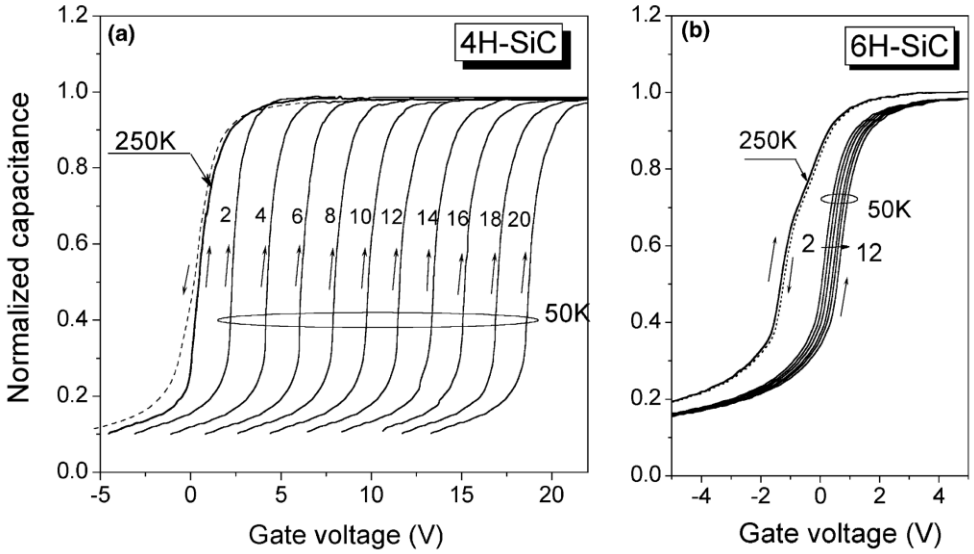

Fig.2.2.5. High-frequency C–V curves for (a) 4H-SiC and (b) 6H-SiC n-type MOS capacitors at temperatures of 50 K-250 K [18].

Gray-Brown technique characterizes interface traps by high frequency C-V measurements as a function of temperature [17]. The reduction of temperature causes the Fermi level to shift towards the majority carrier band edge. As a result, the interface traps below the Fermi level will be occupied by electrons, which brings additional negative charge to the effective charge Q_{eff} at

low temperature causing a flat band voltage shift. This is seen in C-V measurements on both 4H-SiC and 6H-SiC MOS capacitors, as presented in Fig.2.2.5 [18] and the corresponding flat band voltage shift provides an estimation of the density of the effective trapped charge at the interface by

$$V_G(T_2) - V_G(T_1) = \frac{q\int_{E_F(T_1)}^{E_F(T_2)} D_{it}(E)dE}{C_{ox}} = \frac{qN_{it}}{C_{ox}} \tag{2.45}$$

where $V_G(T_1)$ and $V_G(T_2)$ are the gate voltage to maintain the same band-bending at temperature T_1 and T_2. This technique extends the range of D_{it} profile closer to the conduction band edge for n-type capacitors.

2.2.5 Constant capacitance deep-level transient spectroscopy (CCDLTS)

Transient capacitance spectroscopy is widely used to measure defect energy levels in a semiconductor band gap and effective cross sections of point defect for capturing charge carriers as well as defect densities [19]. Deep level transient spectroscopy (DLTS) is a large signal time-domain technique developed by Lang [20] to detect capture and emission of charge carriers at bulk deep levels [21]. Unlike the bulk deep levels with discrete energies and spatial distribution, the interface deep levels are continuously distributed in energy [22]. The qualitative features of DLTS measurement of interface states are illustrated in Fig.2.2.6 [22] with energy band diagram for a MOS structure on a n-type semiconductor. During DLTS measurement, the gate is applied with a superposition of a dc value to bias the device to depletion, and periodic voltage pulses. The gate

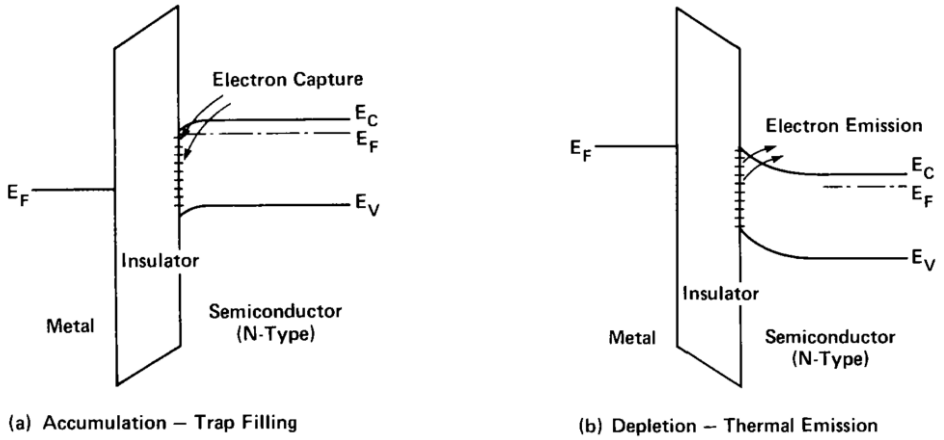

Fig.2.2.6. Energy band diagram for a MOS structure on a n-type semiconductor for (a) pulsed accumulation bias and (b) nonequilibrium depletion bias [22].

voltage is pulsed to drive the device into accumulation in order to populate the interface states with electrons (majority carriers), as shown in Fig.2.2.6 (a). After the voltage pulse returns to the depletion value, the trapped carriers will be emitted by interface states due to the thermal emission process, as shown in Fig.2.2.6 (b).

Constant capacitance deep level transient spectroscopy (CCDLTS) differs from regular DLTS in that instead of monitoring the capacitance transient arising from trap emission, the gate voltage is adjusted so that a constant capacitance is maintained throughout the emission phase. The device is initially biased in depletion to obtain a depletion capacitance C_{HF} at gate bias V_{DC}. A voltage pulse V_{pulse} drives the device into accumulation. The variation in the gate voltage is then related to the number of defects which emit electrons [23]. The capacitance and voltage waveforms are represented in Fig.2.2.7 [22]. The capacitance is kept constant by dynamically varying the gate voltage after a pulse into accumulation. The CCDLTS signal ΔV_G is the difference of the gate voltages measured at two delay times t_1 and t_2 after a charging pulse. This signal is recorded in a temperature scan to form a trap-emission spectrum. The signal ΔV_G at a peak temperature T_0 is directly proportional to the interface trap density. The interface trap density can be expressed as [24]

$$N_{it} = \frac{3C_{ox}\Delta V_G(T_0)\Delta W}{q} \tag{2.46}$$

where the factor of 3 is due to the rate window, which is instruments related. ΔW is the ration of integrated CCDLTS intensity over the measured temperature range to the one of a CCDLTS peak

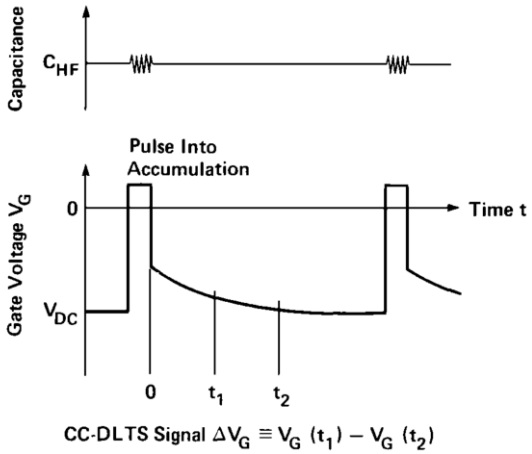

Fig.2.2.7. Schematic diagrams of the capacitance and gate voltage waveforms in a CCDLTS measurement on MOS capacitor [22].

for a trap having a single energy level. The amplitude of the CCDLTS peak for a trap having a single energy level is given by [25]

$$S(T) = A(T_0)[\exp(-e_N t_1) - \exp(-e_N t_2)] \quad (2.47)$$

S(T) is equal to $\Delta V_G(T_0)$ when $A(T_0) = 3\Delta V_G(T_0)$. e_N is the trap emission rate, given by

$$e_N = \sigma \cdot v_{th} \cdot N_C \cdot \exp(-\frac{E_0}{kT}) \quad (2.48)$$

where σ is the trap cross section, v_{th} is the electron thermal velocity and N_C is the conduction band density of states. E_0 is the energy difference between the interface trap level E_T and the conduction band edge E_C.

2.2.6 Subthreshold slope method for extracting D_{it} in MOSFETs

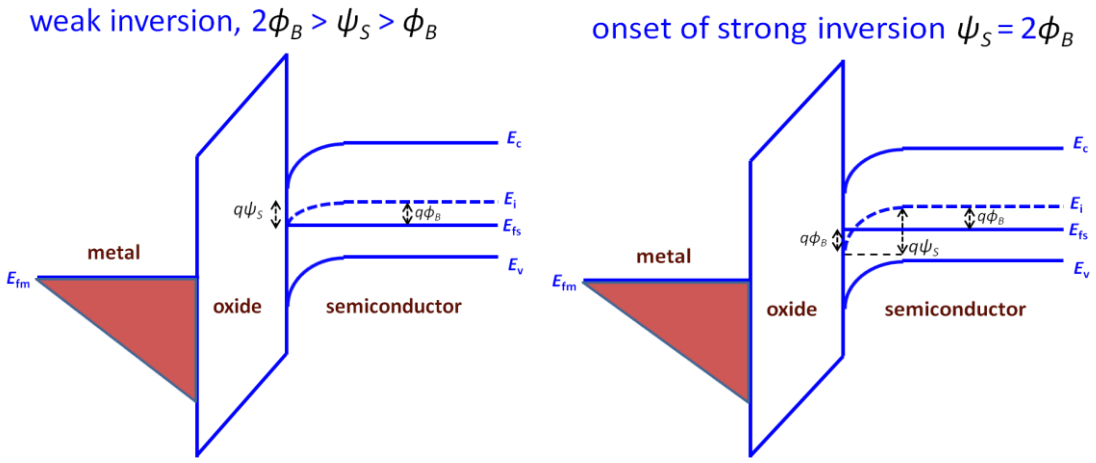

Fig.2.2.8. Band diagrams of a p-type MOSFET at (a) week inversion and (b) onset on strong inversion.

Interface trap can be also characterized directly on MOSFETs by subthreshold I-V characteristics [26]. Subthreshold region is in weak inversion where the surface potential ψ_s at the source is in between bulk potential ψ_B and $2\psi_B$, shown in Fig.2.2.8. The characteristic of a n-channel MOSFET in this region is very important in determining switching performance [27]. In weak inversion, the drain current is determined by diffusion of electrons from the source to the drain and increases exponentially with gate bias. It is given by [27]

$$I_D = \frac{W}{L} I' e^{\frac{q(V_G - V_T)}{nkT}} (1 - e^{-\frac{qV_D}{kT}}) \quad (2.49)$$

where I' and n are constants defined as

$$I' = \mu \frac{\sqrt{2q\varepsilon_S N_A}}{2\sqrt{2\psi_B}} \psi^2 \tag{2.50}$$

$$n = 1 + (C_D + C_{it})/C_{ox} \tag{2.51}$$

Ideally n = 1 due to the negligible C_D compared to C_{ox} with a relatively low doping without taking interface charges into account. n > 1 when the doping increases and taking the interface charges into account.

When V_D is larger than a few of kT/q, the drain current can be expressed by

$$I_D = \frac{W}{L} I' e^{\frac{q(V_G - V_T)}{nkT}} \tag{2.52}$$

$$log(I_D) = \log\left(\frac{W}{L} I'\right) + \frac{q(V_G - V_T)}{nkT} \tag{2.53}$$

The subthreshold slope SS is defined as the gate voltage necessary to change the drain current by one decade, which is

$$SS \equiv ln10 \frac{\partial V_G}{\partial ln I_D} \cong \ln(10) \frac{kT}{q} (1 + \frac{C_D + C_{it}}{C_{ox}}) \tag{2.54}$$

The interface trap density D_{it} and the change in D_{it} can be obtained from Eq.2.53 as

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{qSS}{\ln(10)\, kT} - 1\right) - \frac{C_D}{q^2} \tag{2.55}$$

$$\Delta D_{it} = \frac{C_{ox}}{\ln(10)\, qkT} (SS_{after} - SS_{before}) \tag{2.56}$$

The subthreshold slope is desired to be as small as possible since it is a parameter determining how fast to switch a MOSFET from off-state to on-state. The degradation of SS is a measure of interface trap density. According to Eq.2.55, D_{it} profile can be obtained by subthreshold slope from I-V characteristics as a function of temperature. In addition, the change of D_{it} in Eq.2.56 demonstrates the uniformity of D_{it} distribution with energy levels in the band gap. The energy level was calculated at a certain surface potential of $2\psi_B$ since the change of C_D between ψ_B and $2\psi_B$ is negligible compared to C_{ox}.

2.3 Channel carrier mobility

The carrier mobility is a critical parameter, which influences the device performance through frequency or time response [28]. Higher mobility material results in higher frequency response due to the proportional relationship between carrier velocity and the mobility at low electric fields. In addition, higher mobility devices lead to higher currents that charge capacitances more rapidly thus resulting in a higher frequency response.

In Si MOSFETs, the main factors limiting the inversion channel mobility are the fixed charge and surface roughness since the interface state density formed by adequate processes is low enough not to limit channel mobility [29]. In SiC MOSFETs, Coulomb scattering had been proposed as the main limiting factor since mobility increases with temperature increasing at elevated temperature due to higher interface trap density. However, more careful investigations have proposed the more likely reason for this mobility behavior, which is thermally activated transport or electron localization in inversion layers [30-32]. The channel mobility (n-channel) is usually estimated by several methods based on different definitions as described below.

2.3.1 Effective mobility μ_{eff}

We consider an n-channel MOSFET of gate length L and width W. The drain current I_D is a combination of drift and diffusion currents, given by

$$I_D = \frac{WQ_n\mu_{eff}V_D}{L} - W\mu_{eff}\frac{kT}{q}\frac{dQ_n}{dx} \tag{2.57}$$

where Q_n is mobile channel charge density and μ_{eff} is effective mobility, usually measured at V_D = 25~100 mV. Lower V_D is better, because then the channel charge is more uniform from source to drain, allowing the diffusive second term in Eq.2.57 to be dropped. Then effective mobility can be expressed by

$$\mu_{eff} = \frac{Lg_d}{WQ_n} \tag{2.58}$$

where the drain conductance g_d is defined by

$$g_d = \frac{\partial I_D}{\partial V_D}|_{V_G=constant} \tag{2.59}$$

The channel charge density is approximated by

$$Q_n = C_{ox}(V_G - V_T) \tag{2.60}$$

$$\mu_{eff} = \frac{L}{WC_{ox}(V_G - V_T)} \frac{\partial I_D}{\partial V_D} |_{V_G=constant} \quad (2.61)$$

This approach has some deficiencies. First, the calculation of channel charge density by $C_{ox}(V_G-V_T)$ is only accurate when V_G is above V_T but not valid for sub-threshold region due to the existence of channel charge. Second, the threshold voltage is not necessarily well known due to different definitions. One usually observes a significant mobility drop near $V_G = V_T$ is because the channel charge density is not accurate, the threshold voltage is not precisely known, and the channel charge density decreases with V_G decreasing and the ionized impurity scattering becomes more important while it is less significant at higher V_G due to the effective scattering screen by inversion charge [28].

2.3.2 Field-effect mobility μ_{FE}

Field-effect mobility is determined from the transconductance, defined by

$$g_m = \frac{\partial I_D}{\partial V_G} |_{V_D=constant} \quad (2.62)$$

The drift component of drain current is given by

$$I_D = \frac{W}{L} \mu_{FE} Q_n V_D = \frac{W}{L} \mu_{FE} C_{ox}(V_G - V_T) V_D \quad (2.63)$$

When the field-effect mobility is fixed, the transconductance can be expressed by

$$g_m = \frac{W}{L} \mu_{FE} C_{ox} V_D \quad (2.64)$$

Thus,

$$\mu_{FE} = \frac{L g_m}{WC_{ox} V_D} \quad (2.65)$$

The field-effect mobility defined by Eq.2.65 is generally lower than then effective mobility defined by Eq.2.61, as illustrated in Fig.2.3.1 [28]. This discrepancy is due to the neglect of the electric field dependence of the mobility in the derivation of Eq.2.65 [33, 34]. Considering the μ_{eff} dependence on gate voltage, gives the transconductance,

$$g_m = \frac{W}{L} \mu_{eff} C_{ox} V_D (1 + \frac{(V_G - V_T)}{\mu_{eff}} \frac{d\mu_{eff}}{dV_G}) \quad (2.66)$$

Then the field-effect mobility becomes

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_D(1 + \frac{(V_G - V_T)}{\mu_{eff}}\frac{d\mu_{eff}}{dV_G})} \tag{2.67}$$

Since μ_{eff} decreases with V_G increasing, $d\mu_{eff}/dV_G < 0$. Therefore, μ_{eff} calculated by Eq.2.67 is higher than the one calculated by Eq.2.65.

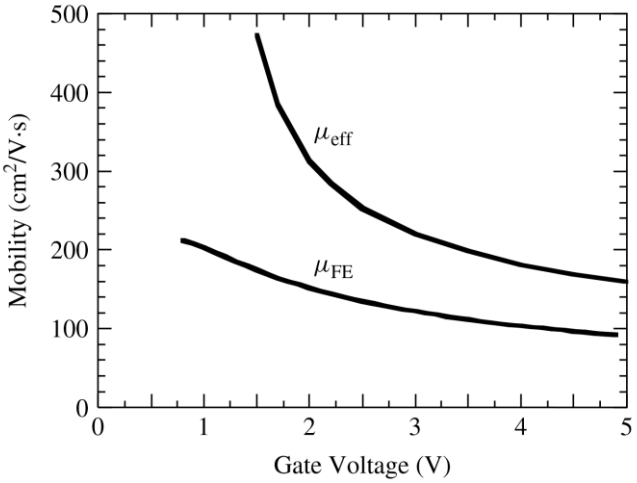

Fig.2.3.1. Comparison between effective mobility and field-effect mobility on the same device [28].

In the two estimates discussed above, it is assumed that all the electrons in the inversion layer are mobile, traveling from the source to the drain with the sheet electron density in the inversion layer approximated by $C_{ox}(V_G-V_T)$. However, the interface state density in SiC MOS structures can be of the same order as the sheet electron density. Electrons trapped by interface traps must be almost immobile. If 80% of mobile electrons are trapped, for example, only 20% of electrons contribute to the drain current. Even if the electrons drift with a mobility of 100 cm^2/Vs, the channel mobility is calculated as 20 cm^2/Vs. Therefore, both approaches underestimate the real electron mobility.

2.3.3 Hall mobility

The real mobility of mobile electrons in the conduction band can be obtained by MOS-Hall effect measurement. The Hall effect measurement technique has found wide application in the characterization of semiconductor materials because it gives the resistivity, the carrier density, and

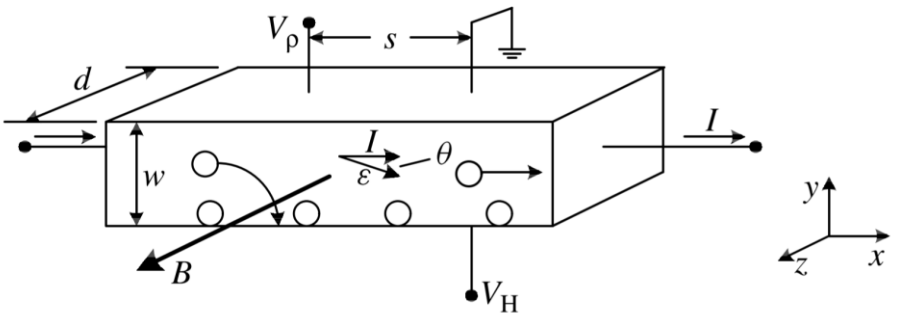

Fig. 2.3.2. Schematic illustrating the Hall effect in a p-type semiconductor [28].

the mobility. The Hall effect describes the behavior of the free carriers in a semiconductor when applying an electric and a magnetic field.

Consider a p-type semiconductor in Fig.2.3.2 [28]. When a magnetic field applied to the semiconductor is perpendicular to the current flow direction, an electric field perpendicular to the magnetic field and the current will be produced. A current I flows in the x-direction, indicated by the holes flowing to the right and a magnetic field B is applied in the z-direction. The current is given by

$$I = qApv_x = qwdpv_x \tag{2.68}$$

The voltage along the x-direction Vρ then is given by

$$V_\rho = \frac{\rho sI}{wd} \tag{2.69}$$

Solving the resistivity from Eq.2.69, is

$$\rho = \frac{wd}{s}\frac{V_\rho}{I} \tag{2.70}$$

The force on the holes is vector expression of both electric force and Lorenz force,

$$\boldsymbol{F} = q(\boldsymbol{E} + \boldsymbol{v} \times \boldsymbol{B}) \tag{2.71}$$

In y-direction, the net force is zero because no current is flowing in this direction. Combine Eq.2.68 and Eq.2.71 gives,

$$E_y = Bv_x = \frac{BI}{qwdp} \tag{2.72}$$

The electric field in y-direction produces the Hall voltage V_H,

$$\int_0^{V_H} dV = V_H = \int_0^w E_y dy = \int_0^w \frac{BI}{qwdp} dy = \frac{BI}{qdp} \tag{2.73}$$

The Hall coefficient R_H is defined as

$$R_H = \frac{dV_H}{BI} \tag{2.74}$$

Combine Eq.2.73 and Eq.2.74 gives

$$p = \frac{1}{qR_H} \tag{2.75}$$

Eq.2.75 is derived under simplifying assumptions of energy independent scattering mechanisms. With this assumption relaxed, the expression for the hole density becomes [35],

$$p = \frac{r}{qR_H} \tag{2.76}$$

where r is the Hall scattering factor, defined by

$$r = <\tau^2> / <\tau>^2 \tag{2.77}$$

where τ is the mean time between carrier collisions. The scattering factor depends on the type of scattering mechanism in the semiconductor and generally lies between 1 and 2. For lattice scattering, r =3π/8=1.18, for impurity scattering r =315π/512=1.93, and for neutral impurity scattering r =1 [36, 37]. The scattering factor is also a function of magnetic field and temperature and can be determined by measuring R_H in the high magnetic field limit. In the high field limit r→1 and for most Hall measurements r > 1. Typical magnetic fields used for Hall measurements lie between 0.05 and 1 T.

The Hall mobility μ_H is defined by

$$\mu_H = \frac{R_H}{\rho} = R_H \sigma = r\mu_p \tag{2.78}$$

where μ_p is the hole conductivity mobility, which is given by

$$\mu_p = \sigma/qp = 1/q\rho p \tag{2.79}$$

A typical pattern configuration called bridge-type Hall bar for Hall effect measurements of a MOSFET is shown in Fig.2.3.3 [26]. The current flows into 1 and out of 4, the Hall voltage is measured between 2 and 6 or between 3 and 5 in the presence of a magnetic field. The resistivity is determined in the absence of the magnetic field by measuring the voltage between 2 and 3 or between 6 and 5. The equations above apply for this geometry.

In MOS-Hall effect measurements, not only the Hall mobility but also the mobile electron density can be determined. Thus, the degree of electron trapping can be estimated by comparing

the real electron density extracted by Hall effect measurement and the total density of induced electrons calculated as $C_{ox}(V_G-V_T)$.

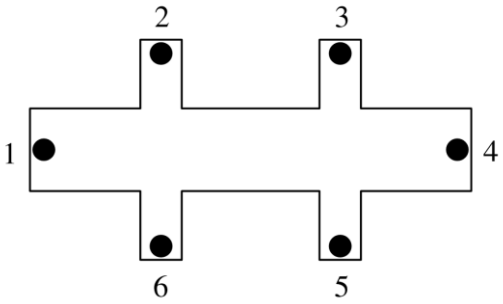

Fig. 2.3.3. Bridge-type Hall bar pattern configuration [26].

2.3.4 Mobility limiting mechanisms

The total mobility follows Matthiessen's rule: the inverse of the total mobility equals to the sum of the inverse of each contributing part, given by

$$\frac{1}{\mu} = \frac{1}{\mu_C} + \frac{1}{\mu_{sp}} + \frac{1}{\mu_{sr}} + \cdots\cdots \tag{2.80}$$

where μ_C is the Coulomb scattering mobility, μ_{sp} is the surface phonon scattering mobility, and μ_{sr} is the surface roughness scattering mobility. Each mobility is limited by their corresponding scattering mechanism. The net mobility is dominated by the lowest mobility. The universal inversion layer mobility in Si MOSFETs reported by S. Tagaki *et al*. [38] is shown in Fig.2.3.4

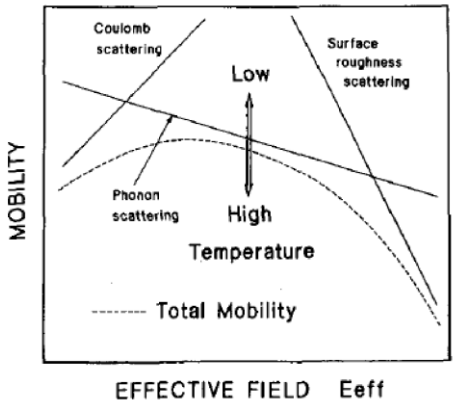

Fig.2.3.4 Schematic diagram of E_{eff} dependence of mobility in inversion layer by three dominant scattering mechanisms [38].

[38]. According to this diagram, the universal curve can be divided into Coulomb scattering, phonon scattering and surface roughness scattering terms in different regions of effective electric field.

In SiC MOSFETs, the mobility scattering mechanisms can be similar to those in Si MOSFETs. Each mobility component depends on either temperature or effective field or both. For Coulomb scattering, the trap charges and the ionized impurities act as scattering center, creating Coulombic interaction with free electrons in the inversion layer. Coulomb scattering mobility increases as the temperature goes up as a result of the reduction of scattering centers as well as higher screening of Coulomb scattering centers by more free electrons due to lower Fermi energy level. The Coulomb scattering mobility in strong inversion is given by [39]

$$\mu_C = \frac{\Gamma_C T}{N_T}(1 + \frac{n}{n_{scr}})^{\xi'} \tag{2.81}$$

where Γ_C is a coefficient parameter, N_T is the sum of all the surface charges, n is the electron concentration and n_{scr} and ξ' are empirical parameters.

Surface phonon scattering is due to the crystal lattice vibration. As temperature increases, the lattice vibration becomes stronger, which results in an increase in the number of surface phonons. The effective electric field has only a small effect on phonon scattering, while the temperature is the dominant factor. The simulated surface phonon mobility component by S. Potbhare *et al*. [40] is given by

$$\mu_{sp} = \frac{A}{E_{eff}} + \frac{B}{TE_{eff}^{1/3}} \tag{2.82}$$

where A and B are empirical parameters.

The interface between semiconductor and thermally grown SiO_2 is not perfectly smooth. As the gate electric field increases, the electron carriers are attracted with stronger force to the interface. Therefore, surface roughness scattering is primarily dominated by the surface electric field with a weak dependence on temperature. The surface roughness mobility component is given by [40]

$$\mu_{sr} = \frac{\Gamma_{sr}}{E_{eff}^2} \tag{2.82}$$

where Γ_{sr} is a parameter that depends on the roughness of the SiO_2/SiC interface. This is seen on most other MOS systems as well.

2.4 Summary

In this chapter, the fundamentals of MOS devices in different working modes has been discussed. The existence of interface traps in SiC MOS structures dramatically degrades channel mobility. Several interface trap characterizations have been introduced, including high-low frequency C-V, C-ψ_s, CCDLTS and subthreshold slope. We also discussed channel mobilities defined by different methods as well as the scattering limit factors to channel mobilities.

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Chapter 3

Sb Counter-doping in channel region of heavily p-well doped 4H-SiC MOSFETs

SiC MOSFETs have historically had poor channel mobility due to large number of electron traps at the interface of SiO_2/SiC. Various channel engineering processes have been proposed to address this issue beyond NO annealing [1], which is currently applied by commercial power MOSFETs. Okamoto *et al*. reported ~75-100 cm^2/Vs of channel mobility and lower interface trap density compared to NO annealing by using $POCl_3$. However, with the formation of phosphosilicate glass (PSG) layer during passivation process, which brings polarization charges, a large negative threshold voltage shift has been observed at high temperature [2]. Modic *et al*. reported that a surface counter-doping layer around 10 nm deep in channel region by Antimony (Sb) improves the low-field channel mobility of lightly doped p-well ($1x10^{16}/cm^3$) 4H-SiC MOSFETs [3]. The difference between such a shallow implanted channel and a buried channel is in the case of a buried channel, the implantation of the opposite dopants to the substrate is implanted deeper into the substrate, away from the semiconductor-oxide interface. If the implanted impurity generates enough minority carriers in the substrate to switch the semiconductor type, a channel is formed between the source and drain even when the applied gate voltage is zero, which results in a normally-on MOSFET [4].

In the case of the shallow Sb implantation, the n-type Sb dopants provide higher electron density in the channel, which results in higher transconductance as well as lower carrier scattering at low electric fields. Unlike other group-V elements, such as N and P, interface trap passivation effects observed in the Sb surface counter-doping process are minimal and the primary effect of Sb is counter-doping the p-type SiC surface [5]. However, this process does not improve the mobility at high transverse fields compared to standard NO annealing and results in slight lowering of V_{th} due to the surface counter-doping, which is not desirable for power devices.

For SiC power MOSFETs, due to the large noisy environment in power system as well as NBTI issues [6], a relatively large V_{th} is desired to keep the device under safe operation range, which explains why the p-well doping of SiC power MOSFETs is high (above $10^{17}/cm^3$). Desired

V_{th} could be achieved by varying p-well doping concentration to some extent. Higher p-well doping results in higher V_{th}. For SiC power MOSFETs with heavily doped p-wells (above $10^{17}/cm^3$), low channel mobility and poor subthreshold slope are still challenges for further development. In this chapter, the effect of Sb counter-doping with various doping doses combining with NO annealing on threshold voltage, subthreshold slope and channel mobility of 4H-SiC MOSFETs with heavily doped p-wells will be discussed.

3.1 Al and Sb profile simulation and ion implantation process

The element applied for p-well doping in this study is Al. The purpose to use Sb as donor dopants is to differentiate the counter-doping from trap passivation effect on channel transport. Although Sb is an element in group-V, it is not expected to passivate interface traps due to the larger atomic radius than nitrogen and phosphorus. Also, Sb has heavier atomic weight (~8 times

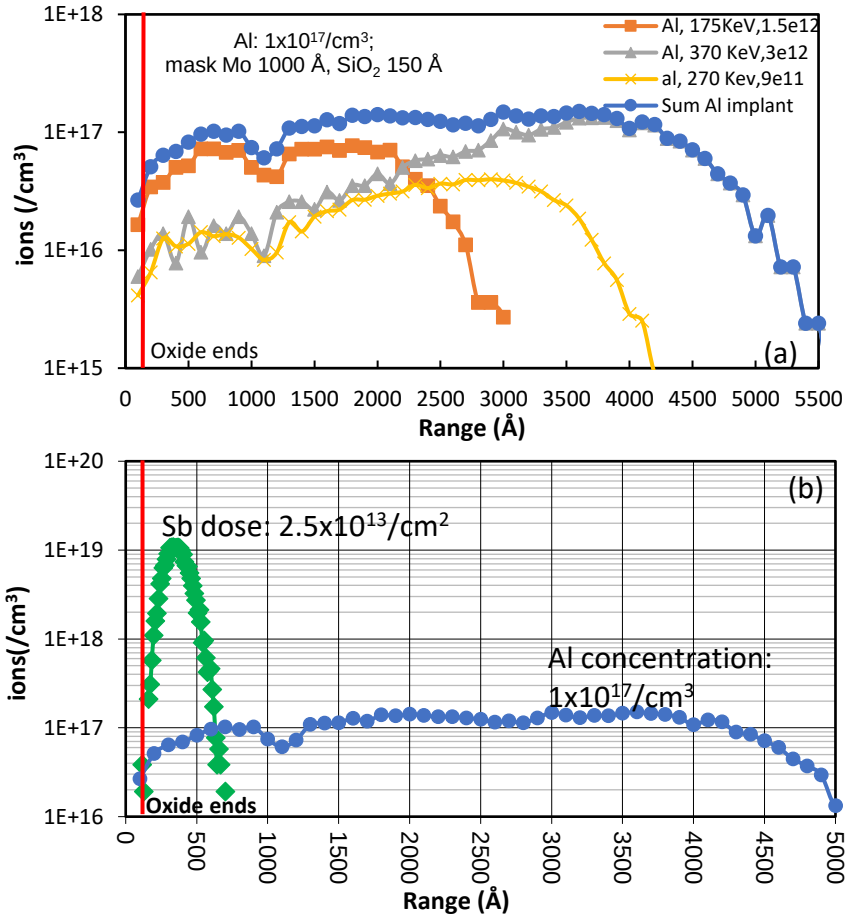


Fig.3.1.1. The simulated profile for (a) Al doping with multiple implantations and (b) Sb doping with single implantation by SRIM.

heavier than nitrogen), providing more accurate control over shallower ion implantation profiles. Both Al and Sb distribution profile in SiC were simulated by the Stopping and Range of Ions in Matter (SRIM) before implantation process. SRIM is one widely used simulation tool for implantation and other ion bean processes and it involves ion species, doping range implantation energy, and dose in the setup input [7]. To obtain box profile with constant doping concentration in SiC for heavy p-well doping, multiple implantations with various energies and doses should be implemented. Sb doping was realized by a single implantation with a Gaussian profile. To protect the source and drain areas from multiple implantations for p-well doping, a mask of Molybdenum with ~1000 Å was deposited on S/D areas. Also, a thin layer of oxide with ~150 Å was thermally grown to protect the surface of channel area from both p-well doping and counter-doping. Fig.3.1.1 shows the simulated profile for Al with concentration of $1x10^{17}/cm^3$ and Sb with dose of $2.5x10^{13}/cm^2$ in SiC and Table 3-1 shows all the doping configurations studied in this experiment.

Table 3-1. Doping profiles for Al and Sb

Implantation element	Implantation concentration	Implantation energy and dose	Implantation temperature
Sb	Gaussian	80 keV, $2.5x10^{13}/cm^2$	23°C
		100 keV, $2.5x10^{13}/cm^2$	
		80 keV, $5x10^{13}/cm^2$	
Al	$1x10^{16}/cm^3$	Epi-layer	700°C
	$1x10^{17}/cm^3$	175 keV, $1.5x10^{12}/cm^2$; 370 keV, $3x10^{12}/cm^2$; 270 keV, $9x10^{11}/cm^2$	
	$5x10^{17}/cm^3$	175 keV, $7x10^{12}/cm^2$; 370 keV, $1.2x10^{13}/cm^2$; 270 keV, $4x10^{12}/cm^2$	

3.2 Lateral MOSFET fabrication process

Long channel lateral MOSFETs (150 µm length x 290 µm width) were fabricated on Si-face of 4H-SiC with Al and Sb ion implantation in the p-well and the channel regions. Al was first implanted with multiple implantations to obtain a box profile at 700°C with $1x10^{17}/cm^3$ and $5x10^{17}/cm^3$, respectively. Sb was implanted with Gaussian distribution at 80 keV/100 keV at room temperature with doses of $2.5x10^{13}/cm^2$ and $5x10^{13}/cm^2$, respectively. This was followed by dopant activation annealing at 1650°C using a graphic carbon cap. To investigate the difference between samples with Sb (referred to as 'Sb counter-doping') and without Sb (referred to as 'standard NO')

implantation on electrical results, some samples only received Al implantation without Sb. Following standard RCA cleaning, dry oxidation at 1150°C for 12 hours and NO annealing at 1175°C for 30 minutes were processed on all devices in the same procedure. Molybdenum and Ni were sputtered as the gate and source/drain metals. Ohmic contact annealing on source/drain was performed in the annealing furnace at 800°C with Ar flowing. The fabrication process flow is illustrated in Fig.3.2.1.

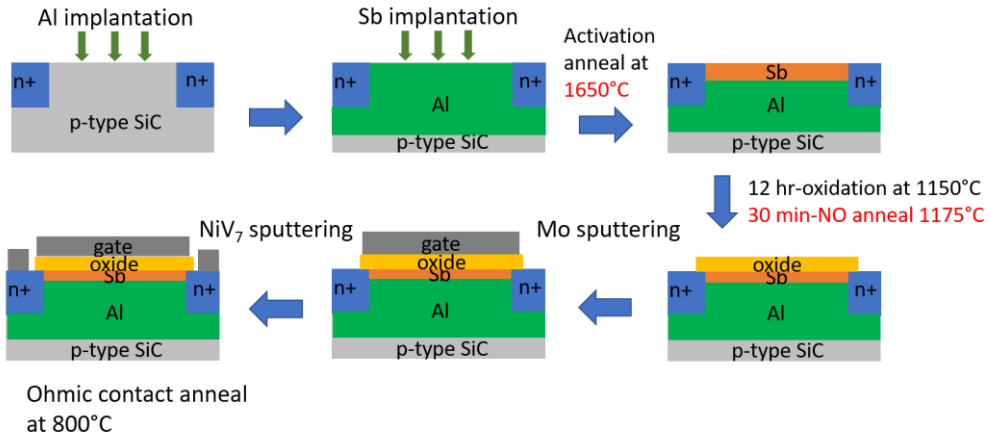


Fig.3.2.1. The fabrication process flow for MOSFETs with various processes.

3.3 Sb profile characterization by secondary ion mass spectrometry (SIMS)

SIMS is a technique used to analyze the composition of solid surfaces, especially semiconductors and thin films by slow sputtering away the surface of the sample with a focused primary ion beam (usually O_2^+ or Cs^+) and collecting and analyzing ejected secondary ions. The mass/charge ratios of these secondary ions are measured with a mass spectrometer to provide

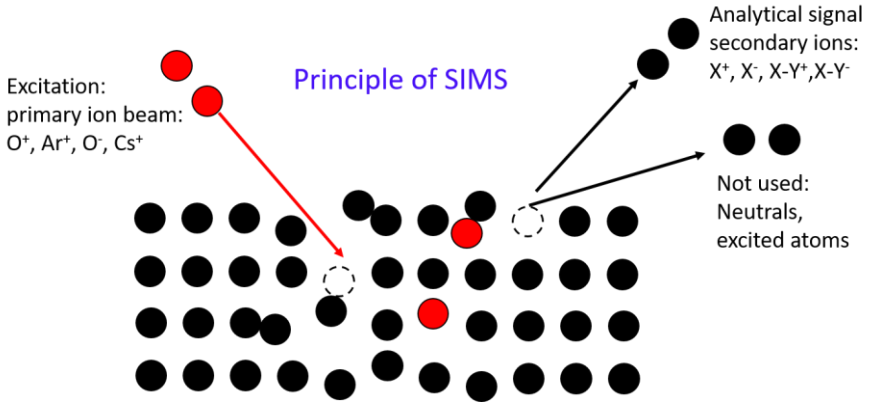


Fig.3.3.1. The principle of secondary ion mass spectrometry.

elemental depth profiles over a wide depth range from a few angstroms (Å) to tens of micrometers (μm). Fig.3.3.1 shows the basic principle of SIMS.

To accurately verify the simulated implantation profile and dose of Sb, experimental Sb implant profiles and doses were measured by SIMS. Also, it is important to measure Sb profile before and after activation anneal and gate oxidation to examine the effects of the activation anneal as well as the percentage of residual Sb. All the SIMS measurements were carried out on the companion MOS capacitors after stripping the gate metal. Note all the companion capacitors are with lightly doped epi-layer ($1x10^{16}/cm^3$). To obtain depth profile of Sb in SiC, the samples were sent to a commercial vendor [8] to this end. To detect Sb, Cs^+ ions were applied as the primary ion beam to sputter the surfaces of the samples generating secondary ions that are collected by a mass spectrometer. SIMS data accounts two stable isotopes, which are ^{121}Sb (57.21%) and ^{123}Sb (42.79%). SIMS has a detection limit of $5x10^{16}/cm^3$ in this study. Concentrations lower than this limit are treated as zero for recorded purposes.

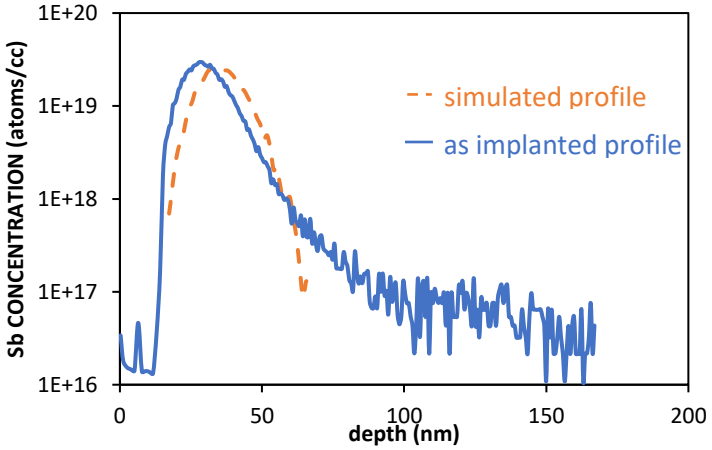


Fig.3.3.2. Comparison between simulated Sb profile and as implanted Sb profile by SIMS. The simulated dose is $5x10^{13}/cm^2$.

Fig.3.3.2 shows the similarity between the simulated Sb profile with the dose of $5x10^{13}/cm^2$ and as implanted Sb profile by SIMS indicating that the simulated profile is accurate. Both the simulated and the as implanted profile and show a ~15 nm oxide layer, which is the blocking oxide to protect the surface of SiC. The graphic carbon cap was formed on the surface of SiC (Appendix I) for all the samples to protect the samples from surface roughness during the high temperature activation annealing [9]. To remove the residual carbon after activation annealing, reactive ion etching (RIE) was carried out with etching gas of O_2 for 90 mins. However, the SIMS profiles in

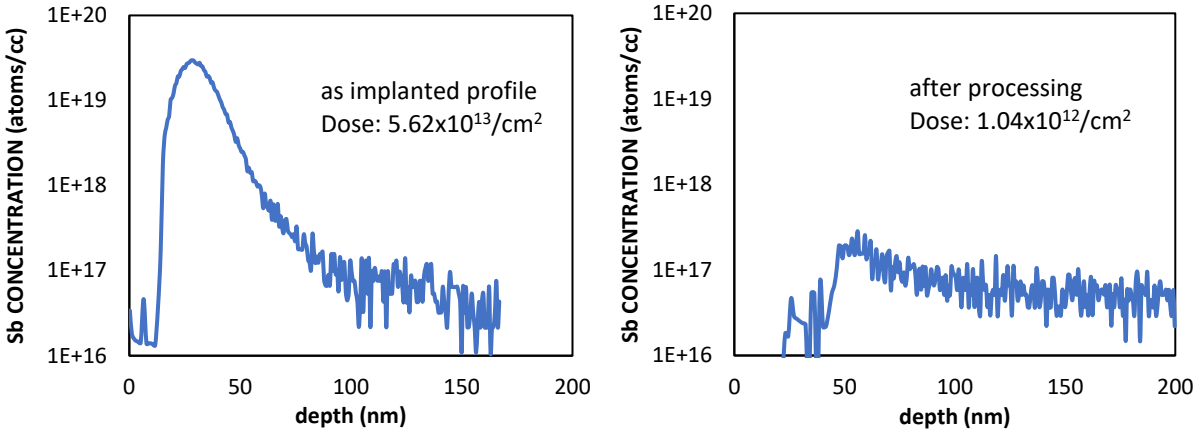


Fig.3.3.3. The as implanted profile and Sb profile after oxidation for gate oxide. The simulated dose is $5x10^{13}/cm^2$.

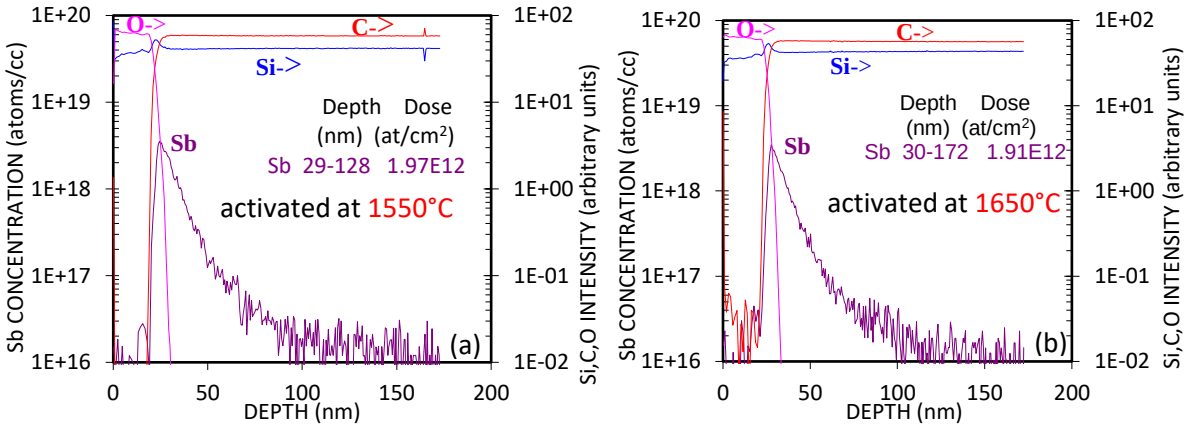
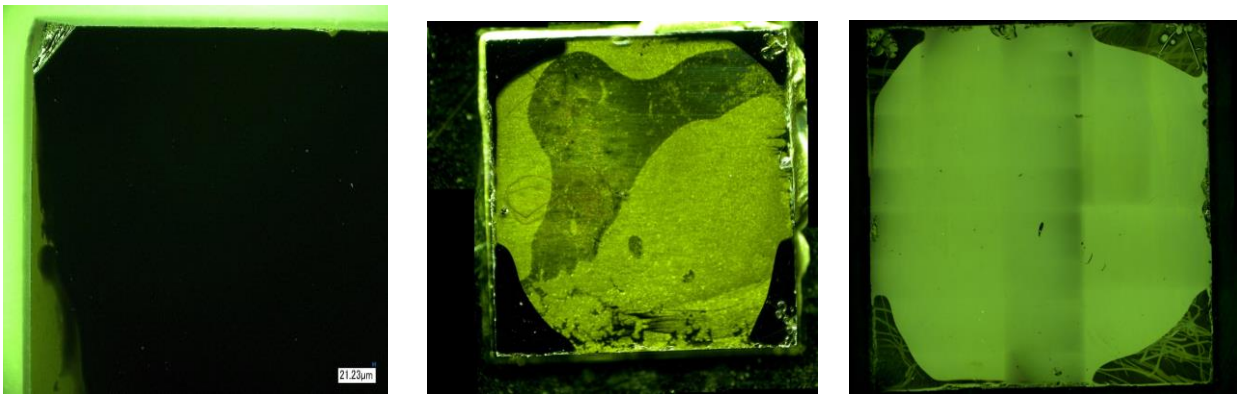


Fig.3.3.4 SIMS Sb profile of samples with target dose of $2.5x10^{13}/cm^2$ activated at (a) 1550°C and (b) 1650°C after RIE.

Fig.3.3.3 indicate ~97% of Sb was lost after fabrication process, much higher than previously reported of ~75% [3]. To figure out the main reason for such high dose of Sb loss, another set of SIMS measurement was carried out on the samples activated at 1550°C and 1650°C with dose of $2.5x10^{13}/cm^2$ right after RIE. The similarity of SIMS profile between samples activated at both 1550°C and 1650°C shown in Fig.3.3.4 demonstrates that ~85% of Sb was lost after RIE on both samples and the percentage of Sb loss does not depend on the activation temperature.

To obtain the optimized dose of Sb, the effect of RIE on amount of Sb lost has been investigated by changing the etching time. Fig.3.3.5 shows the residual carbon prior to RIE, after 20-min RIE and 25-min RIE. After 25-min RIE, the residual carbon was almost completely etched. This explains well that ~97% of Sb loss after 90-min RIE on previous samples. Therefore, the



Prior to etch 20-min RIE 25-min RIE

Fig.3.3.5. Residual carbon prior to RIE, after 20-min RIE and 25-min RIE.

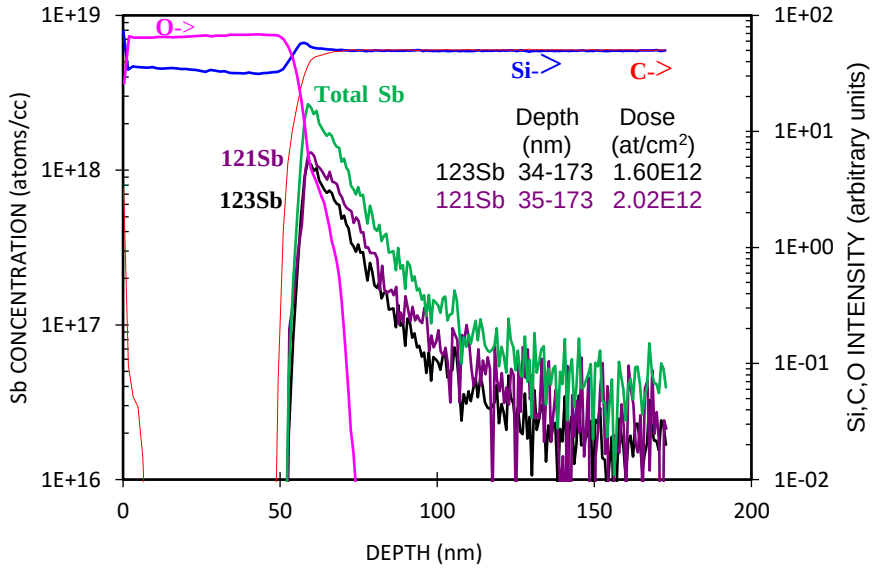


Fig.3.3.6. SIMS Sb profile of samples with dose of $2.5x10^{13}/cm^2$ after the improvement of carbon etching process.

carbon etching process has been transferred from RIE to O_2 etching by directly locating samples in the furnace flowing O_2 at 800°C for 30 mins. At 800°C, all the carbon was clearly removed and no extra growth of oxide is expected on SiC. Fig.3.3.6 shows the Sb profile after the improvement of carbon etching process with target dose of $2.5x10^{13}/cm^2$. The result indicates the total Sb loss is ~$2.1x10^{13}/cm^2$ after all fabrication processes including activation annealing, O_2 etching and oxidation for gate oxide. The oxide thickness is ~60 nm. SIMS results suggest that most of the Sb

loss is due to the oxidation process and Sb concentrates near the interface between the oxide and SiC with ~10 nm in SiC. Sb is expected to be confined in SiC side but it is possible that the Sb distributes into SiO_2 as well due to the Sb loss by diffusing out through oxide. The rate of Sb diffusion through SiO_2 reported by Aoyama *et al*. revealed that antimony can diffuse through several hundred nanometers of SiO_2 within 10 hours of annealing at 1200°C [10]. More investigation is necessary to understand the out-diffusion process.

3.4 Electrical characterization of Sb-doped MOS devices

3.4.1 Effect of Sb implantation energy on channel transport of MOSFETs

In this study, Sb implantations were carried out with two implantation energies, which are 80 keV and 100 keV at the same dose of $2.5x10^{13}/cm^2$ to investigate the effect of implantation energy (implantation depth) on the channel transport of lightly doped p-well ($1x10^{16}/cm^3$) 4H-SiC MOSFETs. I_D-V_G measurements were performed on the Sb implanted MOSFETs with a constant drain voltage of 25 mV at room temperature. Fig.3.4.1 shows the log scale of I_D-V_G curves and the field-effect mobility extracted by the transconductance of drain current. The results indicate that

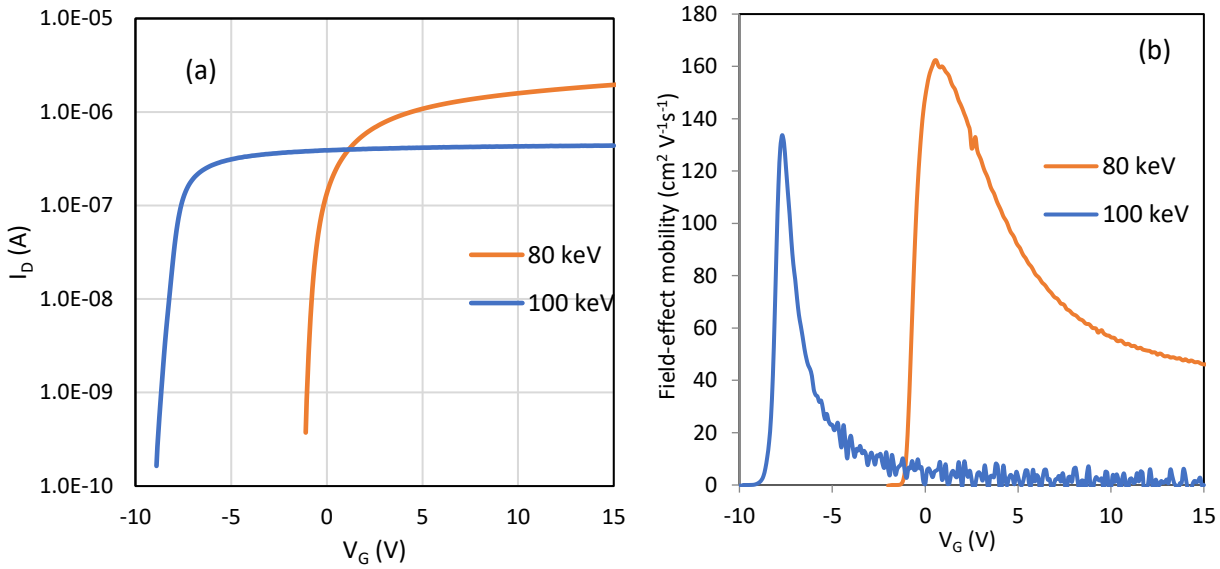


Fig.3.4.1. (a) Log scale of I_D-V_G and (b) Field-effect mobility of Sb implanted MOSFETs with implantation energies of 80 keV and 100 keV.

the higher implantation energy of 100 keV results in normally-on devices and the sharper peak field-effect mobility compared to low implantation energy of 80 keV due to larger depth of Sb

distribution in the channel region of the MOSFETs. The normally-on Sb implanted MOSFETs will be discussed in chapter 5 in details. In the following work, all Sb implanted MOSFETs were processed with implantation energy of 80 keV due to the undesirable normally-on characteristics resulted from implantation energy of 100 keV.

3.4.2 High-low frequency capacitance-voltage with different Sb doses

The simultaneous high-low frequency capacitance-voltage (hi-lo C-V) characterization with high frequency of 100 kHz at room temperature was performed on the companion n-type MOS capacitors with different Sb doses. The C-V curves at high frequency in Fig.3.4.2 (a) show that with increasing Sb dose, the C-V curve is more and more stretched out indicating the shallow Sb implantation makes depletion harder compared to the capacitor without Sb. Oxide thickness was determined by the measured capacitance in complete accumulation region. Since interface trap density (D_{it}) calculation is not expected to be accurate with Sb implantation by hi-lo C-V due to the high concentration of n-type dopants near the surface, D_{it} was extracted by the hi-lo C-V on the capacitor without the Sb implantation shown in Fig.3.4.2 (b). The D_{it} of the other two capacitors with Sb implantation is assumed to be similar to the one without Sb implantation since no

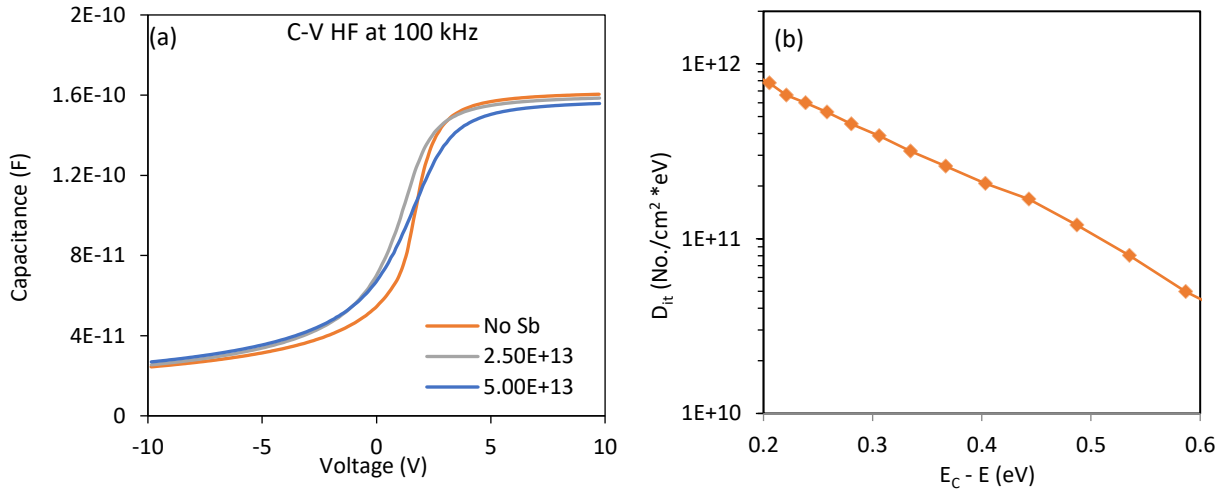


Fig.3.4.2. (a) 100 kHz C-V at room temperature on capacitors with different Sb doses and (b) D_{it} profile as a function of energy.

passivation effect of Sb was observed in previous study [5]. A summary of MOSCAPs with various processes is shown in Table 3-2.

Table 3-2. Summary of companion capacitors with various processes

Sample	n-type doping	Sb dose 80 keV	Average oxide thickness	D_{it} at 0.2 eV (hi-lo C-V)
MOSCAPs	$1x10^{16}/cm^3$	X	60 nm	$7.8x10^{11}/cm^2eV$
		$2.5x10^{13}/cm^2$	61 nm	
		$5.0x10^{13}/cm^2$	62 nm	

To verify p-well doping concentration in SiC, high frequency C-V was carried out on the p-type capacitor on the same pattern as MOSFETs with the simulated Al doping concentration of $1x10^{17}/cm^3$ without Sb implantation. The high frequency capacitance as a function of gave voltage is given by

$$C_{HF} = \sqrt{\frac{q\varepsilon_s N_A A^2}{2V_G}} \tag{3.1}$$

where N_A is the doping concentration of p-type substrate, ε_s is the dielectric permittivity of 4H-SiC, and A is the gate area of the capacitor. Therefore, the doping concentration N_A can be expressed by

$$N_A = \frac{2}{q\varepsilon_s A^2}\frac{V_G}{1/C_{HF}^2} \tag{3.2}$$

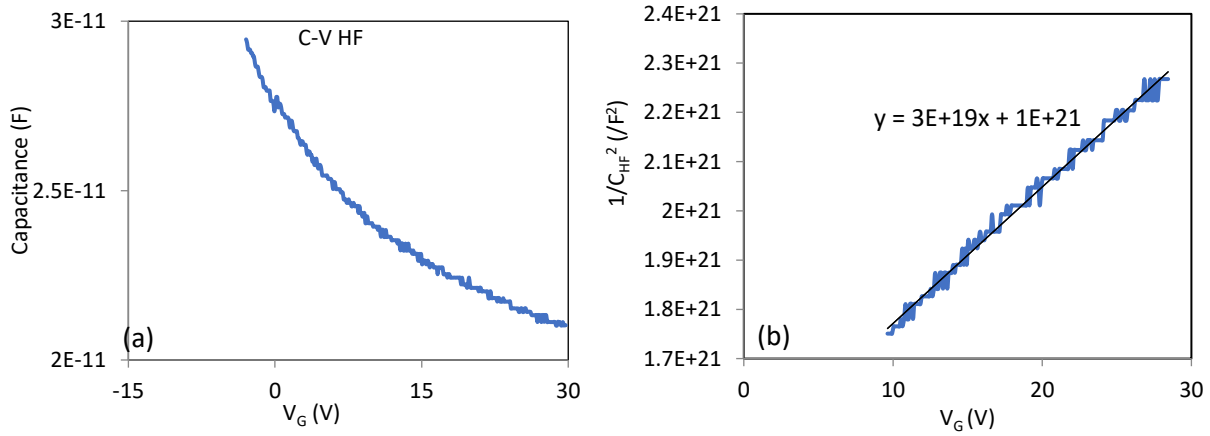


Fig.3.4.3. (a) 100 kHz C-V on p-type capacitor with Al doping concentration of $1x10^{17}/cm^3$ and (b) $1/C_{HF}^2$ as a function of V_G in deep depletion.

The doping concentration was obtained by plotting out $1/C_{HF}^2$ as a function of V_G in deep depletion shown in Fig.3.4.3, which is ~$1.065x10^{17}/cm^3$. This is in good agreement with the simulated doping concentration.

3.4.3 Constant capacitance deep-level transient spectroscopy

Although Sb is an element in group-V, it is not expected to passivate interface traps due to the larger atomic radius than nitrogen and phosphorus. In previous study about the effect of Sb implantation on channel transport, the primary effect for the improvement of channel mobility is observed as counter-doping effect [5, 11]. Fig.3.4.4 [11] shows the low temperature 100 kHz C-V curves of Sb implanted capacitors with and without NO annealing from previous study. It revealed a huge flat band voltage shift of ~9 V for the sample without NO annealing at 79 K compared to

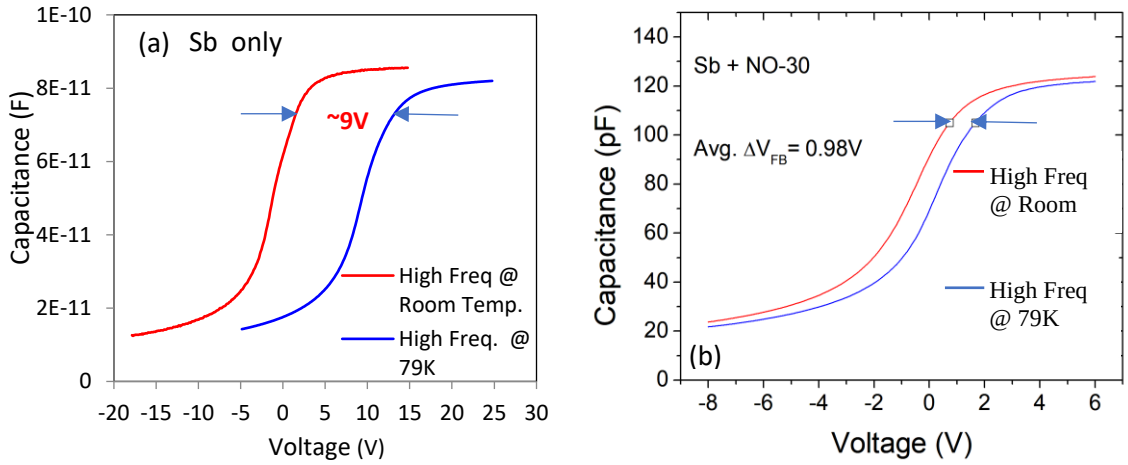


Fig.3.4.4. Low temperature 100 kHz C-V on capacitors with Sb implantation (a) without NO annealing and (b) with NO annealing [11].

room temperature indicating a large density of acceptor-like traps near the interface that are energetically located very close to the conduction band of 4H-SiC based on Gray-Brown theory [12]. While in the case of the sample with NO annealing, the flat band voltage shift is as small as the sample does with NO annealing without Sb (not shown). When Sb freezes out, the device behaves like a unpassivated device.

To verify the mechanism by which Sb at the SiO_2/SiC interface improves the channel mobility of 4H-SiC MOSFETs, constant capacitance deep level transient spectroscopy (CCDLTS) measurements were performed on both NO annealed and Sb implanted 4H-SiC MOS capacitors.

Table 3-3. Sample identification and fabrication processes

Sample	Sb implant dose	Sb activation anneal	NO anneal time	Device area
NO-120	X	X	120 mins	$20x10^{-4}$ cm^2
Sb+NO-30	$2.5x10^{13}/cm^2$	1650°C	30 mins	$20x10^{-4}$ cm^2
2Sb+NO-30	$5.0x10^{13}/cm^2$	1650°C	30 mins	$20x10^{-4}$ cm^2

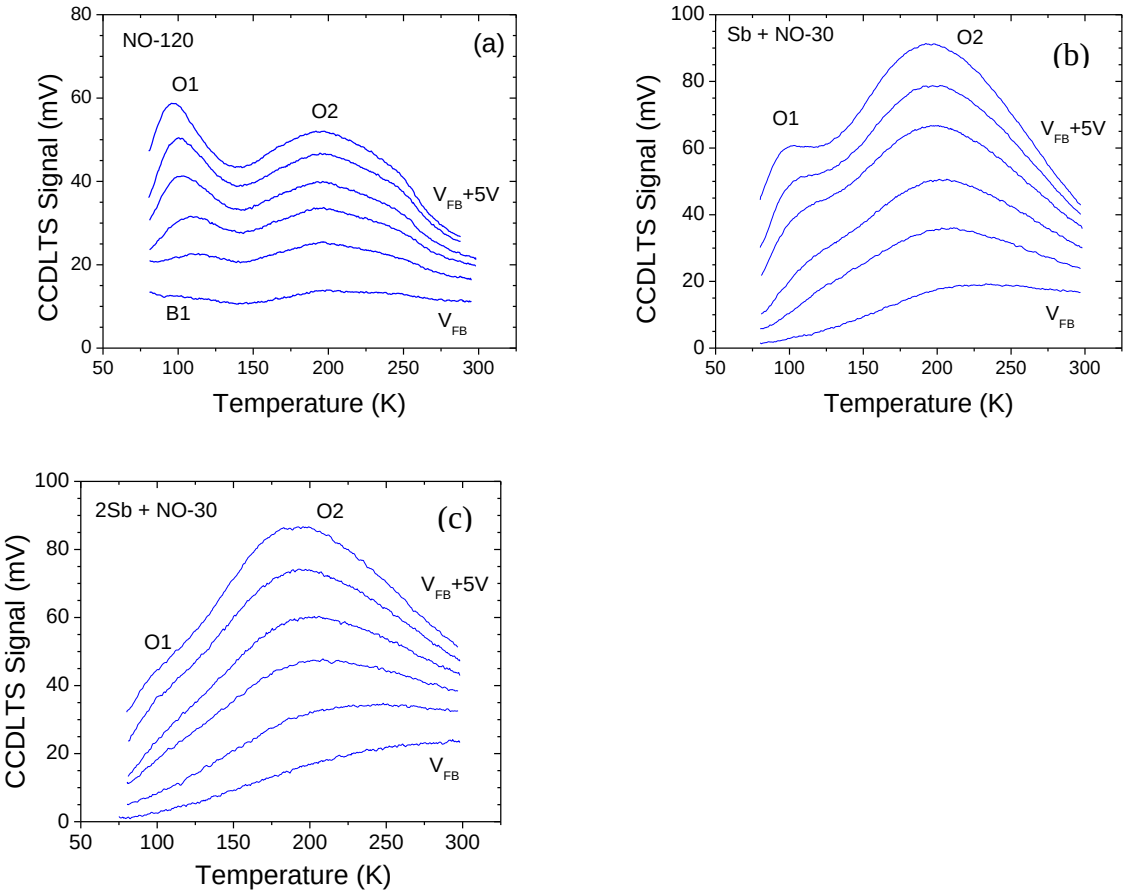


Fig.3.4.5 CCDLTS spectra of samples that were (a) NO annealed for 120 mins, (b) NO annealed for 30 mins with Sb dose of $2.5x10^{13}/cm^2$, and (c) NO annealed for 30 mins with Sb dose of $5.0x10^{13}/cm^2$ [5]. The constant capacitance was 37 pF and the electron emission rate was 465 s^{-1}.

All the CCDLTS measurements discussed in this study were performed at Simon Fraser University. Sample identification and fabrication processes are shown in Table 3-3.

Fig.3.4.5 [5] is CCDLTS spectra in the temperature range of 80-300 K for each sample. Each one shows a series of spectra taken at increasing trap filling voltages where oxide traps are detected at trap filling voltages ranging from $V_p = V_{FB}$ to $V_p = V_{FB} + 5$ V. These spectra all show the same features, labeled O1 and O2, as the spectra reported previously for NO-annealed 4H-SiC

MOS capacitors [13]. These broad features are indicative of distributions of energy levels, with O1 centered at 0.15 ± 0.05 eV and O2 centered at 0.39 ± 0.1 eV. The O1 defects were suggested to be carbon dimers substituted for O dimers ($C_O = C_O$) in SiO_2 and the O2 defects to be interstitial Si (Si_i) in SiO_2, based on *ab initio* calculations of defect energy levels [14]. The areal trap density in each sample calculated from the peak CCDLTS signal, ΔV, when $V_p = V_{FB} + 5$ V is shown in Table 3-4.

Table 3-4. Density of the near-interface oxide traps calculated from the CCDLTS spectra.

Sample	Avg. N_{it} (O1)	Avg. N_{it} (O2)	Avg. N_{it} (CCDLTS)
NO-120	$2.4x10^{10}/cm^2$	$1.0x10^{11}/cm^2$	$1.2x10^{11}/cm^2$
Sb+NO-30	$1.3x10^{10}/cm^2$	$1.5x10^{11}/cm^2$	$1.6x10^{11}/cm^2$
2Sb+NO-30	$0.5x10^{10}/cm^2$	$1.3x10^{11}/cm^2$	$1.4x10^{11}/cm^2$

Since the CCDLTS signal continues to increase as V_p is further increased above $V_{FB} + 5$ V due to electrons tunneling into the oxide when the sample is biased in accumulation, this calculation underestimates the total near-interface oxide trap density [13]. However, it is useful for understanding the effects of these fabrication processes by comparing the O1 and O2 signals. The Sb implant does not seem to have effect on the O2 trap density but O1 trap density is reduced by a factor of 2 in sample Sb+NO-30 compared with NO annealed sample. O1 trap density is further reduced by a factor of 3 when the implanted Sb dose is doubled. However, the effect of Sb on the deeper O2 is minimal. Since O2 density is ~10 times higher than O1, the total effect of Sb on trap reduction is very small. This is consistent with the finding in previous studies [3, 11].

While O1 is reduced in Sb implanted samples, it cannot be ascertained that Sb chemically passivates near-interface defects by changing the bonding configuration and thus changing the defect energy level because: 1) Sb could compensate the defects close to the conduction band edge since they are acceptor-like; 2) The band bending and hence surface Fermi level may be affected by Sb donors.

CCDLTS measurements taken with $V_p \leq V_{FB}$ in depletion, were also performed to detect defects in SiC introduced by Sb ion implantation. It was taken at temperatures down to about 45 K revealing traps in SiC having energy levels close to E_C. At low temperatures, only the shallower donor is ionized and the deeper N donor level (N2) acts as a trap [15], as is seen in the CCDLTS spectrum from 'Sb+NO' sample in Fig.3.4.6. The only ion-implantation defect observed in Sb-implanted sample is with an activation energy of ~0.2 eV with very low concentration. Also, the

N2 defects in ‘Sb+NO’ sample is much lower than the one induced by N implantation in 4H-SiC MOS capacitors reported by another group [16]. Clearly, annealing at 1650°C combined with dry oxidation is effective in removing the dominant ion implantation induced defects.

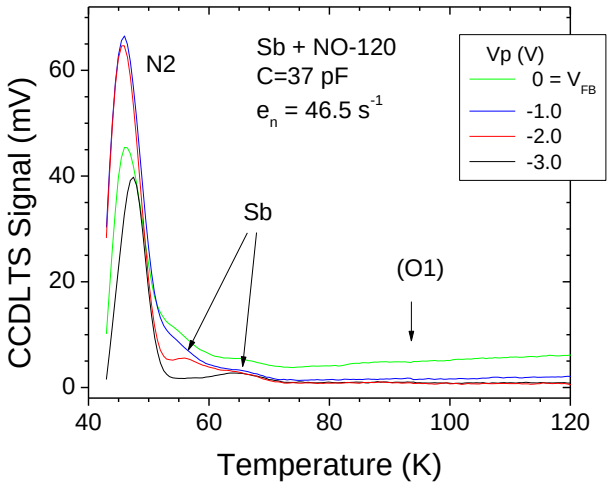


Fig.3.4.6. CCDLTS spectra of ‘Sb+NO’ sample with filling voltages decreasing from $V_p = V_{FB}$.

3.4.4 Threshold voltage, subthreshold slope and field-effect mobility

Threshold voltage V_{th} of MOSFETs with different implantation processes was characterized by drain current gate voltage (I_D–V_G) measurements at 293 K with a fixed drain voltage (V_D = 25 mV). Fig.3.4.7 (a) shows V_{th} increases with p-well doping concentration as

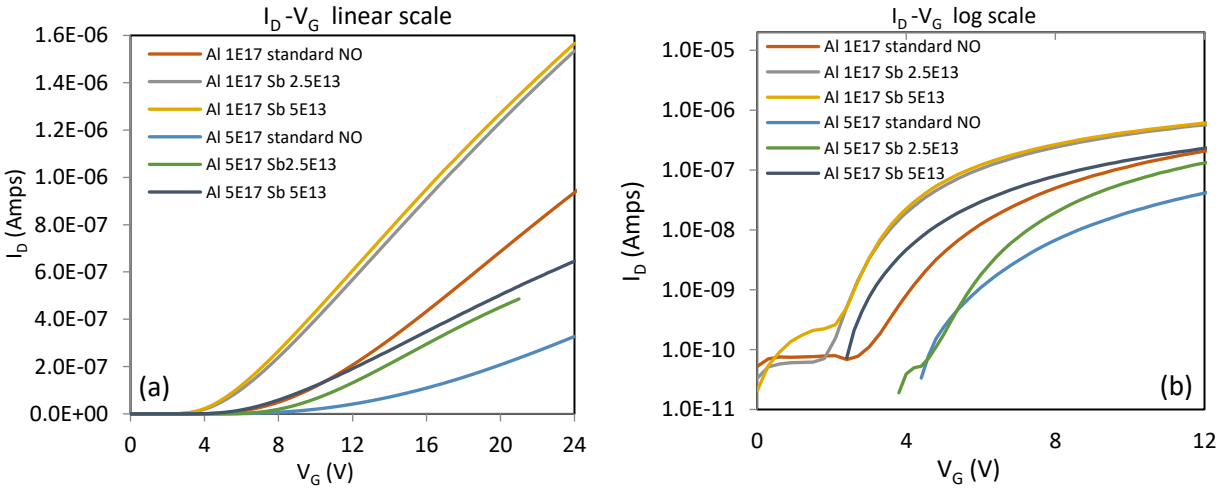


Fig.3.4.7. (a) Linear scale and (b) Log scale of I_D -V_G curves of MOSFETs at room temperature with heavy p-well doping with and without Sb counter-doping.

expected. In addition, V_{th} of devices with Sb counter-doping shifts to left compared with standard NO annealing device, as a result of compensation of the Al acceptors in the surface region by Sb donors. An improvement of subthreshold slope (SS) with Sb counter-doping was observed compared with standard NO as shown in Fig.3.4.7 (b). In addition, lower Sb dose of $2.5x10^{13}/cm^2$ shows slightly more improved subthreshold slope than higher dose of $5.0x10^{13}/cm^2$ for the devices with p-well doping of $5.0x10^{17}/cm^3$. However, no significant difference of SS was observed between higher and lower Sb doses for the devices with p-well doping of $1x10^{17}/cm^3$.

Field-effect mobility of the fabricated devices as a function of gate voltage is shown in Fig.3.4.8. With p-well doping of $1x10^{17}/cm^3$, the peak mobility is as twice as that with p-well

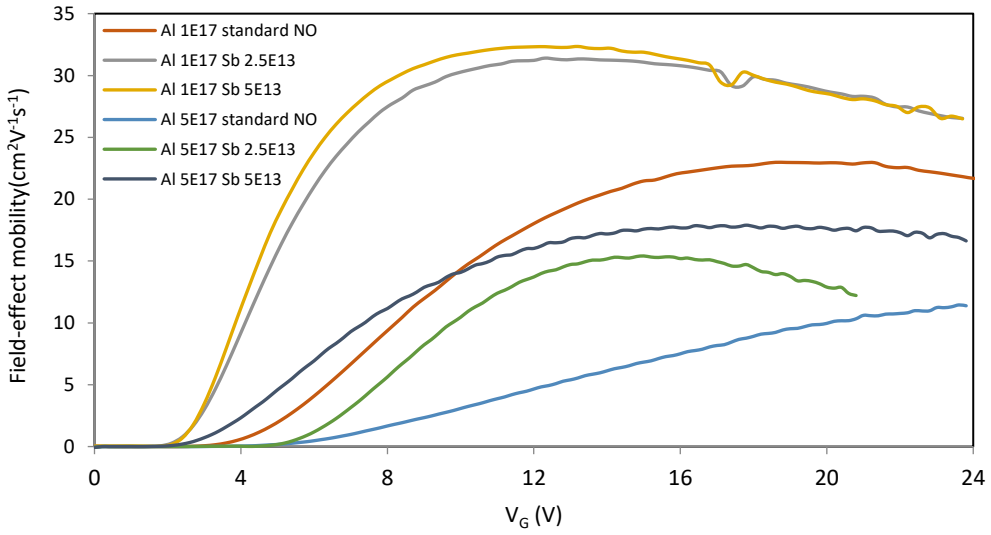


Fig.3.4.8. Field-effect mobility of MOSFETs with heavy p-well doping with and without Sb counter-doping.

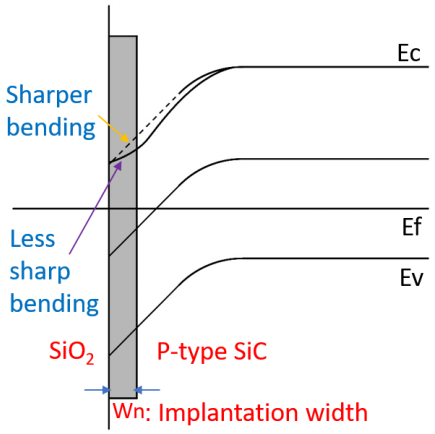


Fig.3.4.9. The mechanism of Sb counter-doping effect.

doping of $5x10^{17}/cm^3$ with or without Sb counter-doping. However, only a slightly peak mobility difference between Sb dose of $2.5x10^{13}/cm^2$ and $5.0x10^{13}/cm^2$ is observed with the same trend at high gate voltage. For $5x10^{17}/cm^3$ p-well doping, the mobility keeps a relatively high value within a larger range of gate voltage with $5.0x10^{13}/cm^2$ Sb dose compared with $2.5x10^{13}/cm^2$ while peak mobility is similar. All the slight differences between Sb doses of $2.5x10^{13}/cm^2$ and $5.0x10^{13}/cm^2$ are probably due to Sb loss during fabrication processes, which results in similar number of activated Sb ions. SIMS measurement on the companion capacitors shows that over ~85% of Sb got lost from $2.5x10^{13}/cm^2$ capacitor and ~90% of Sb got lost from $5.0x10^{13}/cm^2$ capacitor, which is consistent with the mobility results. Even with very low residual dose, Sb counter-doping effect is still obvious. The field-effect mobility from our study with p-well doping of $5x10^{17}/cm^3$ at room temperature is in good agreement with the one reported by C. Strenger *et al.* with N_2 annealed devices [17]. The mechanism of Sb counter-doping shown in Fig.3.4.9 on the reduction of V_{th} and the improvement of SS and μ_{FE} is probably: 1) Higher free carrier density at the same V_G and more efficient screening of Coulomb scattering; 2) Less filled traps at V_{th} due to less band bending; 3) Lower surface roughness due to lower electric field at the surface with the same carrier density.

To better understand the scattering mechanism on field-effect mobility for the Sb implanted MOSFETs with different p-well doping concentrations, the mobility of MOSFETs as a function of oxide field with and without Sb implantation have been compared at room temperature. Fig.3.4.10 shows the peak field-effect mobility increases with decreasing p-well doping

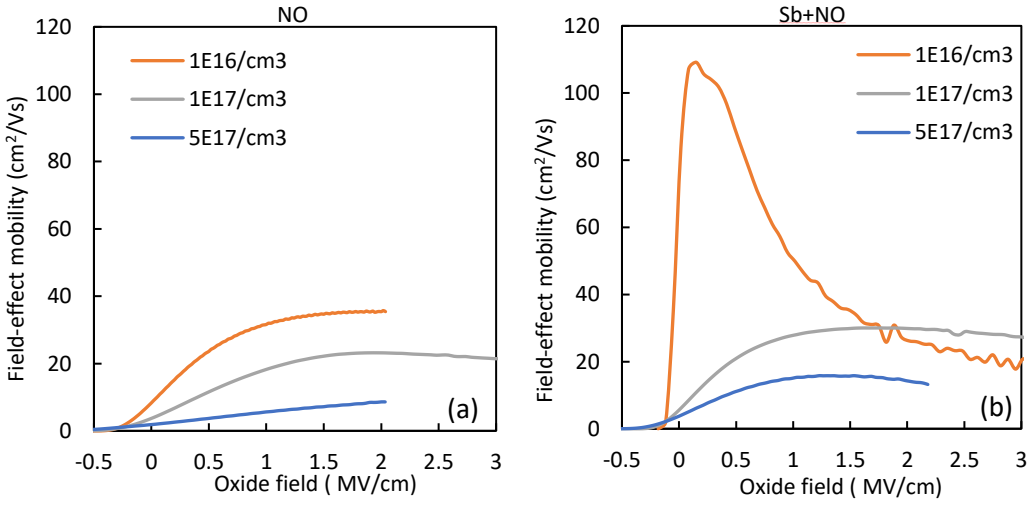


Fig.3.4.10. Field-effect mobility of MOSFETs with heavy p-well doping (a) without and (b) with Sb counter-doping. Sb dose is $2.5x10^{13}/cm^2$.

concentration for both ‘NO’ and ‘Sb+NO’ MOSFETs. Also, field-effect mobility is higher with Sb implantation than without Sb implantation at the same p-well doping concentration. This is caused by a reduction in the bulk potential therefore a reduction of filled interface traps at strong inversion with lower p-well doping concentration as well as lower scattering centers. However, this is only obvious at low oxide field region due to the dominance of higher free carrier density at low fields. As the oxide field increases, surface phonon scattering and surface roughness start to play a role. For NO annealed MOSFETs, it has been observed with a universal mobility at high oxide fields dominant by surface roughness scattering [11]. In Fig.3.4.10 (a), it is not clear if there is a universal mobility behavior with different p-well doping concentrations since the measurement range did not include high enough oxide fields. For ‘Sb+NO’ MOSFETs shown in Fig.3.4.10 (b), the trend of mobility merging at high fields was observed.

3.5 Summary

Antimony was successfully implanted as surface counter-dopants into SiC with heavily doped p-wells to improve the channel transport of 4H-SiC MOSFETs. The Sb profile in SiC have been characterized by SIMS measurement and it was found that the as implanted Sb profile is similar to the simulated profile. Also, the p-well doping estimated by high frequency C-V measurement on the p-type capacitor on the same wafer with the MOSFETs is in good agreement with the simulated concentration as well. After transferring the carbon removing process from RIE to O_2, Sb loss was significantly improved. The challenge for Sb channel doping is to obtain an optimal Sb dose remain after fabrication process to achieve the best counter-doping effect with normally-off characteristics. Although the Sb loss was ~85% due to the oxidation process after the process improvement, the best counter-doping effect was observed in this experiment.

High-low frequency C-V measurement, CCDLTS and I_D-V_G measurement were performed on the companion capacitors and MOSFETs with various processes to characterize interface trap density, threshold voltage, subthreshold slope and field-effect mobility. The results show the primary effect of Sb is counter-doping while it does not have too much influence on trap passivation. The field-effect mobility on the MOSFETs with and without Sb implantation reveals the effects of Coulomb scattering at low oxide fields and phonon scattering as well as surface

roughness scattering at high oxide fields. Sb counter-doping effect is only obvious at low oxide fields is because Coulomb scattering is the dominant factor at low fields.

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Chapter 4

Borosilicate glass (BSG) as gate dielectric for 4H-SiC MOSFETs

Borosilicate glass (BSG) as gate dielectric for 4H-SiC MOSFETs was first reported by Okamoto *et al.* [1]. By post oxidation annealing using boron nitride planar diffusion source, a low interface trap density and a high channel mobility of ~100 $cm^2/V \cdot s$ for a wide range of surface transverse electric fields have been obtained. The mechanism of B diffusion for low interface trap density and high channel mobility has been suggested to be stress relaxation of SiO_2 by B doping [1]. It also has been reported that a significant improvement of the electrical forward characteristics of VDMOS, including channel mobility and specific on-resistance was realized by a combination of thermal oxide treated by boron diffusion and deposited TEOS oxide [2]. Also, a relatively good threshold voltage stability under both positive and negative bias stress at room temperature has been reported by Cabello *et al.* [3]. However, threshold voltage stability with high temperature bias stress has not been widely studied. While highlighting the advantage of BSG gate dielectric from the point of view of interface traps and channel mobility, more study is absolutely necessary to understand the mechanism of B treatment on thermal oxide to utilize the attractive properties of BSG on power MOSFETs.

4.1 The chemical structure of BSG

The diffusion of boron into thermally grown SiO_2 has been continuously studied because of the importance of this effect in CMOS manufacturing, where boron is used as BSG or BPSG for dielectric passivation as a network former which allows better glass flow [4, 5]. On the other hand, from the device reliability point of view, the diffusion of boron from doped poly Si gates through SiO_2 into the channel region of MOSFETs can cause an undesirable shift in the threshold voltage and degrade gate oxide reliability [6].

Obtaining information on the structure of the glasses is not only necessary for understanding the nature of the glass state, but also for directed synthesis of materials with defined properties. The properties of BSG are determined to a significant degree by the coordination and structural position of boron in BSG, which can change its coordination number from three to four

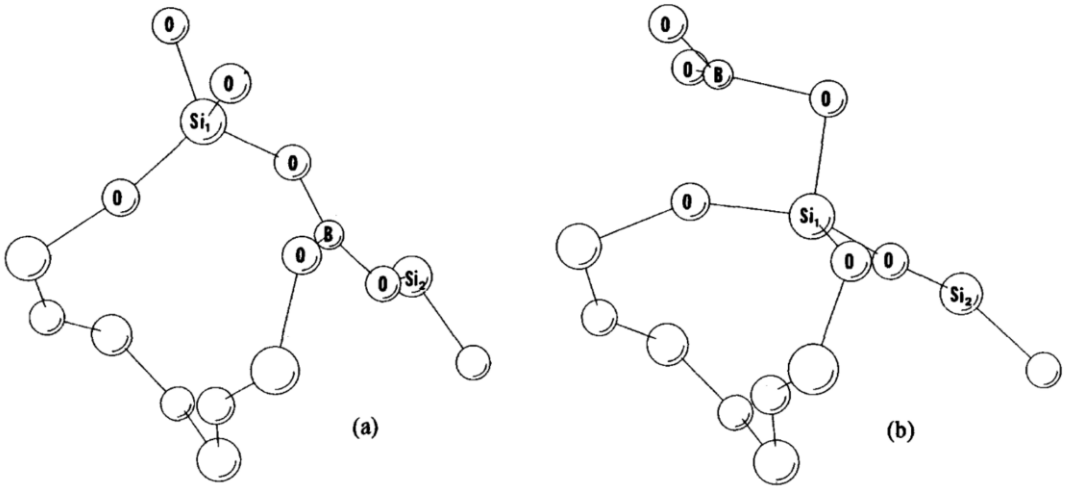

Fig.4.1.1. Possible initial (a) and final (b) configurations for boron exchange with a silicon in silicon dioxide [8].

as a function of the composition. Varying the concentration of boron in the glasses allows controlling the properties within wide limits, which is of interest with respect to using BSG as promising materials in materials science [4]. It has been reported that in bulk glass, boron has a tendency to three-coordinate with oxygen [7]. Hence, boron diffusion was suggested to involve a process in which threefold boron and fourfold silicon exchange positions, with corresponding oxygen motion to maintain the proper coordination [8]. However, the nearby silicon will not be equally good candidate to be exchanged with a boron. If consider the three silicon atoms connected to the boron through its three neighboring oxygens, a possible geometry is shown in Fig.4.1.1 (a) [8]. Si_1 is one of the silicon atoms that lies below the plane of the three oxygens and Si_2 lies nearly in the plane of the three oxygens. Looking at the structure, we can imagine a boron exchanges with a Si_1 instead of Si_2 to drag along a neighboring oxygen to maintain its fourfold coordination. Thus, Fig. 4.1.1 (a) and (b) [8] show how such an exchange could take place.

The diffusion of boron into thermally grown silicon dioxide requires high concentration of B as a diffusion source at high temperature. The addition of boron to silicon dioxide can significantly reduce the temperature in the glass transition and melting. If the diffusion temperature is higher than the melting temperature, the liquidation will occur. Subsequently, the neighboring undoped oxide will dissolve rapidly until the consequent dilution of the liquid region reduces the concentration of boron and the molten region begins to solidify [9]. This dissolution process is much more rapidly than solid-phase diffusion and thus is the primary means of transport when it

occurs. It can occur repeatedly until the B concentration is uniform in BSG layer. The dissolution process is illustrated schematically in Fig.4.1.2 [10], which shows the formation of a thick layer of diluted BSG with 18% B_2O_3 from the original thinner BSG source with 35% B_2O_3.

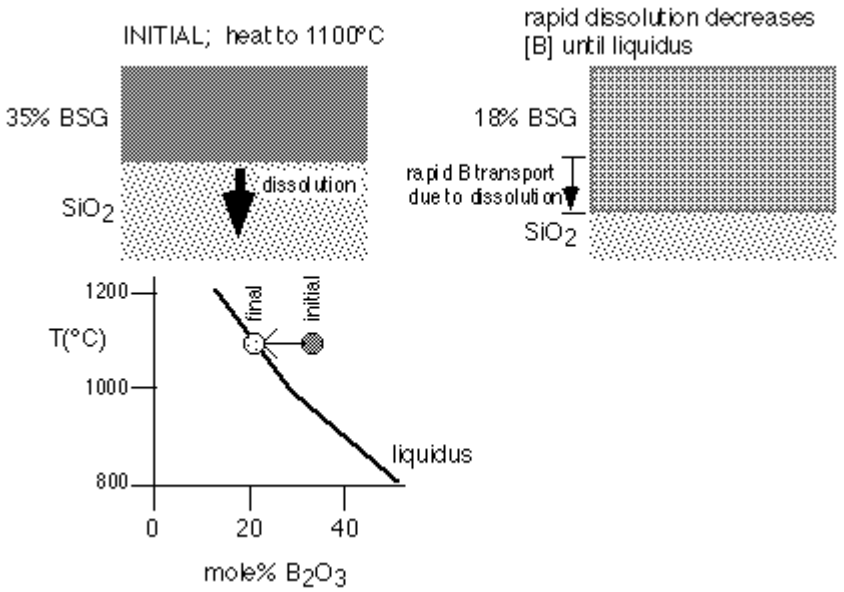

Fig.4.1.2. The kinetics of dissolution in the liquid/solid mixture of BSG/oxide, accompanied by the transport of B_2O_3 [10].

The diffusion of B into thermally grown silicon dioxide is also strongly influenced by the ambient: H_2 and F can cause 10-40x increases in diffusivity vs. N_2 ambient because H_2 and F both act to reduce the total number of bonds holding silicon atoms while N_2 increases the coordination and density of the lattice [10]. Table 4-1 shows the typical values of diffusivity of B in SiO_2 with ambient of H_2 and N_2 at 1100°C.

Table 4-1. Typical values of diffusivity of B in SiO_2 with ambient of H_2 and N_2 at 1100°C.

ambient	medium	Diffusivity (cm^2/s)
H_2	SiO_2	$1x10^{-15}$
N_2	SiO_2	$3x10^{-17}$

4.2 The formation of BSG

4.2.1 Planar diffusion source (PDS) annealing

In this chapter, most of the devices with BSG dielectric were formed by post oxidation annealing using a 3-inch B_2O_3 planar diffusion source (Techneglas, GS-139) purchased from

Techneglas. This source was produced from high-purity raw materials containing B_2O_3 and the extremely stable oxides of BaO, MgO, Al_2O_3 and SiO_2 with tight limits by unique manufacturing process. The typical impurity analysis of the source is shown in Table 4-2, which are undesirable

Table 4-2. Typical impurity ananlysis of B_2O_3 source

Metal	PPM	Metal	PPM
Na	2	Pt	<5
K	<1	Rh	<1
Li	<1	As	<0.5
Fe	2	P	<5
PB	1	Sb	<0.5
Cr	2	Bi	<0.5
Cu	0.5	V	<1
Sn	<.05	Co	<2
Zn	<2	Mo	1
Ti	2	Ca	20
Ni	2	Sr	20
Ag	<0.5	Mn	<1
Au	<0.5		

contaminations for V_{th} stability. Also, Na can improve mobility as well. Therefore, the effect of B% change on electrical results was studied in this work to be sure the improvement of channel transport by B, which will be discussed in the following sections.

Fig.4.2.1 (a) shows the picture of the diffusion annealing furnace that has been used for BSG formation. The formation of BSG in this furnace includes two steps: 1) Place the device in

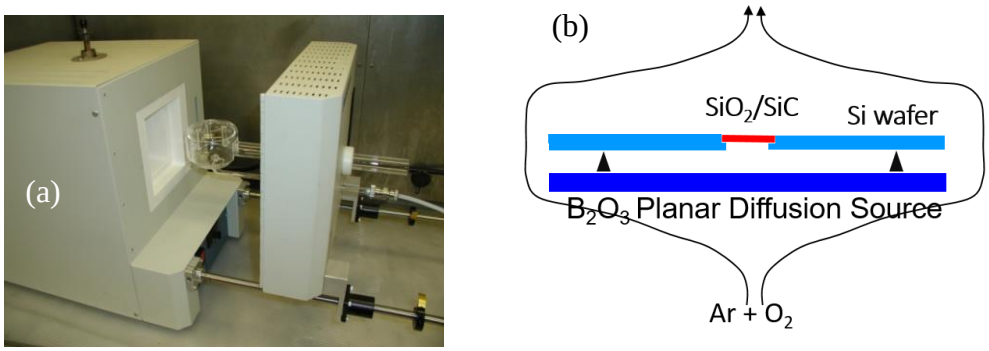

Fig.4.2.1. (a) The picture of the diffusion annealing furnace. (b) Schematic of the layout of the PDS furnace chamber.

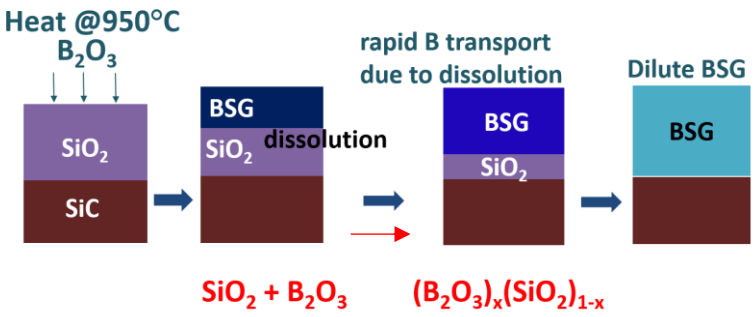

Fig.4.2.2. The formation of BSG by PDS at 950°C.

the chamber with the thermal oxide facing to the B_2O_3 source sitting on a support structure with ~1 cm spacing, as shown in Fig.4.2.1 (b). Flow Ar (50 sccm) and O_2 (5 sccm) at 950°C for 30 mins; 2) Flow Ar at 50 sccm at 950°C for 2 hours after taking the B_2O_3 source out of the furnace. The kinetics of BSG formation is depicted schematically in Fig.4.2.2. The B_2O_3 planar diffusion source was conditioned at 1015°C for 4-5 hours before each diffusion process to obtain stable output of B.

4.2.2 Plasma-enhanced chemical vapor deposition (PECVD)

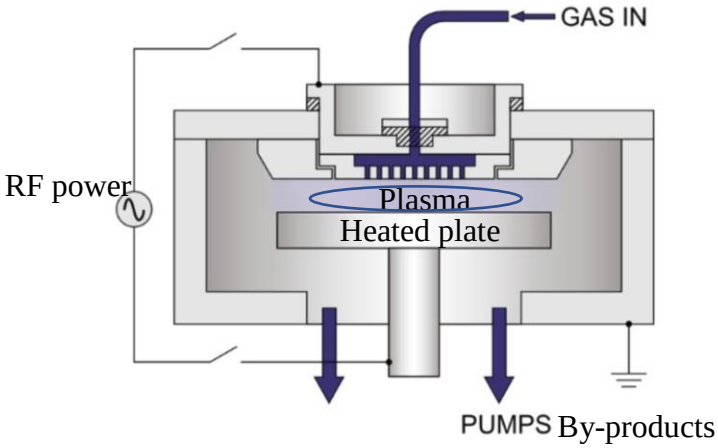

Fig.4.2.3. A schematic diagram of the PECVD system.

Plasma-enhanced chemical vapor deposition (PECVD) is a chemical vapor deposition process for thin film deposition, where chemical reactions are involved in the process and occur after creation of a plasma of the reacting gases. The deposition of PECVD BSG in this study was all performed in the Oxford 100 PECVD system at Cornell university after a thin interlayer oxide (~15 nm) was thermally grown on SiC. Without the interlayer, the PECVD BSG was too leaky. The PECVD process was carried out employing the precursor gases silane (SiH_4), nitrous oxide (N_2O), and diborane (B_2H_6) at 400°C and 1.4 Torr. The BSG thickness and B concentration can be adjusted by changing the gas flow ratio. Our required BSG thickness and B concentration were 60 nm and 2% for this study. Fig.4.2.3 shows a schematic diagram of the PECVD system. The PECVD reaction process to produce BSG is given by [11]

$$(1-x)SiH_4 + xB_2H_6 + 2[O_2] \xrightarrow{N_2O} (SiO_2)_{1-x}(B_2O_3)_x + [H_2]$$

For PECVD BSG, both BSG thickness and B concentration can be adjusted by changing the ratio of precursor gases. However, the particle contamination under continuous plasma operation or at the end of the process when the plasma is turned off have harmful effects on device performance, reliability and yield [12]. Compared with PECVD BSG, it is more difficult to reproduce results from BSG formed by PDS annealing since the whole process is not under precise control. The B concentration shows variation from run to run, which produces devices with different electrical characteristics. The contaminations during the annealing process from the source and ambient also cause poor device performance, especially the stability under bias temperature stress. However, in this study, BSG formed by PDS generally results in higher B concentration than PECVD BSG, which results in lower interface trap density and higher field-effect mobility.

4.3 B concentration characterization

4.3.1 X-ray photoelectron spectroscopy (XPS)

X-Ray Photoelectron Spectroscopy (XPS), also known as Electron Spectroscopy for Chemical Analysis (ESCA), is an analysis technique used to obtain chemical information about the surfaces of solid materials. Fig.4.3.1 shows the basic components of a XPS system. XPS spectra are obtained by irradiating a material with a beam of X-rays while simultaneously measuring the kinetic energy and number of electrons that escape from several nanometers of the material being analyzed. From the binding energy and intensity of a photoelectron peak, the

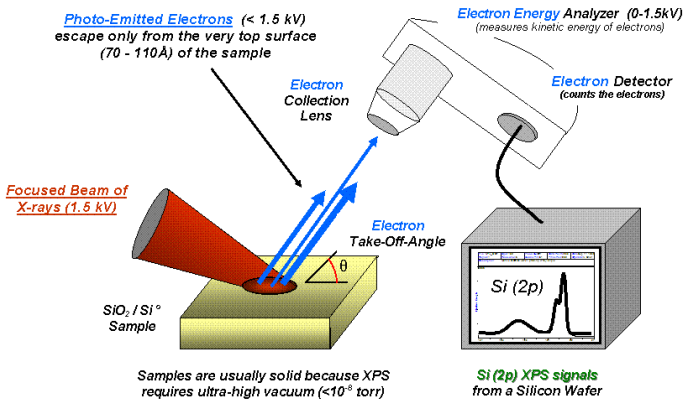

Fig.4.3.1. Basic components of a XPS system.

elemental identity, chemical state, and quantity of a detected element can be determined. The average depth of analysis for an XPS measurement is approximately 5-10 nm.

To investigate the B concentration in the oxide and SiC on the devices with PDS BSG and PECVD BSG, XPS measurements were carried out on the MOS capacitors after removing gate material with the detecting limit of 0.01%. Fig.4.3.2 shows the XPS spectra of different samples through the same thermal oxidation and B_2O_3 PDS annealing process flow (thermal oxidation at 1150°C for 10 hours, B_2O_3 PDS annealing at 950°C for 30 mins and drive in at 950°C for 2 hours) but from different experiment runs. The B concentration is calculated based on the detection of B1s. As mentioned in previous section, it clearly shows a variation of B concentration from

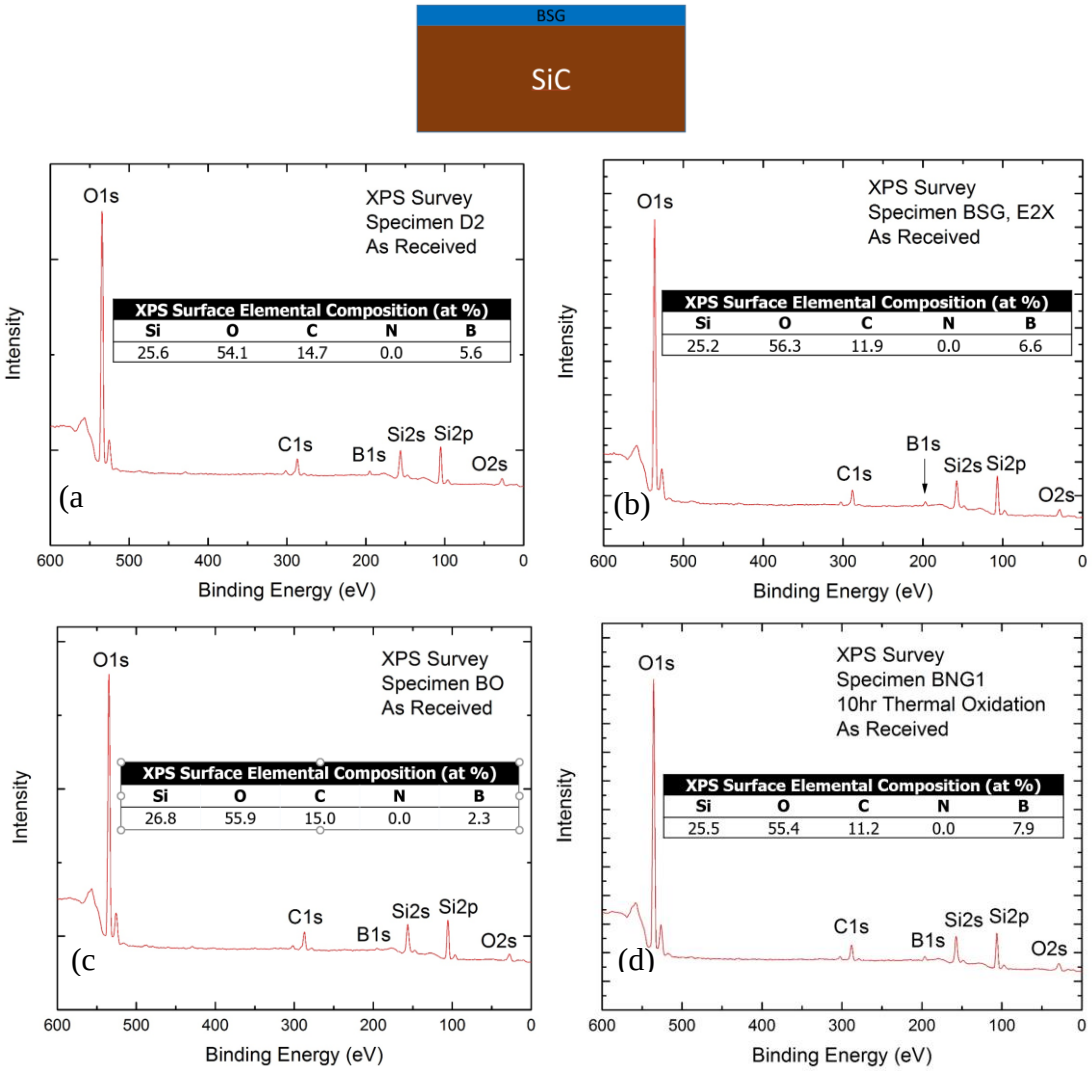

Fig.4.3.2. XPS spectra of different samples through the same thermal oxidation and B_2O_3 PDS annealing process flow but from different experiment runs.

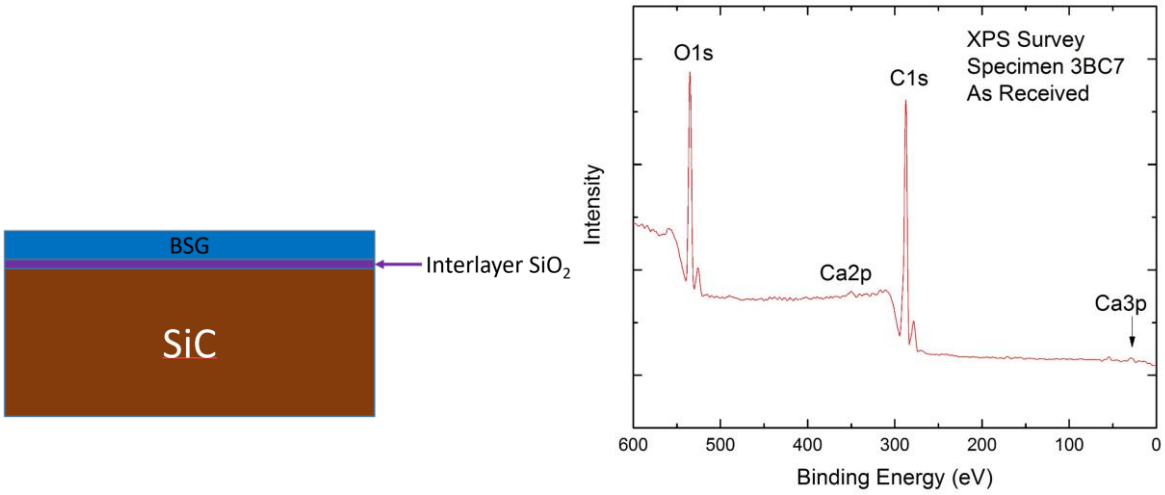

Fig.4.3.3. XPS spectra of PECVD BSG.

experiment run to run. The XPS spectra of PECVD BSG shown in Fig.4.3.3 indicates no B signal was detected by XPS measurement, which did not match up with the expected concentration of 2%. This might be due to the calculation error caused by detection limit of XPS measurement. The detection limit or the quality of a XPS spectra depends both on sample composition and the localized signal intensity, which may change due to instrumental measurement conditions, such as X-ray flux and the area of sample available for analysis.

Unlike phosphosilicate glass (PSG) with a remnant unetchable layer by buffered oxide etch (BOE) [13], no B signal was detected by XPS measurements in PDS BSG or PECVD BSG after removing the oxide layer by BOE, as shown in Fig.4.3.4.

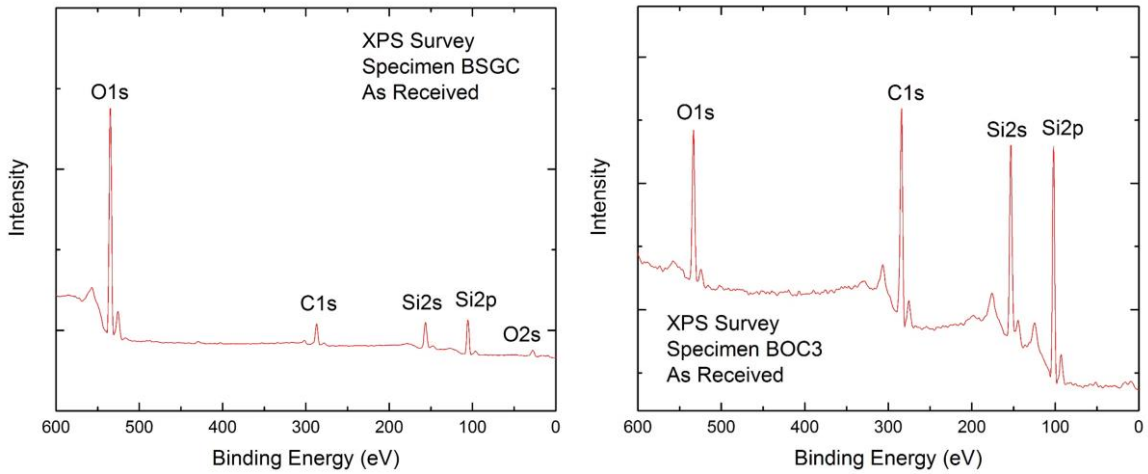

Fig.4.3.4. XPS spectra of (a) PDS BSG and (b) PECVD BSG after removing oxide.

XPS measurements on thin BSG

Due to the passivation effect of B on interface traps of BSG/4H-SiC in 4H-SiC MOSFETs (electrical results will be shown in next sections), a thin BSG layer would be promising as the interlayer between thermal oxide/PECVD oxide and SiC for further improvement of channel transport with lower contamination of gate oxide compared to a think BSG as gate dielectric. Therefore, thin BSG with different thicknesses were grown by different oxidation conditions in this experiment, as summarized in Table 4-3 to investigate the correlation between B concentration and BSG thickness. The B concentration and BSG thickness were characterized by XPS and atomic force microscope (AFM), respectively. Based on these results, no obvious variation of B concentration with BSG thickness was observed at this range, which may be because B concentration is not sensitive to BSG thickness when it is within ~10 nm.

Table 4-3. Summary of thin BSG with different oxidation conditions

sample	Oxidation temperature	Oxidation time	B_2O_3 PDS annealing	Drive in	Oxide thickness	B concentration
O1	950°C	2 hours	30 mins	1 hour	2.77 nm	8.1%
O2	1000°C	2 hours	30 mins	1 hour	5.77 nm	8.2%
O3	1100°C	2 hours	30 mins	1 hour	6.95 nm	9.6%
O4	1150°C	2 hours	30 mins	1 hour	11.74 nm	9.2%

XPS measurements on BSG with different drive-in times

The effect of drive-in time on B concentration and BSG thickness was also studied by changing drive-in time after the same PDS annealing process. The results are summarized in Table 4. The B concentration as a function of drive-in time is shown in Fig.4.3.5. The results indicate that BSG thickness increases with drive-in time while B concentration decreases with drive-in time and BSG thickness. It was expected to see the highest B concentration in the sample without drive-in process. However, no B was detected by XPS in this sample. It is possible that B was deposited on top of SiO_2 by PDS annealing but no dissolution occurred without drive-in process and in return

Table 4-4. Summary of BSG results with different drive-in times

sample	Oxidation temperature	Oxidation time	B_2O_3 PDS annealing	Drive-in	Oxide thickness	B concentration
D0	1150°C	10 hours	30 mins	0 hour	65 nm	0%
D1	1150°C	10 hours	30 mins	1 hour	77 nm	5.3%
D2	1150°C	10 hours	30 mins	2 hours	77 nm	5.6%
D3	1150°C	10 hours	30 mins	3 hours	85 nm	4.2%

B was removed during gate metal striping. Another possibility is B concentration is too low, which is below the detection limit of XPS measurement. In this case, the maximum B concentration would occur when the drive in time is ~2 hours.

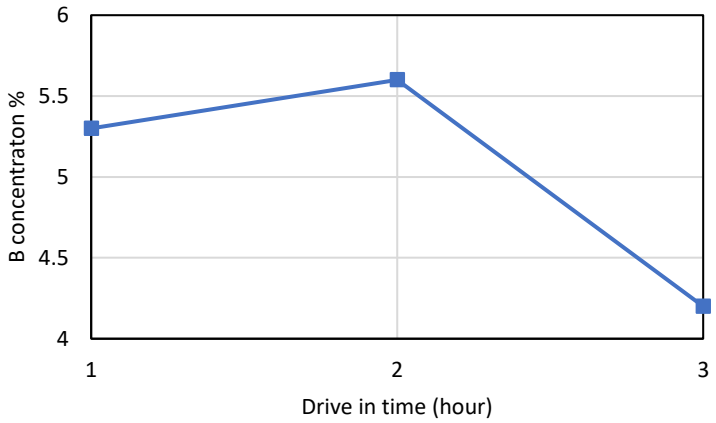

Fig.4.3.5. B concentration as a function of drive in time.

4.3.2 Secondary ion mass spectrometry (SIMS) for B profile

To obtain the accurate B distribution profile in both oxide and SiC of the samples with PDS BSG and PECVD BSG and correlate it to the electrical results, SIMS measurements were performed with O_2 ions as the primary beam on MOS capacitors that have been measured by XPS since XPS does not destroy samples. Fig.4.3.6 (a) shows the B profile in BSG/SiC of the sample from Fig.4.3.2 (c) by SIMS with detection limit of $4x10^{16}/cm^3$. The profile indicates that for this

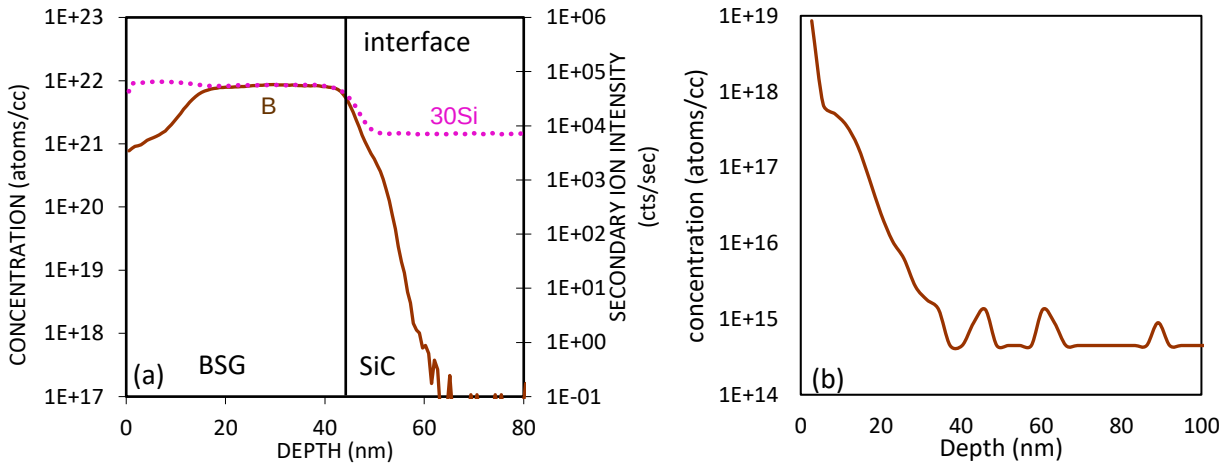

Fig.4.3.6. SIMS profile of B of sample annealed by PDS (a) in the oxide and SiC (b) in SiC after removing oxide.

particular sample, B distributes throughout the oxide with a concentration of ~$1x10^{22}/cm^3$ and decreases to ~$3x10^{21}/cm^3$ at the interface. The interface was defined at the depth where the half of the peak concentration of Si is. Similar SIMS profiles of B were obtained on other samples annealed by PDS (not shown) with different B concentrations. This B profile in SiC is not accurate due to the knock-on effect during SIMS measurement. Additional SIMS measurement was also carried out after stripping oxide. The result shown in Fig.4.3.6 (b) shows B penetrates ~40 nm into SiC down to the detection limit of $3x10^{14}/cm^3$. Most of the B is confined to the top ~10 nm with total dose of ~$2x10^{13}/cm^2$.

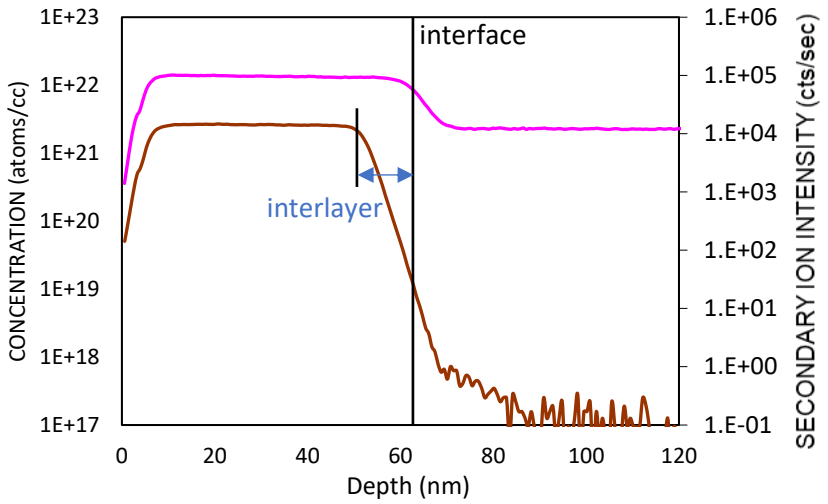

Fig.4.3.7. SIMS profile of B of sample with PECVD BSG.

Fig.4.3.7 shows the SIMS profile of B of the sample from Fig.4.3.3 with PECVD BSG with detection limit of $4x10^{16}/cm^3$. The B concentration in the oxide is ~$2.6x10^{21}/cm^3$ and decreases to ~$7.88x10^{18}/cm^3$ at the interface. It is clearly showing an interlayer in the SIMS profile with ~10 nm.

The atomic B percentage to SiO_2 in the bulk of the oxide and at the interface from SIMS measurement was also calculated. The B percentages from XPS and SIMS for two samples shown above are summarized in Table 4-5. The B concentration through the top of the oxide with several

Table 4-5. The atomic B percentage to SiO_2 in the bulk of the oxide and at the interface from XPS and SIMS

Sample	B% (XPS)	B% in the bulk of oxide (SIMS)	B% at interface (SIMS)
PDS BSG	2.3%	10.4%	4.0%
PECVD BSG	0%	3.16%	0.01%

nanometers is relatively low for both samples shown in SIMS profile, which can explain the lower B% from XPS measurement than that in the bulk of the oxide from SIMS for the PDS BSG sample. For PECVD BSG sample, the low B concentration near the surface might be lower than the detection limit of XPS, which result in 0% of B.

4.4 Electrical characterization of BSG-gated MOS devices

4.4.1 Breakdown field of BSG

It is important to understand the mechanism of the gate oxide breakdown of SiC MOS devices for making high quality SiC power devices. It is well known from past studies on Si-based devices that the gate oxide reliability is intimately related to several carrier tunneling effects, which finally result in oxide breakdown [14]. In SiC-based MOS structures, the oxide reliability is essentially limited not only by the oxide traps and interface traps but also by the smaller band offset between SiC and SiO_2 compared to silicon shown in Fig.4.4.1 (a) [16], leading to higher tunneling currents at high electric field governed by Fowler-Nordheim tunneling [15-17]. Electron injection occurs from SiC into gate oxide during F-N tunneling shown in Fig.4.4.1 (b) [15] and it is enhanced at high temperature and high electric field [16].

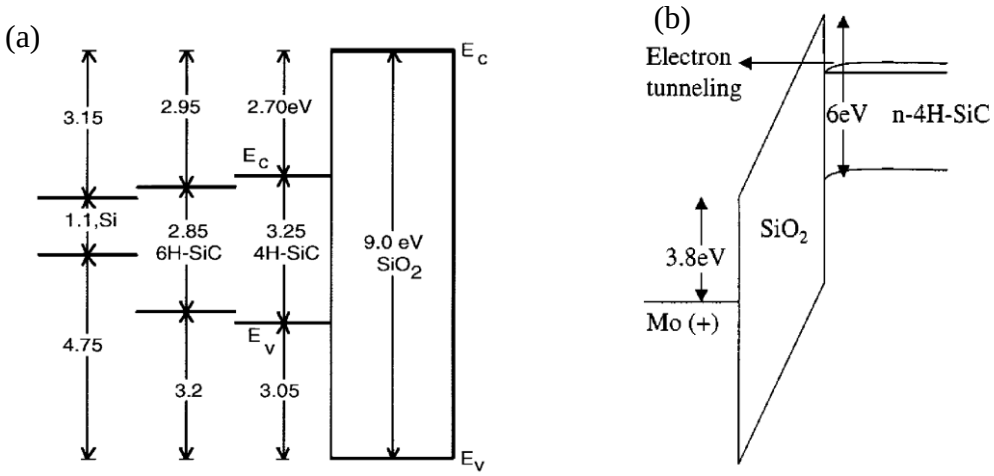

Fig.4.4.1. Energy band diagrams of (a) Si, 6H-SiC, 4H-SiC and SiO_2 illustrating barrier heights for F-N electron injection from semiconductor into the gate oxide [16] and (b) n-type 4H-SiC MOS capacitor in accumulation at high oxide fields showing electron tunneling [15].

Fig.4.4.2 presents typical I-V plots for n-type SiC MOS capacitors in accumulation with NO annealed (2 hours at 1175°) thermal SiO_2 and BSG as gate dielectric. Both capacitors are with Mo gate and the same gate area. The gate current is increasing through the oxide due to the onset of F-N tunneling of electrons. If we consider $1x10^{-6}$ A as the breakdown current, the breakdown field for NO and BSG capacitors is very similar, ~8.3 MV/cm.

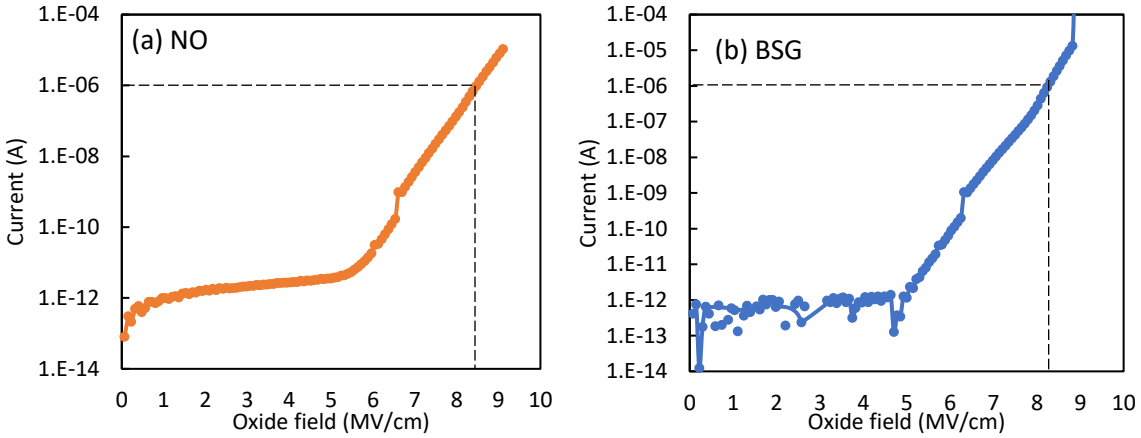

Fig.4.4.2. The oxide breakdown field of MOS capacitors with (a) NO annealing and (b) PDS BSG. The gate metal is Mo.

Fig.4.4.3 shows the oxide breakdown field of the PDS BSG capacitors with Al gate and Mo gate. The reason to plot out current density as a function of oxide field is because of different gate areas of these two samples. The results show the J-E curves with Al and Mo gate are overlapped with each other. The capacitor with Al gate breaks down at relatively lower oxide field than the capacitor with Mo gate, which may be due to some contamination during Al evaporation.

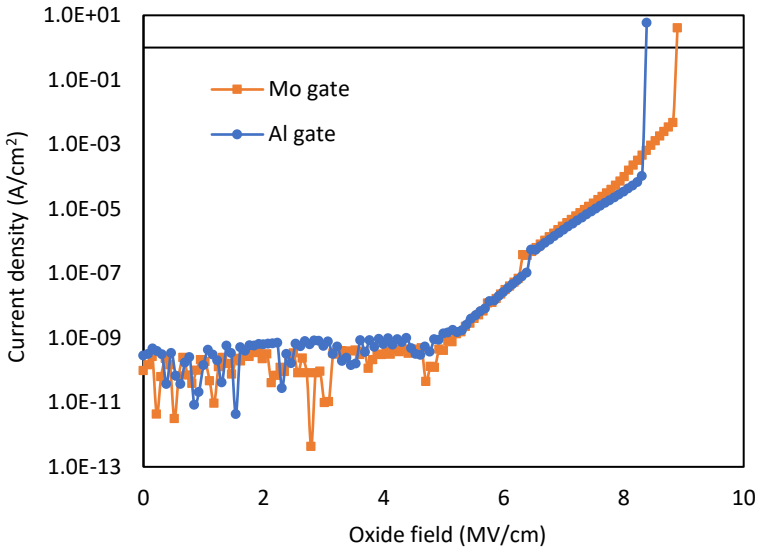

Fig.4.4.3. The oxide breakdown field of MOS capacitors of PDS BSG with Al gate and Mo gate.

4.4.2 Interface trap characterization

4.4.2.1 High-low frequency capacitance-voltage

As discussed in chapter 2, the interface trap density (D_{it}) profile in the band gap of 4H-SiC can be directly estimated from simultaneous hi-lo frequency capacitance-voltage measurements. The high frequency used in all the C-V measurements in this study is 100 kHz. The low frequency determines the depth of interface traps energetically in the bandgap. At lower frequency, interface states deeper into the bandgap can follow the pulse [18]. The limit of high and low frequency for estimation of D_{it} from C-V measurements depends on the emission time constant τ of electrons from interface states [19], which follows the equation [18, 20],

$$\tau(E) = \frac{1}{\sigma_n v_{th} N_C} \exp\left(\frac{E_C - E}{k_B T}\right) \tag{4.4}$$

where σ_n is the capture cross section, v_{th} is the thermal velocity of electrons, N_C is the effective density of states of the conduction band, E_C is the energy of the conduction band edge, k_B is the Boltzmann constant, and T is the temperature. Fig.4.4.4 [19] shows the emission time constant of electrons from the interface states as a function of the energy level, assuming a capture cross section of 1×10^{-15} cm^2. Horizontal lines indicated the frequency and energy limits of several

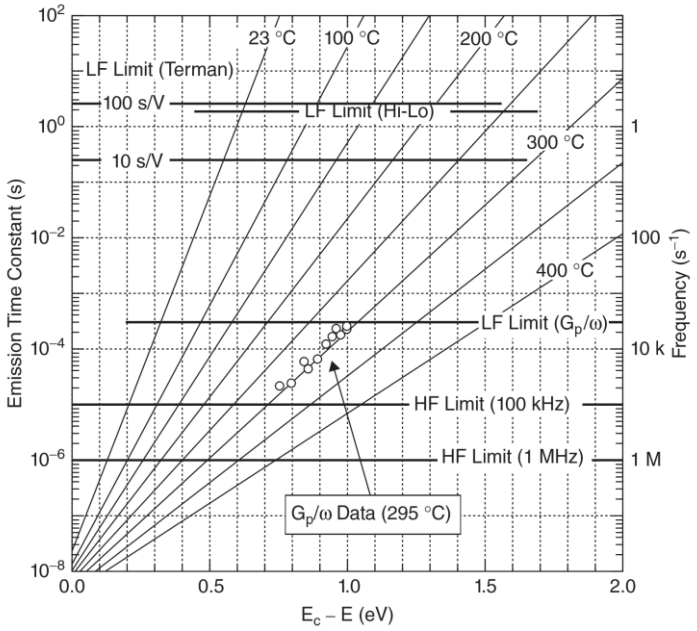

Fig.4.4.4. Emission time constant of electrons from the interface states as a function of the energy level, assuming a capture cross section of 1×10^{-15} cm^2 [19].

common MOS interface trap analysis techniques. For hi-lo C-V, the low frequency limit of ~0.9 Hz can detect the traps as deep as 0.6 eV from E_C while the high frequency limit of 100 kHz can detect the traps at 0.2 eV (flat-band) from E_C at room temperature. Therefore, the D_{it} profile extracted from hi-lo C-V with high frequency of 100 kHz is generally in the energy range from 0.2 eV to 0.6 eV.

Fig.4.4.5 (a) shows the comparison of D_{it} as a function of energy level from conduction band of 4H-SiC for n-type capacitors with NO annealing, PDS BSG and PECVD BSG. The energy level is determined from the surface potential, given by [21]

$$\frac{1}{(C_D + C_{it})^2} \approx \frac{1}{{C_D}^2} = -\frac{2\psi_s}{\varepsilon_{SiC} q N_D A^2} \tag{4.5}$$

where C_D, C_{it}, ε_{SiC} are the depletion capacitance, the interface trap capacitance and the dielectric constant of 4H-SiC. At sufficiently high frequency upon depletion, the interface states do not

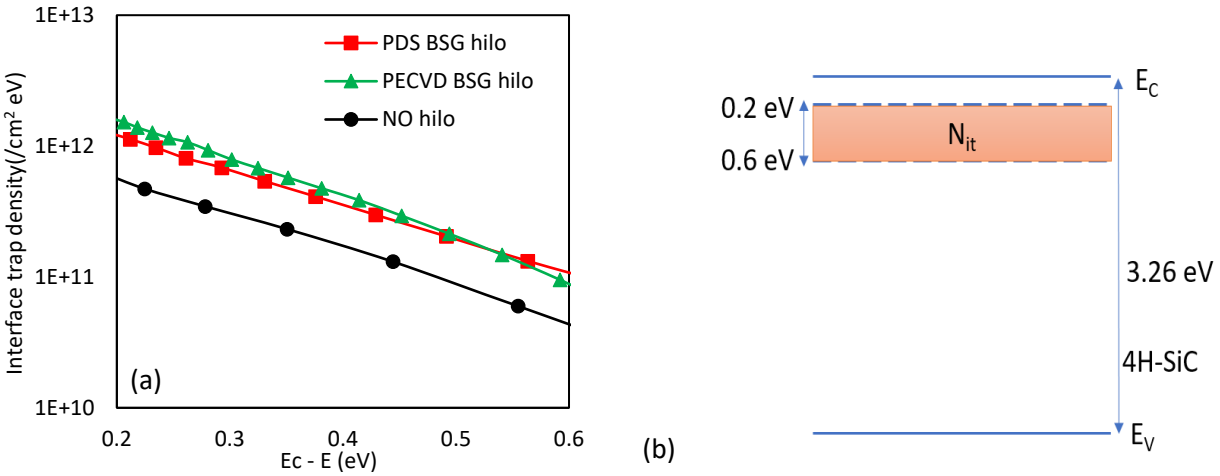

Fig.4.4.5. (a) Interface trap density profiles extracted by hi-lo C-V for n-type capacitors with NO annealing, PDS BSG and PECVD BSG. (b) The schematic of N_{it} integration range in 4H-SiC.

respond and no inversion carriers are generated. Therefore, C_D+C_{it} can be approximated as C_D. Compared to NO annealed capacitor, D_{it} detected by hi-lo C-V for BSG capacitor is overall higher. D_{it} for PECVD BSG is slightly higher than that for PDS BSG. Interface trap charge density N_{it} can be obtained by integration of D_{it}. The corresponding integration range of N_{it} in 4H-SiC from Fig.4.4.5 (a) is shown Fig.4.4.5 (b).

4.4.2.2 C-ψ_s analysis

The essential assumption is that the interface states fully respond to a frequency used for low frequency C-V measurements and do not respond at all to a frequency used for high frequency C-V. In return, all the interface states contribute to the low frequency capacitance and no contribution to the high frequency capacitance from interface states, which underestimates D_{it} due to the detection limit of fast traps that are able to respond to high frequencies above the one applied to the C-V measurements. The C-ψ_s analysis is a modified version of the hi-lo method by using the theoretical capacitance, which considerably extends the high frequency limit. The theoretical semiconductor capacitance and interface trap density can be obtained using the obtained surface potential by Eq.2.43 and Eq.2.44.

Fig.4.4.6 shows the comparison of D_{it} extracted by C-ψ_s analysis for the capacitors from Fig.4.4.5 (a). It is evident from the results that there is a big discrepancy of D_{it} between the hi-lo C-V and C-ψ_s analysis for NO capacitors. On the other hand, the D_{it} extracted from both methods is very similar for the PDS BSG capacitors compared to PECVD BSG and NO capacitors. The discrepancy can be attributed to the existence of very fast interface traps indicating that the primary effect of B is the reduction of such fast traps, similar to PSG reported by Jiao. *et al.* [22]. Fast interface trap generation has been attributed to high temperature NO annealing in nitride interfaces [23], which make the underestimation of D_{it} by hi-lo C-V method more severe in NO capacitors.

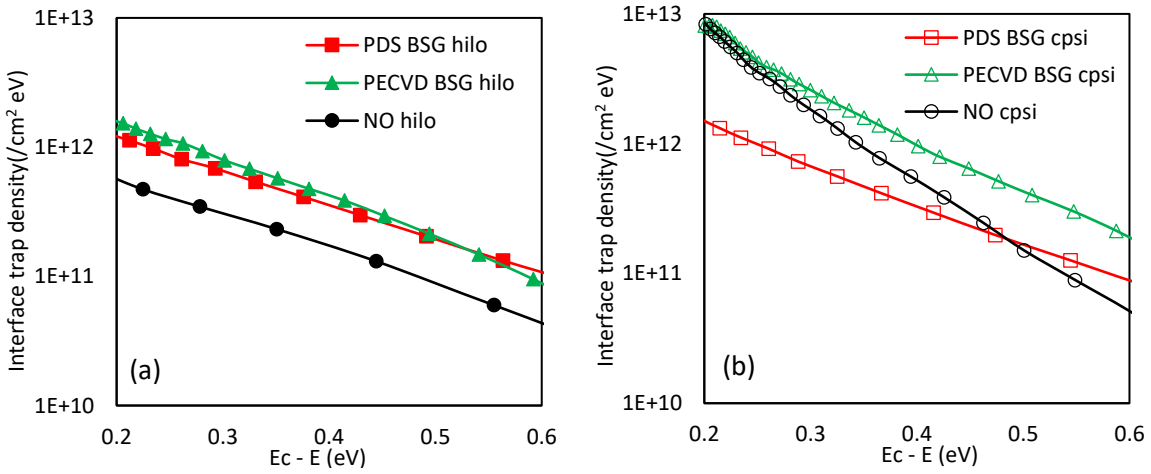

Fig.4.4.6. Interface trap density profiles for n-type capacitors with NO annealing, PDS BSG and PECVD BSG extracted by (a) hi-lo C-V and (b) C-ψ_s analysis.

4.4.2.3 Gray-Brown technique

As discussed in chapter 2, the Gray-Brown technique characterizes interface traps by high frequency C-V measurements as a function of temperature [24]. The interface trap density can be extracted from the flat band voltage shift from room temperature to low temperature by

$$V_G(T_2) - V_G(T_1) = \frac{q\int_{E_F(T_1)}^{E_F(T_2)} D_{it}(E)dE}{C_{ox}} = \frac{qN_{it}}{C_{ox}} \quad (4.6)$$

where $V_G(T_1)$ and $V_G(T_2)$ are the gate voltage to maintain the same band-bending at temperature T_1 and T_2. The difference of $V_G(T_1)$ and $V_G(T_2)$ is equal to the flat band voltage shift.

Fig.4.4.7 shows the C-V curves measured at 79 K and 293 K for n-type NO and PDS BSG capacitors. The measurements were taken at 100 kHz. Both NO and BSG capacitors show a right shift of flat band voltage at 79 K compared to 293 K due to the presence of additional negative charges with very similar N_{it} extracted by flat-band voltage shift. The results from this technique are summarized in Table 4-6. The flat-band voltage shift is the average value selected among multiple devices. Note this technique is useful to monitor the electron trapping at shallow (but slow) near interface states when a higher positive voltage is applied. But similar to hi-lo C-V method, it is an obstacle for accurate characterization of fast traps using C-V curves.

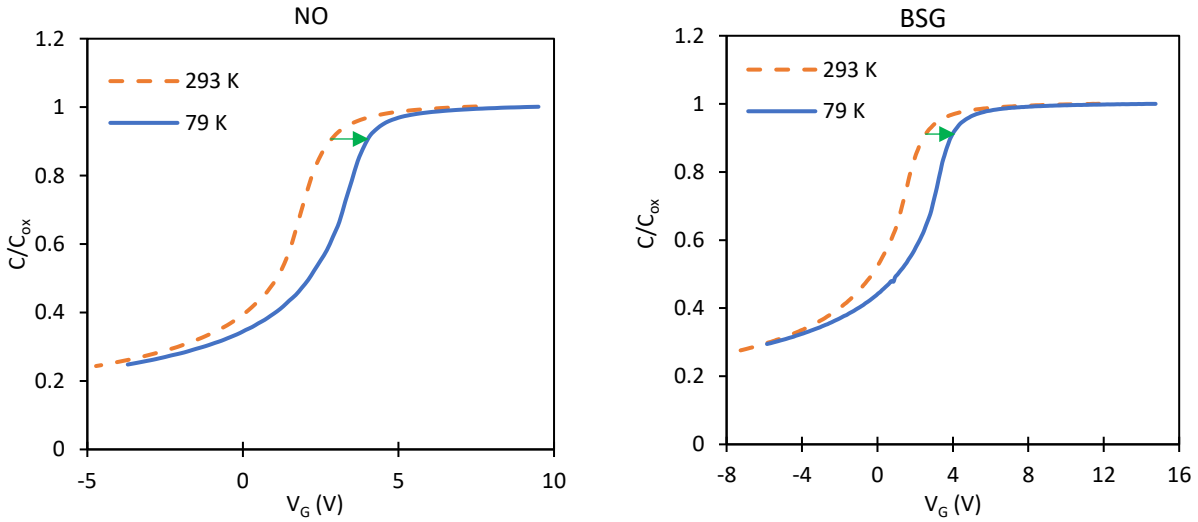

Fig.4.4.7. Gray-Brown technique: C-V curves with 100 kHz measured at 79 K and 293 K on (a) NO capacitor and (b) PDS BSG capacitor.

Table 4-6. Summary of results from Gray-Brown technique for NO and PDS BSG capacitors

Sample	Oxide thickness	V_{FB} at 293 K	V_{FB} at 79 K	ΔV_{FB}	N_{it}
NO	62 nm	2.53 V	3.79 V	1.33 V	$4.37\text{x}10^{11}/\text{cm}^2$
PDS BSG	75 nm	2.27 V	3.81 V	1.54 V	$4.41\text{x}10^{11}/\text{cm}^2$

4.4.2.4 Subthreshold slope (SS) of MOSFETs

The interface trap density was also characterized by I_D-V_G measurements with a fixed drain voltage (V_D = 25 mV) on NO and PDS BSG MOSFETs. The I_D-V_G measurements were performed in a vacuum cryo-chamber at a temperature range of 50-293 K to evaluate D_{it} within about 0.2 eV from E_C by the temperature dependence of subthreshold slope (SS) using the method detailed in [20, 25], given by

$$SS \equiv ln10 \frac{\partial V_G}{\partial ln I_D} \cong \ln(10) \frac{kT}{q} (1 + \frac{C_D + C_{it}}{C_{ox}}) \quad (4.7)$$

$$D_{it} = \frac{C_{ox}}{q^2} \left(\frac{qSS}{\ln(10)\, kT} - 1 \right) - \frac{C_D}{q^2} \quad (4.8)$$

SS values were extracted at a given drain current region (10^{-9} A < I_D < 10^{-8} A). The energy level E_C - E was calculated based on the theoretical surface potential at strong inversion corresponding to each temperature [26].

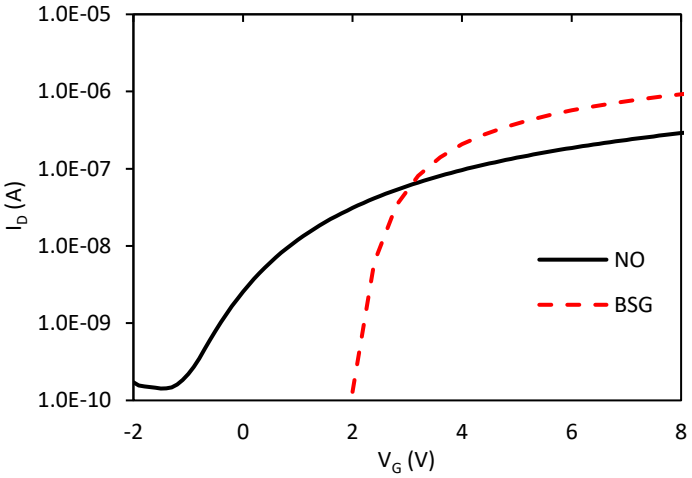

Fig.4.4.8. Log scale of I_D-V_G curves for NO and PDS BSG MOSFETs at room temperature.

The log scale of I_D-V_G curves for NO and BSG MOSFETs shown in Fig.4.4.8 depicts that compared to NO MOSFET, BSG MOSFET has higher V_{th} associated with higher amount of fixed negative charge in the oxide and/or additional doping of the MOSFET p-well by B. The SIMS result shown in chapter 3 indicates B penetrates into SiC and most of the B is confined to the top 10 nm. But since the annealing process was performed at 950°C, only a very small fraction is expected to be electrically active at such low temperature. 'BSG' has a steeper subthreshold slope than 'NO' indicating a faster switch on.

In Fig.4.4.9 (a), the decrease of SS with increasing temperature was observed on both MOSFETs due to the high concentration of traps near E_C. At any temperature, SS value for NO MOSFET is about twice of that for BSG MOSFET, reflecting the lower D_{it} at BSG/4H-SiC interfaces. The D_{it} extracted from SS is shown in Fig.4.4.9 (b) along with that determined by C-ψ_s method on the companion capacitors. For BSG samples, the two methods are in good agreement. For NO samples, there is a fair discrepancy close to 0.2 eV between SS and C-ψ_s method, which may due to the sensitivity of the D_{it} under the assumption of a fixed C_D at $2\psi_B$ with large degradation of SS at low temperature.

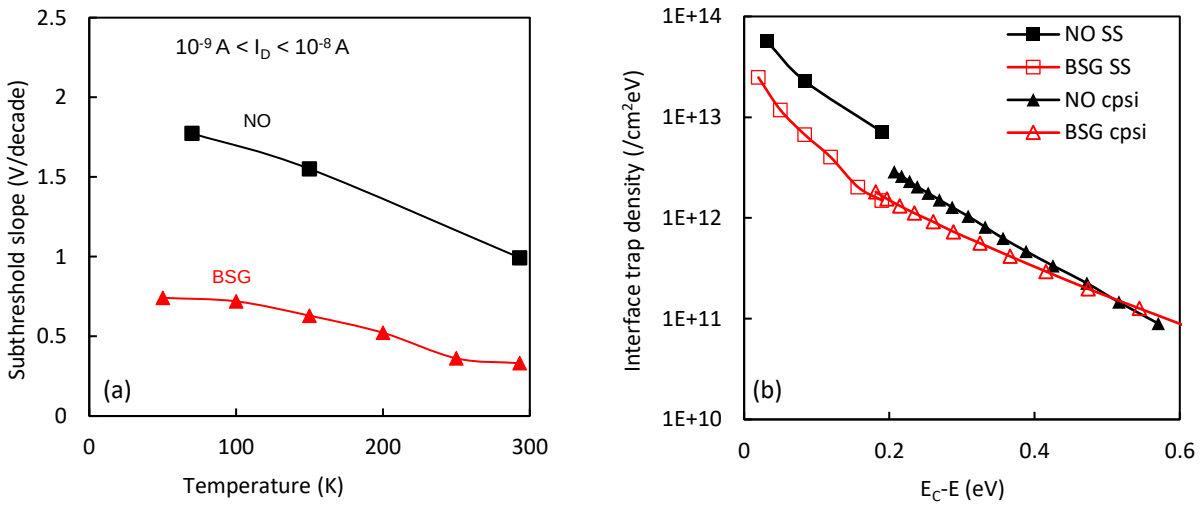

Fig.4.4.9. (a) Temperature dependence of subthreshold slope for NO and PDS BSG MOSFETs and (b) D_{it} extracted from subthreshold slope and C-ψ_s.

4.4.3 Field-effect mobility μ_{FE}

Field-effect mobility μ_{FE} was extracted by I_D-V_G characteristics of NO and BSG MOSFETs, given by

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_D} \tag{4.9}$$

where $g_m = \frac{\partial I_D}{\partial V_G}|_{V_D=constant}$. Drain voltage V_D was set as 25 mV. Threshold voltage V_{th} was determined by the corresponding gate voltage at a constant drain current of 10^{-8} A. Since the oxide thickness is different for different devices, μ_{FE} was plot out as a function of oxide field, which is calculated by [37],

$$E_{ox} = \frac{V_G - V_{th} + \sqrt{2\varepsilon_{SiC} q N_A (2\psi_B)}/C_{ox}}{d_{ox}} \quad (4.10)$$

where C_{ox} is the oxide capacitance per unit area, ε_{SiC} (= 9.66) is the dielectric constant of 4H-SiC, N_A is SiC epilayer doping concentration, ψ_B is bulk potential and d_{ox} is the oxide thickness.

Fig.4.4.10 shows the significant mobility improvement in BSG MOSFETs at both low and high electric fields and the peak field-effect mobility is 140 $cm^2/V{\cdot}s$, a factor of 4 higher than NO MOSFET due to lower fast trap density. This result is consistent with the correlation between channel mobility and fast trap density as reported in [10, 28], claiming that fast traps are the dominant limiting factor to channel mobility.

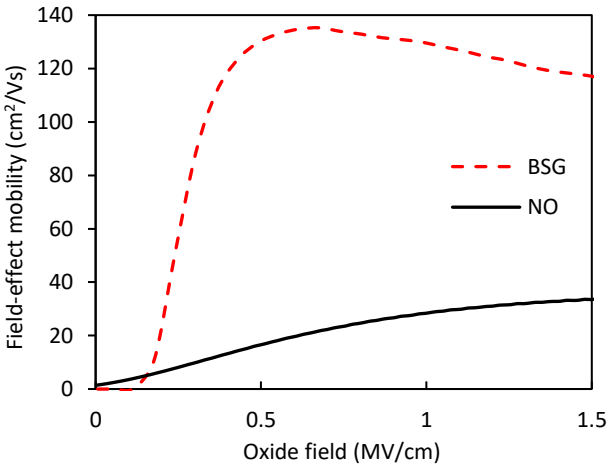

Fig.4.4.10. Field-effect mobility of NO and PDS BSG 4H-SiC MOSFETs at room temperature.

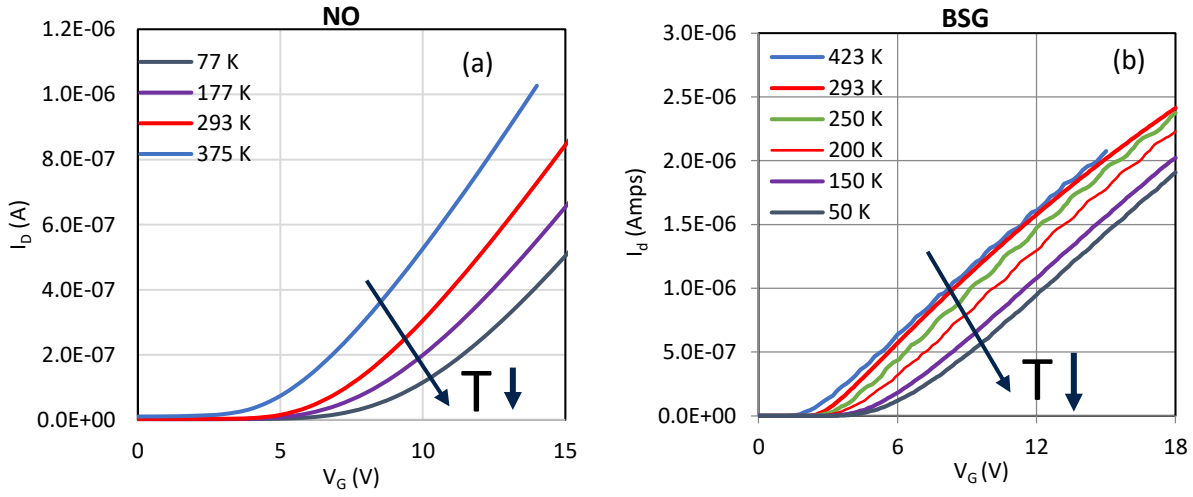

Fig.4.4.11. I_D-V_G curves of (a) NO MOSFET and (b) BSG MOSFET measured at different temperatures.

To investigate the dependence of field-effect mobility on temperature, μ_{FE} was also extracted from experimental I_D-V_G data on NO and BSG MOSFETs at different temperatures. Fig.4.4.11 shows I_D-V_G curves for NO and BSG MOSFET measured at different temperatures. I_D-V_G curves of NO show an increasing of transconductance with temperature increasing from 70 K to 293 K while the transconductance keeps almost constant on the BSG MOSFET from 50 K to 423 K. This result indicates the μ_{FE} of the BSG MOSFET has a weak dependence on temperature due to lower fast interface trap density than NO MOSFET. The μ_{FE} at different temperatures is extracted and shown in Fig.4.4.12. For both NO and BSG, the peak μ_{FE} occurs at higher gate voltage at low temperature compared to 293 K due to greater electron trapping very close to E_C near V_{th}, as also observed in Si MOSFETs [29].

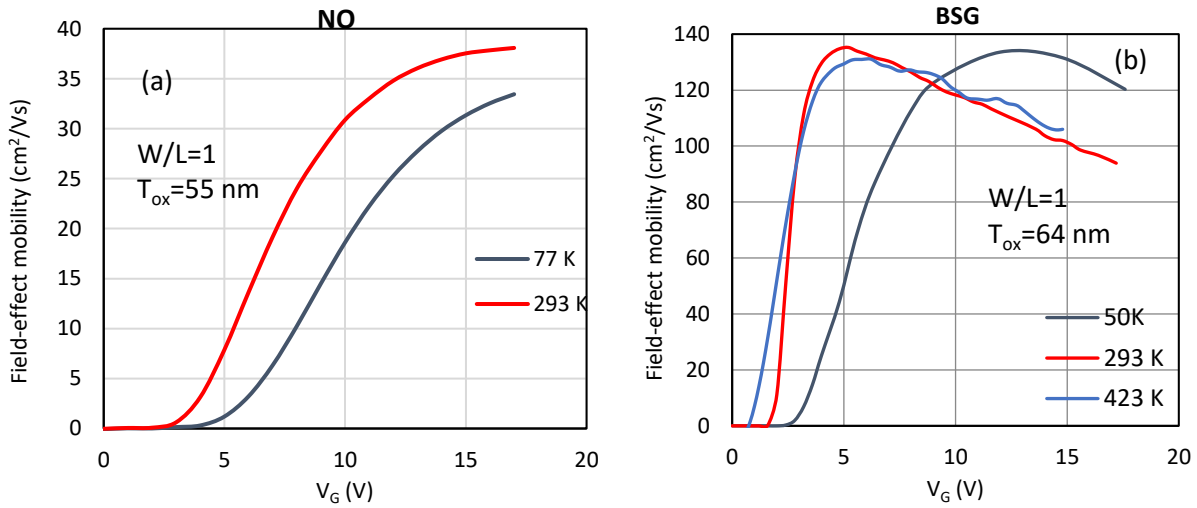

Fig.4.4.12. Field-effect mobility of (a) NO MOSFET and (b) BSG MOSFET at different temperatures.

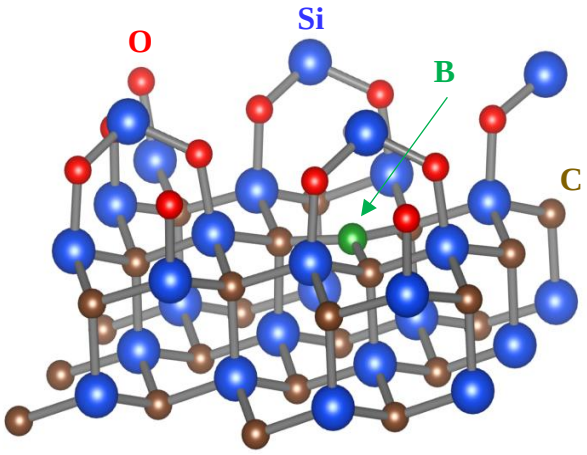

Fig.4.4.13. Proposed mechanism of B passivation effect at the interface of BSG/SiC [31].

It has been suggested the reduction of D_{it} is due to a structural change in SiO_2 by B near the interface resulting in stress relaxation [30]. This could be caused by the occupation of Si site by B at the interface due to lower electronegativity of Si than C shown in Fig.4.4.13 [31], which results in a reduction of required oxygen bonds to Si therefore a relaxation of oxide stress [31].

4.4.4 Correlation between B concentration and electrical results

In order to investigate the correlation between B concentration at the interface of SiO_2/SiC, interface trap density and field-effect mobility, lateral 4H-SiC MOSFETs and their companion capacitors with various B concentrations have been characterized by SIMS, C-ψ_s analysis and I-V measurements. Fig.4.4.14 (a) shows the comparison of D_{it} extracted by C-ψ_s method on all the companion capacitors. This result indicates that the PDS annealing process is more effective for reducing fast traps than PECVD and NO annealing and it results in lower D_{it} than PECVD and NO annealing. The field-effect mobility of the devices in Fig.4.4.14 (a) are shown in 4.4.14 (b). The higher μ_{fe} of PDS BSG MOSFETs than NO annealed MOSFET and PECVD BSG MOSFET is due to lower interface fast trap density. The μ_{fe} of PECVD BSG MOSFET is lower than that of NO devices as a consistency with the higher fast D_{it}.

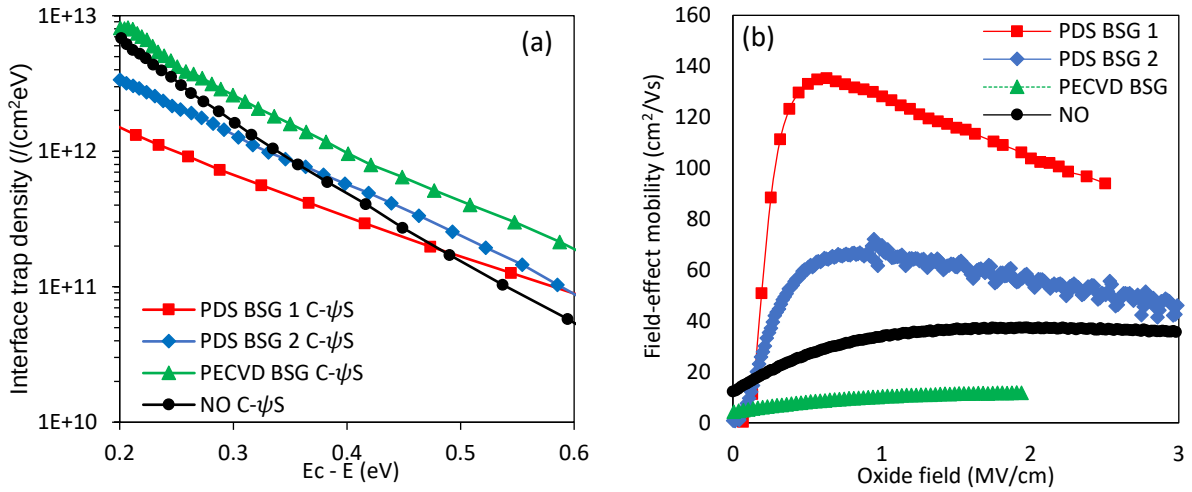

Fig.4.4.14. (a) D_{it} as a function of energy from E_C of 4H-SiC extracted by C-ψ_s analysis on companion capacitors of PDS BSG, PECVD BSG and NO MOSFETs. (b) Field-effect mobility of corresponding MOSFETs at room temperature.

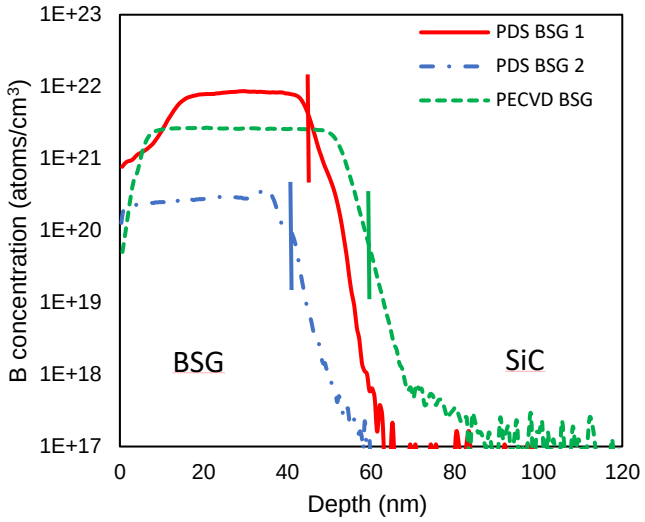

Fig.4.4.15. B profiles in BSG and SiC by SIMS for PDS BSG and PECVD BSG devices. The detection limit is $4x10^{16}/cm^3$.

Table 4-7. Results of samples

Sample	B% in the bulk (SIMS)	B% at the interface (SIMS)	N_{it} (cm^{-2}) ($C-\psi_s$)	Peak mobility ($cm^2\ V^{-1}s^{-1}$)
PDS BSG 1	10.4%	4%	$1.68x10^{11}$	140
PDS BSG 2	0.34%	0.09%	$3.84x10^{11}$	65
PECVD BSG	3.16%	0.01%	$7.53x10^{11}$	12

The B profiles of the companion capacitors above characterized by SIMS are shown in Fig.4.4.15. The B atomic percentages in the bulk of the oxide and at the interface were both estimated from SIMS measurements for 'PDS BSG 1', 'PDS BSG 2' and 'PECVD BSG'. The interface can be defined by the depth where the half of the maximum intensity of detected Si is. The estimated B concentrations along with interface trap densities extracted by C-ψ_s analysis and corresponding field-effect mobility are summarized in Table 4-7. These results indicate that the higher B concentration at the interface results in lower interface fast trap density and higher channel mobility. The B concentration in the bulk of the oxide does not seem to be the dominant factor for interface trap density and channel mobility.

4.4.5 Bias temperature instability of BSG

As noted in section 1, if the polysilicon gate of an MOS device is doped with boron, during processing the boron may diffuse into and through the oxide and enter the silicon substrate. The boron can change the electrical characteristics of the device in undesirable ways. The penetration of small amount of B into SiC substrate has been also observed in our study based on SIMS measurements. From the device reliability point of view, the diffusion of boron from doped poly Si gates through SiO_2 into the channel region of MOSFETs can cause an undesirable shift in the threshold voltage and degrade gate oxide reliability [6].

The bias temperature stress instability (BTI) of BSG on 4H-SiC MOSFETs has been reported by Soler *et al.* [2] and Cabello *et al.* [3]. Good threshold voltage stability under both positive and negative bias stress at room temperature has been obtained. However, threshold voltage stability of BSG-gated SiC MOSFETs with high temperature bias stress has not been widely studied.

In our study, in order to evaluate the bias temperature instability of BSG, bias temperature stress (BTS) tests were carried out on both BSG-gated 4H-SiC MOS capacitors and MOSFETs. Fig.4.4.16 shows flat-band shift characterized by high frequency (100 kHz) C-V measurements under positive bias stress of +1.5 MV/cm at 150°C for 5 mins on PDS BSG capacitors from different experiment runs. For both capacitors, V_{FB} shifts to right under positive bias stress indicating the presence of electron trapping. Significant small shift of V_{FB} has been observed on the capacitor in Fig.4.4.16 (a) than Fig.4.4.16 (b). As discussed in previous sections in this chapter, B concentration varies from experiment run to run causing different electrical results. The

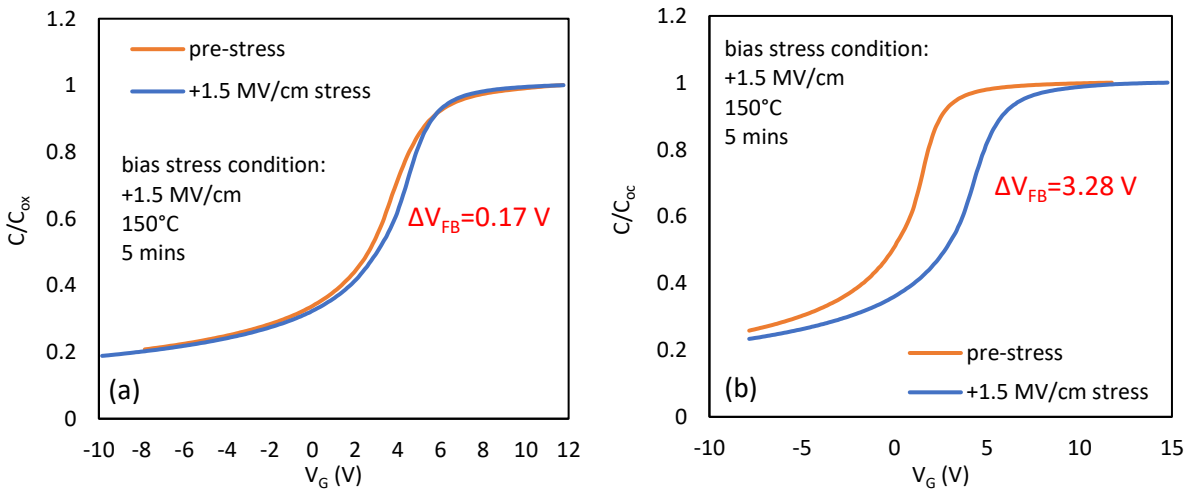

Fig.4.4.16. High frequency C-V curves of PDS BSG 4H-SiC MOS capacitors with flat band voltage shift of (a) 0.17 V and (b) 3.28 V under +1.5 MV/cm bias stress at 150 °C for 5 min.

difference between ΔV_{FB} shown in Fig.4.4.16 (a) and Fig.4.4.16 (b) could be due to the difference of B concentrations.

The bias temperature instability of BSG was also investigated on PECVD BSG capacitors with the same bias stress condition. As presented in Fig.4.4.17 (a), the as received PECVD BSG shows a large flat band voltage shift (~16 V) to left under positive bias stress indicating either presence of polarization charge or mobilie ions generated from the PECVD process. This also has been observed on PSG capacitors [22]. After a relaxiation for 4 days, the flat band voltage recovered a little bit but still with a very large left shift compared to that before bias stress, possibly due to a combination of mobile ions and a small amount of polarization charges. After the as received PECVD BSG was annealed by O_2 at 550°C for 30 mins, a good flat band voltage stability was obtained with a small right shift of ~0.46 V, as shown in Fig.4.4.17 (b). Similar to PDS BSG, the existence of electron trapping now is observed. The result indicates that O_2 annealing is effective to reduce mobile ions or/and polarization charge.

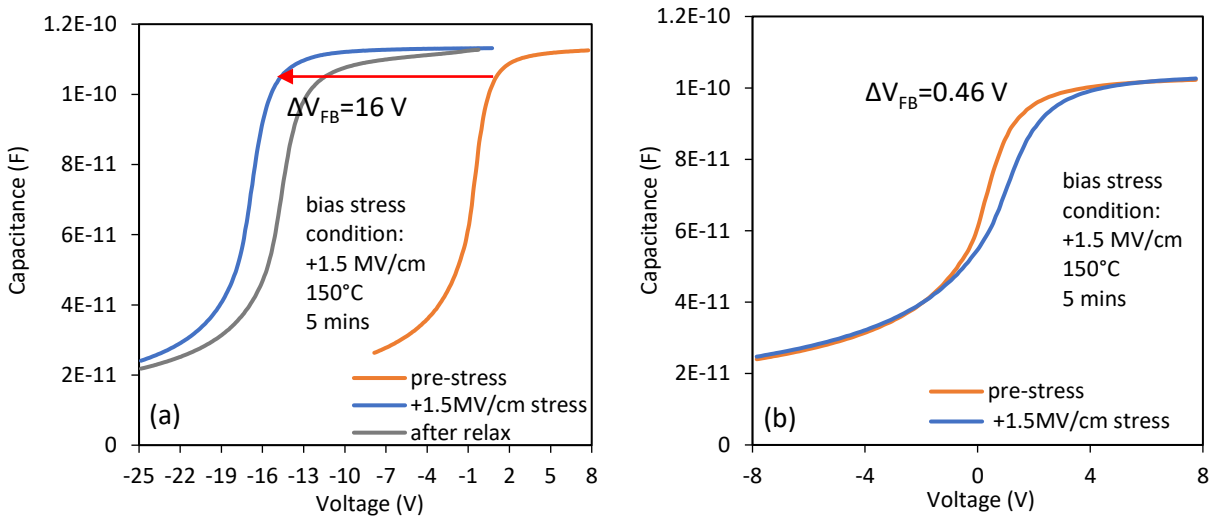

Fig.4.4.17. Flat band voltage shift characterized by high frequency C-V measurements under BTS on (a) as received PECVD BSG 4H-SiC MOS capacitor and (b) O_2 annealed PECVD BSG capacitor.

The instability of threshold voltage of PDS BSG-gated 4H-SiC MOSFETs under positive bias temperature stress (PBTI) was characterized. V_{th} was determined by the corresponding gate voltage at a constant drain current of 10^{-8} A. Fig.4.4.18 shows the I_D-V_G curves of NO and PDS BSG MOSFETs (with peak mobility of 140 $cm^2/V \cdot s$) before and after bias temperature stress. The bias temperature stress was carried out with +1.5 MV/cm at 150°C for 5 min. The results show

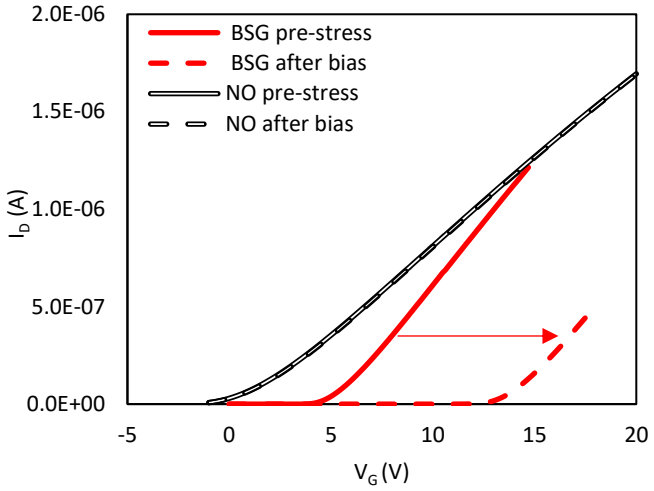

Fig.4.4.18. PBTI of NO and PDS BSG 4H-SiC MOSFETs under the same bias temperature stress condition.

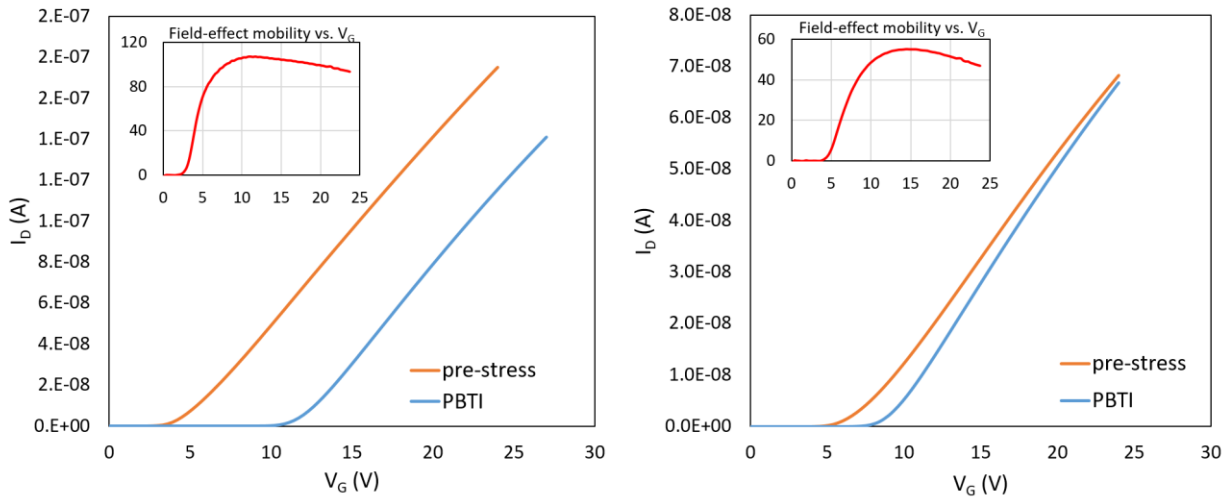

Fig.4.4.19. PBTI of PDS BSG 4H-SiC MOSFETs with different field-effect mobilities under the same bias temperature stress condition.

that compared to the negligible V_{th} shift (~0 V) on NO MOSFETs, the V_{th} of PDS BSG MOSFETs shifts to right with ~8 V under the same stress condition, which is consistent with V_{FB} shift on PDS BSG capacitors, indicating the presence of significant oxide traps under BTS in BSG. Similar behavior of V_{th} shift was also observed on different PDS BSG MOSFETs with different field-effect mobilities meaning different B concentrations, as shown in Fig.4.4.19. The results show a right shift of V_{th} on both devices and the one with higher mobility (higher B concentration) results

in larger V_{th} shift. The detailed results are summarized in Table 4-8. However, it is still not clear whether the instability of V_{th} is correlated with B concentration.

Table 4-8. Summary of PBTI resluts of devices with different field-effect mobilities

sample	ΔV_{th}	Peak mobility
PDS BSG 1	8.3 V	140 $cm^2 V^{-1}s^{-1}$
PDS BSG 2	7.2 V	107 $cm^2 V^{-1}s^{-1}$
PDS BSG 3	2.0 V	55 $cm^2 V^{-1}s^{-1}$

The mechanism of poor BTI in BSG could be related to similar instability observed in Si MOSFETs due to additional fixed oxide charges by unintentional B impurity in the gate oxide and extra B doping in Si substrate [32, 33]. Also, it has been reported that boron diffusion results in the deterioration of the electrical characteristics of Si MOS capacitors due to the creation of mid-gap interface states after high temperature annealing [34]. Further study of BTI on BSG/4H-SiC interface, such as the characterization of oxide charge, the activated B in SiC after annealing as well as the interface trap density in deeper energy levels from conduction band, needs to be conducted to improve stability by process optimization for the utilization of this promising dielectric for SiC power MOSFETs.

4.5 4H-SiC MOSFETs with borosilicate glass gate dielectric combining with Sb counter-doping

4.5.1 Motivation of combination of BSG and Sb counter-doping

As discussed in previous chapter and sections, a surface counter-doping layer around 10 nm deep in channel region by Sb improves the low-field channel mobility due to higher electron density in the channel as well as lower carrier scattering at low electric fields. This process also results in slight lowering of V_{th} due to the surface counter-doping effect. On the other hand, using BSG as the gate dielectric for 4H-SiC MOSFETs, a high channel mobility can be obtained for a wide range of surface transverse electric fields along with a larger V_{th} than NO MOSFETs [6–8]. For vertical power MOSFETs with heavier doped p-wells ($\sim 10^{17}/cm^3$), it is expected that BSG gate dielectric would cause further increase of V_{th}, which would be undesirable. Therefore, in this study, the motivation for combining the Sb surface doping process with BSG gate dielectric was two-fold: (1) Achieve higher channel mobility using Sb counter-doping while retaining the high-

field mobility characteristics of BSG. (2) Tune V_{th} to adequate value using Sb counter-doping. The results obtained indicate that these goals were achieved by this approach.

Long channel [200 um (length) × 200 um (width)] lateral MOSFETs were fabricated on 4°-off Si-face (0001) of p-type 4H-SiC epitaxial layers doped at ~$1\times10^{16}/cm^3$. Following implantation of N (~$10^{20}/cm^3$) in the source-drain regions, Sb was implanted in the channel region with 80 keV singly charged ions at room temperature with a dose of $2.5\times10^{13}/cm^2$. Subsequently, post-implantation activation annealing at 1650°C using a graphitic carbon cap layer was performed. Next, dry oxidation at 1150°C was performed followed by post-oxidation annealing using a B_2O_3 PDS (Technеglas, GS-139) in a gas mixture of Ar (50 sccm) and O_2 (5 sccm) at 950°C for 30 minutes. Samples not annealed in boron were annealed in NO after the same oxidation process as reference samples. After Mo and Ni were sputtered as the gate and the source/drain contact metals respectively, ohmic contact annealing was carried out at 800°C in Argon. Samples that received only boron annealing are referred to as 'BSG' and samples that underwent both Sb counter-doping and NO annealing or boron annealing are referred to as 'Sb+NO' or 'Sb+BSG' respectively. The process flow is shown in Fig.4.5.1 and a summary of the samples is shown in Table 4-9.

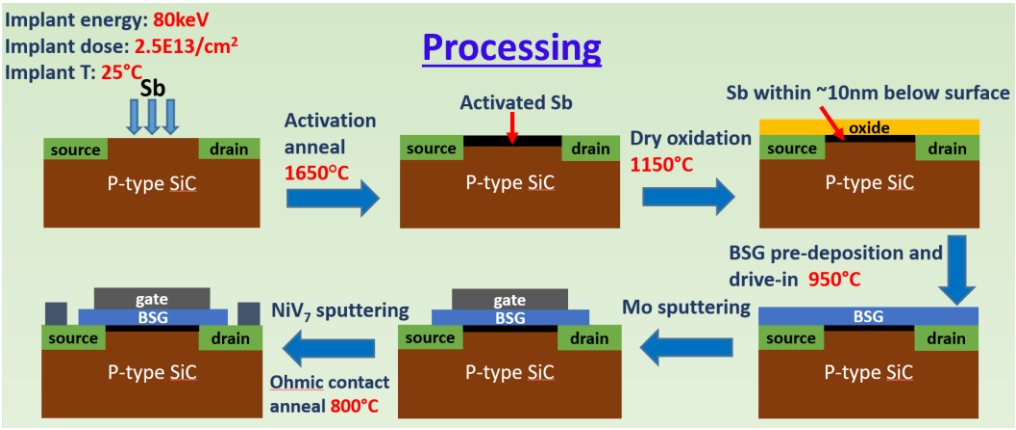

Fig.4.5.1. Fabrication process flow of 4H-SiC MOSFETs with BSG gate dielectric and Sb counter-doping.

Table 4-9. Summary of samples

Sample	Sb implant energy and dose	Oxidation process	Post oxidation anneal	Oxide thickness
Sb+NO	80 keV $2.5x10^{13}$ cm^{-2}	Thermal, 1150°C	NO anneal, 1175°C	60 nm
BSG	N/A	Thermal, 1150°C	Boron anneal, 950°C	64 nm
Sb+BSG	80 keV $2.5x10^{13}$ cm^{-2}	Thermal, 1150°C	Boron anneal, 950°C	68 nm

4.5.2 Results and discussion

Fig.4.5.2 shows the C-V curves measured at 79 K and 293 K on n-type 'BSG' and 'Sb+BSG' capacitors. The measurements were taken at 100 kHz. The C-V curves of 'Sb+BSG' capacitors are more stretched out than that of 'BSG' capacitor due to the presence of Sb, which has been discussed in chapter 3. Both 'BSG' and 'Sb+BSG' capacitors show a right shift of flat band voltage at 79 K compared to 293 K with similar N_{it} extracted by flat band voltage shift. This is consistent with the results in chapter 3, showing the primary effect of Sb is counter-doping instead of passivation. The results are summarized in Table 4-10.

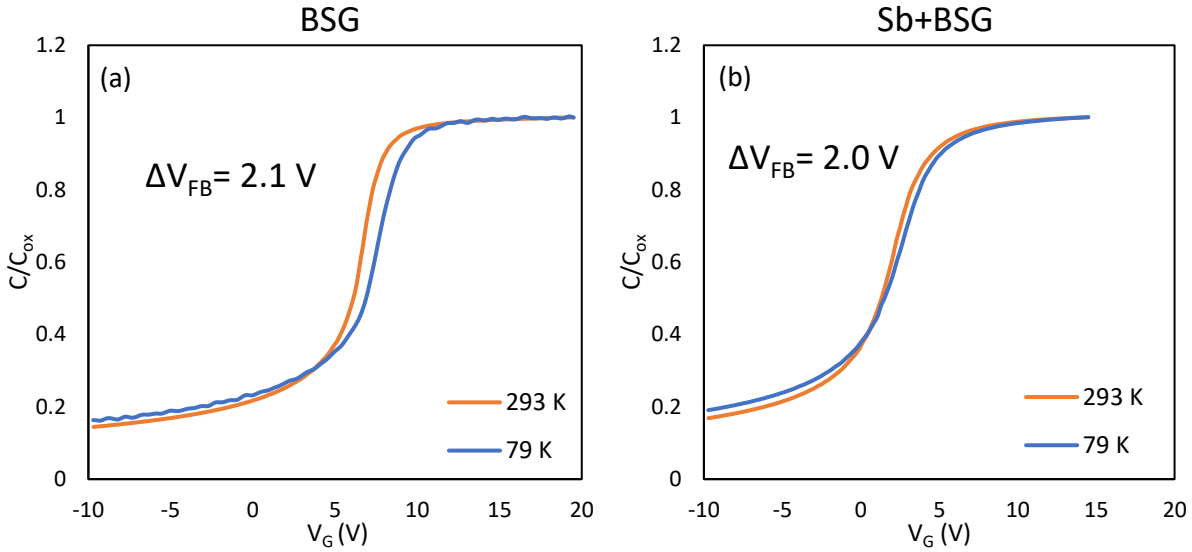

Fig.4.5.2. Gray-Brown technique: C-V curves with 100 kHz measured at 79 K and 293 K on (a) 'BSG' capacitor and (b) 'Sb+BSG' capacitor.

Table 4-10. Summary of results from Gray-Brown technique for 'BSG' and 'Sb+BSG'capacitors

Sample	Oxide thickness	V_{FB} at 293 K	V_{FB} at 79 K	ΔV_{FB}	N_{it}
BSG	64 nm	7.6 V	9.7 V	2.1 V	$7.1 \times 10^{11}/cm^2$
Sb+BSG	66 nm	3.7 V	5.7 V	2.0 V	$6.5 \times 10^{11}/cm^2$

Fig.4.5.3 shows the I_D –V_G characteristics at 293 K with a fixed drain voltage (V_D = 25 mV) and μ_{FE} of 'BSG' and 'Sb+BSG' MOSFETs extracted by I_D-V_G curves. V_{th} was determined by the corresponding gate voltage at a constant drain current of 10^{-8} A. Fig.4.5.3 (a) depicts that compared to 'BSG', 'Sb+BSG' tunes V_{th} from 2.5 V to 0.9 V along with a similar subthreshold slope to 'BSG'. With Sb counter-doping, V_{th} shifts to the left compared to devices without Sb

implantation, as a result of compensation of the p-acceptors in the surface region by Sb donors. Fig.4.5.3 (b) shows compared to 'BSG', further mobility enhancement at low fields was observed on 'Sb+BSG' with a peak value of 180 $cm^2/V{\cdot}s$ and 94 $cm^2/V{\cdot}s$ at 2 MV/cm. The high field-mobility similarity between 'Sb+BSG' and 'BSG' indicates that the counter-doping effect is dominant in the low field regime.

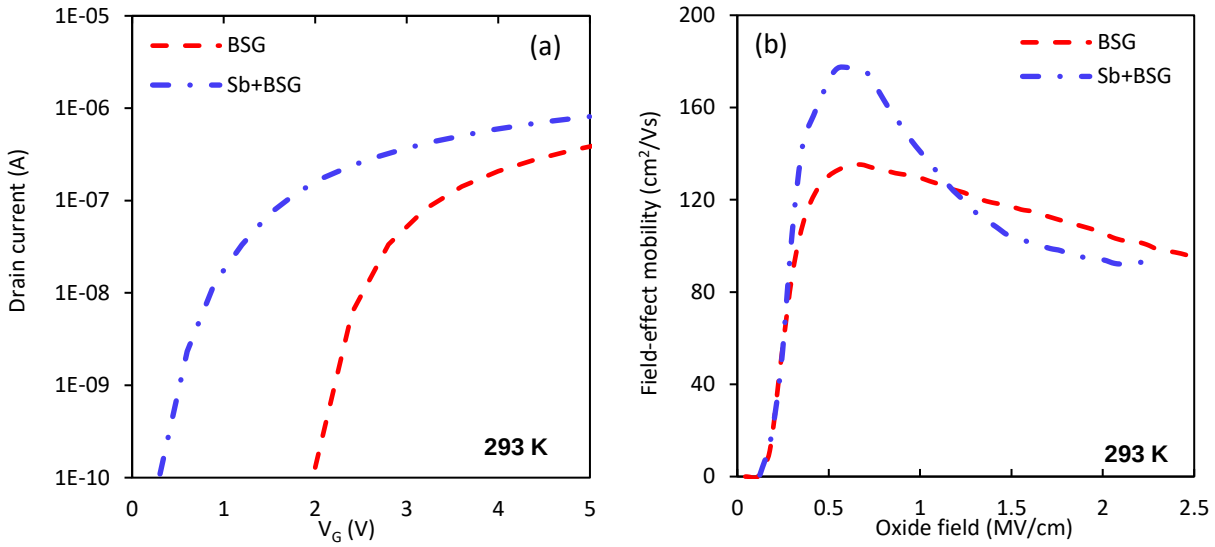

Fig.4.5.3. (a) Log scale of I_D–V_G characteristics and (b) Field-effect mobility of 'BSG' and 'Sb+BSG' 4H-SiC MOSFETs.

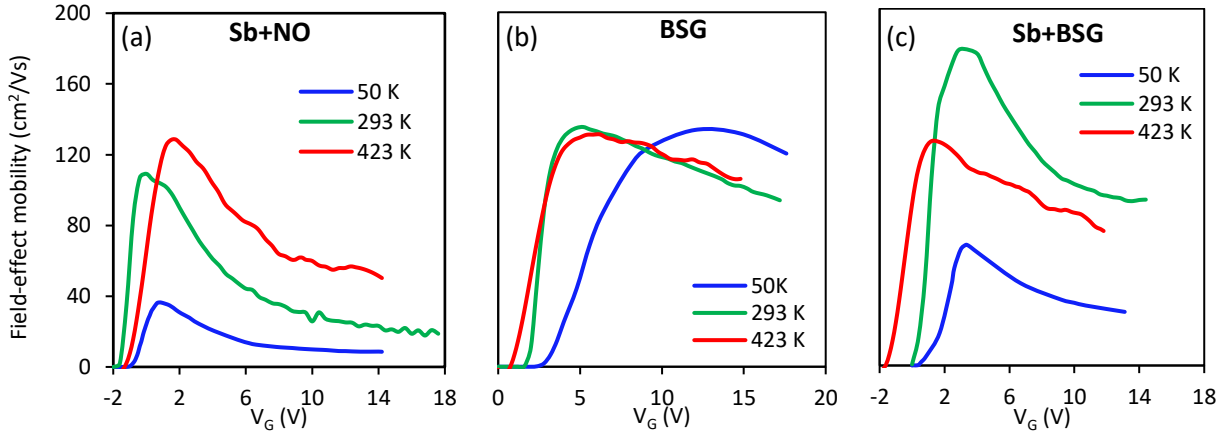

Fig.4.5.4. Field-effect mobility of (a) 'Sb+NO' (b) 'BSG' and (c) 'Sb+BSG' 4H-SiC MOSFETs at different temperatures.

The μ_{FE} temperature dependence of the different interface configurations is shown in Fig.4.5.4. For 'BSG', the μ_{FE} displays a weak dependence on temperature due to lower D_{it}. As discussed in previous chapters, the peak μ_{FE} occurs at higher oxide fields at 50 K compared to 293

K and 423 K due to greater electron trapping very close to E_C near V_{th}. For 'Sb+NO', μ_{FE} increases monotonically with temperature at both low and high fields. At higher temperatures, low field μ_{FE} increases due to the increase of carrier concentration resulting from greater ionization of Sb donors. It is not clear what causes the increase of high field μ_{FE} at higher temperature as this regime is expected to be surface roughness scattering limited. Possible reasons could be: (i) Greater screening from surface roughness scattering by more free carriers. (ii) The higher D_{it} in 'Sb+NO' extends the effect of Coulomb scattering to higher oxide fields. As Coulomb mobility increases with temperature, the total mobility also shows this temperature dependence. For 'Sb+BSG', compared to 293 K, reduction of μ_{FE} is observed at both 50 K and 423 K. The low field μ_{FE} behavior at 50 K and 293 K can also be attributed to the Sb ionization. But at 423 K, the lower μ_{FE} than 293 K are suggesting a phonon scattering component in stark contrast to 'BSG'. It was expected to see a higher peak mobility at room temperature and high temperature on 'Sb+BSG' than 'BSG' as well as a similar mobility to 'BSG' at 50 K since we assumed the D_{it} was similar, also shown from Gray-Brown method. However, lower mobility was observed at 50 K and 423 K than 'BSG', which is probably due to the interaction between the Sb and B processes.

4.6 Summary

In this chapter, the effect of BSG gate dielectric on channel transport of lateral 4H-SiC MOSFETs has been investigated. C-ψ_s analysis indicates a significantly lower fast interface trap density with BSG formed by planar diffusion source at BSG/4H-SiC interfaces compared to nitrided SiO_2/4H-SiC interfaces. Improvement of channel mobility over a wide range of transverse electric fields compared to standard NO annealed MOSFETs was achieved by 'PDS BSG'. These results are consistent with a mechanism where interfacial B significantly reduces the density of fast traps and improves the channel mobility. In addition, the correlation between B concentration, interface trap density and channel mobility has been investigated as well. The results show that interface trap density decreases with increasing B concentration, which in turn, results in higher channel mobility with higher B concentration.

By combining BSG gate dielectric with Sb surface doped channels in lateral 4H-SiC MOSFETs, further improvement of channel mobility, a tunable threshold voltage and good subthreshold slope were achieved with the best μ-V_{th} trade-off.

While these results highlight the advantage of BSG gate dielectric for 4H-SiC MOSFETs from the point of view of channel mobility, further study on the stability of BSG should be carried out to understand the mechanism of B-induced device instability for SiC MOSFETs and further improvement of the BTI is absolutely necessary to utilize the attractive properties of BSG on power MOSFETs.

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Chapter 5

Hall effect characterization on 4H-SiC MOSFETs

5.1 Motivation

In the previous chapters, field-effect mobility μ_{FE} has been used for the characteristics of channel transport of 4H-SiC MOSFETs calculated by the transconductance of I_D-V_G. However, the experimental drain current and transconductance are strongly affected by large densities of interface states within the bandgap of 4H-SiC in three distinct ways: (1) Larger gate-voltage swings required to produce a change in inversion charge due to the trapping of gate-induced charges that result in the transconductance decreasing at any given gate voltage. (2) The mobile inversion charge density at any gate voltage is lower. (3) The drift mobility of inversion-layer electrons is lowered by Coulomb scattering by the trapped charges. Thus, both the drain current and transconductance of MOS devices at any gate voltage are lower [1].

As to effective mobility μ_{eff} discussed in chapter 2, which is estimated by inversion layer conductance assuming the density of free carrier n_{free} is equal to the total density of inversion layer electrons n_{total} extracted by $C_{ox}(V_G-V_{th})/q$. This approach is correct only if $n_{free} = n_{total}$, which is in the absence of electron trapping [2]. Therefore, effective mobility underestimates the actual carrier mobility in inversion layer, as demonstrated by Saks *et al.* [3] in Fig.5.1.1.

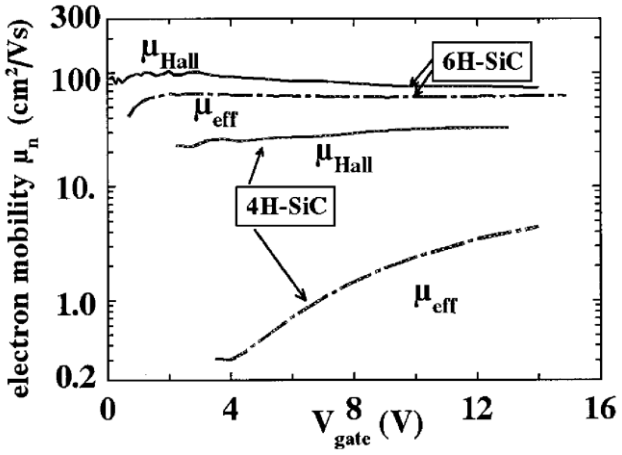

Fig.5.1.1. Comparison of Hall and effective mobilities in 4H and 6H SiC MOS Hall bars [3].

Compared to the techniques employed to determine the mobility above, a major advantage of Hall effect measurements is that actual carrier mobility and n_{free} are correctly determined independently without consideration of threshold voltage, which is difficult to accurately determine in the case of considerable interface trapping [3]. Moreover, the Hall effect allows the estimation of D_{it}, as reported by Saks *et al.* [4], without needing to use companion n-type MOS capacitors for D_{it} characterization. By using Hall effect measurement, the precise nature of surface passivation on interface traps as well as the mechanism of different scattering effects on carrier mobility can be understood.

5.2 Theory of Hall effect in semiconductor

Edwin Hall discovered Hall effect in 1879. As discussed in chapter 2, when a current is flowing in a semiconductor perpendicular to an external magnetic field, a voltage drop will be established that is perpendicular to both the current and the magnetic field due to the creation of electric field produced by the separation of electrons and holes under Lorenz force. This voltage

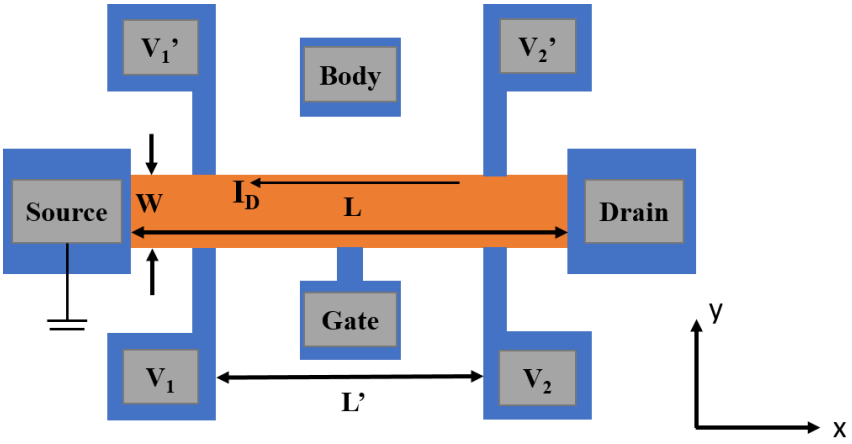

Fig.5.2.1. The schematic illustration of a Hall bar structure for Hall effect measurements.

drop is called Hall voltage V_H. A typical pattern configuration for Hall effect measurement is the bridge Hall bar geometry, as shown schematically in Fig.5.2.1. Experimentally, the resistivity of the channel is determined by the current flowing between source and drain when apply a constant voltage V_D (generally the source terminal is grounded), the voltage drop V_2 -V_1 or V_2' -V_1' as well

as the Hall voltage V_2 -V_2' or V_1 -V_1' as a function of magnetic field in z direction. The relationship between the components of the resistance and the measured voltages are

$$\rho_x = \frac{V_2 - V_1}{I_D}\frac{W}{L'} \tag{5.1}$$

$$\rho_y = \frac{V_2 - V_2'}{I_D} = \frac{B}{en_e} \tag{5.2}$$

Thus, the charge carrier density can be obtained by

$$n_e = (e\frac{d\rho_y}{dB})^{-1} = \frac{I_D/e}{dV_H/dB} \tag{5.3}$$

where V_H is the Hall voltage. The mobility of the electrons can be determined by

$$\mu_H = \frac{\sigma_0}{en_e} \tag{5.4}$$

where σ_0 is the conductivity of the channel.

5.3 Processing of Hall MOSFETs and wire-bonding configuration

So far, the precise nature of surface passivation is still not sufficiently well understood to optimize passivation technology on the interface of SiC MOSFETs. The field-effect mobilities reported for inversion-type 4H-SiC MOSFETs vary as much as two orders of magnitude [1]. In this study, in order to better understand effect of NO annealing, BSG gate dielectric and Sb channel implantation on electron trapping by interface traps as well as the mechanism of different scattering effects on carrier mobility, hall bar MOSFETs (600 µm length x 40 µm width) with NO annealing, BSG gate dielectric and Sb channel implantation were fabricated on 4°-off Si-face (0001) of p-type 4H-SiC epitaxial layers doped at ~1×10^{16}/cm^3. The Hall bar structures have two voltage taps on either side to measure the conductivity voltage and the Hall voltage. Sb was first implanted with Gaussian distribution at 80 keV at room temperature with dose of $2.5\text{x}10^{13}$/cm^2, as discussed in chapter 3. This was followed by dopant activation annealing at 1650°C using a carbon cap. Before processing gate oxidation, a thick layer (~600 nm) of field-oxide was patterned by low pressure chemical vapor deposition (LPCVD) and etched to define the active area. Subsequently, dry oxidation at 1150°C for 10 hours followed by NO annealing and B_2O_3 PDS annealing were processed on the corresponding devices in the same procedure. Al was evaporated in vacuum (~10^-

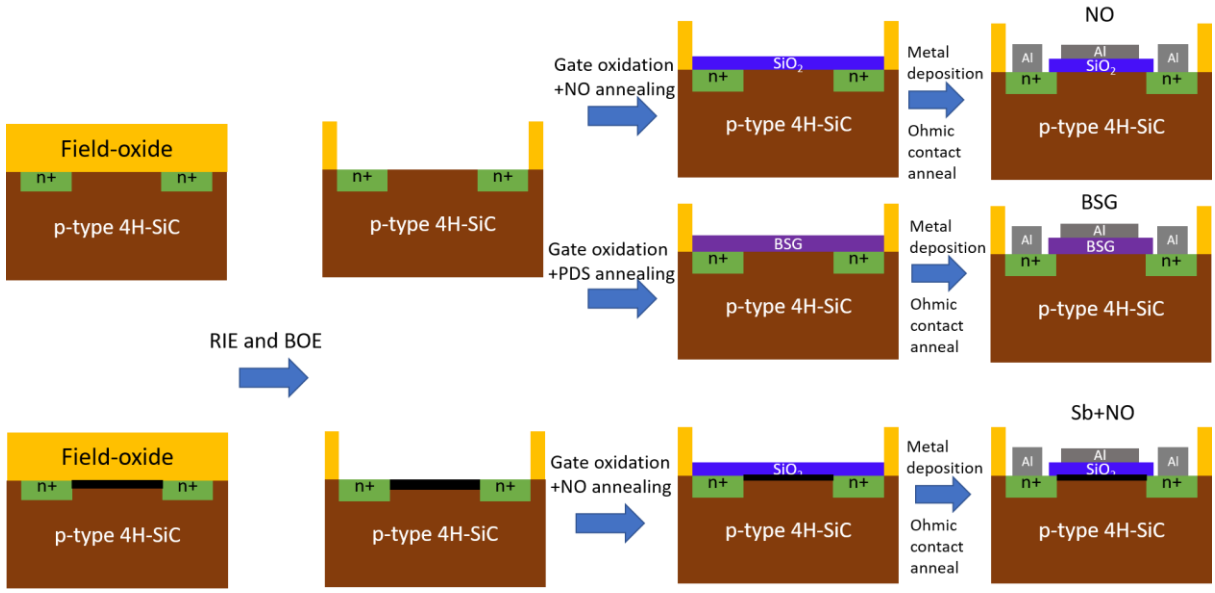

Fig.5.3.1. The fabrication process flow for 'NO', 'BSG' and 'Sb+NO' Hall bar MOSFETs.

[7] Torr) as the gate, source/drain and body pad metals, which is for better contacts for wire-bonding. Ohmic contact annealing on source/drain was performed in the annealing furnace at 800°C with Ar flowing. The fabrication process flow is illustrated in Fig.5.3.1.

To make interconnection between the Hall bar MOSFET and Hall system for Hall effect measurements, wedge wire bonding with gold wire has been utilized on the devices needed to be characterized. The wedge wire bonding method is widely used for the electric wiring of Si chips

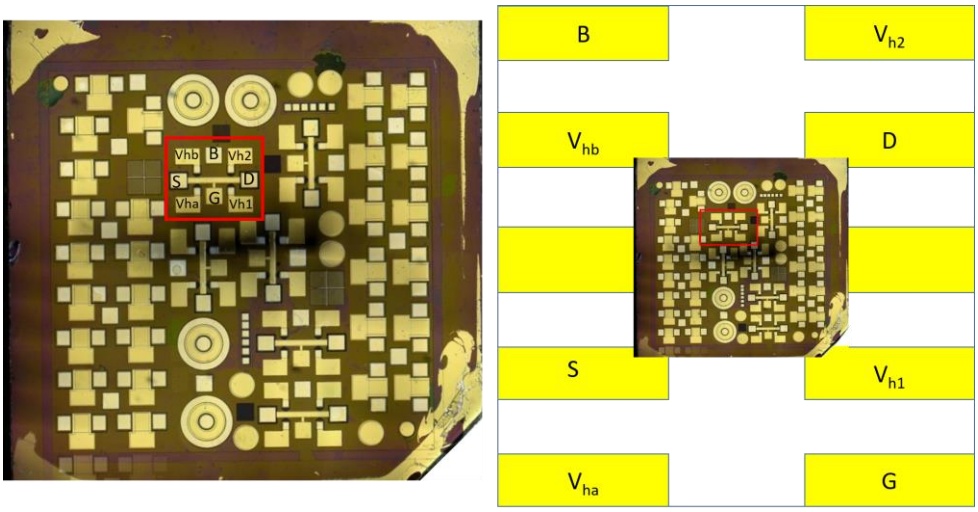

Fig.5.3.2. The schematic configuration of Hall bar MOSFETs before wire bonding.

in power semiconductor device, such as MOSFET, IGBT etc. and the packages are always plated gold film for high reliability [5]. All the wire bonding was carried out in the Department of Electrical Engineering at Auburn university. Before wire bonding, all samples were mounted on separate alumina substrates with gold pads by thermal conductive epoxy and baked for 4 hours at 120°C for wire-bonding. The configuration of Hall bar MOSFETs before and after wire bonding is shown in Fig.5.3.2 and Fig.5.3.3.

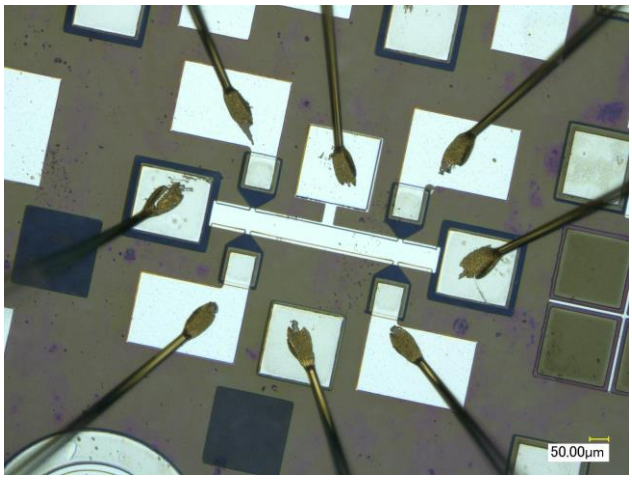

Fig.5.3.3. The schematic configuration of Hall bar MOSFETs after wire bonding.

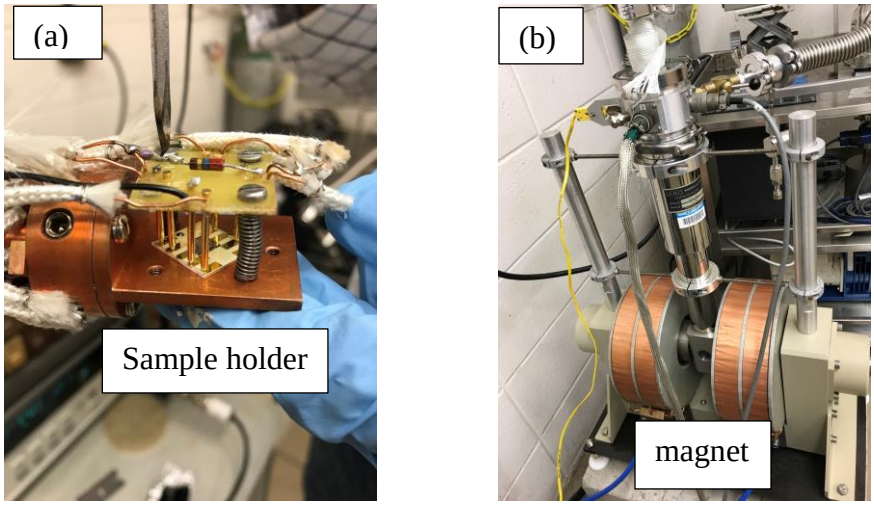

Fig.5.4.1. (a) The schematic illustration of connection between sample and sample holder; (b) Magnetic field generator in Hall system.

5.4 Hall system and measurement setup

Hall effect measurements on Hall bar MOSFETs in this study were performed in the Hall system in our lab, including an electro-magnet to provide magnetic field by a generator with the maximum B-field of 0.6 Tesla, a sample holder and environmental control system (for temperature change), as shown in Fig.5.4.1. The sample was connected to the measurement system by the sample holder through 8 pins according to 8 gold pads that are wire bonded to the metal contacts of the sample. These pins are connected to a capacitor and a resistor to protect the sample from damage under high gate voltage. After the sample was well connected to the holder, it was loaded in the chamber vertically to make sure the plane of the sample is perpendicular to the direction of magnetic field.

The selection of measurement equipment is based on sample's total resistance. Fig.5.4.2 shows the overview of instrumentation solutions for Hall effect measurements on samples with different resistance provided by Keithley [6]. The measurement equipment used in this study are all Keithley instruments. For SiC devices, the total resistance is in mid-to super-high range (100 mΩ to 10 TΩ). Thus, 1 model 6220 precision current source, 1 model 6514 electrometer, 1 model 7001 switch mainframe, 1 model 2410 sourcemeter and 1 model 2182A nanovoltmeter have been used for the measurements. The Hall system is also connected to a magnet power supply and a temperature controller to generate magnetic field and control temperatures in the chamber, respectively.

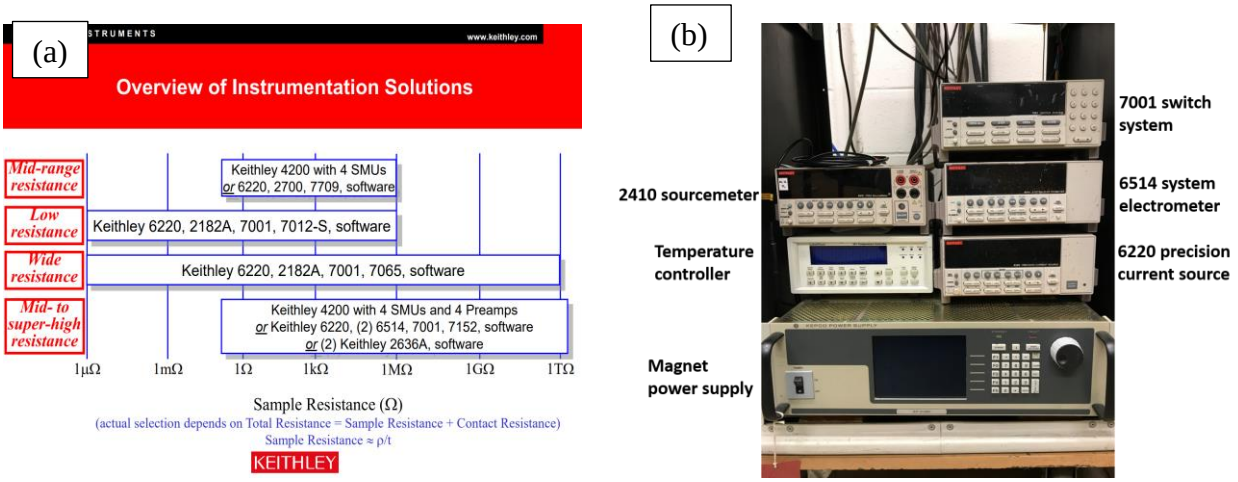

Fig.5.4.2. (a) Overview of instrumentation solutions for Hall effect measurements [6]; (b) The measurement equipment used in this study.

5.5 Results and discussion

Note the 'BSG' MOSFETs studied in this chapter are with low B% and 'Sb+NO' MOSFETs are normally-on devices due to more activated Sb in channel region. I_D-V_G measurements were performed at room temperature on 'NO', 'Sb+NO' and 'BSG' Hall bar MOSFETs before and after loading in the Hall system to make sure the consistency of results measured in different systems. Sheet resistance and Hall measurements were carried out on the same Hall bar MOSFETs at different temperatures. Field-effect mobility μ_{FE}, free carrier density n_{free} and Hall mobility μ_H were extracted from the I_D-V_G and Hall data assuming a Hall scattering factor of 1, which is believed accurate to within ~ ± 10% [7]. A summary of sample with various processes is shown in Table 5-1.

Table 5-1. Summary of samples with different processes

Sample	p-well doping	Sb implantion	Oxidation process
NO	$1x10^{16}/cm^3$	N/A	Thermal + NO annealing
Sb+NO	$1x10^{16}/cm^3$	Dose: $2.5x10^{13}/cm^2$	Thermal + NO annealing
BSG	$1x10^{16}/cm^3$	N/A	Thermal + PDS annealing

Fig.5.5.1 shows the comparison of field-effect mobilities of 'BSG' Hall bar MOSFET extracted by I_D–V_G measurements before and after loading the samples in the Hall system at 293 K with a fixed drain voltage V_D = 25 mV and 0.75 V, respectively. The results indicate good agreement of field-effect mobility obtained in different measurement systems. The shift of the

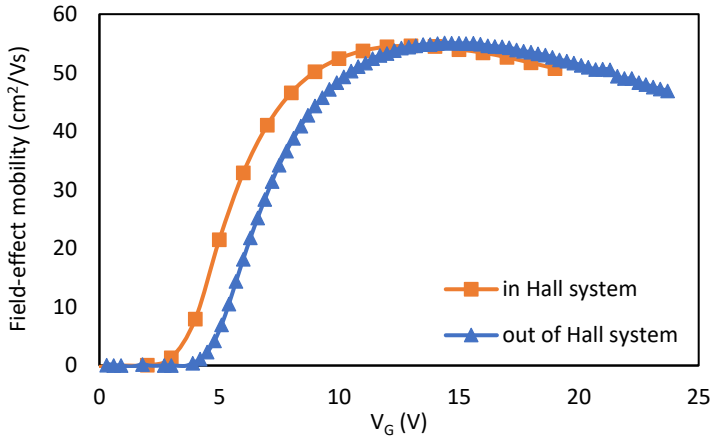

Fig.5.5.1. Field-effect mobilities of 'BSG' Hall bar MOSFET extracted by I_D–V_G measurements in and out of the Hall system at 293 K.

mobility curve should be due to different calibrations in different systems or V_{th} shift by repeated measurements.

5.5.1 Free carrier density as a function of gate voltage

The Hall effect measurements were carried out with a magnetic field of 0.6 T and V_D of 0.75 V. Also, I_D–V_G measurements were performed before sheet resistance and after Hall measurements to make sure the V_{th} does not move during the whole measurements at each temperature to keep the accuracy of sheet resistance, n_{free} and μ_H. n_{free} as a function of V_G at room temperature for the 'NO', 'Sb+NO' and 'BSG' Hall bar MOSFETs are shown in Fig.5.5.2. Since the total free carrier density can be determined by $C_{ox}(V_G-V_{th})$ in strong inversion, the degree of electron trapping in strong inversion can be estimated by the ratio of the slope of n_{free}-V_G characteristic and C_{ox}/q [8]. In this regard, the slope of the n_{free} vs.V_G curve is ~ 16.5%, 12.7% and 23.0% of C_{ox}/q for 'NO', 'Sb+NO' and 'BSG' MOSFETs, respectively. As discussed in previous chapter, the D_{it} for 'NO' and 'Sb+NO' MOSFETs is expected to be similar since the primary effect of Sb is counter-doping. The lower degree of electron trapping for 'Sb+NO' device than 'NO' should be attributed to higher free carrier concentration by counter-doping and the small effect of trap passivation by Sb. However, with passivation effect of fast interface traps, electron trapping

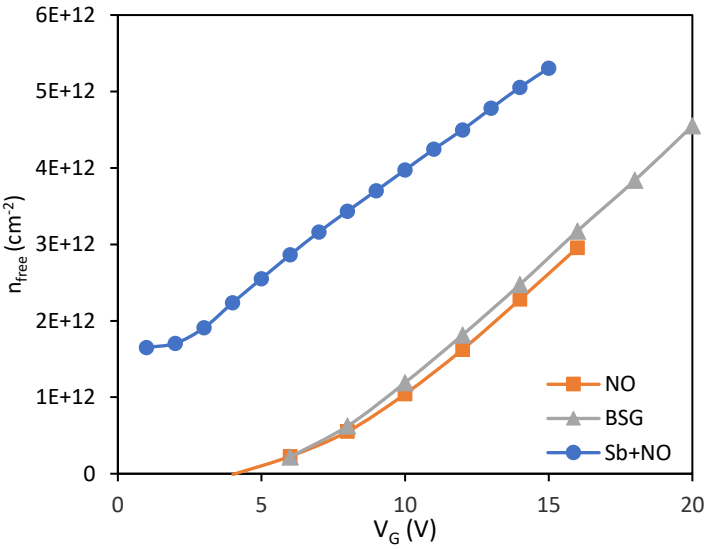

Fig.5.5.2. n_{free} as a function of V_G at 293 K for 'NO', 'Sb+NO' and 'BSG' Hall bar MOSFETs.

degree of 'BSG' is higher than 'NO'. This should be caused by higher D_{it} with lower B% in BSG. The degree of electron trapping of 3 Hall bar MOSFETs was summarized in Table 5-2.

Table 5-2. The degree of electron trapping estimated from n_{free} vs. V_G at 293 K

Sample	Slope of n_{free} vs. V_G	C_{ox}/q	Degree of electron trapping
NO	3.34×10^{11}/V·cm^2	4.0×10^{11}/V·cm^2	16.5%
Sb+NO	2.62×10^{11}/V·cm^2	3.0×10^{11}/V·cm^2	12.7%
BSG	3.45×10^{11}/V·cm^2	4.48×10^{11}/V·cm^2	23.0%

Fig.5.5.3 shows the free electron density from Hall measurements on 'NO', 'Sb+NO' and 'BSG' hall bar MOSFETs as a function of gate voltage at different temperatures. It can be seen the slope of the n_{free} vs. V_G on 'BSG' keeps almost constant from 77 K to 293 K and slightly increases at 375 K due to less electron trapping or higher Sb ionization at higher temperature.

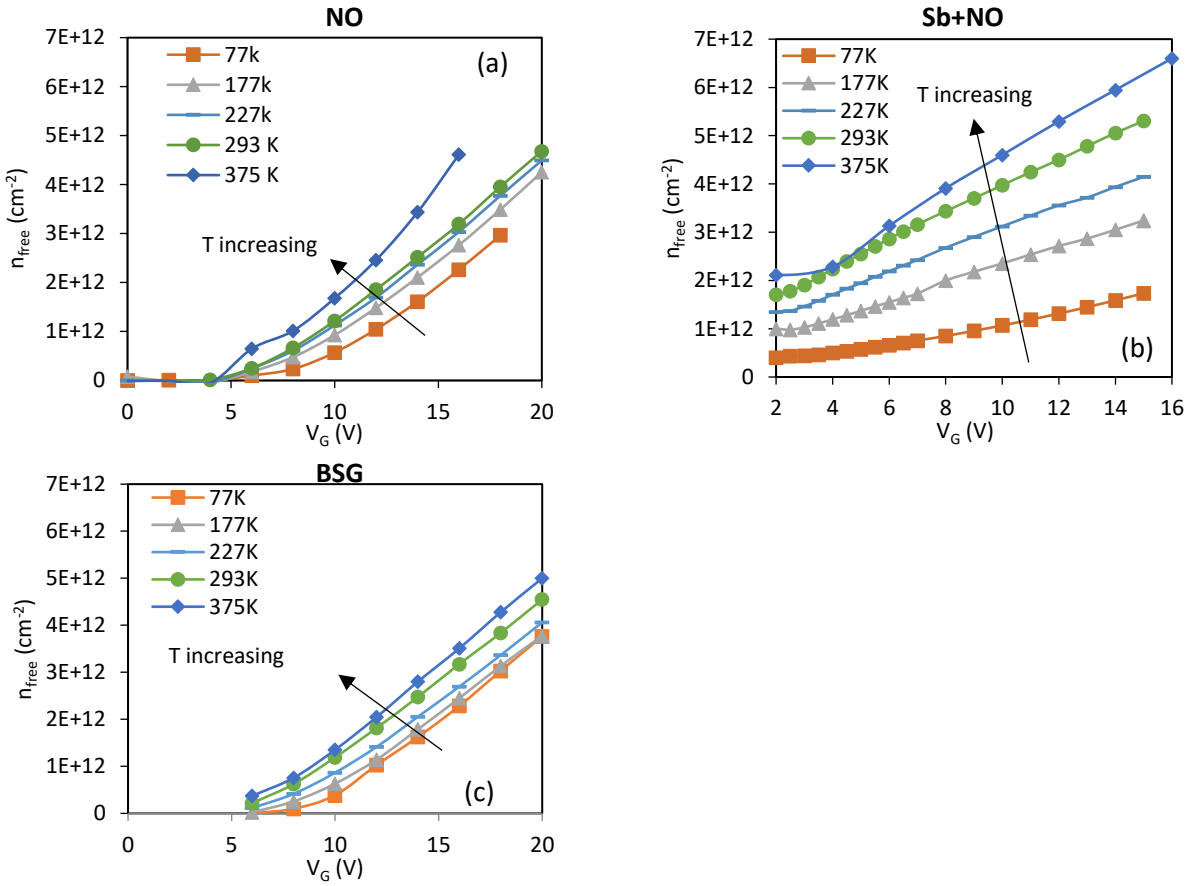

Fig.5.5.3. Free electron density vs. V_G as a function of temperature in (a) 'NO' (b) 'Sb+NO' and (c) 'BSG' Hall bar MOSFETs.

Similar behavior of temperature dependence of free electron was observed on 'NO', except for a fast increasing of n_{free} with V_G at 375 K, which is possibly due to some mobile ions. On the other hand, the slope of the n_{free} vs. V_G on 'Sb+NO' increases with temperature due to the increase of carrier concentration resulting from greater ionization of Sb donors at higher temperatures.

5.5.2 Electron mobility in depletion mode of Sb-doped n-channel MOSFETs

The utilization of accumulation-mode n-channel MOSFETs has been suggested to circumvent large on-state resistance due to poor inversion-layer mobility, which is attributed to high interface trap density [9, 10]. The accumulation-mode n-channel MOSFETs are realized by the implantation of n-type dopants (typically nitrogen) in the channel region located between 0.2 μm and 0.7 μm from the surface of the substrate [11, 12]. When the MOSFETs are biased in accumulation, the conduction of electrons occurs both through the surface accumulation layer and the bulk channel created by positive gate voltage. Thus, it is expected that accumulation-layer mobility is larger than inversion-layer mobility as seen in Si MOS technology [13]. The operation of accumulation-mode n-channel MOSFETs under negative and positive gate biases is shown in Fig.5.5.4.

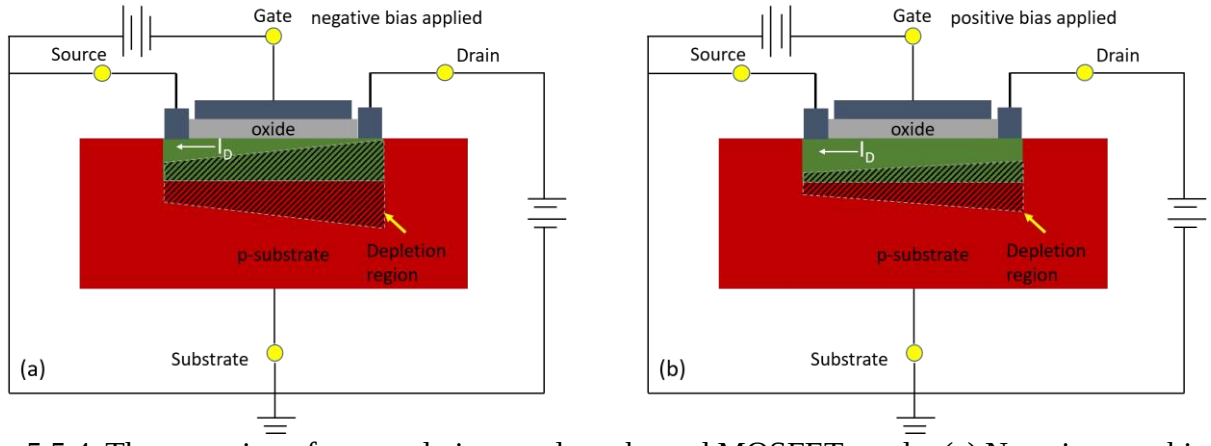

Fig.5.5.4. The operation of accumulation-mode n-channel MOSFETs under (a) Negative gate bias and (b) Positive gate bias.

The ‘Sb+NO’ Hall bar MOSFET studied in this experiment is an accumulation-mode n-channel MOSFET realized by a deeper Sb implantation in the channel region than the one studied in previous chapters. The I_D-V_G characteristics of ‘NO’ and ‘Sb+NO’ Hall bar MOSFETs at room temperature is shown in Fig.5.5.5 (a). It is clearly seen a normally-on behavior on the ‘Sb+NO’ sample with a high drain current of ~$7x10^{-7}$ A at negative gate voltage range due to Sb implantation. In accumulation-layer mode with high enough positive gate bias, the conduction through the surface accumulation layer and the inversion channel results in a much higher drain current on ‘Sb+NO’ than on ‘NO’ at the same gate voltage. Also, the Hall mobility with Sb implantation is ~3 times higher than that with NO annealing only, as shown in Fig.5.5.5 (b).

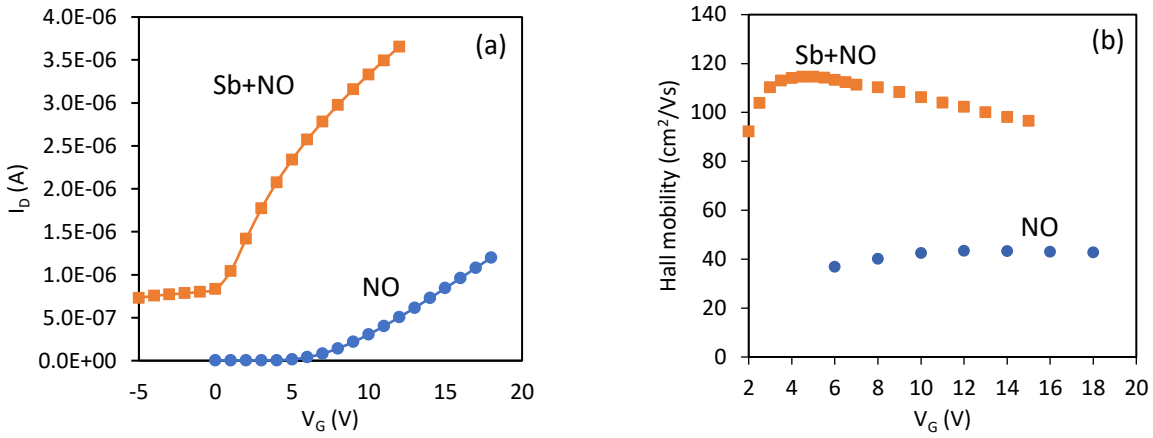

Fig.5.5.5. (a) I_D-V_G characteristics and (b) Hall mobility of ‘NO’ and ‘Sb+NO’ Hall bar MOSFETs at room temperature.

5.5.3 Carrier scattering mechanisms in inversion layer

It is widely accepted that the channel mobility in SiC MOSFETs is determined by the following scattering mechanisms: Coulomb scattering by interface charges and ionized impurities in the bulk, surface roughness scattering at high electric fields normal to the surface as well as surface phonon and bulk phonon scattering [8, 14]. To better identify the dominant scattering mechanism on various interface configurations, the dependence of Hall mobility on free carrier concentration n_{free} has been evaluated for ‘NO’, ‘Sb+NO’ and ‘BSG’ MOSFETs as a function of temperature. Fig.5.5.6 shows the Hall mobility as a function of free carrier concentration n_{free} at different temperatures ranging from 77 K to 375 K for ‘NO’, ‘Sb+NO’ and ‘BSG’ Hall bar

MOSFETs. For 'NO', as shown in Fig.5.5.6 (a), Hall mobility proportionally increases with carrier concentration with a power of ~0.2 at low n_{free} range below $10^{12}/cm^2$ at each temperature, representing the screening effect by increasing n_{free} from the Coulomb scattering centers trapped by interface traps, which is consistent with the results reported in [15]. When n_{free} is above $10^{12}/cm^2$, the Hall mobility shows carrier independence behavior with constant value at each temperature, clearly indicating surface phonon scattering or/and surface roughness scattering starts to play a role. The asymptotic trends of Hall mobility components associated with the surface phonon scattering has been reported to be $n_{free}^{-1/3}$ [8]. Thus, the results indicate a competing of Coulomb scattering and surface phonon scattering or/and surface roughness scattering on Hall

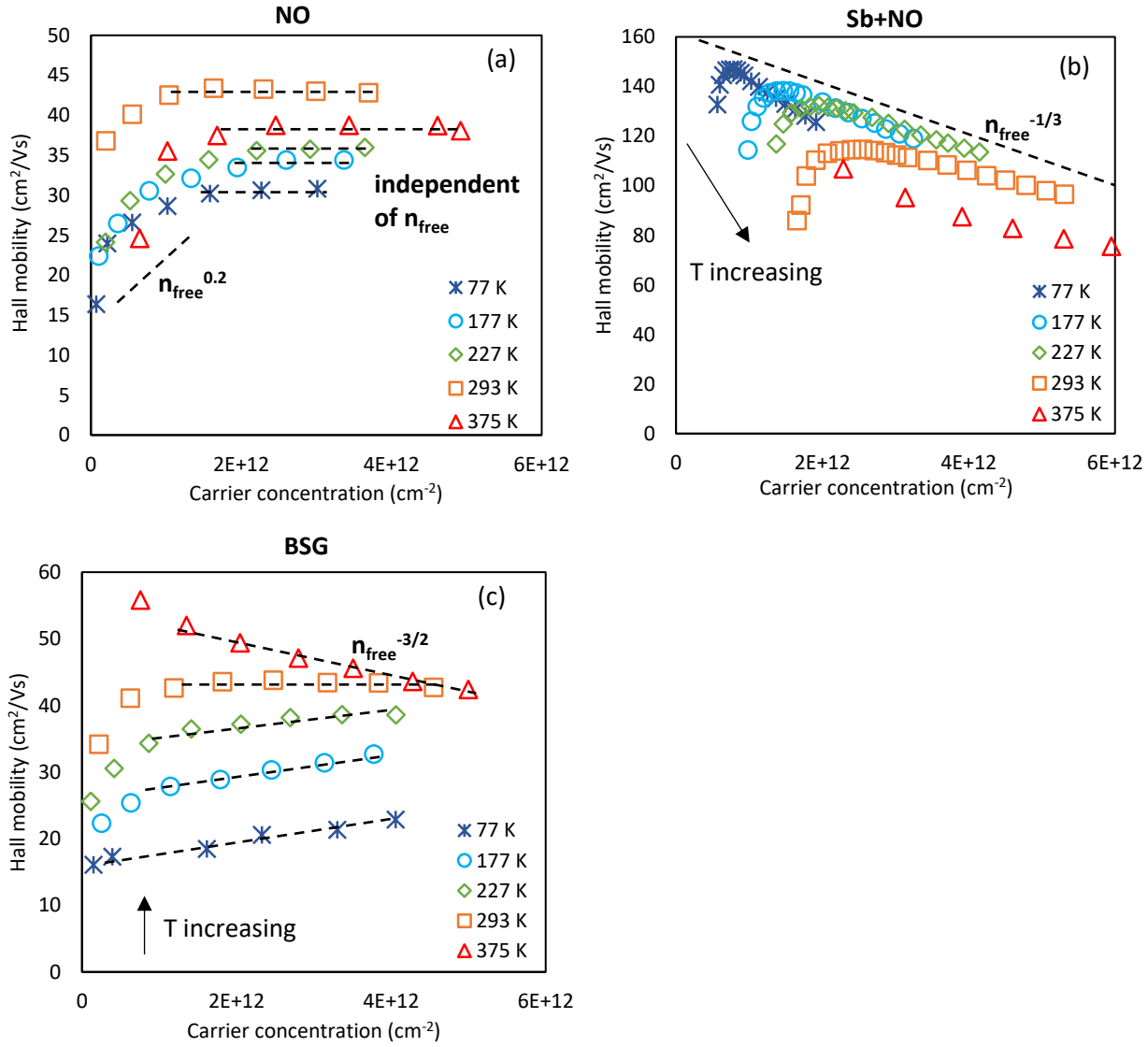

Fig.5.5.6. Dependence of Hall mobility on free carrier concentration n_{free} as a function of temperature for (a) 'NO', (b) 'Sb+NO' and (c) 'BSG' Hall bar MOSFETs.

mobility. For 'Sb+NO', the increasing of Hall mobility with n_{free} at weak accumulation range was also observed due to Coulomb scattering screening, as shown in Fig.5.5.6 (b). Right after maximum, Hall mobility decreases with n_{free} at high n_{free} region approximately following the $n_{free}^{-1/3}$ trend at each temperature, which allows us to conclude that it is the phonon scattering dominant regime. Compared to 'NO', the weaker Coulomb scattering effect on 'Sb+NO' is probably because the electrons are flowing in a wider channel and the electrons farther away from the interface are weakly affected by scattering centers at the interface. In Fig.5.5.6 (c), a similar behavior of Hall mobility to 'NO' and 'Sb+NO' at low n_{free} range was observed on 'BSG' as well. However, Hall mobility keeps increasing slowly with n_{free} at high n_{free} region from 77 K to 293 K, reflecting a strong Coulomb scattering effect extending to higher n_{free} regime and competing with a weak phonon scattering effect and/or surface roughness scattering. The effect of Coulomb scattering at high n_{free} is getting weaker with temperature increasing due to higher phonon scattering getting involved. At 375 K, Hall mobility is shown to be limited by both phonon scattering and surface roughness scattering following a trend of $n_{free}^{-3/2}$ due to more severe degradation by surface roughness with the trend of n_{free}^{-2} [8].

It should be noted that each scattering mechanism has its specific temperature dependence. Coulomb scattering decreases with temperature increasing while phonon scattering increases. Surface roughness scattering is almost independent of temperature. Fig.5.5.7 shows the Hall mobility as a function of temperature ranging from 77 K to 375 K with different free carrier concentrations for 'NO', 'Sb+NO' and 'BSG' Hall bar MOSFETs. For 'NO', Hall mobility clearly reveals three temperature dependence regimes at each n_{free}, as shown in Fig.5.5.7 (a). Hall mobility proportionally increases with temperature with a power of ~0.15 from 77 K to 227 K and a power of ~0.8 from 227 K to 293 K respectively, as a result of weaker Coulomb scattering at higher temperatures. This is a signature of a Coulomb scattering limited regime. Above 293 K, the power-law relationship of $\sim T^{-0.4}$ represents the dominance of phonon scattering effects. For 'Sb+NO', Hall mobility monotonically decreases with temperature increasing at any n_{free} following a trend of $\sim T^{-0.3}$, reflecting a phonon scattering limited mobility in the studied temperature range, as shown in Fig.5.5.7 (b). This is in stark contrast to the temperature dependence behavior of field-effect mobility, which increases with temperature from 77 K to room temperature greater ionization of Sb donors. Fig.5.5.7 (c) shows the Hall mobility for 'BSG' increases with temperature increasing

at each n_{free} with a power-low relationship of ~$T^{0.6}$, which is an evidence of Coulomb scattering dominant regime.

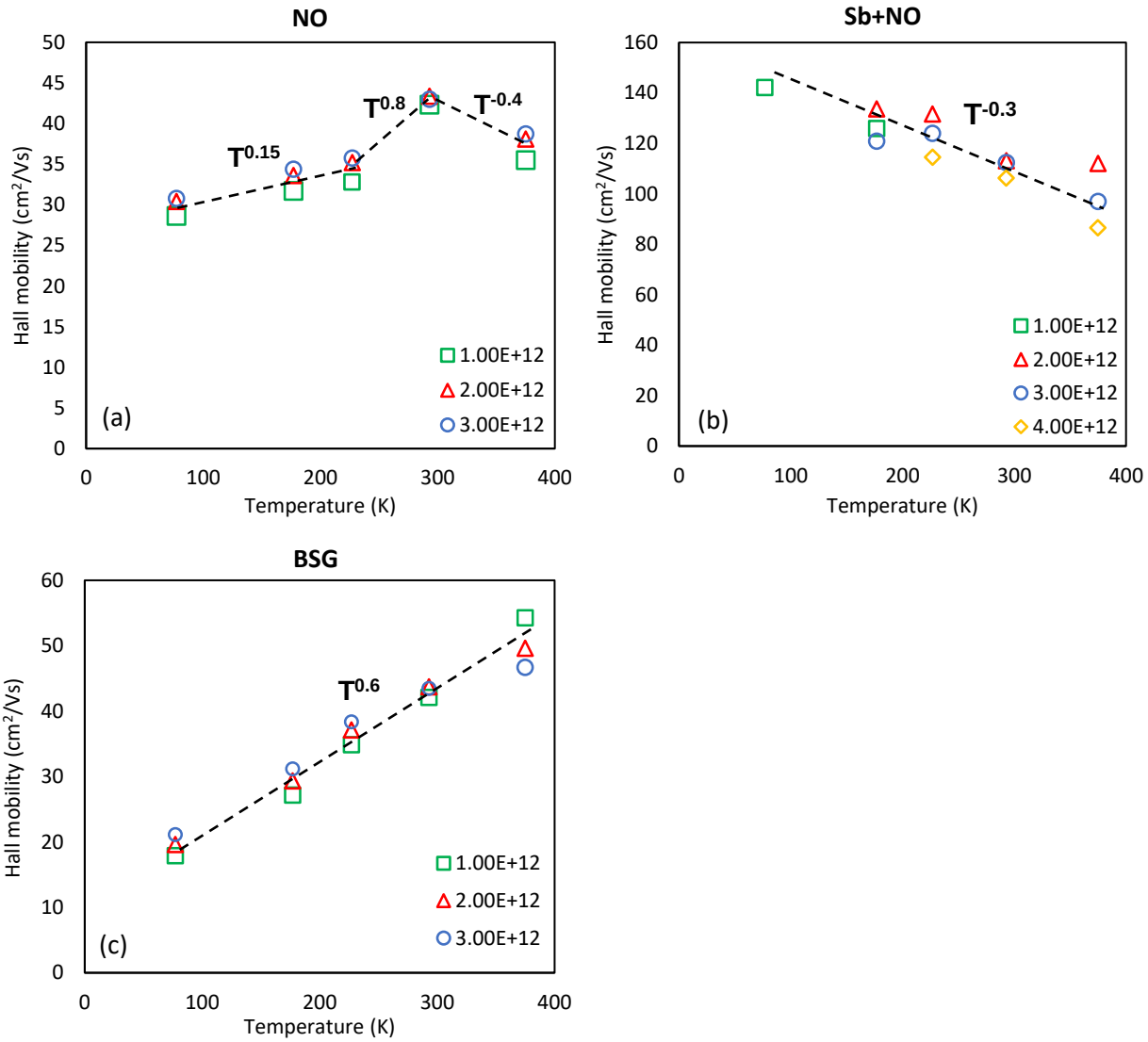

Fig.5.5.7. Dependence of Hall mobility on temperature as a function of free carrier concentration n_{free} for (a) 'NO', (b) 'Sb+NO' and (c) 'BSG' Hall bar MOSFETs.

In Si MOSFETs, the electron channel mobility shows a universal behavior at high electric fields normal to the surface, where interface configurations and doping concentrations do not affect the channel mobility in this regime significantly [16, 17]. This result is an evidence that the channel mobility of Si MOSFETs is predominantly limited by the phonon scattering and surface roughness scattering. However, for SiC MOSFETs, channel mobility is mainly limited by Coulomb

scattering, especially at low electric field due to the considerably large density of interface traps. In this study, it can be seen the dominance of Coulomb scattering on 'BSG' MOSFETs and a competing mechanism between Coulomb scattering and phonon scattering or/and surface roughness scattering on 'NO' MOSFETs as a result of high interface trap density. It is interesting to note that for 'Sb+NO', no significant Coulomb scattering effect was observed at the same n_{free} as 'NO' and 'BSG'. This should not be associated with higher screening of Coulomb scattering with the same n_{free}. Instead, it may be caused by wider channel by Sb implantation.

5.5.4 Comparison of field-effect mobility and Hall mobility

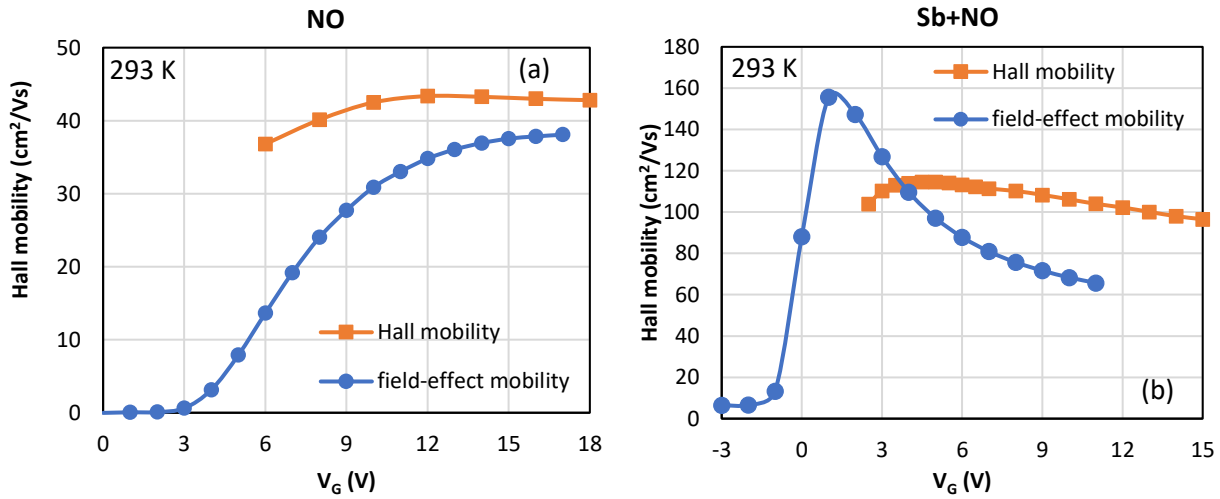

Fig.5.5.8. Comparison of field-effect mobility and Hall mobility at room temperature for (a) 'NO', (b) 'Sb+NO' Hall bar MOSFETs.

Fig.5.5.8 shows the comparison of field-effect mobility and Hall mobility at room temperature on 'NO' and 'Sb+NO' MOSFETs. The field-effect mobility and Hall mobility were both measured in the Hall system. For 'NO' MOSFETs, Hall mobility is higher than field-effect mobility, which confirms that field-effect mobility underestimates the actual electron mobility due to electron trapping by interface traps. However, Hall mobility is lower than field-effect mobility at low electric fields for 'Sb+NO' MOSFETs, which is caused by Sb counter-doping effect at low fields. This also indicates the limit of drain current transconductance for electron mobility characterization, as a result of the sensitivity to the combination effect of free electron density and

electron mobility. Hall mobility is higher than field-effect mobility at the gate voltage above 2 V with the dominance of phonon scattering effect.

5.6 Summary

In this chapter, we employed Hall effect measurements to determine the free carrier concentration and the carrier mobility of 4H-SiC Hall bar MOSFETs with different interface configurations. Compared with field-effect mobility and effective mobility analysis, the major advantage of Hall effect measurements is that actual carrier mobility and n_{free} are correctly determined independently without consideration of threshold voltage, which is difficult to accurately determine in the case of considerable interface trapping.

In order to better understand the effect of NO annealing, BSG gate dielectric and Sb channel implantation on electron trapping by interface traps as well as the mechanism of different scattering effects on carrier mobility, 'NO', 'Sb+NO' and 'BSG' hall bar MOSFETs were fabricated, wire bonded and characterized by Hall effect measurements. Unlike a universal behavior at high electric fields shown in Si MOSFETs, channel mobility is mainly limited by Coulomb scattering for SiC MOSFETs, especially at low electric field due to the considerably large density of interface traps. It can be seen the dominance of Coulomb scattering on 'BSG' (low B%) MOSFETs and a competing mechanism between Coulomb scattering and phonon scattering or/and surface roughness scattering on 'NO' MOSFETs as a result of high interface trap density. For 'Sb+NO' (normally-on), no significant Coulomb scattering effect was observed at the same n_{free} as 'NO' and 'BSG'. Instead, a strong effect of phonon scattering is dominant, which is probably associated with wider channel by Sb implantation. The higher field-effect mobility than Hall mobility observed on the 'Sb+NO' MOSFETs at low electric fields confirms the limit of field-effect mobility and the necessity of Hall effect characterization to accurately obtain electron mobility of SiC MOSFETs.

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Chapter 6

Conclusion and future work

6.1 Conclusion

SiC is one of the most promising materials for high voltage power electronics due to its wide bandgap, high thermal conductivity and high breakdown field. 4H-SiC is more advantaged than other polytypes since it has larger bandgap and higher electron mobility. However, low channel mobility and oxide reliability concerns attributed to the existence of different types of charge traps, either in gate oxide or at the SiO_2/SiC interface are challenges for further development of SiC power devices. Various channel engineering processes have been proposed to address these issues beyond post oxidation annealing by NO, which is the standard process to obtain the most stable gate oxide together with improved channel mobility from single digit to ~35 $cm^2/V{\cdot}s$. Although (0001) Si-face 4H-SiC power devices have been commercialized by NO annealing process, the quality of the gate oxide and interface of oxide/4H-SiC is still far from a satisfactory level. Further improvement in channel mobility and device stability is absolutely required for the development of next-generation SiC power devices.

In this dissertation, shallow antimony (Sb) implantations ($2.5x10^{13}/cm^2$ and $5.0x10^{13}/cm^2$) in channel region with heavily doped p-wells ($1x10^{17}/cm^3$ and $5x10^{17}/cm^3$) have been demonstrated for the improvement of channel transport for 4H-SiC MOSFETs. Borosilicate glass (BSG) gate dielectric formed by different processes has been employed on 4H-SiC MOSFETs for the investigation of the impact of BSG on interface traps and channel mobility. The combination of Sb implantation and BSG gate dielectric for 4H-SiC MOSFETs also has been carried out for further improvement of device performance. In order to better understand the mechanism of different scattering effects on carrier mobility, Hall effect measurements have been performed on the Hall bar MOSFETs with various interface configurations. The major findings in this work are:

- Compared with standard NO annealing, an improvement of subthreshold slope (SS) as well as channel mobility (~1.5x) has been observed on the MOSFETs with Sb doping. A

reduction of V_{th} on devices with Sb doping has been also observed due to the compensation of the p-type acceptors in the surface region by Sb donors.

- The mechanism of Sb counter-doping on the improvement of SS and μ_{FE} is probably: 1) Higher free carrier density at the same V_G and more efficient screening of Coulomb scattering; 2) Less filled traps at V_{th} due to less band bending; 3) Lower surface roughness due to lower electric field at the surface with the same carrier density.
- The field-effect mobility with Sb implantation reveals the effects of Coulomb scattering at low oxide fields and phonon scattering as well as surface roughness scattering at high oxide fields. Sb counter-doping effect is obvious at low oxide fields due to higher free electron density and wider channel.
- Improvement of channel mobility over a wide range of transverse electric fields with peak value of 140 $cm^2/V{\cdot}s$ was achieved by using BSG gate dielectric due to significantly low fast interface trap density estimated by C-ψ_s analysis. The correlation between B concentration and electrical results indicates that interface trap density decreases with increasing B concentration, which in turn, results in higher channel mobility with higher B concentration.
- V_{th} shifts to right has been observed on BSG-gated 4H-SiC MOSFETs under positive bias temperature stress, indicating the presence of significant oxide traps and electron trapping under BTS in BSG. It also shows larger V_{th} shift with higher channel mobility (higher B concentration). However, it is still not clear whether the instability of V_{th} is correlated with B concentration.
- By combining BSG gate dielectric and Sb surface doped channels in lateral 4H-SiC MOSFETs, further improvement of channel mobility and a tunable threshold voltage were achieved with the best μ-V_{th} trade-off.
- Carrier concentration and carrier mobility estimated by Hall effect measurements on 4H-SiC MOSFETs with NO annealing, ‘Sb+NO’ (normally-on) and ‘BSG’ (low B%) gate dielectric shows the dominance of Coulomb scattering on ‘BSG’ MOSFETs and a competing mechanism between Coulomb scattering and phonon scattering or/and surface roughness scattering on ‘NO’ MOSFETs as a result of high interface trap density. For ‘Sb+NO’, instead of Coulomb scattering, a strong effect of phonon scattering is dominant, which is probably associated with heavy Sb ions vibration near the surface and in the bulk.

- The higher field-effect mobility than Hall mobility observed on the 'Sb+NO' MOSFETs at low electric fields confirms the limit of field-effect mobility and the necessity of Hall effect characterization to accurately obtain electron mobility of SiC MOSFETs. The limit of field-effect mobility is caused by the sensitivity to the combination effect of free electron density and electron mobility.

6.2 Future work

- Sb channel doping:

  The challenge for the application of Sb channel doping is the optimization of Sb profile in the channel region of 4H-SiC MOSFETs. In this work, Sb loss was intentional in order to obtain normally-off devices. However, counter-doping effect will be dramatically reduced with large amount of Sb loss. Therefore, it is important to optimize Sb dose and depth in channel region to realize normally-off devices with good counter-doping effect.

- While the results discussed in previous chapters highlight the advantage of BSG gate dielectric for 4H-SiC MOSFETs from the point of view of interface traps and channel mobility, further study on the stability of BSG should be carried out to understand the mechanism of B-induced device instability for SiC MOSFETs from the following points:
  a) Instead of interface traps, characterize on oxide traps.
  b) It has not been clarified the percentage of activated B in SiC during the annealing process. The penetration of B could result in V_{th} variation and it could be a big issue for the stability of V_{th}. This penetration effect of B can be studied by making a diode on 4H-SiC substrate after removing BSG.
- It is necessary to find better methods for BSG formation to obtain high and consistent B%.
- The stacking dielectric should be formed by thin BSG combined with deposited SiO_2 to address the stability issues caused by B in the bulk of BSG.
- Hall effect characterization on MOSFETs with high B%.
- Hall effect characterization on the normally-on 'Sb+NO' MOSFETs as a function of body bias to investigate the effect of vertical electrical fields on Hall mobility with constant free carrier concentration.

Appendix A. Atomic boron percentage calculation

1. 1 mol = 6.02×10^{23} molecules (The number of molecules in 1 mol)
2. 1 SiO_2 molecule has 3 atoms
3. 1 mol SiO_2 = 6.02×10^{23} x 3 atoms (The number of atoms in 1 mol SiO_2)
4. Molar mass of SiO_2 = (28 + 32) g/mol = 60 g/mol
5. Density of SiO_2 = 2.65 g/cm^3
6. Concentration of SiO_2 = 2.65 x 6.02×10^{23} x 3 /60 = 7.9765×10^{22} $atoms/cm^3$
7. B% =concentration of B (from SIMS) / concentration of SiO_2

Appendix B. Sample cleaning process

1. Use a cotton swab and acetone to remove the glue on SiC sample surface. The next set of steps removes organic compounds on sample surface.
2. After surface appears clean by inspection with microscope, place sample in a beaker of acetone and place in the ultrasonic system for 5 min.
3. Remove sample and place in trichloroethylene (TCE) beaker in ultrasonic cleaner for 5 min.
4. Remove sample and place in acetone beaker in ultrasonic cleaner for 5 min.
5. Remove sample and place in methanol beaker in ultrasonic cleaner for 5 min.
6. Remove sample and place in a second methanol beaker in ultrasonic cleaner for 5 min.
7. Remove sample and place in deionized water (DI water) beaker in ultrasonic cleaner for 5 min.
8. Remove sample and place in buffered oxide etch (BOE) for 5 min.
9. Rinse sample in DI water.

The next set of steps removes inorganic compounds on sample surface.

10. Mix a solution of 1:1 H_2SO_4:H_2O_2 and place sample in solution for 15 min.
11. Rinse sample in DI water, then place sample in BOE for 2 min.
12. Mix a solution of 3:1:1 DI water:H_2O_2:NH_4OH and heat to 100-115°C.
13. Rinse sample in DI water and place in solution for 15 min.
14. Rinse sample in DI water and place in BOE for 2 min.
15. Mix a solution of 3:1:1 DI water:H_2O_2:HCl and heat to 100-115°C.
16. Rinse sample in DI water and place in solution for 15 min.
17. Rinse sample in DI water and place in BOE for 2 min.
18. Rinse sample and dry with N_2 air gun.

Appendix C. Sample oxidation process

1. Vacuum oxidation furnace tube until base pressure is less than 1 torr.
2. Prepare argon tank and fill oxidation furnace tube to atmospheric pressure.
3. Flush oxidation furnace tube with argon for 10-15 min to remove residual gases.
4. Load samples into oxidation furnace tube.
5. Vacuum oxidation furnace tube for 10-15 min.
6. When pressure is less than 1 torr, fill and flush with argon for 10-15 min.
7. Set oxidation furnace temperature to 1150°C and the ramp rate to 5°C/min.
8. When temperature is at 1150°C, stop argon flow and begin oxygen flow at 500 sccm.
9. Record the start time.
10. Let oxidation run for the desired time.
11. Record finish time.
12. Stop oxygen flow and begin argon flow.
13. Let sample anneal in argon for 30 min post oxidation.

Steps 14-22 are for NO passivation. If no NO passivation necessary, skip to step 23.

14. Increase temperature to 1175°C.
15. Flow argon through NO lines.
16. Begin NO flow and turn off argon flow.
17. Set NO regulator to 30 psi.
18. Flow NO at 575 sccm and anneal for 2h.
19. After anneal is finished, stop NO.
20. Let NO pressure drop to zero, and then flush NO lines with argon.
21. Stop argon flow in NO lines and vacuum NO lines until pressure is zero.
22. Stop vacuum of NO lines.
23. Set oxidation furnace temperature ramp rate to 10°C/min and ramp temperature down to oxidation furnace base temperature.
24. Remove samples from oxidation furnace tube.

Appendix D. B_2O_3 PDS annealing procedure

1. Load B_2O_3 planar diffusion source in the annealing furnace.
2. Load samples in the furnace with oxide facing to the B_2O_3 source.
3. Flush annealing furnace with argon at 50 sccm for 25 min to remove residual gases.
4. With argon flowing at 50 sccm, increase temperature to 950°C in 30 min.
5. As the temperature reaches 950°C, flow O_2 at 5sccm with argon for 30 min.
6. Stop O_2 after 30 min.
7. Decrease temperature to c.
8. Remove B_2O_3 planar diffusion source from the furnace.

Step 9-14 is the drive in process.

9. Load samples in the furnace.
10. With argon flowing at 50 sccm, increase temperature to 950°C in 30 min.
11. Keep the temperature at 950°C for 2 hours with argon flow.
12. Decrease temperature to 25°C in 30 min.
13. Remove samples from the furnace.
14. Stop argon.

Appendix E. Photolithography procedure

1. Place a drop of 5214E photoresist glue on the silicon wafer.
2. Attach sample to the wafer and put it in a 105°C oven. Do not let the oven temperature exceed 110°C.
3. Cook sample for 10 min in oven.
4. Begin mask aligner start-up procedure.
5. Remove wafer from oven.
6. Start spinner.
7. Put water in center of spinner.
8. Use a pipet with a disposable tip to cover sample with 5214E photoresist.
9. Run spinner for 30 seconds at 4000 RPM.
10. Place wafer in oven for 1 min. Do not exceed 1 min or 105°C.
11. Remove wafer.
12. Place wafer in mask aligner and adjust mask for appropriate pattern.
13. Expose sample to UV lamp for 30 seconds.
14. Remove wafer and place in a 1:4 ratio of AZ 400:H_2O for 10 sec and then quickly put it under running DI water.
15. The pattern should be visible when viewed under a microscope. If it is not, repeat step 14 for a few seconds.
16. When the pattern is clearly visible, check it under the microscope. If all of the lines are sharp, the pattern has been properly set.

Appendix F. DC sputtering procedure

1. Load samples into sputter system.
2. Put correct metal targets on sputter guns.
3. Close sputter system and vacuum pressure to 10-7 torr or less.
4. Flow Ultra High Pure Argon through sputter system, adjusting pressure to 18 mtorr.
5. Flow argon gas for 3 min.
6. Adjust voltage and current to appropriate settings for the selected metal target.
7. Pre-sputter for 2 min on dummy sample.
8. Sputter metal onto sample for appropriate length of time.
9. Stop argon flow.
10. Allow vacuum pump to empty chamber.
11. Stop vacuum pump and fill chamber to atmospheric pressure with nitrogen.
12. Remove samples.
13. Complete any necessary steps to return sputter system to stand-by mode.

Appendix G. Al evaporation procedure

1. Load Al pellets in the bridge holder.
2. Load samples with oxide facing down to the bridge holder.
3. When pressure is 10^{-7} torr, turn on AC power.
4. Pre-evaporate for 20 seconds when Al starts to glow on the cover plate.
5. Remove the cover plate and expose samples to the bridge holder.
6. Evaporate for 4 min.
7. Turn off AC power.
8. Cool the evaporation system for 10 min.
9. Remove samples and return the system to stand-by mode.

Appendix H. Reactive ion etch procedure

1. Open glass window of etcher.
2. Remove blank Si wafer.
3. Place and center sample on electrode.
4. Use large tweezers to press down on wafer to ensure it is securely in place.
5. Close the glass window and tighten until snug.
6. Vacuum system for 20-30 min or until system reaches base pressure (9-10 mtorr).
7. Open all valves to etch gas line and turn on the appropriate switch on the flow controller.
8. Turn on cooling water and open all water valves to system.
9. Turn on RF power supply.
10. Adjust power setting to about three (3) watts higher than the desired power.
11. Once the pressure has stabilized, turn on power supply.
12. If necessary, adjust power to appropriate level and adjust matching network to obtain the lowest possible reflected power.
13. After desired etch time, turn off the RF power.
14. Turn off the etchant gas and allow system to vacuum to base pressure.
15. If no other etching is required, close all valves and turn off system.
16. Fill etchant chamber to atmospheric pressure with nitrogen.
17. Remove the wafer with the sample and replace it with the blank Si wafer.

Appendix I. Ohmic anneal furnace procedure

1. Flow argon through Ohmic anneal furnace tube until atmospheric pressure is reached.
2. Adjust argon flow rate to 8 L/min.
3. Open loading area and load samples.
4. Close loading area.
5. Flush Ohmic anneal system with argon for 5 min.
6. Stop argon flow and vacuum Ohmic anneal furnace tube until 10-7 torr.
7. Stop vacuuming and flush system with argon for 5min at 12 L/min.
8. Insert samples into furnace and start timing for 30 seconds once sample temperature reaches 800°C.
9. After 30 seconds annealing is finished, transfer samples from furnace to loading area.
10. Remove samples from system.
11. Complete any necessary steps to return Ohmic anneal system to stand-by mode.

Appendix J. Carbon cap procedure

1. Mount sample on Si wafer with water soluble wax.
2. Spin on 5214E photoresist at 4000 RPM for 30 sec.
3. Remove sample from wafer and put in water for 15 min.
4. Bake photoresist-covered SiC in oven at 100-110°C for 15 min.
5. Put the sample into the designated carbon cap carbon box, with photoresist facing up.
6. Place this box into a high temperature anneal system.
7. Reduce system pressure to 10-7 torr.
8. Fill chamber with argon.
9. Reduce argon flow to 3-4 psi.
10. Create a table containing these columns: variac %; system operation time; current temperature of the system.
11. Increase variac to 10% and wait ten minutes and make recordings in table.
12. Increase variac 5% every two minutes and make recordings in table.
13. When temperature nears 600°C, adjust variac until temperature stabilizes near 600°C.
14. Keep the system at 600°C±5°C for 30 min.
15. Turn off variac.
16. When temperature is less than 50°C, open high temperature anneal system.
17. Carefully remove sample and return carbon cap box to its storage container.
18. Stop argon flow.
19. Vacuum system to base pressure.

Appendix K. SiC dopant activation anneal procedure

1. Complete carbon cap process first (Appendix J).
2. Place sample, with carbon cap face down, in designated carbon box for activation anneal.
3. Fill high temperature anneal system with argon, and then load the sample.
4. Vacuum system until pressure is 8x10-7 torr.
5. Stop vacuuming and fill with argon to atmospheric pressure.
6. Flow argon at 12 psi.
7. Increase variac 1% every ten seconds until variac is at 60%.
8. When temperature approaches 1650°C, adjust variac until temperature stabilizes ~1650°C.
9. Hold temperature at 1650°C±5°C for 30 min.
10. Turn off variac.
11. When temperature is less than 50°C, open high temperature anneal system.
12. Carefully remove sample and return the carbon cap box to its storage container.
13. Stop argon flow.
14. Vacuum system down to base pressure.