CMOS STRESS SENSOR CIRCUITS

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CMOS STRESS SENSOR CIRCUITS

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Yonggang Chen, son of Jigeng Chen and Xi'ai Ren, was born November 17, 1968, in Taiyuan, People's Republic of China. He graduated from Taiyuan No. 5 High School in 1987. He enrolled at Xi'an Jiaotong University in Xi'an, P. R. China, in September 1987, completing a Bachelor of Engineering degree in Semiconductor Physics and Devices in July of 1991. After working as an engineer at Beijing General Research Institute for Nonferrous Metals (GRINM), in Beijing, P. R. China, for 8 years, he joined the Alabama Microelectronics Science and Technology Center at the Auburn University Electrical and Computer Engineering Department in 2000. He received his M. S degree in 2003 and remained at Auburn as he worked towards his PhD degree. He married Ye Wu, daughter of Zhaoliang Wu and Yuxian Bai, on July 3, 1996.

DISSERTATION ABSTRACT

CMOS STRESS SENSOR CIRCUITS

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Two CMOS piezoresistive stress sensor circuits based on piezoresistive MOSFETs (PiFETs) are the focus of this dissertation. The first design is a multiplexed array of 512 piezoresistive sensors fabricated on a 2.2 by 2.2mm^2 tiny chip. This array is composed of a PMOS array of 256 sensors and an NMOS array of 256 sensors, and an on-chip counter is used to scan the sensors in the array sequentially so that the sensors can be accessed with a limited number of I/O pins from the chip, allowing the data to be collected very efficiently. In the second design, a PMOS current mirror is used as a sensor cell and a delta-sigma modulator is used to detect the mismatch induced by stress. The output of the circuit is a modulated square wave that includes the sensor response information, and this can be either captured by digital equipment such as a counter, or by a radio receiver. The duty cycle of the output and DSBSC (Double side-band suppressed carrier) signal tone shift are proportional to the mismatch or applied stresses.

MOSIS AMI_ABN 1.5um CMOS technology was used for the chip design and chip fabrication for this study. The calibration process was performed using a chip-on-beam technique, which utilized finite element analysis by ANSYS to determine the stress distribution on the die surface under load applied by a four-point-bending (4PB) fixture. The sensor array chip is used to measure the die stress for chip-on-beam under 4PB load, chip-on-beam encapsulated with ME525 underfill and DIP40 package encapsulated with ME525 underfill. The highest resolution die stress mapping thus far available was obtained using the sensor array constructed for this project. The delta-sigma modulation based stress sensor proposed here did not include the low pass filters normally used with delta-sigma ADC, as the spectra used here are located in the portion of the bandwidth which is normally filtered in an ADC. The frequency shift of the signal reflects the mismatch induced by stress. This delta-sigma modulation sensor offers an effective way to implement a sensor with a transmitter, which may be used for remote or embedded sensor applications in which it is difficult to contact the sensor.

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CHAPTER 1.   INTRODUCTION

The electrical resistivity of silicon changes when stress is applied. This change of the electrical resistivity upon the application of an external stress is called the piezoresistive effect, and it has found many applications in the sensor area [1-21], of which pizoresistive stress sensors are important. Electronic packages typically involve materials with thermal expansion coefficient mismatches, which results in stresses inside the packages and silicon chips as the temperature changes. These stresses can degrade the performance and tolerances of both analog and digital circuits and in extreme cases may even lead to failure of the circuits. The growing demand for more reliable parts has led to the development of experimental techniques that can detect the stress distribution on the die, thus improving packages and minimizing stress induced failures.

Piezoresistive stress sensors may offer a much higher sensitivity than metallic stress sensors and can be fabricated into a die using microelectronic technology, thus providing non-intrusive measurements of the surface stress on a chip within encapsulated packages. As a result, piezoresistive stress sensors are now widely used for experimental structural analyses of electronic packages [1, 2, 6, 7, 15, 22-35].

Normally the piezoresistive stress sensors are constructed as resistors, MOSFETs (Metal-Oxide-Semiconductor Field-Effect-Transistors) [3, 31, 36-46], piezojunctions [47-50], Van der Pauw (VDP) sensors [51], inversion layer VDPs (ILVDP) [51], four-terminal Xducers [52-57], and current or voltage amplifiers [40]. These devices are measured directly to get a voltage or current change induced by the applied stress, and the stress values are then calculated accordingly. Interfaces used to read the sensor signals can be categorized as direct resistance measurements, bridges or amplifier offset sensors. All these devices generate analog signals, which are not only difficult to interface to digital instruments such as computers, but are also very sensitive to noise. Another problem is that the number of sensors that can be built on the chip is limited, so the special resolution of the information obtained by the sensors is low. Furthermore, errors from one sensor element may result in an improper determination of a many stress components.

Previously, 4x4 arrays of PMOS stress sensors exploiting the transverse pseudo-Hall effect in MOSFETs were used for wire-bonding characterization [45, 58]. CMOS arrays composed of CMOS differential pairs have been used for die stress characterization, but the number of sensors was limited by the available I/O pads that can be used to access the sensors in the array and hence only 49 sensors were built in the array with a die with 40 I/O pads [31].

The work in this dissertation focuses on two types of CMOS stress sensor designs[59, 60]. The first is a wireless capable stress sensor with digital and/or RF output. Highly precise components are difficult to implement on IC chips and all components may be disturbed by stress simultaneously, which make high precision sensor interfaces difficult to build. The new approach to building a sensor interface used in this study is based on sigma-delta modulation. The sensor core here is an orthogonal MOSFET current mirror, where a mismatch is generated between the transistors in the CMOS current mirror when a stress is applied. The mismatch information can then be extracted by comparing the currents going through two mirrored transistors and accumulating the difference using a delta-sigma modulator. At the same time the output is digitized, thus allowing the output signal to be averaged by a counter, captured by a computer, or monitored with a radio receiver. This makes the sensor output very convenient to process. Another advantage is that the sigma-delta type modulation can reveal precise mismatching information without requiring the use of highly precise analog components, which make it possible to build a highly precise sensor interface even in integrated circuits. Another advantage of this sensor system is that the output signal may be transmitted wirelessly and captured by a radio receiver, with the signal splitting around a center frequency that corresponds to zero mismatch. The second design used in this work is a CMOS stress sensor array made up of 512 current mirror type stress sensor cells, of which 256 are PMOS that sense in-plane normal stress differences and the other 256 cells are NMOS that sense in-plane shear stress. An on-chip counter was built to generate a signal that drives multiplexers in order to scan the sensors sequentially, which expands the ability to access more sensors, simplifies the measurement process, and increases the characterization through-put significantly. Both designs have been fabricated by MOSIS 1.5 μm CMOS technology. Sensor chips are calibrated using chip-on-beam with four point bending fixture, and sensor array chips are demonstrated in three applications.

In this dissertation, an overview of the principles of CMOS stress sensors will be given, along with a review of basic piezoresistive theories and CMOS mismatches in Chapter 2. Principles and design of a CMOS stress sensor with modulated output are described in Chapter 3, followed by a description of the design of CMOS stress sensor arrays in Chapter 4. In Chapter 5 the procedures involved in the calibration and characterization of stress sensor chips are described, and the results of these measurements are presented. The final chapter summarizes the study and gives suggestion for future research.

CHAPTER 2. CMOS STRESS SENSOR

This chapter reviews basic piezoresistive theory and the equations that govern piezoresistive MOSFET stress sensors and the MOSFET mismatches induced by the piezoresistive effect, concluding with a description of CMOS stress sensor cells.

2.1 Piezoresistive Effects

When a stress is applied to a piece of material, the resistance of the material will change. The resistance R of a rectangular conducting material is expressed by

$$R = \rho \frac{l}{wt} \tag{2.1}$$

where ρ is the resistivity and l, w and t are the length, width and thickness of the conductor, respectively. When stress is applied, the material will deform and the relative dimension changes will be $\Delta l/l$, $\Delta w/w$ and $\Delta t/t$, all of which contribute to the resistance change. The resistivity ρ may also change for some materials such as silicon due to the piezoresistive effect [47, 61, 62], so the total normalized resistance change can be written as

$$\frac{\Delta R}{R_0} = \frac{\Delta l}{l} - \frac{\Delta w}{w_0} - \frac{\Delta t}{t_0} + \frac{\Delta \rho}{\rho_0} \tag{2.2}$$

For those materials with no piezoresistive effect, the resistivity ρ remains constant and resistance changes due to the changes in dimensions dominate. In contrast, resistivity changes dominate for a material which is subject to the piezoresistive effect, while the change in resistance due to dimensional changes of the material can be neglected. This explains why a higher resistance change due to stress is found for semiconductor materials than for metals.

The conductivity of a semiconductor material is determined by both majority and minority carrier concentration and their mobility

$$\sigma = qn\mu_n + qp\mu_p \tag{2.3}$$

For a doped semiconductor with complete ionization, the majority concentration is determined by the doping level and the majority carrier concentration is much higher than the minority concentration, and the minority contribution can be neglected. For example, the conductivity of n-type silicon can be rewritten as

$$\sigma \cong qn\mu_n \tag{2.4}$$

Thus, the change of conductivity is proportional to the carrier mobility change

$$\frac{\Delta\rho}{\rho} = -\frac{\Delta\sigma}{\sigma} = -\frac{\Delta\mu}{\mu} \tag{2.5}$$

Neglecting resistance changes due to dimensional changes, Eq. (2.2) for a semiconductor simplifies to

$$\frac{\Delta R}{R} \cong -\frac{\Delta\mu}{\mu} \tag{2.6}$$

The physics of the piezoresistive effect in silicon has been well studied [47, 49, 61-68]. The mobility of the carriers is inversely proportional to their effective mass. The effective masses of the majority carriers in both n- and p-type silicon change under stress, but the basic mechanisms for n-type silicon and p-type silicon are different. For n-type silicon under stress, conducting electrons will be redistributed between energy valleys in different directions where the effective masses of carriers in different energy valleys are different from each other, with a resulting change in the overall mobility of the conducting electrons. For p-type silicon, the energy bands with different effective masses are aligned in the same direction when no stress is applied, but separate from each other under stress. This separation of the energy bands results in a redistribution of holes among the energy bands, which will change the average effective mass and, therefore, the overall mobility. Stress may enhance or degrade the performance of the transistors [69-71].

2.2 Si Piezoresistive Stress Sensors

2.2.1 Resistor Stress Sensor

An arbitrarily oriented silicon filamentary conductor is shown in Fig. 2-1. The unprimed axes $x_1 = [100]$, $x_2 = [010]$ and $x_3 = [001]$ are the principal crystallographic directions of the cubic silicon crystal.

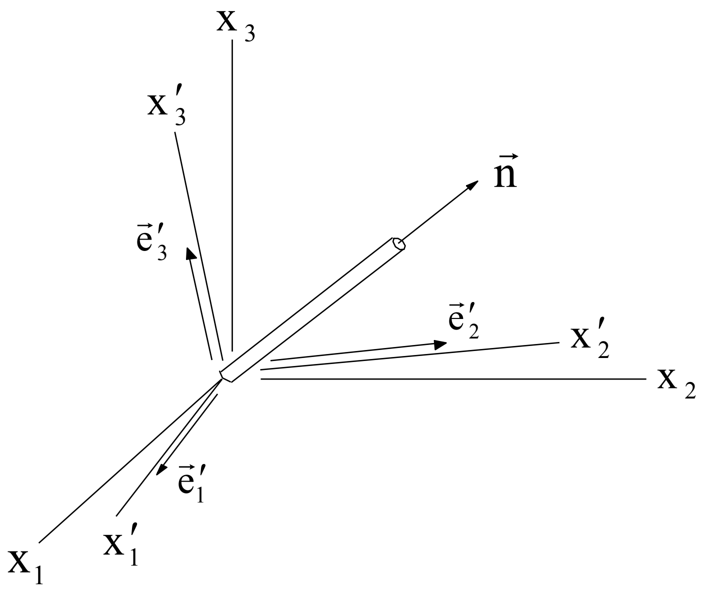


Fig. 2-1 Arbitrarily Oriented Filamentary Silicon Conductor

The primed coordinate system is arbitrarily rotated with respect to the unprimed system. For this conductor, the normalized change in resistance can be expressed in terms of the off-axis (primed) components using

$$\begin{aligned}\frac{\Delta R}{R} &= [\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})]l^2 + [\pi_{11}\sigma_{22} + \pi_{12}(\sigma_{11} + \sigma_{33})]m^2 \\ &\quad + [\pi_{11}\sigma_{33} + \pi_{12}(\sigma_{11} + \sigma_{22})]n^2 + 2\pi_{44}[\sigma_{12}lm + \sigma_{13}nl + \sigma_{23}mn \\ &\quad + [\alpha_1\Delta T + \alpha_2(\Delta T)^2 + \ldots]\end{aligned} \tag{2.7}$$

where *l*, *m*, *n* are the direction cosines of the conductor orientation with respect to the unprimed (crystallographic) axes, and $\pi_{11}, \pi_{12}, \pi_{44}$ are the three unique on-axis piezoresistive coefficients (evaluated in the unprimed coordinate system aligned with the crystallographic axes) [2, 25]. Therefore, the resistance change of an arbitrarily oriented silicon resistor depends on all six stress components, the three unique piezoresistive coefficients and the temperature.

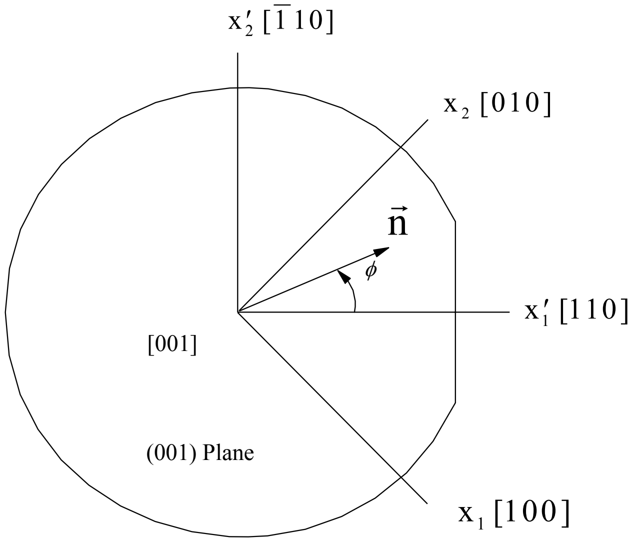


Fig. 2-2 Principal and Primed Coordinate System for (100) Silicon

For a (100) silicon wafer, the principal and primed coordinate systems are oriented as shown in Fig. 2-2. The surface of the wafer is a (001) plane, and the [001] direction is normal to the wafer plane. The primed coordinate system is rotated 45o from the principal crystallographic axes. The primed axes $x_1^{'} =$ [110] and $x_2^{'} = [\bar{1}10]$ are parallel and perpendicular, respectively, to the primary flat of the wafer.

Substitution of the off-axis piezoresistive coefficients calculated using the direction cosines yields

$$
\begin{aligned}
\frac{\Delta R}{R} &= [(\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma_{11}' + (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma_{22}']\cos^2\phi \\
&+[(\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma_{11}' + (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma_{22}']\sin^2\phi \\
&+\pi_{12}\sigma_{33}' + (\pi_{11}-\pi_{12})\sigma_{12}'\sin 2\phi \\
&+[\alpha_1\Delta T + \alpha_2(\Delta T)^2 + \cdots]
\end{aligned}
\tag{2.8}
$$

where $l' = \cos\phi, m' = \sin\phi$ and $n' = 0$ have been introduced, and ϕ is the angle between the x_1'-axis and the resistor orientation. The out-of-plane shear stresses σ_{13}' and σ_{23}' do not appear in Eq. (2.8), which indicates that a sensor rosette fabricated on (100) silicon can at best measure four of the six unique piezoresistive coefficients.

For a four-element rosette with elements oriented at $\phi = 0^o$, $\phi = 90^o$, $\phi = 45^o$ and $\phi = -45^o$, with a controlled application of in-plane stresses $\sigma_{11}', \sigma_{22}'$ and σ_{12}', the equation for each resistor can be simplified as

$$
\begin{aligned}
\frac{\Delta R_0}{R_0} &= (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma_{11}' + (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma_{22}' + \alpha_1\Delta T + \alpha_2\Delta T^2 + \cdots \\
\frac{\Delta R_{90}}{R_{90}} &= (\frac{\pi_{11}+\pi_{12}-\pi_{44}}{2})\sigma_{11}' + (\frac{\pi_{11}+\pi_{12}+\pi_{44}}{2})\sigma_{22}' + \alpha_1\Delta T + \alpha_2\Delta T^2 + \cdots \\
\frac{\Delta R_{45}}{R_{45}} &= (\frac{\pi_{11}+\pi_{12}}{2})(\sigma_{11}' + \sigma_{22}') + (\pi_{11}-\pi_{12})\sigma_{12}' + \alpha_1\Delta T + \alpha_2\Delta T^2 + \cdots \\
\frac{\Delta R_{-45}}{R_{-45}} &= (\frac{\pi_{11}+\pi_{12}}{2})(\sigma_{11}' + \sigma_{22}') - (\pi_{11}-\pi_{12})\sigma_{12}' + \alpha_1\Delta T + \alpha_2\Delta T^2 + \cdots
\end{aligned}
\tag{2.9}
$$

2.2.2 Other Types of Stress Sensors

The relatively large size of resistor sensors means that these sensors can provide measurements of only the average stress over the large sensor area, and their stress sensitivity is also limited by the high doping concentrations required [63, 64]. The large junction area of resistor sensors tends to cause large leakage currents and thus limit their application to temperatures below 100°C~125ºC. In addition, it is difficult to multiplex these sensors to form a high-density sensor array. Successful application of the sensors also requires temperature compensated coefficient calibration and stress component measurements. As a result of these limitations, other basic types of stress sensors have been developed based on the same piezoresistive effect as resistor sensors.

2.2.2.1 Van der Pauw Structure Stress Sensors

The Van der Pauw (VDP) method is a widely used approach to measuring the sheet resistance of thin layer materials [72-75]. For silicon, the sheet resistance is stress sensitive, so VDP structures can also be used as stress sensors [51, 76]. The basic VDP structure requires only one square of material, and its characteristics are size independent. As a result, the VDP structure stress sensors can be made small enough to detect stress variation over a very small area without loss of sensitivity [51]. In order to minimize measurement errors, the VDP structures need to be fabricated with high sheet resistance, and the effect of contacts to the square should be minimized [77].

2.2.2.2 MOSFET Stress Sensors

When a MOSFET is biased in the saturation region its drain current is inversely proportion to its channel resistance, so a MOSFET can be treated as a resistor that is controlled by its gate voltage. The channel resistance at fixed gate bias is sensitive to applied stress [78], so a FET type stress sensor has been developed. Due to the small size of the channel region, sensors based on FETs are expected to yield a better estimate of localized stresses. Also, sensors based on FET are likely to be far more sensitive to stress than the resistor sensors due to the light-doping characteristic of the channel region. The piezoresistive MOSFET will be examined in more detail later in this chapter.

2.2.2.3 Inversion Layer van der Pauw Stress Sensors (ILVDP)

The idea for this type of sensor came from the combination of the best feathers of VDP and MOSFET stress sensors. The sensitivity of a VDP stress sensor is limited by its doping concentration, and the MOSFET type has light-doping properties in the channel when it is properly biased. By using a gate to generate an inversion layer in silicon and then using VDP method to characterize the resistivity response to mechanical stress, an inversion layer Van der Pauw (ILVDP) stress sensors was developed [44].

2.2.2.4 Piezojunction Stress Sensors

Mechanical stress has a pronounced influence on the saturation current of bipolar transistors, which is known as the piezojunction effect. For a first order approximation, this can be explained as the carrier redistribution between energy bands when those energy bands with different effective masses are separated due to the applied stresses [47, 79]. This causes the average mobility change, and hence the saturation current of the pn junction, to change with the applied stress, which is physically the same as piezoresistive effect. This effect has also been used to construct stress sensors [48, 49, 79, 80]. Research has shown that this type of sensor can reduce power consumption compared to sensors based on the piezoresistive effect [50].

2.2.2.5 Four-terminal Stress Sensors (X-Ducers)

Kanda found that the offset voltage of a Hall-effect device is very sensitive to mechanical strain without the application of a magnetic field. This effect is called the Kanda effect [53, 63]. Based on this effect, a four-terminal stress sensor has been developed [10-13, 56, 57, 81-84]. This four-terminal structure stress sensor, known as ‘xducer’, is similar to a VDP stress sensor. The current is applied by the two diagonal ports and the outputs are taken from the other two ports. It has been shown that the sensitivities of the xducer are approximately equal to those of a Wheatstone bridge circuit [52] and can be expressed in terms of the piezoresistive coefficients.

Recently, 4x4 arrays of PMOS stress sensors were used for wire-bonding characterization in [45, 58], where the sensor used is actually an inversion layer four-terminal ‘xducer’. The active layer in the sensor is an inversion layer under the gate oxide of an MOS structure, and four terminals are designed to form an output voltage based on the Kanda effect.

2.3 Piezoresistive MOSFET

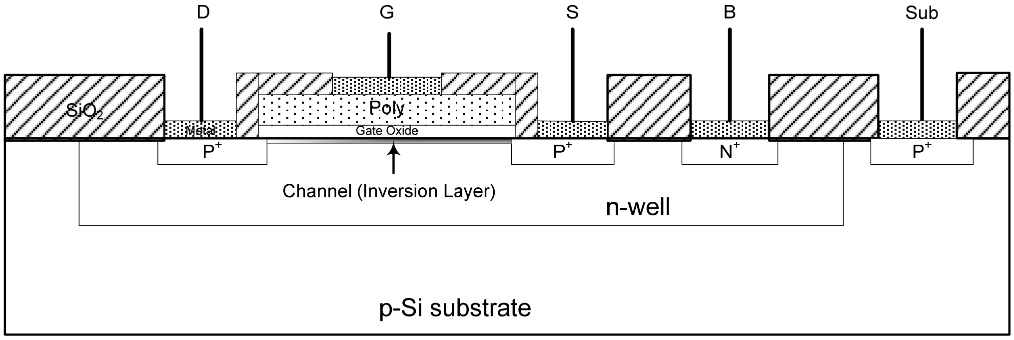


Fig. 2-3 Cross-section of a p-channel Enhancement-type MOSFET

2.3.1 MOSFET Characteristics

A typical p-channel enhancement-type MOSFET fabricated by n-well CMOS process is shown in Fig. 2-3. A gate terminal is separated by a high quality thin insulator from the silicon, and the potential on the gate terminal controls the surface potential of the silicon and the conducting status of the device channel. The structure is symmetrical, and the source and drain terminals are determined by their relative potentials and from which terminal the carrier comes from. For this p-MOS transistor, the source is the relative high potential terminal where carriers, or holes, come from, and the carriers then go to the other terminal, which is called the drain. Normally the p-type substrate is connected to the low potential and the n-well is connected to the high potential, or source, of the MOSFET. If no channel is formed, the p^+ diffusion regions, drain and source of the MOSFET are isolated by the n region and no current will flow between the drain and source except for a small little leakage current through the reverse-biased $p^+ - n$ junction. The MOSFET is "TURNED OFF". When the potential applied to the gate is lower than the threshold of the MOSFET, V_T, a p channel will be formed between the source and drain under the gate, and a current may flow if there is a potential difference between the drain and source. In this case, the

MOSFET is “TURNED ON”, and the current flowing from source to drain is primarily determined by the gate voltage applied. A graph showing typical output characteristics is shown in Fig. 2-4.

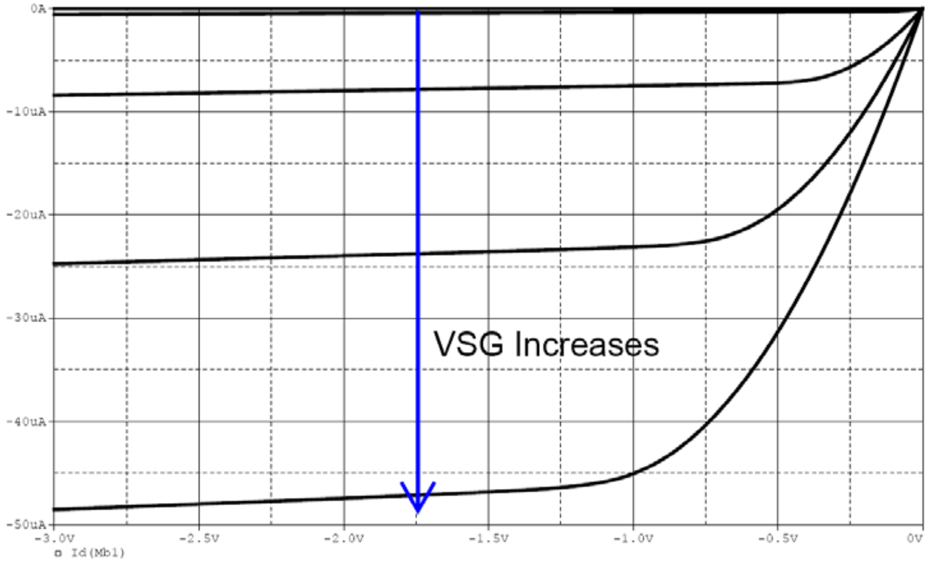


Fig. 2-4 A Typical Output Characteristics of a p-channel Enhancement-type MOSFET

2.3.2 MOSFET Mismatches

Mismatches represent random variations in physical properties among identically designed devices. The importance of matching is widely recognized in circuit design, especially in analog circuit design, as the performance of analog circuits is usually dependent on the ratio of the components [85-104]. Mismatches in the elements of CMOS integrated circuits can be categorized into global variations and local variations. Global variations are long distance correlated variations which characterize the variations of identically designed devices on different sites of the wafer and devices fabricated in different batches, and may include inherently uneven doping distributions on the wafer, non uniform defect density distributions on the wafer, and process parameter variations between different wafers in the same batch and wafers in different batches. Local variations are short distance correlated variations that account for variations in a component value with reference to an adjacent component on the same chip. This variation is a random error that differs from element to element. The mismatches considered here are primarily local variations.

The physical sources of mismatches may include edge effects, implantation and surface-state charges, oxide effects and mobility effects [105]. The local edge variation is usually caused by the granular nature of the gate edge, which may arise due to either the jagged edge of the developed photoresist, or the random nature of the etching process. The ion implantation that is used to adjust the threshold voltage in a typical MOS process causes randomly distributed charges in the channel and therefore some inherent surface-state charge exists at and inside the interface of the silicon and oxide [106]. The oxide variations may be caused by the granularity of the polysilicon, surface defects of crystal silicon, etc. The uncertainty of both oxide thickness and permittivity will cause random errors in an MOS capacitor. The effective channel carrier mobility varies randomly due to impurities and also because of the lattice scattering and piezoresistive effect. Mismatch models of MOSFET and mismatch parameter extraction have been developed for use in optimizing the circuit design [3, 86, 101, 102, 107-127].

The mobility mismatch due to mechanical stress is the parameter that stress sensors are designed to detect. Therefore all other mismatches need to be kept as small as possible except the stress induced mobility mismatch for the piezoresistive stress sensor design.

For convenience, a MOSFET conduction factor is defined as

$$K = \frac{\mu_p C_{ox}^{'} W}{L} \tag{2.10}$$

where $C_{ox}^{'}$ is the gate capacitance per unit area, μ_p is the carrier mobility in the channel, and W and L are the channel width and channel length, respectively. The drain to source current of a PMOS transistor in the saturation region can be written as

$$I_D = \frac{K}{2}(V_G - V_T)^2 \tag{2.11}$$

where V_T is the threshold voltage. The normalized drain current change can be expressed as

$$\frac{\Delta I_D}{I_D} = \frac{\Delta K}{K} - 2\frac{\Delta V_T}{(V_G - V_T)} \tag{2.12}$$

Eq. (2.12) implies that the threshold voltage mismatch, ΔV_T, will dominate if the MOSFET is biased at a low overdrive voltage $(V_G - V_T)$, and while it is biased at a high overdrive voltage $(V_G - V_T)$ the conduction factor mismatch, ΔK, will dominate. The main source of ΔK is the mobility mismatch caused by the stress applied, which is the mismatch to be detected by the sensors developed for this study. Therefore, the MOSFET stress sensor should be biased at a high overdrive condition ensuring that the effects from threshold change are negligible.

2.3.3 Piezoresistive Theory of MOSFET

The piezoresistive theory of MOSFET was first developed by Mikoshiba in 1981 [78], and the results predicted by the theory were then confirmed experimentally [78, 128]. The theory for a p-channel device can be briefly described as follows.

When a p-channel MOSFET is biased in the linear region with $0 \leq |V_{DS}| \leq |V_{GS} - V_T|$, no pinch-off occurs and the drain current can be expressed as

$$I_D \cong \frac{\mu_p W}{L} Q_C V_{SD} \tag{2.13}$$

where the channel carrier charge per unit area Q_C is defined as

$$Q_C = C_{OX} \left(V_{GS} - V_T\right) \tag{2.14}$$

The drain current change due to applying a mechanical stress may be observed in order to utilize it as a stress sensor. Assuming a uniaxial stress σ is applied along the drain current direction, the relative drain current change due to the stress can be expressed as

$$\frac{1}{\sigma}\left(\frac{\Delta I_D}{I_D}\right) = \frac{1}{\sigma}\left(\frac{\Delta W}{W}\right) - \frac{1}{\sigma}\left(\frac{\Delta L}{L}\right) + \frac{1}{\sigma}\left(\frac{\Delta \mu}{\mu}\right) + \frac{1}{\sigma}\left(\frac{\Delta Q_C}{Q_C}\right) \tag{2.15}$$

In silicon, the piezoresistive coefficients that characterize the stress induced changes in carrier mobility are typically an order or two larger in magnitude than the coefficients that quantify the stress induced by dimensional changes. Thus, discarding the terms in Eq. (2.15) that involve dimensional changes, the relationship can be simplified as

$$\frac{1}{\sigma}(\frac{\Delta I_D}{I_D}) \cong \frac{1}{\sigma}(\frac{\Delta \mu}{\mu}) + \frac{1}{\sigma}(\frac{\Delta Q_C}{Q_C}) \tag{2.16}$$

Assuming there are no stress-induced changes in the oxide capacitance and gate-semiconductor work function difference, the stress dependence of the mobile charge density in the channel is described by the following relationship [78]

$$\begin{aligned} \frac{\Delta Q_C}{Q_C} = \left(\frac{\Delta p_n}{p_{n0}}\right)\left(M\sqrt{-U_{S0}}+1\right)\left(\frac{\gamma}{-2U_{S0}}\right)\left(\sqrt{\left(1+\frac{\gamma}{-U_{S0}}\right)}-1\right)^{-1} \\ \cdot\left(M\sqrt{-U_{S0}}\sqrt{\left(1+\frac{\gamma}{-U_{S0}}\right)}+\left(1+\gamma\right)\right)^{-1} \end{aligned} \tag{2.17}$$

where $U_{S0} = \phi_s / V_t$ is the unstressed electrostatic potential at the semiconductor surface normalized to $V_t \equiv \frac{kT}{q}$, which is usually referred to as the normalized surface potential. p_n is the minority carrier density in the bulk. The parameters in Eq. (2.17) are defined as

$$M \equiv \frac{C_{OX}}{q}\sqrt{\frac{2kT}{\varepsilon_{Si} N_D}} \qquad \text{and} \qquad \gamma \equiv \left(\frac{p_{n0}}{N_D}\right) e^{-U_{S0}} \tag{2.18}$$

Note that p_{n0} and U_{S0} are both functions of applied stress.

If the normalized electrostatic potential at the semiconductor surface is used as a parameter and the source of the p-FET is connected to ground, the working region of the device can be defined as follows:

$$\begin{aligned} &\text{Strong inversion:} && U_S < -2U_F - 6 \\ &\text{Moderate inversion:} && -2U_F - 6 < U_S < -2U_F \\ &\text{Weak inversion:} && -2U_F < U_S < -U_F \end{aligned} \tag{2.19}$$

where $U_F = \phi_F / V_t = \ln(\frac{N_D}{n_i}) < 0$ and $U_S < 0$.

2.3.3.1 Piezoresistive FET in Strong Inversion

Substituting the data from Table 2-1 and $U_{S0} = -2\ln(\frac{N_D}{n_i}) - 6$ into Eq. (2.18) and Eq. (2.17) yields

$$\begin{aligned} &\gamma = 403 \\ &M = 0.59 \\ &\frac{\Delta Q_C}{Q_{C0}} = 0.049\left(\frac{\Delta p_n}{p_{n0}}\right) \end{aligned} \tag{2.20}$$

Table 2-1 Typical Parameters for p-FET at T = 293 K

Gate Oxide Thickness	314	$\overset{o}{A}$
Substrate Doping	1×10^{16}	cm^{-3}
Intrinsic Carrier Density	1×10^{10}	cm^{-3}

For unstressed silicon, assuming complete ionization, the relationship $p_{n0}N_D = n_i^2 = Ce^{-\frac{E_{go}}{kT}}$ holds and N_D is the doping concentration, which is independent of stress. However, when the energy band gap changes with stress, the minority concentration in the silicon changes

$$\frac{p_{n0} + \Delta p_{n0}}{p_{n0}} = e^{-\frac{\Delta E_g}{kT}} \tag{2.21}$$

If $\Delta E_g \ll kT$, the above equation can be approximated as

$$\frac{\Delta p_{n0}}{p_{n0}} = -\frac{\Delta E_g}{kT} \tag{2.22}$$

The pressure coefficient of the band gap of silicon is very low. The value of the stress response of the carrier concentration in the pFET channel was estimated to be

$\frac{1}{\sigma}(\frac{\Delta Q_c}{Q_{c0}}) \cong -30\times10^{-12} Pa^{-1}$, which is much lower than the stress induced mobility change [128].

Thus, neglecting the carrier density change due to stress, the drain current change of the FET in the strong inversion region can be written as

$$\frac{1}{\sigma}(\frac{\Delta I_D}{I_D}) \cong \frac{1}{\sigma}(\frac{\Delta \mu}{\mu}) \qquad (2.23)$$

2.3.3.2 Piezoresistive FET in Moderate Inversion

In the moderate inversion region $U_{S0} = -2\ln(\frac{N_D}{n_i})$, so the estimated values in Eqs. (2.18) and (2.17) are

$$\begin{aligned} &\gamma = 1 \\ &M = 0.59 \\ &\frac{\Delta Q_C}{Q_{C0}} = 1.61\left(\frac{\Delta p_n}{p_{n0}}\right) \end{aligned} \qquad (2.24)$$

Under this condition the carrier concentration change in the channel is about 30 times higher than that in the strong inversion region and cannot be neglected. Here, Eq. (2.16) is required to obtain the drain current change due to an applied stress.

Based on the previous discussion, biasing MOSFETs in the strong inversion region is likely to be a good choice for a stress sensor.

2.4 CMOS Stress Sensor Cell

As the piezoresistive coefficient for silicon is anisotropic, in order to create stress sensors with a high sensitivity, the choice of orientation and doping type is crucial. Due to the high piezoresistive coefficient value of π_{44}^p and $\pi_{11}^n - \pi_{12}^n$, p-channel MOSFETs should be chosen for normal stress difference sensors, and n-channel MOSFETs should be chosen for the shear stress sensors [40]. The piezoresistive coefficients of the MOSFETs are then represented by $\Pi's$ instead of $\pi's$, as the piezoresistive coefficient in MOSFETs may include other effects such as threshold and channel charge variations due to stress.

2.4.1 Piezoresistive Equations for Piezo-MOSFET

Combining Eqs. (2.6), (2.8) and (2.23), the normalized change in the drain currents of the MOSFETs on (100) silicon due to stress may be written as

$$\begin{aligned}\frac{\Delta I_D}{I_D} = &-[(\frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2})\sigma'_{11} + (\frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2})\sigma'_{22}]\cos^2\phi \\ &-[(\frac{\Pi_{11}+\Pi_{12}-\Pi_{44}}{2})\sigma'_{11} + (\frac{\Pi_{11}+\Pi_{12}+\Pi_{44}}{2})\sigma'_{22}]\sin^2\phi \\ &-\Pi_{12}\sigma'_{33} - (\Pi_{11}-\Pi_{12})\sigma'_{12}\sin 2\phi \\ &-[\alpha_1\Delta T + \alpha_2(\Delta T)^2 + \cdots]\end{aligned} \tag{2.25}$$

2.4.1.1 Two-element MOSFET Rosette for Normal Stress Difference

For a two-element sensor rosette with 0^o and 90^o orientated MOSFETs as shown in Fig. 2-5, under the same V_{SG} and V_{SD}, the corresponding normalized current change for each transistor can be written as

$$\begin{aligned}\frac{\Delta I_0}{I_0} &= -(\frac{\Pi^p_{11}+\Pi^p_{12}+\Pi^p_{44}}{2})\sigma'_{11} - (\frac{\Pi^p_{11}+\Pi^p_{12}-\Pi^p_{44}}{2})\sigma'_{22} - \alpha_1{}^p\Delta T - \alpha_2{}^p\Delta T^2 \\ \frac{\Delta I_{90}}{I_{90}} &= -(\frac{\Pi^p_{11}+\Pi^p_{12}-\Pi^p_{44}}{2})\sigma'_{11} - (\frac{\Pi^p_{11}+\Pi^p_{12}+\Pi^p_{44}}{2})\sigma'_{22} - \alpha_1{}^p\Delta T - \alpha_2{}^p\Delta T^2\end{aligned} \tag{2.26}$$

Taking the difference to these two equations gives,

$$\frac{\Delta I_{90}}{I_{90}} - \frac{\Delta I_0}{I_0} = \Pi^p_{44}(\sigma'_{11} - \sigma'_{22}) \tag{2.27}$$

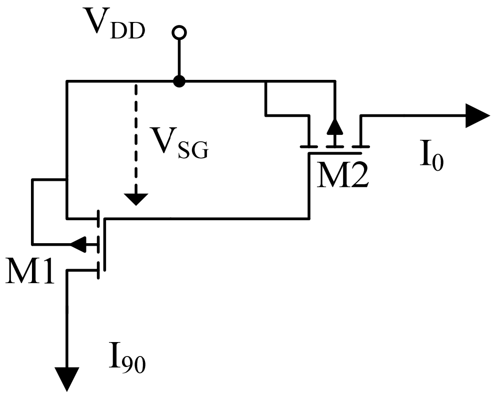


Fig. 2-5 Two-element MOSFET Rosette for Normal Stress Difference

There is no explicit temperature term in this equation, so this measurement is temperature compensated. The weak temperature dependence of the piezoresistive coefficients can be neglected without introducing significant error.

2.4.1.2 Two-element MOSFET Rosette for Shear Stress

A two-element rosette with 45^o and -45^o oriented MOSFET transistors is shown in Fig. 2-6. When two transistors are biased at the same V_{GS} and V_{DS} voltages, the drain to source currents for the two transistors can be expressed as

$$\begin{aligned}\frac{\Delta I_{45}}{I_{45}} &= -\left(\frac{\Pi_{11}^n + \Pi_{12}^n}{2}\right)(\sigma_{11}^{'} + \sigma_{22}^{'}) - (\Pi_{11}^n - \Pi_{12}^n)\sigma_{12}^{'} - \alpha_1^n \Delta T - \alpha_2^n \Delta T^2 \\ \frac{\Delta I_{-45}}{I_{-45}} &= -\left(\frac{\Pi_{11}^n + \Pi_{12}^n}{2}\right)(\sigma_{11}^{'} + \sigma_{22}^{'}) + (\Pi_{11}^n - \Pi_{12}^n)\sigma_{12}^{'} - \alpha_1^n \Delta T - \alpha_2^n \Delta T^2\end{aligned} \tag{2.28}$$

Taking the difference of the two equations in Eq. (2.28) gives

$$\left(\frac{\Delta I_{45}}{I_{45}} - \frac{\Delta I_{-45}}{I_{-45}}\right) = -2(\Pi_{11}^n - \Pi_{12}^n)\sigma_{12}^{'} \tag{2.29}$$

This rosette is temperature compensated as well.

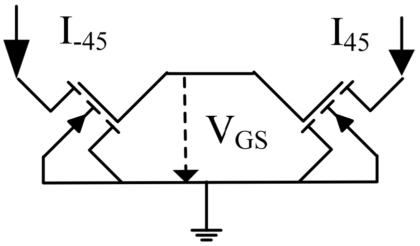


Fig. 2-6 Two-element MOSFET Rosette for Shear Stress

2.4.2 Piezoresistive Equations for PMOS Cell

A normal current mirror is shown in Fig. 2-7. In a normal circuit design both transistors are placed close to each other and oriented in the same direction in order to minimize any mismatch that may be induced by process variations, temperature variation, stress variation and other variations over the surface of the chip. For the sensor application considered here, the mobility change induced by stress is the effect to be detected, and other mismatches should be minimized at all times. Fig. 2-8 illustrates a stress sensitive MOSFET current mirror. The only difference here is that the two transistors are oriented orthogonally.

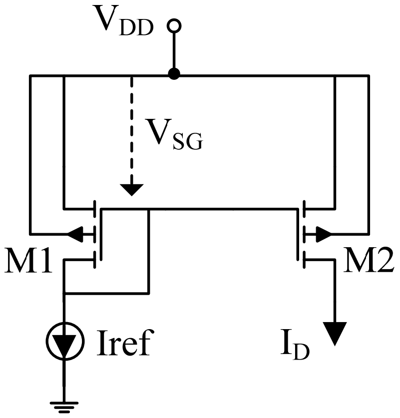


Fig. 2-7 Normal PMOS Current Mirror

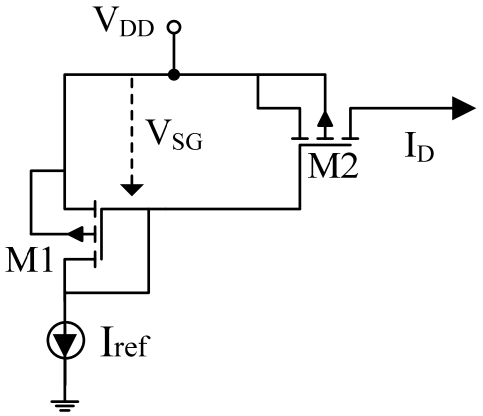


Fig. 2-8 Normal Stress Difference Sensitive Current Mirror

Assuming the transistors are both working in the saturation region, the drain current of M1, I_{D1}, is provided by the reference current

$$I_{ref} = I_{D1} = \frac{\mu_1 C_{ox}'}{2}(\frac{W_1}{L_1})(V_{GS} - V_T)^2 \tag{2.30}$$

The two transistors share the gate source voltage, so the output current is approximately determined by the width over length ratio of the two transistors, the gate capacitance and the mobility, as follows

$$I_D = \frac{\mu_2 C_{ox}'(W/L)_2}{\mu_1 C_{ox}'(W/L)_1} I_{ref} = \frac{\mu_2 (W/L)_2}{\mu_1 (W/L)_1} I_{ref} \tag{2.31}$$

If the two MOSFETs are of the same size and there are no mobility mismatches between the two transistors, then $\mu_1 = \mu_2$, and the output current of the current mirror will be equal to the reference current.

However, when a stress is applied to the current mirror with two transistors oriented differently, it may cause a change in the carrier mobility and the output current will no longer equal to the reference current. As described in Eq. (2.23), the effect of a dimension change or the gate oxide change due to stress is much smaller than the change in mobility due to the stress, so the relative change of the current mirror output current due to stress may be approximated as

$$\frac{\Delta I_D}{I_{ref}} \cong \frac{\Delta \mu_2}{\mu_2} - \frac{\Delta \mu_1}{\mu_1} \tag{2.32}$$

The relationship between the resistivity change and the stress applied, given in Eq.(2.8)and Eq.(2.9), describes the resistivity change for 0^o and 90^o oriented two-element rosettes under a uniaxial stress. In the current mirror shown in Fig. 2-8, M1 is oriented at 90^o and M2 is oriented at 0^o. Combining Eqs. (2.6), (2.8) and (2.32), the in-plane normal stress difference can be determined by the relative change in the output current of the orthogonal current mirror as

$$(\sigma_{11}^{'} - \sigma_{22}^{'}) = \frac{1}{\Pi_{44}^{p}} \frac{\Delta I_D}{I_{ref}} \tag{2.33}$$

Notice that neither $\sigma_{33}^{'}$ nor shear stress are involved here, which means that the current mismatch in the current mirror is independent of both the out-of-plane stress and the shear stress. This stress sensor can thus sense only the difference between two normal stresses, or an applied uniaxial normal stress, and no out-of-plane stress or shear stress can be detected by this sensor. Also, Eq. (2.33) shows that this sensor rosette is temperature compensated.

If a uniaxial stress $\sigma_{11}^{'} = \sigma$ is applied to the current mirror rosette, Eq. (2.33) can be simplified as

$$\sigma = \frac{1}{\Pi_{44}^{p}} \frac{\Delta I_D}{I_{ref}} \tag{2.34}$$

Eqs. (2.33) and (2.34) indicate that there is a simple relationship between current mismatch and applied stress, and the only piezoresistive coefficient involved here is Π_{44}^{p}. The stress value can thus be determined by measuring the current mismatch in an orthogonal current mirror, which in this case is the PMOS sensor cell.

2.4.3 Piezoresistive Equations for NMOS Cell

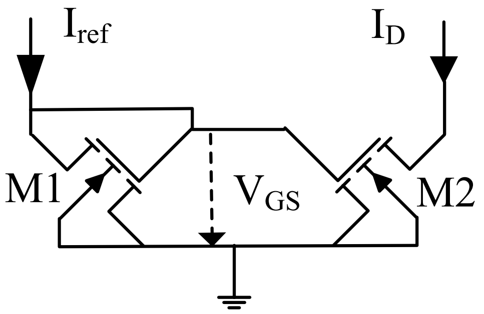


Fig. 2-9 Shear Stress Sensitive Current Mirror

For the current mirror in Fig. 2-9, the relationship between the two drain-to-source currents can similarly be written as Eq. (2.32). Applying Eqs. (2.9) and (2.6) with Eq. (2.32) yields

$$\sigma'_{12} = \frac{1}{-2(\Pi^n_{11} - \Pi^n_{12})}\left(\frac{\Delta I_D}{I_{ref}}\right) \tag{2.35}$$

Eq. (2.35) shows how to determine the in-plane shear stress by measuring the drain current change, using a NMOS sensor cell, and this is again temperature compensated. The only piezoresistive coefficient involved is $(\Pi^n_{11} - \Pi^n_{12})$ or Π^n_D.

CHAPTER 3. DELTA-SIGMA MODULATION STRESS SENSOR

A novel CMOS Delta-Sigma Modulator (DSM) based stress sensor circuit was designed as part of the work. In this sensor, the current mismatch due to stress is detected using a delta-sigma modulator. The system is temperature compensated and provides an RF output that can be sensed without direct connection or can be averaged by digital counter. A one-bit quantizer used in the design is a clocked comparator. A combination of metal-metal and poly-metal capacitors is used to obtain high capacitance and low noise coupling for the integrator. The output is taken from the comparator output through buffers in order to provide high drive capability to interface to the outside load.

3.1 Current Mismatch Detection Schematic

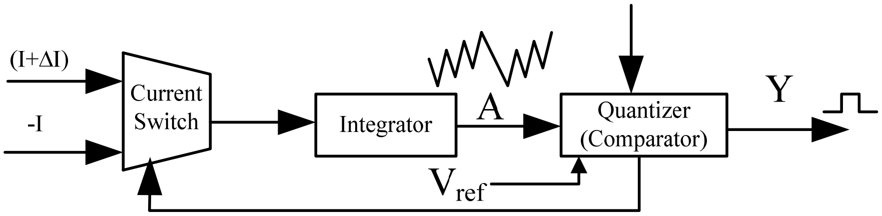


Fig. 3-1 Current Mismatch Detection Schematic

Fig. 3-1 shows the current mismatch detect schematic used in this design. The current switch is controlled by the quantizer output signal, which selects one of the two inputs to pass as the output. The 1-bit quantizer, which is simply a clocked comparator, is designed so that when the input voltage is higher than a reference voltage the output is in one state and the output changes to the other state when the input drops below the reference voltage. The comparator is controlled by a clock signal, so the comparison only occurs during one phase of the clock cycle.

Assuming $\Delta I = 0$, the initial charge stored in the integrator is zero, and the circuit starts in the state of accumulating current I, where the state with current I lasts for a period of time t. When the clock 'compare' phase arrives, the comparator judges the output based on the condition of the input voltage. The output toggles after the integrator has accumulated a charge of $I \bullet t$, which switches the current switch output to $-I$ and maintains this state for a further period of t, during which the integrator accumulates a charge of $-I \bullet t$. Therefore the net charge accumulated in the integrator during the complete cycle period of $2t$ is zero. The process repeats continuously. The output of the comparator is thus a square wave with a period of $2t$.

If $\Delta I > 0$, the circuit works in the same way as before, but here the integrator will accumulate the input current $I + \Delta I$ for a period of time t and then switch the current switch control signal to select $-I$ for a further period of time t, so that during the cycle period of $2t$ the net current accumulated in the integrator is $\Delta I \bullet t$. The net charge remaining in the integrator thus accumulates as the process repeats. After a certain number of periods, $2n \bullet t$, the charge accumulated in the integrator elevates the integrator output voltage at node A so that after an operation of integrating $-I$ in a period of t, the voltage at A remains high enough to preserve the state of the quantizer unchanged. Now the control signal will not switch to $I + \Delta I$, so the integrator will continue to accumulate $-I$ for one more time period of t, after which the net charge in the integrator has decreased to $n\Delta I - I$ at the time point $(2n+1)t$. Assuming $n\Delta I - I \cong 0$, the mismatch can be determined approximately by

$$\frac{\Delta I}{I} = \frac{1}{n} \tag{3.1}$$

If $n\Delta I - I = \Delta I' \neq 0$ after the time period of $(2n+1)t$, the accumulating process will continue to augment the residual charge, $\Delta I' = n\Delta I - I$, and the residual charge will increase by

$\Delta I'$ for every period of $(2n+1)t$. After a time $m\bullet[(2n+1)t]$, the residual current has accumulated to the amount of ΔI and the continuous $-I$ phase will now arrive $2t$ ahead of the 'normal' period of $[(2n+1)t]$. In other words, the continuous $-I$ phase will now occur at time $m\bullet[(2n+1)t]-t$ instead of at time $m\bullet[(2n+1)t]$. Assuming that the accumulated charge in the integrator is discharged to zero after the last continuous $-I$ phase, $m\bullet[n\Delta I - I] = \Delta I$, the current mismatch can be estimated by

$$\frac{\Delta I}{I} = \frac{m}{mn-1} \tag{3.2}$$

The components shown in Fig. 3-1 are all digital components, with a larger noise tolerance, so the small shift in the transistor properties of these parts will not influence the precision of the sensor.

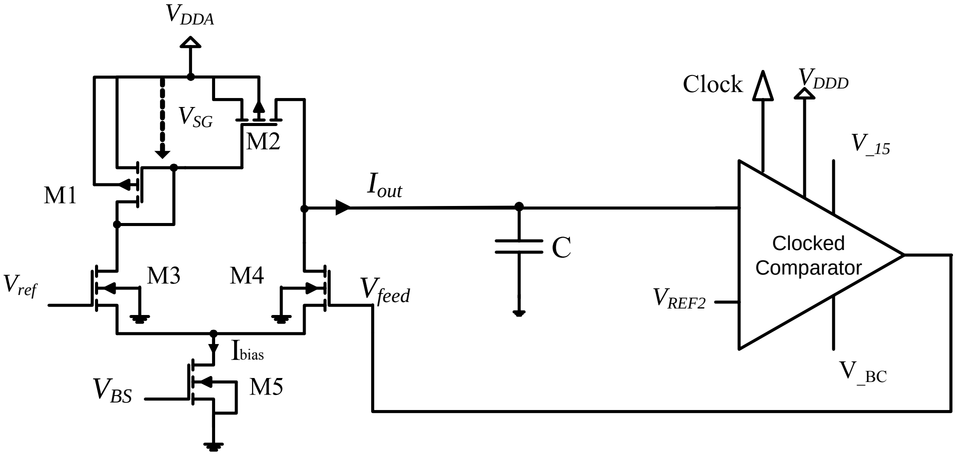


Fig. 3-2 Simplified Schematic of the Circuit

A simplified schematic of the whole circuit, including the sensor, is shown in Fig. 3-2. In this circuit, transistors M1 and M2 are configured as a current mirror type stress sensor cell. Transistor M5 is used to generate the bias current I_{bias}, and the absolute value of I_{bias} is not critical for this circuit providing the current is much larger than any leakage current and the voltage on the capacitor maintain M2 in pinch off. Other than these three transistors, all circuits are working in switching mode, either in the ON or OFF state.

3.2 Stress Sensor and Switch Pair

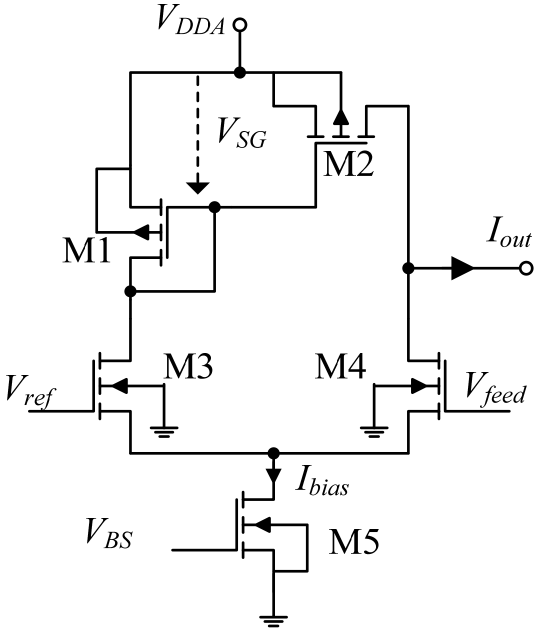


Fig. 3-3 Schematic of Stress Sensor and Switch Pair

The stress sensitive orthogonal current mirror and the differential switch pair are shown in Fig. 3-3. The switch pair acts as the current switch, which is controlled by the feedback signal from the quantizer. In order to eliminate the current mismatch induced by differences in the bias voltage V_{DS} , the voltage at the current output node, which is the drain at M2, must be equal to the voltage at the drain at M1. However, it is impossible to maintain this condition while the circuit is in operation because any current that is injected to the following integrator will change the voltage. Thus, the integrator needs to be designed so that the voltage change at the M2 drain terminal is reasonably small, which requires a fairly large capacitor. The effective current will be the average current over the complete charging and discharging period, rather than the ideal current with one constant value.

The differential pair composed of M3 and M4 works as a switch. When $V_{feed} > V_{ref}$, M4 is turned on and all the bias current I_{bias} goes through M4, so the current flowing through M3 can be neglected and M3 is turned off. When $V_{feed} < V_{ref}$, M3 is turned on and all the bias current flows through M3 so M4 is turned off and no current flows through M4. The current through M3 also flows through M1, which is 'mirrored' by M2. Assuming there is no mismatch between the two transistors which form the current mirror, the output current $I_{out} = I_{bias}$ when M4 is turned off and the entire bias current goes through M3 and is mirrored by M2. When M3 is turned off and M4 is turned on, all the bias current goes through M4 and zero current flows through M3, which is mirrored by the zero current in M2, and the output current $I_{out} = -I_{bias}$. As mentioned earlier, the voltage at the current output node changes when the circuit is working. This fluctuation in the signal may feed through the transistor and thus disturb the bias point, further reducing the circuit performance. Because both of the transistors in the current mirror are biased in the saturation region, the feedback from the drain to the source is very weak and can be neglected. However, for transistor M4 the feedback may cause problems due to the bias point is not designed carefully. If the V_{feed} is in full scale from zero to V_{DD}, when M4 is in the ON mode the transistor is biased in the linear mode, and the drain and the source of the transistor are connected by a low resistive path by the channel resistance. The voltage change at the drain will then feed through the path to the source, so the V_{DS} of the bias transistor M5 will follow the M4 drain voltage. As a result, the bias current will change as the integrator voltage changes and thus extra errors maybe introduced. Fortunately, this problem can be solved by reducing the voltage amplitude of the feedback signal V_{feed}. In order to ensure transistor M4 works in the saturation region, the bias voltage requires $V_{DS4} > V_{GS4} - V_{TN}$ or $V_{GS4} < V_{DS4} + V_{TN} = V_{DS3} + V_{TN}$, which limits the amplitude of the feedback signal. V_{feed} is limited to a value of between zero and half V_{DD} in this design in order to eliminate this error.

3.3 Clocked Comparator

The comparator here requires that the comparison takes place when the clock is high and a steady state is maintained when the clock is low [129], so only one clock is needed in the circuit used here. The diagram is shown in Fig. 3-4.

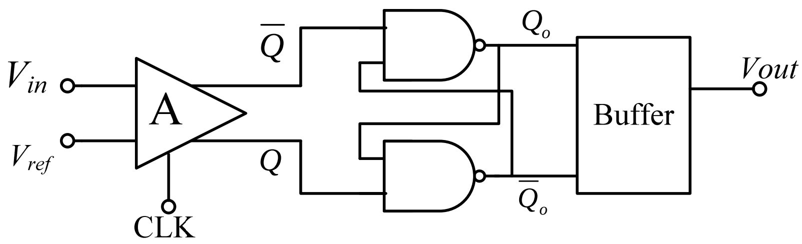


Fig. 3-4 Clocked Comparator Block Diagram

3.3.1 Clocked Amplifier

The basic characteristics of the clocked amplifier, shown in Fig. 3-5, ensure that the input signal is amplified only when the clock signal is high and the output is high when the clock is low. The output of the amplifier is double ended and the amplitude is rail to rail. As a result, a small input signal can be sensed and amplified to close to the full scale of the power supply. The components that process these complementary signals are laid out to minimize stress induced mismatch effects.

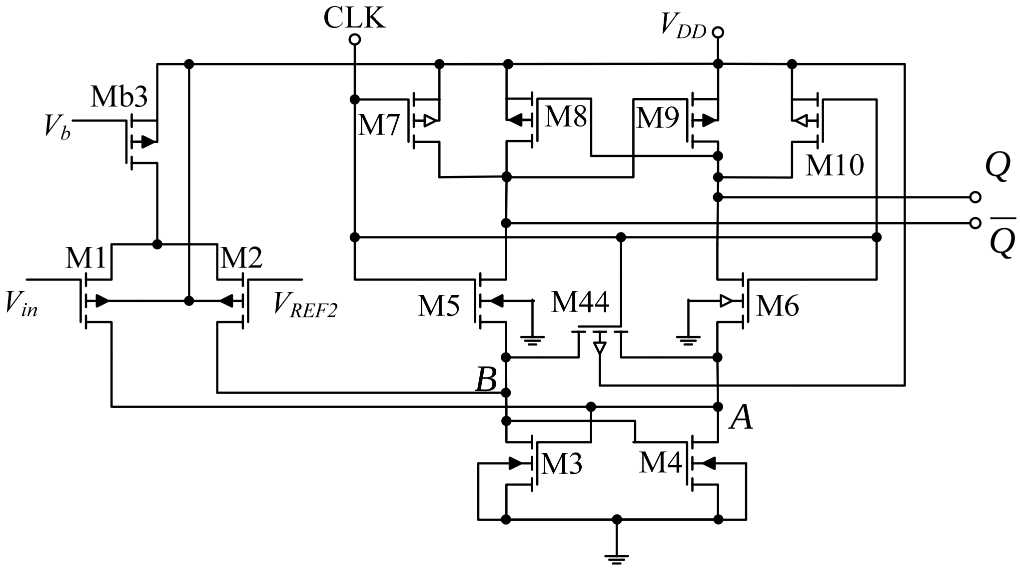


Fig. 3-5 Schematic of the Clocked Amplifier

The amplifier is composed of two stages. The first stage is a differential pair formed by M1 and M2, with Mb3 acting as a current source. The second stage is formed by a cross coupled inverter, M3, M4, M8 and M9, with decoupled transistors M5 and M6. Transistors M7 and M10 are used to force both outputs to high, while M44 is used to force the voltage at nodes A and B to equal to each other. The cross coupled pair of M3 and M4 are set to an unstable state when the clock signal is low. The whole structure is symmetrical, so the members of each pair M1 and M2, M3 and M4, M5 and M6, M8 and M9, M7 and M10 are identical to each other.

The analysis of the clocked amplifier operates in two states, resetting state and the amplifying state. The resetting state describes the circuit operation when the CLK is low, and the amplifying state analyzes the circuit operation when the clock is high. Fig. 3-6 shows the resetting state. In this state, transistors M7, M10 and M44 are working in the linear conducting mode, where the conducting resistance is very low and both outputs Q and $\overline{Q}$ are set close to the power supply voltage, which is logically high. Transistor M44 in the low resistance mode forces the voltage at nodes *A* and *B* to be close to each other and transistor M3 and M4 are put in a high gain unstable mode.

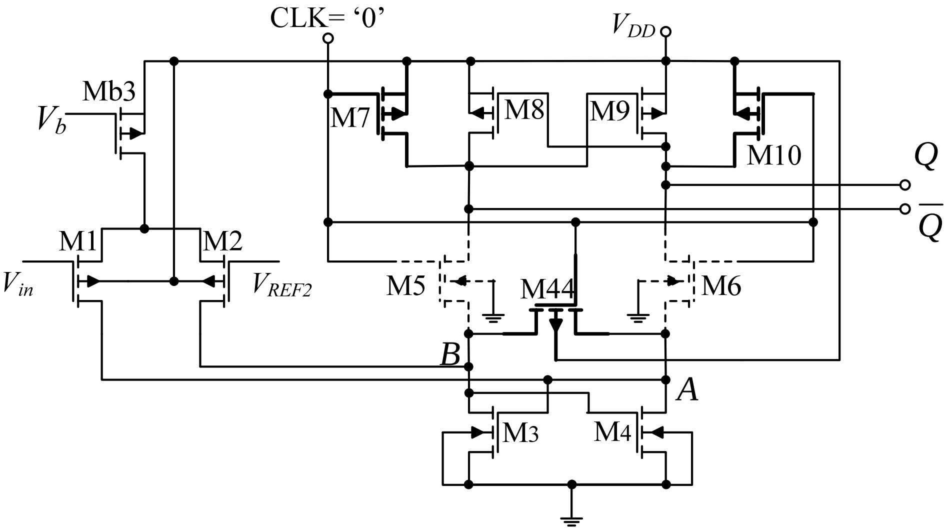


Fig. 3-6 Clocked Amplifier in Resetting Mode

Fig. 3-7 shows a simplified schematic of the clocked amplifier in resetting mode. A resistor R is used to represent the ON resistance of the transistor M44, which is low because M44 is working in the linear mode. The voltages at node A and node B are pulled close to each other, $V_{GS3} = V_{GS4}$ and M3 and M4 are both in the saturation region.

$$I_{DS3} = I_{DS4} = \frac{I_{bias}}{2} \tag{3.3}$$

$$V_{GS3} = V_{GS4} = \sqrt{\frac{I_{bias}}{K_3}} + V_T \tag{3.4}$$

where K_3 is the conduction factor of transistor M3. If $V_{in} = V_{ref}$, the bias current I_{bias} is split into transistors M1 and M2 equally and flows through M3 and M4 equally, so no current goes through R . If one of the voltages of V_{in} or V_{REF2} is much higher than the other, for example $V_{in} \ll V_{REF2}$, almost all the bias current flows through M1 but Eq. (3.3) holds, so half of the bias current goes through R then M4, which is $I_{DS4} = I_R = \frac{I_{bias}}{2}$.

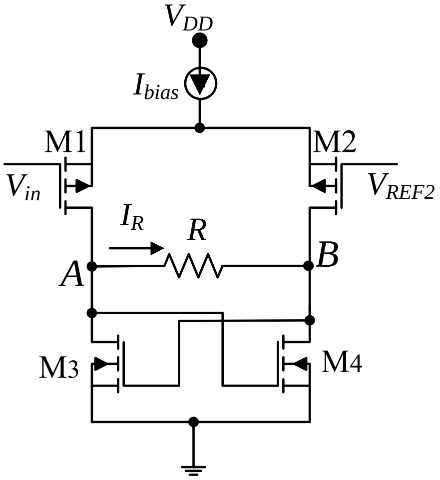


Fig. 3-7 Simplified Clocked Amplifier Circuit Resetting Mode

In the condition where V_{in} is slightly lower than V_{REF2}, which is a small signal condition, the current flowing through M1 is larger than the current through M2 and the current through R is the difference of I_{SD1} and I_{SD2}.

$$\begin{aligned} I_R &= I_{SD1} - I_{SD2} = g_m(V_{ref} - V_{in}) \\ g_m &= \sqrt{K_1 I_{bias}} \end{aligned} \tag{3.5}$$

where K_1 is the conduction factor of transistor M1.

Once the transistor M44 is turned off, the unbalanced current will switch the flip-flop formed by M3 and M4 into the state with the voltage at node A higher than the voltage at node B very rapidly.

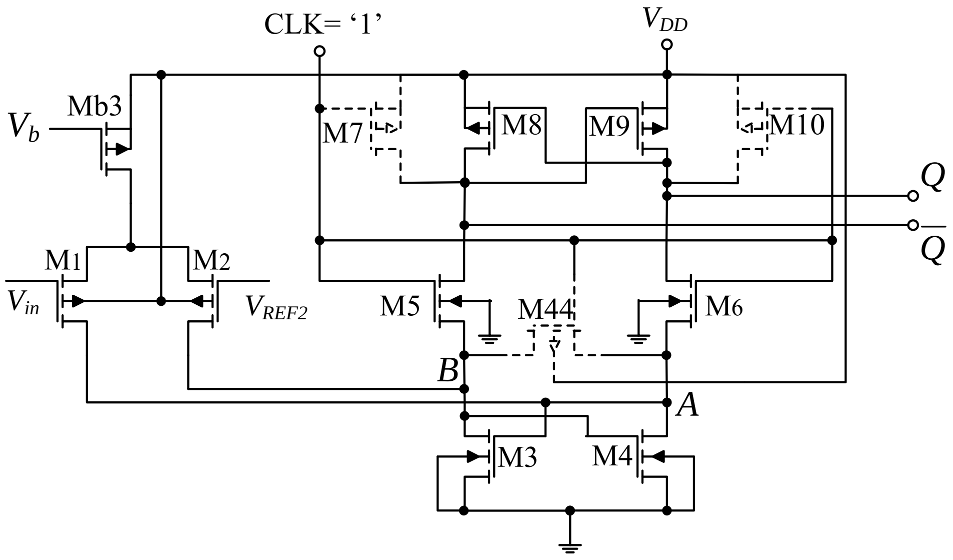


Fig. 3-8 Clocked Amplifier Amplifying Mode

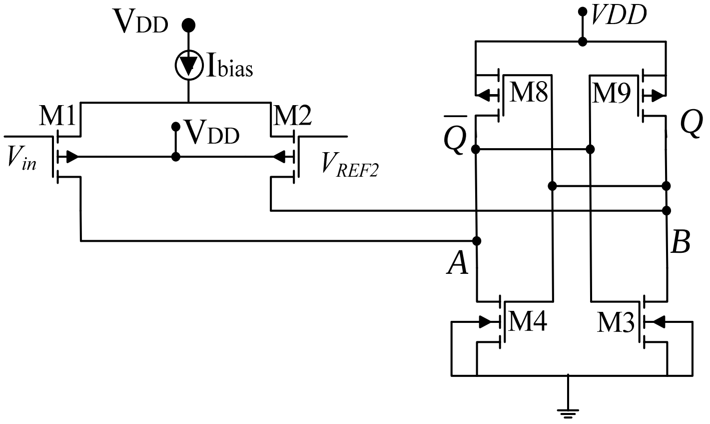


Fig. 3-9 Simplified Clocked Amplifier Circuit in Amplifying Mode

Fig. 3-8 shows the clocked amplifier working in amplifying mode. As the clock is high, the transistors M7, M10 and M44 are cut off, and M5 and M6 are working in a low resistance mode. If the resistances of M5 and M6 can be neglected, the circuit can be simplified as depicted in Fig. 3-9. At the moment that the circuit has just changed to the amplifying mode from the resetting mode, the voltages at A and B are close to each other and the circuit is in an unstable mode. The imbalance of the differential pair will cause different amounts of current $g_m(V_{in} - V_{REF2})$ to be injected into nodes A and B, which will induce a voltage difference between these two nodes. The voltage difference will be sensed by the cross coupled inverter and amplified, so the full complementary output at Q and $\overline{Q}$ will reach either zero or VDD rapidly.

3.3.2 R-S Latch

The R-S latch was implemented using the schematic in Fig. 3-10. Here, two NAND gates are connected to construct an R-S latch, where two inputs are either both high or complementary coming from the clocked amplifier described in the previous section. The truth table for this R-S latch is listed in Table 3-1.

Table 3-1 Truth Table for R-S Latch

Q	$\overline{Q}$	Q_O	$\overline{Q}_o$
0	**0**	**1**	**1**
1	**1**	**Q_O**	$\overline{Q}_o$
1	**0**	**1**	**0**
0	**1**	**0**	**1**

The condition in the first row is not allowed and will not occur in the circuit given here.

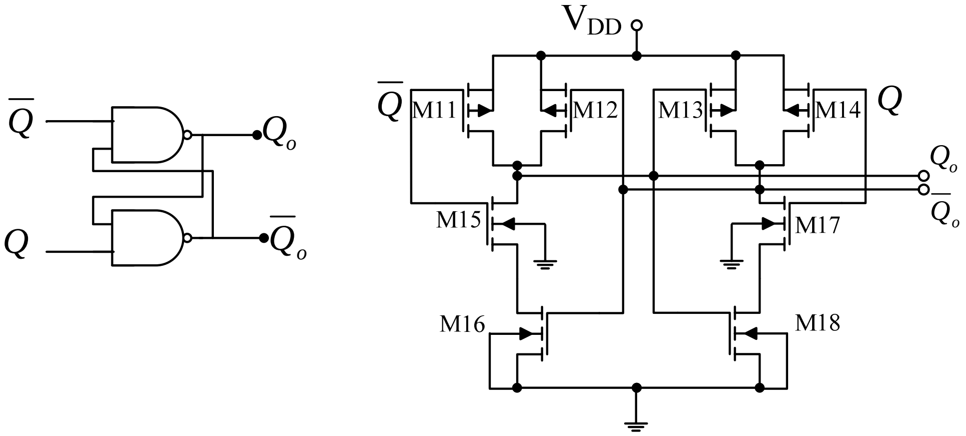


Fig. 3-10 Schematic of R-S Latch

3.3.3 Level-shifted Buffer

As discussed in section 3.2, the voltage level of the feedback signal cannot be as large as full scale, so the output of the R-S latch can not directly drive the switch pair. In this case, a level shifted buffer is required. Fig. 3-11 shows the level shifted two stage buffer driven by a new power supply V_{DC2}, which is lower than the input signal amplitude.

The first stage is composed of two n-MOS transistors, with one of the complimentary signals driving each of them. The second stage is a normal inverter driven by the output of the first stage.

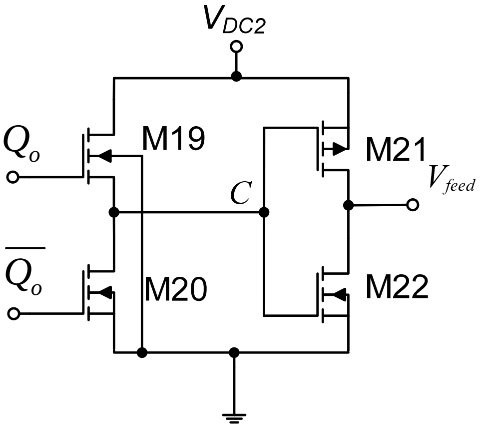


Fig. 3-11 Level-shifted Buffer

3.4 Stress Modulated Output

The final output of the system is taken from the R-S latch output through output buffers that have the same properties as the feedback signal, V_{feed}. The output properties of the system are discussed as following.

3.4.1 Output of the System

The wave forms in Fig. 3-12 are the PSPICE simulated clock signal, the V_{feed} signal, and the voltage at the capacitor, which are shown with no mismatch. The clock signal frequency here is

2 MHz. The feedback signal frequency is at one half the frequency of the clock signal, 1 MHz. When the feedback signal voltage is low, the current is injected into the integrator and the voltage at the integrator (or capacitor) increases; when the feedback signal is high, the current is drawn from the integrator and the voltage decreases. The comparator evaluates the voltage at the integrator when the clock rising edge arrives, and the result determines the V_{feed} signal which controls the switch. The V_{feed} signal then remains in that state until the next rising clock edge comes. The voltage at the integrator is a symmetrical triangular wave with a frequency of 1 MHz, as the charging and discharging current values are equal. Fig. 3-13 shows the DFT (Discrete Fourier Transform) result of the V_{feed} signal, which shows a single peak at 1 MHz.

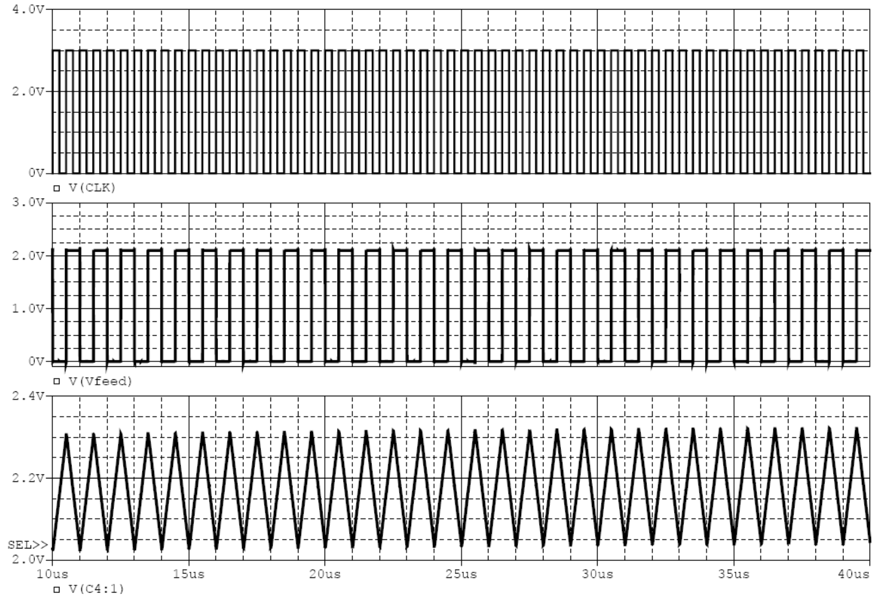


Fig. 3-12 Output Wave Forms of the System with Zero Mismatch

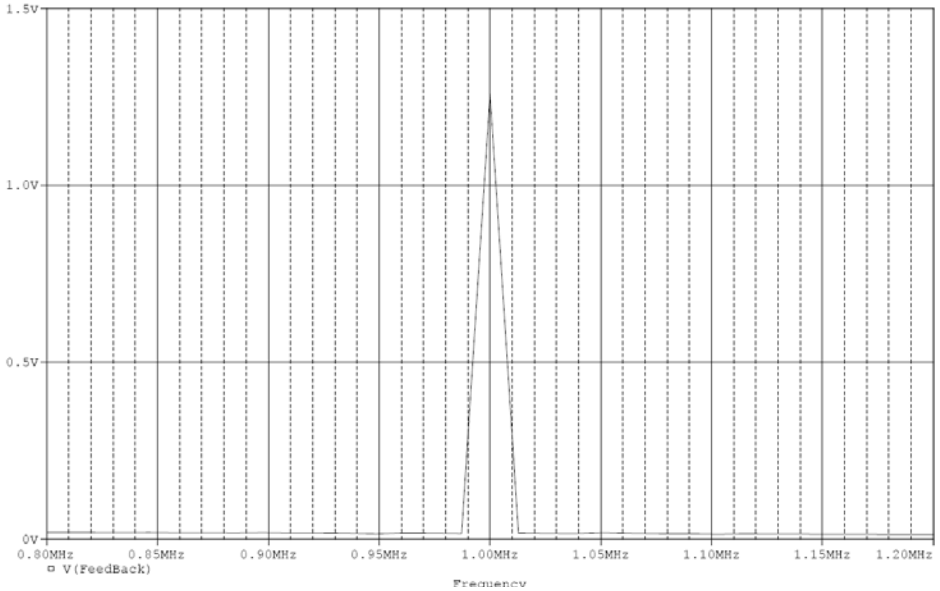


Fig. 3-13 FFT of the Vfeed without Mismatch

If there is some mismatch between the two transistors in the current mirror, the currents charging and discharging the integrator will be different, as shown in Fig. 3-14. The duty cycle of the V_{feed} will no longer be exactly 50% as in Fig. 3-12, and the average duty cycle of the V_{feed} is therefore modulated by the mismatch. The duty cycle is less than 50% when the charging current is larger than the discharging current and more than 50% when the charging current is lower than the discharging current.

3.4.2 Frequency Splitting

The DFT of the feedback signal with zero mismatch shows a single tone dominant in the frequency domain. If there are some mismatches between the two mirrored transistors, the charging and discharging that takes place in the time period will cause a net charge to remain in the integrator, and this difference will be accumulated continuously. The output wave form with an -8.5% mismatch is shown in Fig. 3-14, and the corresponding signal in the frequency domain is plotted in Fig. 3-15. Here the single peak in the matching condition is split in two, and the two frequencies are located equal distances from the single peak obtained for the zero mismatch case.

The mismatch can be estimated approximately using Eq. (3.1). When $n = 12$, the mismatch is estimated as $\frac{1}{n} \times 100\% = 8.3\%$. From Fig. 3-15 the frequency difference between the two split tones is estimated as $84.8kHz$ (or $1042.4kHz - 957.6kHz$), about 8.5% of the single tone when the circuit is exactly matched. This indicates that the magnitude of the frequency split may be proportional to the mismatch.

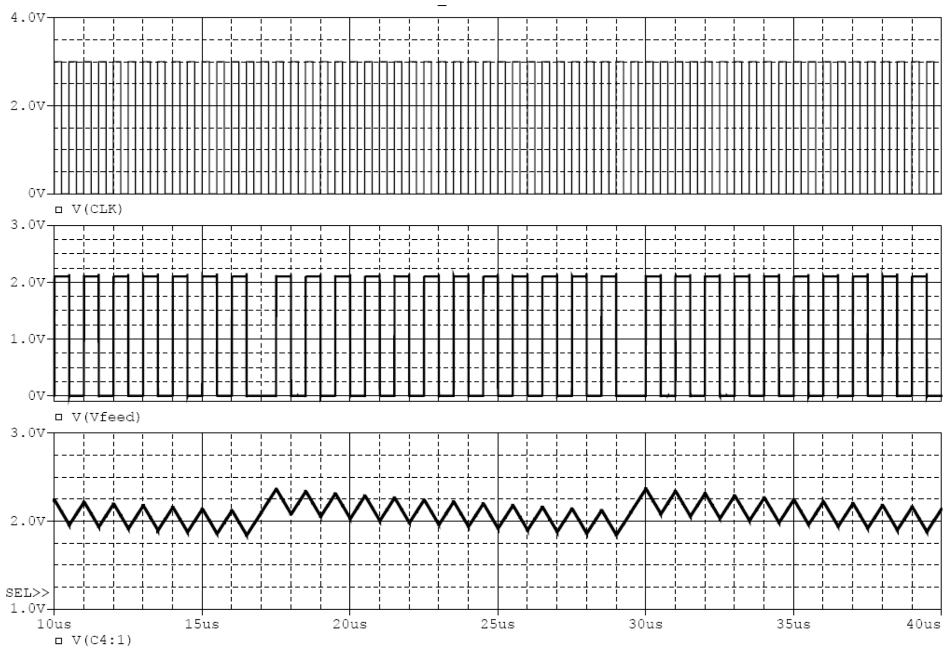


Fig. 3-14 Output Forms with -8.5% Mismatch

Further simulations using different mismatches confirm that the frequency split is indeed proportional to the mismatch between the two transistors in the current mirror; some outputs under different mismatches are shown in Fig. 3-16. Table 3-2 shows the frequency split under different mismatches. Here, the frequency mismatch at one side is written as negative for convenience in order to distinguish the direction of the mismatches. The data in Table 3-2 is plotted in Fig. 3-17 and a linear fitting equation obtained with a correlation factor of 0.99, which indicates that there is a linear relationship between the output frequency split and the mismatch of the mirrored transistors.

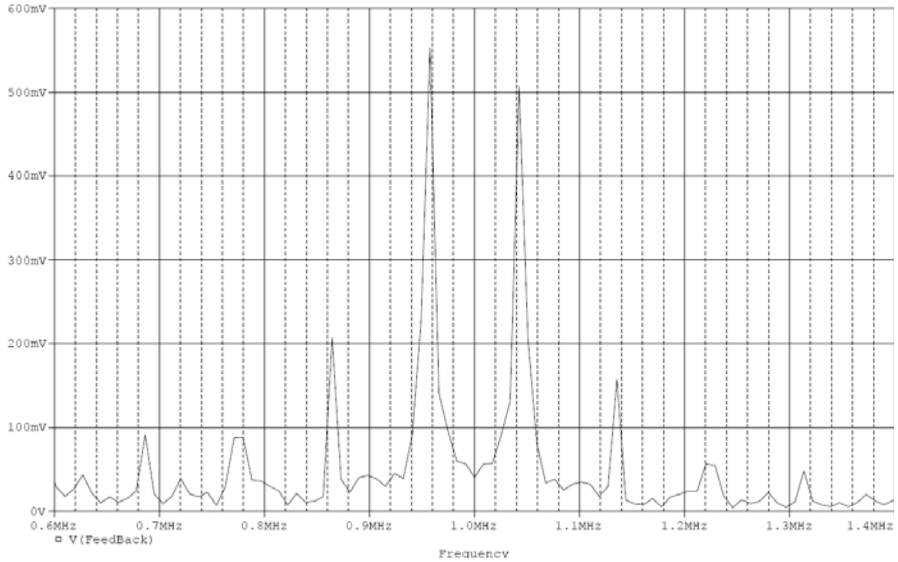


Fig. 3-15 FFT of Vfeed with -8.5% Mismatch

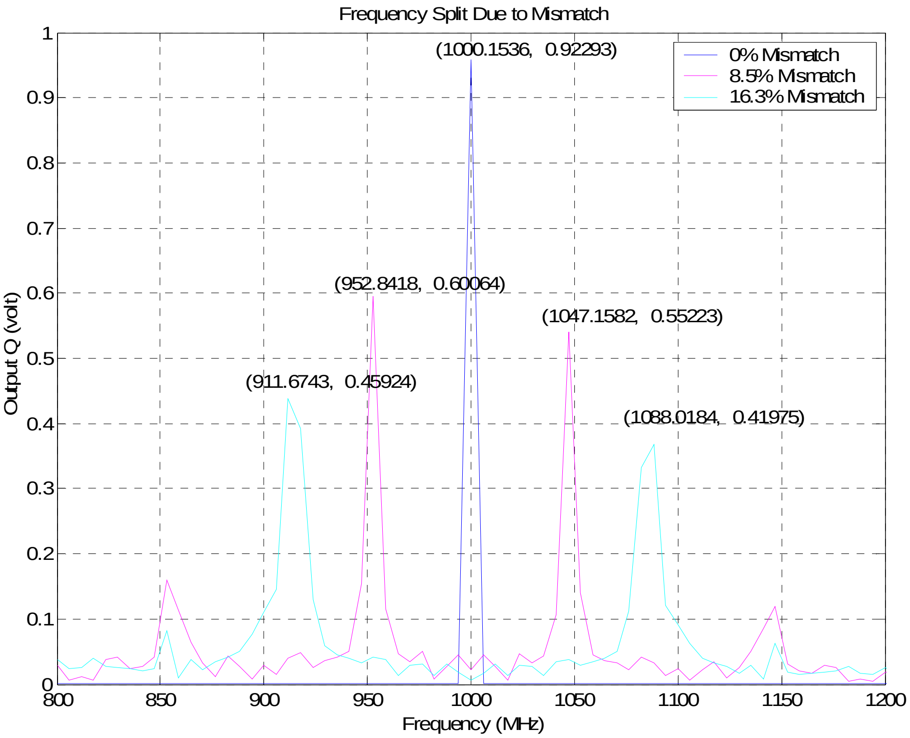


Fig. 3-16 Output Frequency Split vs. Mismatch

Table 3-2 Frequency Split for Different Mismatches

W2'(um)	W2'-W2 (um)	(W2'-W2)/W2 (%)	f1 (kHz)	f2 (kHz)	Δf (kHz)	(f1+f2)/2 (kHz)	Δf/f (%)
10.8	-2.1	-16.28	905.882	1094.1	-188.22	999.99	-18.82
11.2	-1.7	-13.18	923.529	1076.5	-152.97	1000.01	-15.30
11.6	-1.3	-10.08	941.177	1058.8	-117.62	999.99	-11.76
12.0	-0.9	-6.98	964.706	1035.3	-70.59	1000.00	-7.06
12.5	-0.4	-3.10	988.235	1011.8	-23.56	1000.02	-2.36
12.9	0.0	0.00	1000.000	1000.0	0.00	1000.00	0.00
13.4	0.5	3.88	976.471	1023.5	47.03	999.99	4.70
13.8	0.9	6.98	958.824	1041.2	82.38	1000.01	8.24
14.2	1.3	10.08	947.059	1052.9	105.84	999.98	10.58
14.6	1.7	13.18	929.412	1070.6	141.19	1000.01	14.12
15.0	2.1	16.28	911.765	1088.2	176.44	999.98	17.64
15.4	2.5	19.38	900.000	1100.0	200.00	1000.00	20.00

*Here, the frequency difference is written as a negative value when W2'is smaller than W2 for ease in distinguishing mismatches in different directions.

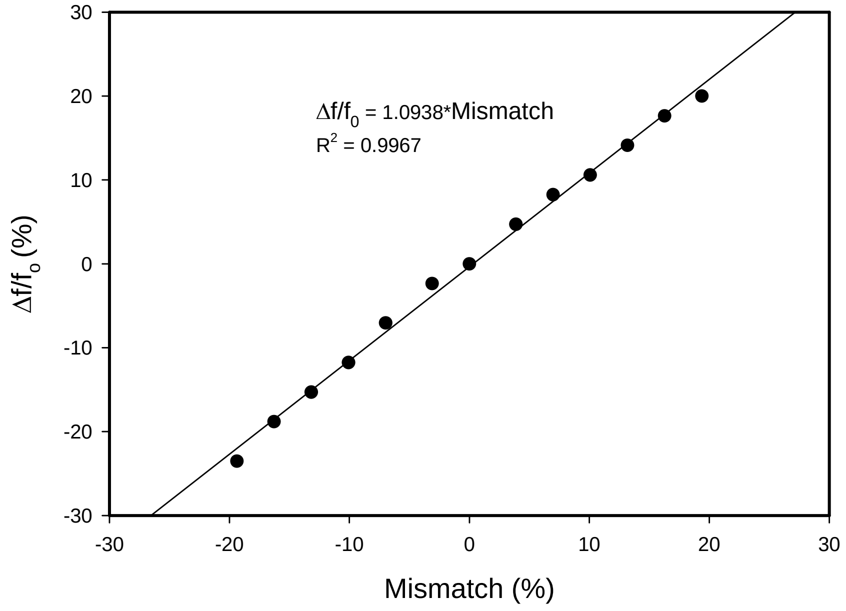


Fig. 3-17 Frequency Split versus Mismatch

3.4.3 Mixing Properties for Two Frequency Signals

The properties of the output of the stress sensor system can be mimicked by mixing two known signals, as shown in Fig. 3-18. The first signal plotted in the Fig. 3-18 is a sinusoidal wave with a period of $1\mu s$ or a frequency of $1MHz$. The second wave form is a sign function with amplitude values of 0.5 and -1.5. The third waveform, C, is the signal obtained by mixing the previous two. Clearly the sensor system output signal includes the information from both A and B, and an analysis of the wave form characteristics reveals the information about the waveform obtained from the sensor system.

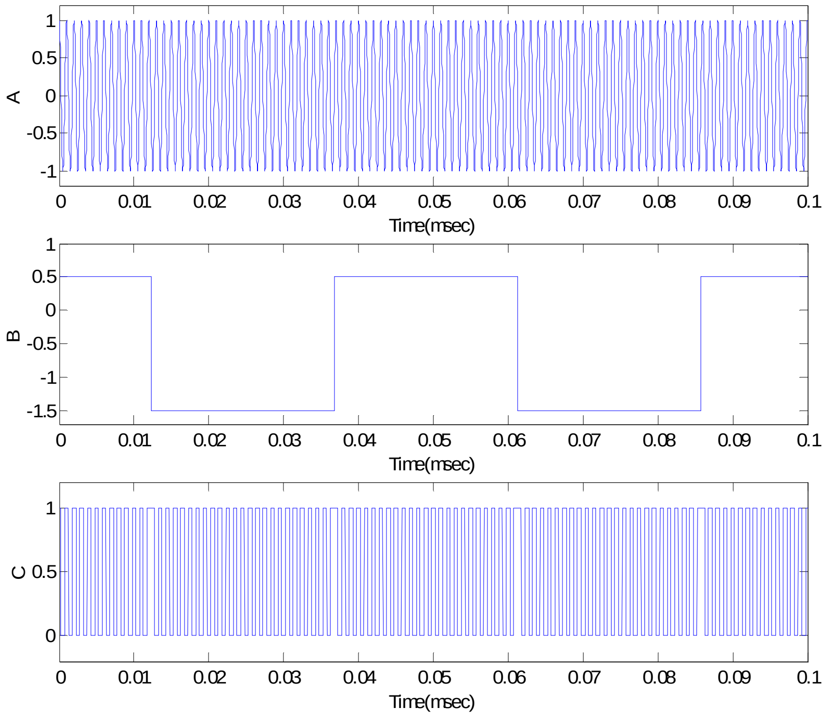


Fig. 3-18 Output Wave Form Obtained by Mixing Two Signals

Signal A is a sinusoidal wave

$$
\begin{aligned}
&A = \cos(\omega_1 t) \\
&\omega_1 = 2\pi / T_1 \\
&T_1 = 1 \times 10^{-6}
\end{aligned}
\tag{3.6}
$$

Signal B is a sign function

$$
\begin{aligned}
&B = sign[\cos(\omega_2 t)] - 1/2 \\
&\omega_2 = 2\pi / T_2 \\
&T_2 = (2n-1)T_1
\end{aligned}
\tag{3.7}
$$

Signal C is the signal obtained by mixing A and B

$$C = \frac{1}{2}[sign(A \bullet B) + 1] \tag{3.8}$$

Expanding the sign function in Eq.(3.7) yields

$$B = \frac{2}{\pi}\cos(\omega_2 t) - \frac{2}{3\pi}\cos(3\omega_2 t) + \ldots \tag{3.9}$$

The amplitude of the $3\omega_2$ component is one third that of the ω_2 component and higher order components are much smaller. When A and B are mixed together and the higher order items are neglected, the result is

$$A \bullet B \cong \frac{1}{\pi}\{\cos[(\omega_1 + \omega_2)t] + \cos[(\omega_1 - \omega_2)t]\} \tag{3.10}$$

This is a DSBSC signal that can be demodulated to recover ω_2. Wave form C is

$$
\begin{aligned}
C &= \frac{1}{2}[sign(A \bullet B) + 1] = \frac{1}{2}\frac{A \bullet B}{|A \bullet B|} + \frac{1}{2} \\
&= a\{\cos[(\omega_1 + \omega_2)t] + \cos[(\omega_1 - \omega_2)t]\} + \frac{1}{2}
\end{aligned}
\tag{3.11}
$$

where $a = \dfrac{1}{2\sqrt{\cos^2[(\omega_1 + \omega_2)t] + \cos^2[(\omega_1 - \omega_2)t]}}$

In the frequency domain, there are two frequency components at $\omega_1 + \omega_2$ and $\omega_1 - \omega_2$ and

$$\frac{|\Delta\omega|}{\omega_1} = \frac{\omega_2}{\omega_1} = \frac{1}{2n-1} \tag{3.12}$$

The DSBSC signal contains frequency shift information directly related to the mismatch, and the mismatch can thus be extracted from the output signal.

3.5 Chip Layout Design

The layout for this design was accomplished by using the public domain *LASI* software on a Windows™ platform [130, 131]. This design follows the MOSIS scalable CMOS (SCMOS) design rules [132], which are transparent to the details of the fabrication processes.

This design was fabricated in a MOSIS AMI ABN 1.5 μm n-well CMOS process. The masks included in this design were n-well, active, n-select, p-select, poly, contact, metal1, via, metal2 and glass. The design was based on an n-well process, where p-channel MOSFETs are located inside an n-well and the body can be connected to the source easily by separating the n-well where the p-FET is built. Here, the body effect can be avoided for most p-FETs, in contrast to n-channel MOSFETs which are built directly on a p-substrate that is always connected to ground (for one positive power supply system), so the body effect can be eliminated only when the source of the transistor is connected to ground. Because an ac signal in the mega hertz range is used in this system, signal coupling and other noise may destroy the desired signal if the layout is not designed properly. Other layout design issues are described in the following sections.

3.5.1 Cross Talk

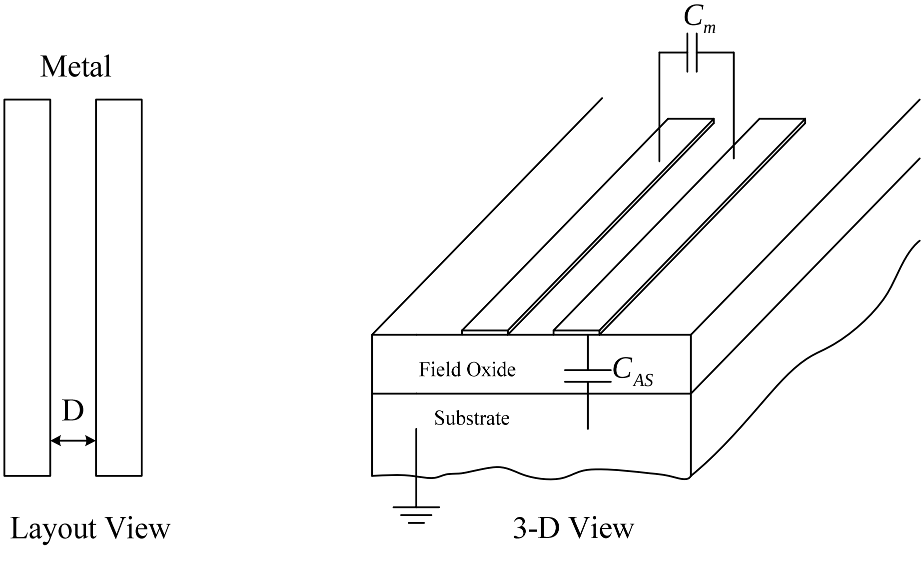


Fig. 3-19 Crosstalk between Metal Conductors

When two conducting traces are close to each other, the signal in one trace interferes with the signal in the other. The term crosstalk is used to describe this coupling of unrelated signals from one circuit to another adjacent circuit.

Consider the two metal wires in the chip shown in Fig. 3-19. The signal voltage propagating along one of the conductors couples a current onto the other conductor. This coupled current can be estimated by

$$I_m = C_m \frac{dV_s}{dt} \tag{3.13}$$

where C_m is the mutual capacitance between the two conductors, V_s is the voltage signal on the source conductor, and I_m is the coupled current. The mutual capacitance, C_m, can be determined experimentally by applying a step voltage to one conductor while measuring the coupled voltage on the adjacent conductor. Because the capacitance per unit area between the layers, Metal1 and the substrate, is specified by the foundry, the capacitance between the adjacent conductor and the substrate is known and the interference voltage can write as

$$\Delta V = V_s \frac{C_m}{C_m + C_{AS}} \tag{3.14}$$

where C_{AS} is the capacitance between the adjacent conductor and the substrate (ground), as in Fig. 3-19. This equation shows that the interference voltage increases with the mutual capacitance and decreases with the capacitance between the adjacent conductor and the substrate. In most cases, C_{AS} is determined by the fabrication process and the area of the conductor, and is therefore not easily changed. V_s is the signal to be propagated on the conductor, so although reducing the signal strength will reduce the interference voltage, the relative interference affecting the signal is not changed, and normally V_s is fixed for a given system. For a high speed circuit, the use of a large C_{AS} increases the signal delay on the conductor, which is undesirable. Therefore, the only way to reduce ΔV is to reduce C_m, so this is the approach normally taken in order to reduce the interference between signal wires.

Between the adjacent metal lines shown in Fig. 3-19 there is also a mutual inductance, which acts as if a transformer is connected between the two conducting lines. A current flowing in one conductor thus induces a voltage in the other conductor and this mutual inductance can be determined experimentally by injecting a current into one conductor and measuring the resulting voltage on the other conductor.

$$V_m = L_m \frac{dI_s}{dt} \tag{3.15}$$

where I_s is the injected current, V_m is the induced voltage in the other conductor, and L_m is the mutual inductance between the two conductors. Obviously, reducing L_m will reduce the inductive crosstalk between the two conductors.

Empirical equations for the mutual capacitance and inductance of the cross section of a coupled micro strip pair in an inhomogeneous medium with the top side exposed to air show that [133]

$$\begin{aligned} C_m &\propto (1/D)^n \qquad n = 0.78 \sim 0.8 \\ L_m &\propto (1/D)^m \qquad \mathrm{m}{=}2.03 \sim 2.6 \end{aligned} \tag{3.16}$$

Both mutual capacitance and inductance are reduced with increasing distance, so increasing the distance between the two conductors is a way to reduce the crosstalk problem. Another way to reduce the crosstalk between the two neighboring conductors is to use a guard trace between them. The grounded guard trace halves the crosstalk compared to the crosstalk between two conductors separated by the same distance without guard trace [130].

For strong signals such as the clock and output in the system, putting guard traces at both sides reduces the crosstalk with other signals [130, 134]. A pair of grounded traces running parallel to a sensitive signal can also reduce the crosstalk from other lines [130]. Both techniques were adopted in this design.

3.5.2 Bypass Capacitance

In high performance designs, bypass capacitors are often used for many reasons, including to supply current bursts for the circuit, and to provide an ac path between the power supply and the ground [135].

A fast switching circuit needs a very high peak current when it switches, but this current burst cannot be provided by the power supply itself due to the ‘ground bounce’ and ‘VCC sap’ effect. A bypass capacitor accumulates charge and then releases it rapidly to supply the current needed for a fast transition. The bypass capacitance used for this purpose must be connected as close as possible to the circuit. The self-inductance of the capacitor here should be very low, while the capacitance value needs to be large in order to supply sufficient current for the current burst.

A current at low frequency returning from the power supply to ground follows the path of least resistance, while a current at high frequency follows the path of least inductance [130]. This is because the impedance of the inductance is far more significant than its resistance for a given return-current path at high frequency. Adding capacitors between the power supply and ground reduces the inductance and overall impedance, allowing the current to easily make high speed transitions.

Metal-to-Metal capacitors are used as bypass capacitors between the power supply and the ground here, as a lot of space on the chip is available here. MOS capacitors are used as bypass capacitors between the reference voltages and ground in this design.

3.5.3 Integrator Capacitor

The integrator capacitance is one of the most critical components in this design; the absolute value itself is not critical, but the consistency of the value over the working voltage range is very important. In order to eliminate the noise coupling from outside, a combination of metal-metal and metal-poly capacitors is used in parallel, as shown in the cross section in Fig. 3-20. One electrode is surrounded by the other with a ground connection, and signals from the outside are shielded by this electrode, protecting the voltage at the capacitor from outside interference.

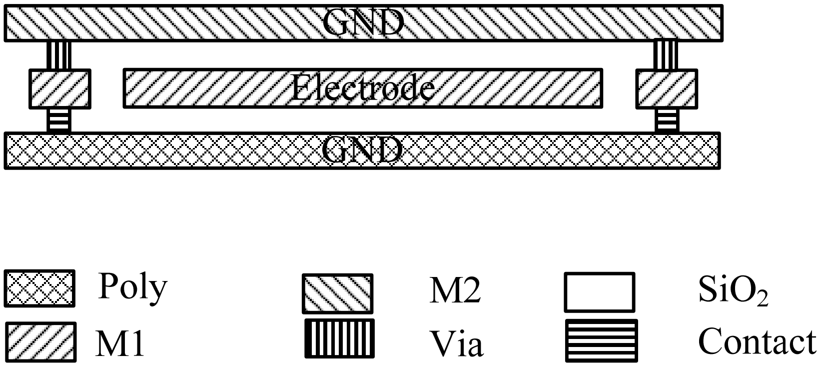


Fig. 3-20 Cross Section of Integrator Capacitance

3.5.4 Layout

Fig. 3-21 shows the chip designed for this study. Two units of the sensor circuit are placed near the mid-edge of the chip and an identical design of current mirrors is placed close to the sensor in the circuit. As a result of this placement, the separate current mirrors can be used as for both comparison and calibration. Fig. 3-22 shows the integrator capacitor layout. Here, four of the cells are used in parallel to obtain the required capacitance value of around $20\,pF$.

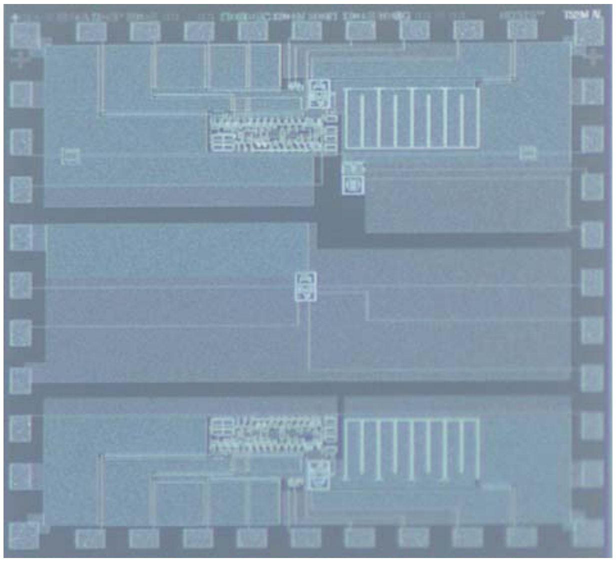


Fig. 3-21 Picture of DSM Chip

Fig. 3-22 Layout of Integrator Capacitance Cell

3.6 Noise Suppression Simulation

Noise suppression is a very important consideration for high precision systems. Fig. 3-23 shows the flow chart used to simulate how the noise influences the mismatch sensitivity of the system. The behavioral simulation was performed using MATLAB. The MATLAB code is attached as Appendix B. The input node of the comparator is most sensitive to noise; any noise at input of the comparator may easily cause the output of the comparator to deviate from the expected value so that the state of the system will no longer be in an ideal state. The noise signal here is defined by $V_n = A_n \bullet rand$. The FFT analysis is applied to the signal $ctrl$.

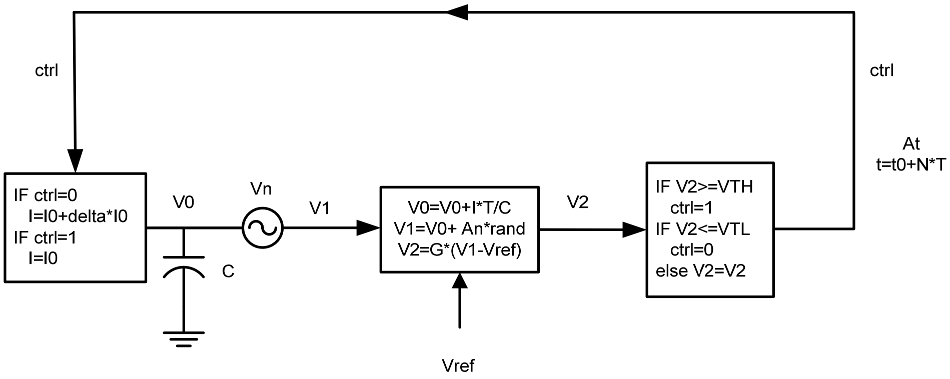


Fig. 3-23 Flowchart for Noise Immunity Simulation

Fig. 3-24 shows the waveforms for the voltages at the capacitance and the ctrl signal and the FFT for the ctrl signal with the noise at zero. Fig. 3-25 and Fig. 3-26 show the corresponding plots with noise levels of 5mV and 20mV. It is important to note that the wave form is disturbed more and more seriously as the noise amplitude increases, but the peak power spectrum location in the frequency domain remains stable providing the noise is not too high. Fig. 3-27 and Fig. 3-28 show the power spectra under different noise levels, revealing that the peak frequencies of the signal are maintained even with a noise level of 32mV, and the amplitude of the signal at the peak frequencies reduces as the noise level increases. When the noise signal is larger than 48mV, the signal strength at the peak frequencies reduces to a level comparable to that of other harmonics, and the signal at the peak frequencies no longer dominates. Fortunately, this occurs only at noise levels of more than 40mV, and the noise level is normally much lower than this level. The simulation implies that this DSM sensor system is relatively insensitive to noise, which is an important characteristic for a mismatch detection system.

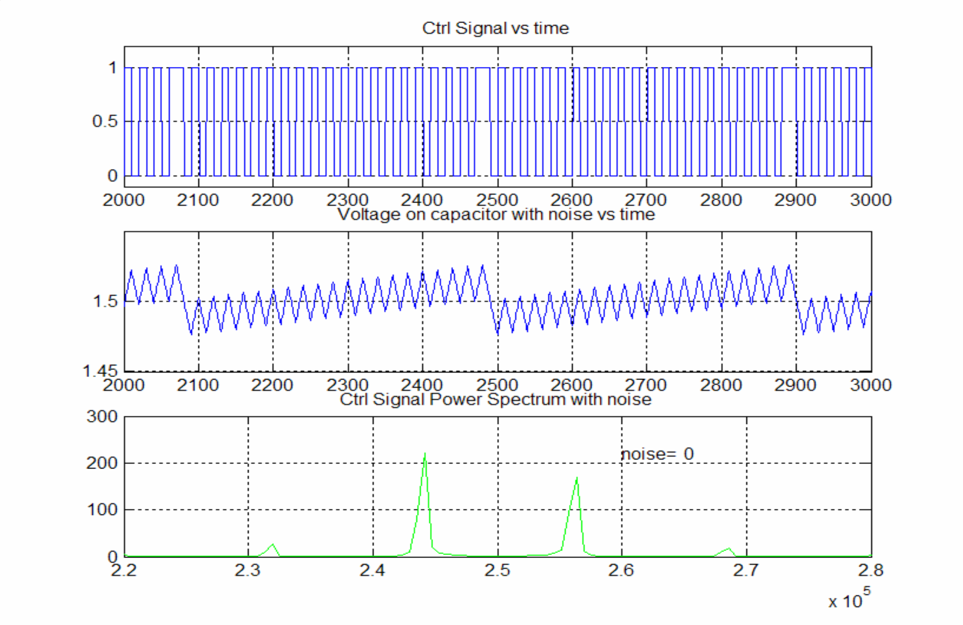


Fig. 3-24 Output Properties of 5% Mismatched PWM with a Noise Level of 0mV

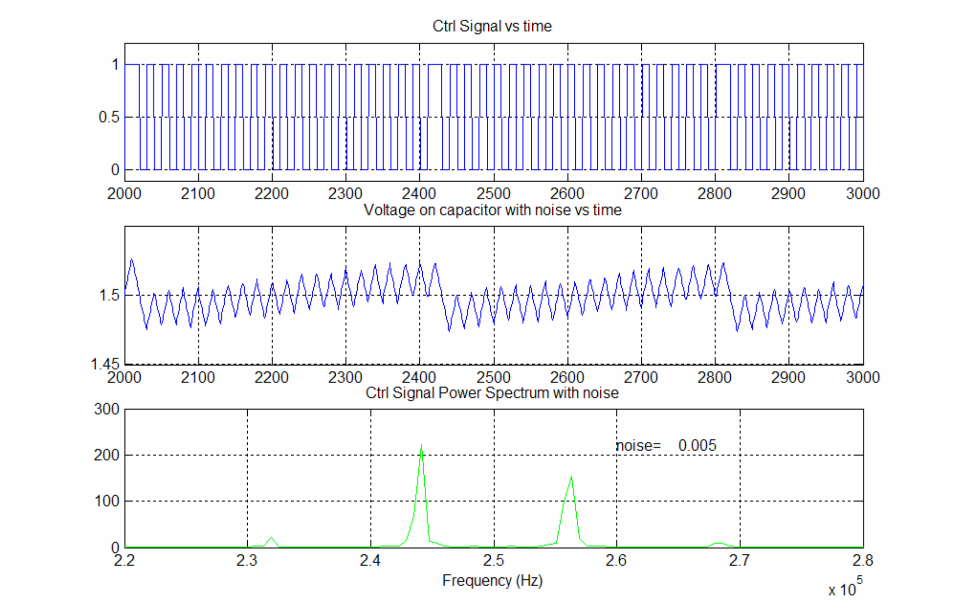


Fig. 3-25 Output Properties of 5% Mismatched PWM with a Noise Level of 5mV

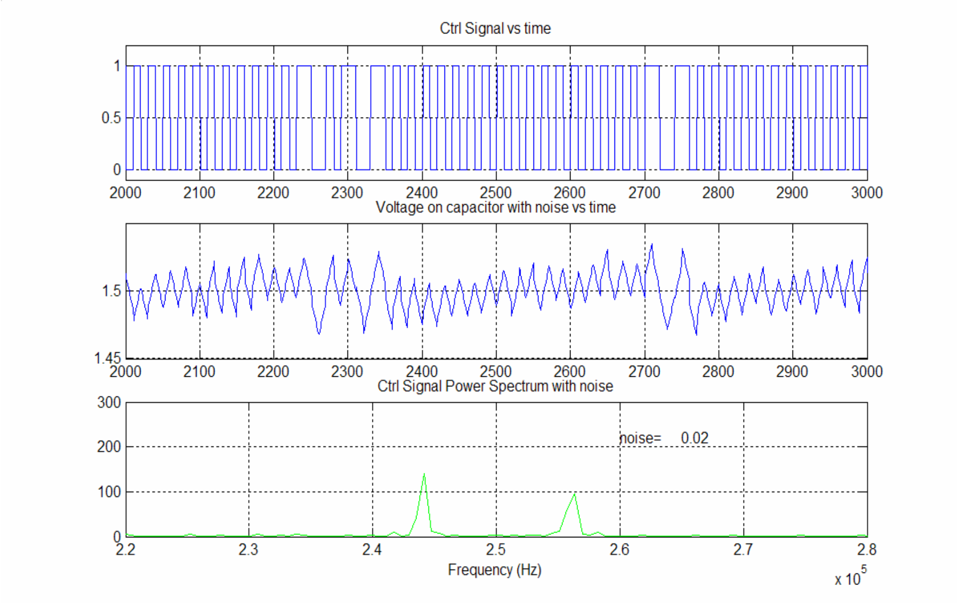


Fig. 3-26 Output Properties of 5% Mismatched PWM with a Noise Level of 20mV

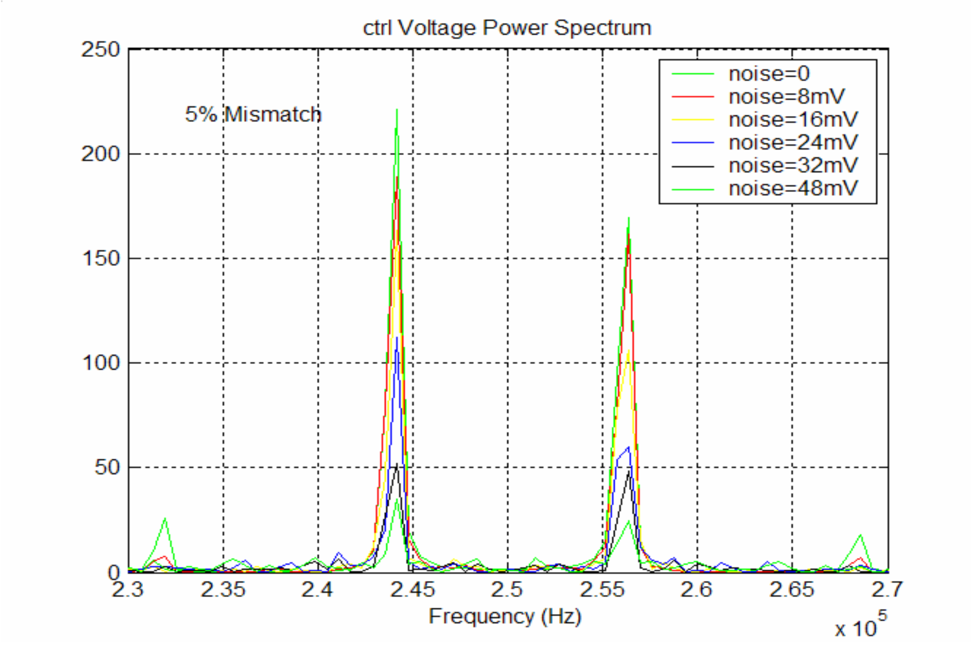


Fig. 3-27 Output Power Spectrum of System under Different Noise Levels

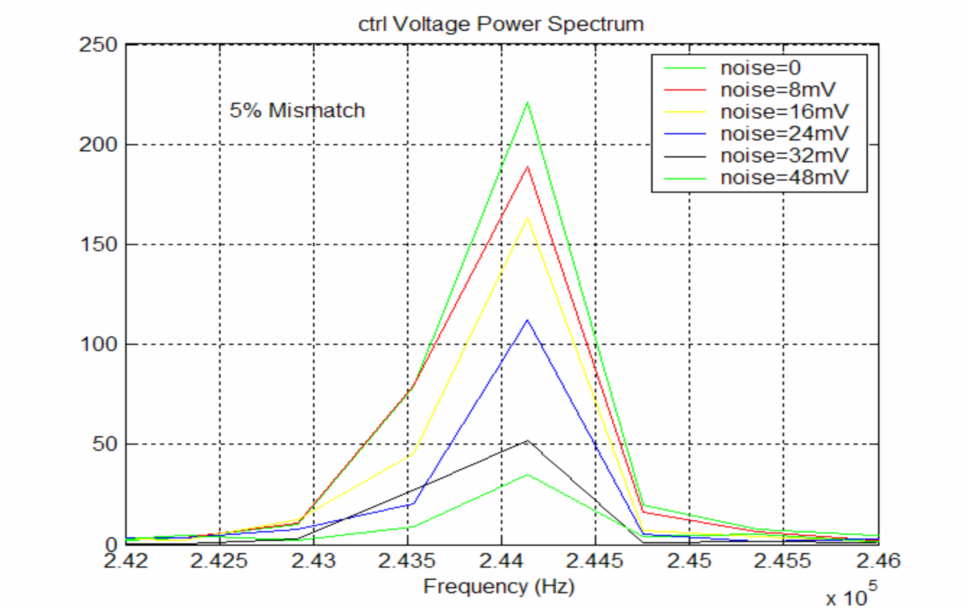


Fig. 3-28 Detail of Power Spectrum Plot under Different Noise Levels

CHAPTER 4. CMOS STRESS SENSOR ARRAY DESIGN

4.1 Cascode Current Mirror versus Regular Current Mirror

In this section, the use of NMOS current mirrors are described as an example and the results are then applied to PMOS current mirrors.

4.1.1 Mismatch Due to V_{DS} Mismatch in a Regular Current Mirror

In the discussion of current mirrors in Section 2.3.1, channel-length modulation was neglected. For the basic NMOS current mirror shown in Fig. 4-1, taking into account the channel length modulation effect, the current flow through the two MOSFET can be expressed as

$$\begin{aligned} I_{D1} = I_{REF} &= \frac{1}{2}\mu_{n1}C_{ox}(\frac{W}{L})_1(V_{GS}-V_{T1})^2(1+\lambda V_{DS1}) \\ I_{D2} = I_{OUT} &= \frac{1}{2}\mu_{n2}C_{ox}(\frac{W}{L})_2(V_{GS}-V_{T2})^2(1+\lambda V_{DS2}) \end{aligned} \tag{4.1}$$

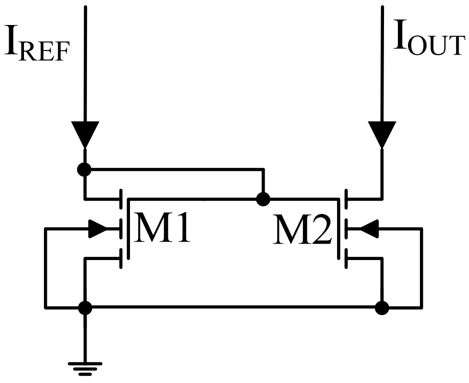


Fig. 4-1 Basic NMOS Current Mirror

The relation between I_{OUT} and I_{REF} can then be written as

$$I_{OUT} = \frac{\mu_{n2}}{\mu_{n1}} \cdot \frac{(W/L)_2}{(W/L)_1} \cdot \frac{(V_{GS} - V_{T2})^2}{(V_{GS} - V_{T1})^2} \cdot \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \cdot I_{REF} \tag{4.2}$$

Assuming the two MOSFETs in the current mirror are identical in terms of their dimensions, doping and mobility, Eq. (4.2) can be simplified to

$$I_{OUT} = \frac{(1 + \lambda V_{DS2})}{(1 + \lambda V_{DS1})} \cdot I_{REF} \tag{4.3}$$

Any difference in the drain-source voltage will introduce a mismatch between the two drain currents. V_{DS1} is determined by I_{REF}, and will not change with V_{DS2}. The relative change of output current due to ΔV_{DS2} can thus be written as

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \frac{\lambda \Delta V_{DS2}}{1 + \lambda V_{DS2}} \approx \lambda \Delta V_{DS2} \tag{4.4}$$

4.1.2 Mismatch Due to V_{DS} Mismatch in a Cascode Current Mirror

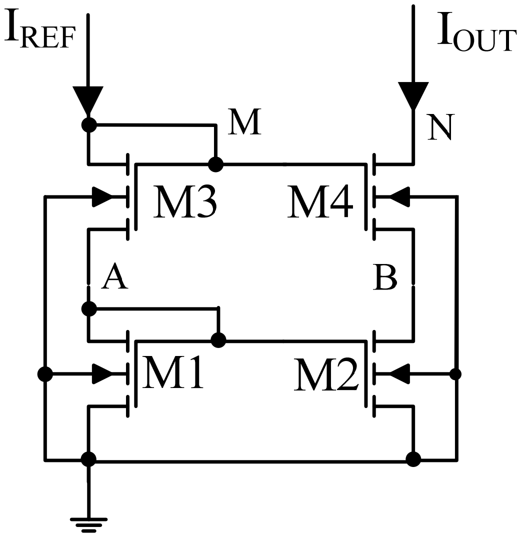


Fig. 4-2 Cascoded NMOS Current Mirror

A cascode current mirror where all the transistors are of the same size is shown in Fig. 4-2. The gate voltages V_G are all controlled by the reference current I_{REF}.

As the bodies of transistors M3 and M4 are not connected to their sources, a body effect exists and the thresholds of the upper two transistors will be different from that of the lower two. Writing $V_{T3} = V_{T4} = V_T'$, the voltage at node M should satisfy the equation:

$$
\begin{aligned}
I_{REF} &= \frac{1}{2}\mu_{n1}C_{ox}(\frac{W}{L})(V_A - V_{T1})^2(1+\lambda V_A) \\
&= \frac{1}{2}\mu_{n3}C_{ox}(\frac{W}{L})(V_M - V_A - V_T')^2[1+\lambda(V_M - V_A)]
\end{aligned}
\tag{4.5}
$$

Thus, the voltages at nodes A and M are determined by the reference current I_{REF}.

Assuming that the voltage at node N, V_N, is high enough to keep transistors M2 and M4 operating in the saturation region, let us now consider how a change in the voltage V_N will affect the voltage at node B. Neglecting the channel length modulation effect, the current through a MOSFET is determined only by the V_{GS} applied, while the channel length modulation effect is included the drain to source voltage applied to the MOSFET will be determined by both V_{GS} and V_{DS}, which means the drain to source voltage will affect the drain current.

In order to simplify the problem, the channel-length modulation effect in transistor M2 will initially be neglected. Once the effect of changing V_N is determined, the channel length modulation effect will be applied to both M2 and M4. The output current I_{OUT} in Fig. 4-2 is determined by V_A and $I_{OUT} = I_{DS2} = I_{REF}$. For transistor M4, the drain current is a constant and satisfies the equation

$$
I_{DS4} = I_{DS2} = \frac{1}{2}\mu_{n4}C_{ox}(\frac{W}{L})(V_M - V_B - V_T')^2[1+\lambda(V_N - V_B)] \tag{4.6}
$$

A change in voltage V_N will induce a change in V_B in order to keep the current a constant. The relative change of V_N and V_B is derived from Eq. (4.6), and can be expressed as

$$
\frac{\Delta V_B}{\Delta V_N} = \frac{V_M - V_B - V_T'}{2(1/\lambda + (V_N - V_B))} \tag{4.7}
$$

In the case of $1/\lambda >> (V_N - V_B)$, Eq. (4.7) can be simplified to

$$\frac{\Delta V_B}{\Delta V_N} \approx \frac{\lambda V_{od}}{2} \tag{4.8}$$

Where V_{od} is the over drive voltage for transistor M4. This equation shows that the ratio of the changes in V_B and V_N is determined by the product of the channel-length modulation coefficient and the overdrive voltage. Normally V_{od} is around a few hundred millivolts, and as λ is about 0.02 for the transistors used here, λV_{od} will be less than a few percent in magnitude. This means that in the cascode current mirror, the voltage change at the output node is shielded by transistor M4.

If the channel-length modulation effect in the transistor M2 is included, the current through transistor M2 can be written as

$$I_{DS2} = \frac{1}{2}\mu_{n2}C_{ox}(\frac{W}{L})(V_A - V_T)^2(1+\lambda V_B) \tag{4.9}$$

Based on Eqs. (4.8) and (4.9), the relative current change due to changes in V_N can be written as

$$\frac{\Delta I_{OUT}}{I_{OUT}} = \frac{\lambda(\frac{\lambda V_{od}}{2})\Delta V_N}{1+\lambda V_B} \approx \frac{\lambda^2 V_{od}\Delta V_N}{2} \tag{4.10}$$

For example, $\lambda = 0.02V^{-1}$ for transistors with $W/L = 8.15\mu m / 5.66\mu m$ such as those used in this design, if $V_{GS} = 1.1V$, $V_{od} = 0.5V$ and $\Delta V_N = 2V$, the change estimated according to Eq.(4.8) is $\Delta V_B = 0.01V$ and $\Delta I_{DS2} / I_{DS2} \approx 0.0002$. Therefore, the current is almost constant when V_N changes providing that the V_N still high enough to maintain transistors in the saturation region. When V_N continues to decrease, transistor M4 first enters the linear region, then voltage V_B starts to decrease following V_N, and the cascode current mirror behaves as a simple current mirror.

The other way to compare the mismatch induced by the drain voltage difference is to compare the output resistance of the current mirror using the small-signal model. The output resistance for the normal current mirror is

$$R_{OUT} = r_{o2} = \frac{V_{DS2} + 1/\lambda}{I_{OUT}} \approx \frac{1}{\lambda I_{OUT}} \tag{4.11}$$

And the output resistance for a cascode current mirror is

$$R'_{OUT} = r_{o4}(1 + g_{m4}r_{o2}) \approx g_{m4}r_{o2}^2 \tag{4.12}$$

The induced current change by a drain voltage difference ΔV_N is ΔV_N divided by the ourput resistance. The normalized current difference for normal current mirror is

$$\frac{\Delta I_{OUT}}{I_{REF}} \approx \lambda \Delta V_N \tag{4.13}$$

And for a cascade current mirror

$$\frac{\Delta I_{OUT}}{I_{REF}} \approx \frac{\lambda^2 V_{od} \Delta V_N}{2} \tag{4.14}$$

The cascode structure eliminates the drain voltage difference induced current mismatch in a current mirror dramatically if all transistors are working in saturation region.

4.1.3 PSPICE Simulation for V_{DS} Sensitivity

PSPICE was used to simulate the behavior of the cascode current mirror. The transistor models were extracted from transistor test results by MOSIS, as listed in Appendices A. The schematic in Fig. 4-3 was used for this simulation. Fig. 4-4 shows the simulation results for voltage V_B and the output current when voltage V_N is changed from 1.2V to 5.0V. The plots show that when V_N changes from 2.0V to 4.0V voltage V_B changes about 0.013V and the relative change of the output current is about $0.18nA$, or 3.6ppm, which is negligible compared to the stress induced changes in the drain-to-source current of the transistors.

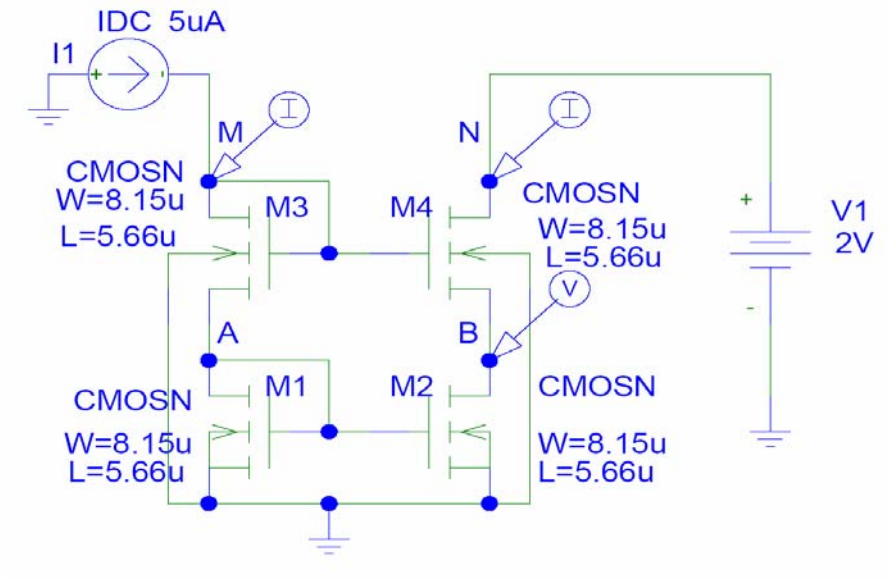


Fig. 4-3 NMOS Cascode CM Schematic Need for Simulation

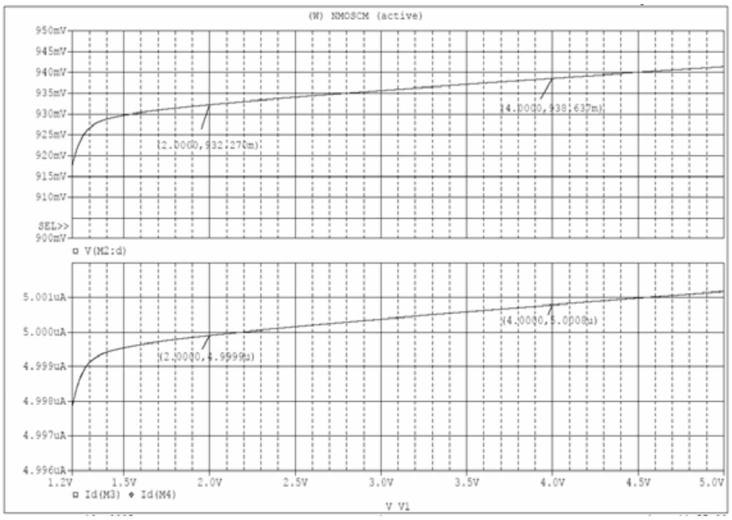


Fig. 4-4 Changes in Voltage VB and Output Current Due to VN Variation

4.2 PMOS Current Mirror Cell for Normal Stress Differences

4.2.1 Characteristics of PMOS Transistor Used in Sensor Cell

The SPICE model used for p-channel MOSFETs in the normal stress difference sensitive current mirror (CM) cell is listed in Appendix A. The channel length of the transistor is $L = 3.2\mu m$ and channel width is $W = 12\mu m$. The PMOS output characteristics simulated by PSPICE are plotted in Fig. 4-5.

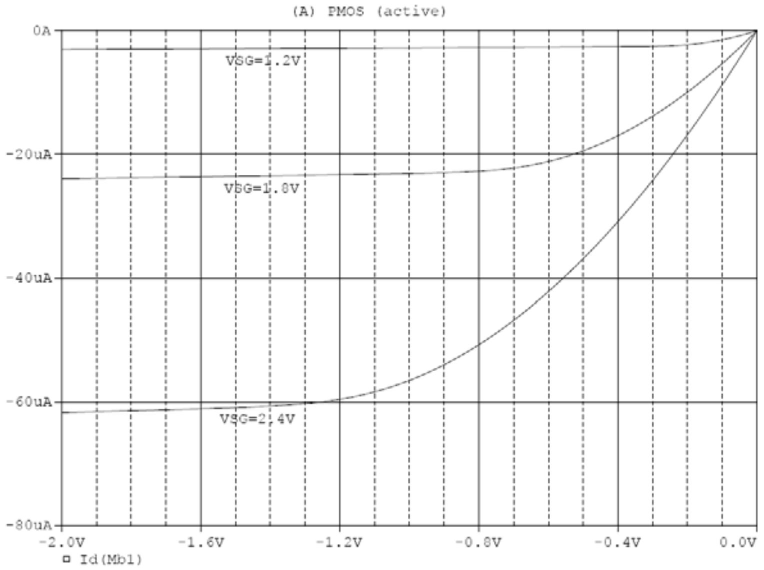


Fig. 4-5 Output Characteristics of a PMOS Transistor in a Sensor Cell

4.2.2 PMOS Current Mirror Cell

The schematic of the PMOS current mirror stress sensor cell needed in this research is shown in Fig. 4-6, and the layout for this cell with transistors of channel length $L = 3.2\mu m$ and channel width $W = 12\mu m$ is shown in Fig. 4-7 (a). Symbols "D1" and "D2" indicate the respective terminals for currents I_{out1} and I_{out2}. Transistors Ms1 and Ms3 are oriented at 90o, while Transistors Ms2 and Ms4 are oriented at 0o relative to the $x_1^{'}$ axis, which is in the $[110]$ direction. The response of the sensor cell to normal stress differences is described in Eq. (2.27), and can here be rewritten as

$$\frac{\Delta I_{out1}}{I_{out1}} - \frac{\Delta I_{out2}}{I_{out2}} = \Pi_{44}^{p}(\sigma_{11}^{'} - \sigma_{22}^{'}) \qquad (4.15)$$

Fig. 4-7 (b) shows a theoretical plot of output versus normal stress difference with a piezoresistive coefficient $\Pi_{44}^{p} = 1000(TPa)^{-1}$.

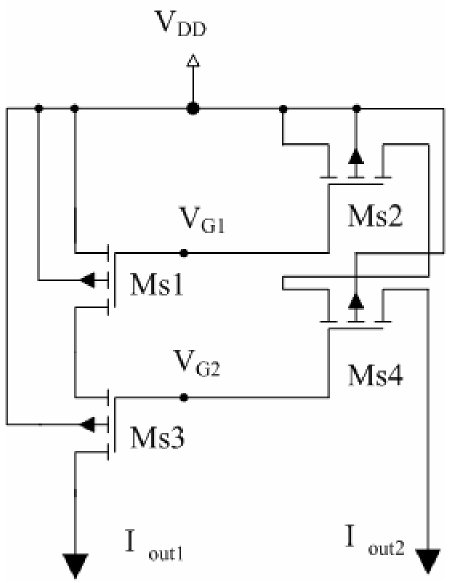
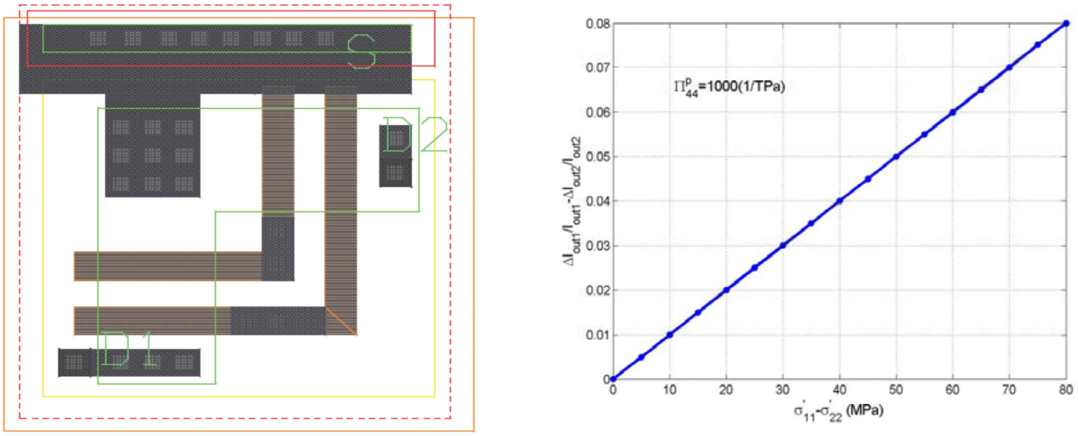


Fig. 4-6 Schematic of the Normal Stress Difference Sensitive PMOS CM Cell



(a)

(b)

Fig. 4-7 (a) Layout of the Normal Stress Difference Sensitive PMOS CM Cell, (b) Sample Plot of Output versus Normal Stress Difference

4.3 NMOS CM Cell for Shear Stress

4.3.1 Characteristics of NMOS Transistor Used in Sensor Cell

The SPICE model used for n-channel MOSFETs in the normal stress difference sensitive current mirror cell is also listed in Appendix A. Here, the channel length of the transistor is $L \approx 4.5\mu m$ and the channel width is $W \approx 6.5\mu m$. Fig. 4-8 shows the output characteristics of the transistor with the designed dimensions based on a PSPICE simulation.

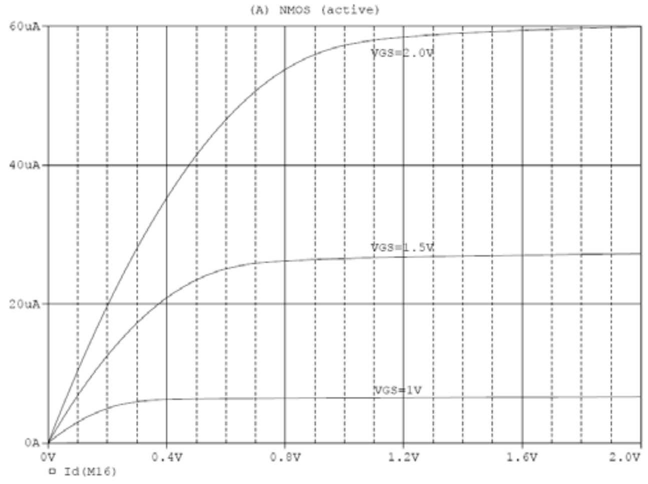


Fig. 4-8 Output Characteristics of an NMOS Transistor in Sensor Cell

4.3.2 NMOS Current Mirror Cell

The schematic of the NMOS current mirror stress sensor cell used in this study is shown in Fig. 4-9, and the layout for this cell with transistors of channel length $L \approx 4.5\mu m$ and channel width $W \approx 6.5\mu m$ is shown in

Fig. 4-10 (a). Once again, symbols “D1” and “D2” indicate the terminals for currents I_{out1} and I_{out2} . Transistors Ms1 and Ms3 are oriented at -45o, while Transistors Ms2 and Ms4 are oriented at 45o relative to the x_1' axis which is in the $[110]$ direction. The response of the sensor cell to the normal stress difference is described in Eq.(2.29), and can here be rewritten as

$$\frac{\Delta I_{out2}}{I_{out2}} - \frac{\Delta I_{out1}}{I_{out1}} = -2(\Pi^{n}_{11} - \Pi^{n}_{12})\sigma'_{12} = -2\Pi^{n}_{D}\sigma'_{12} \qquad (4.16)$$

Fig. 4-10 (b) shows a theoretical plot of output versus shear stress with a piezoresistive coefficient $-2\Pi^{n}_{D} = 1500(TPa)^{-1}$.

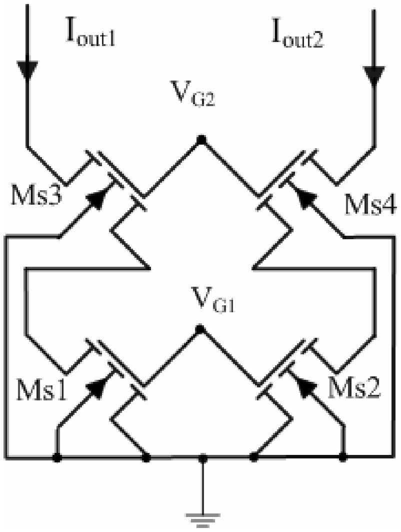
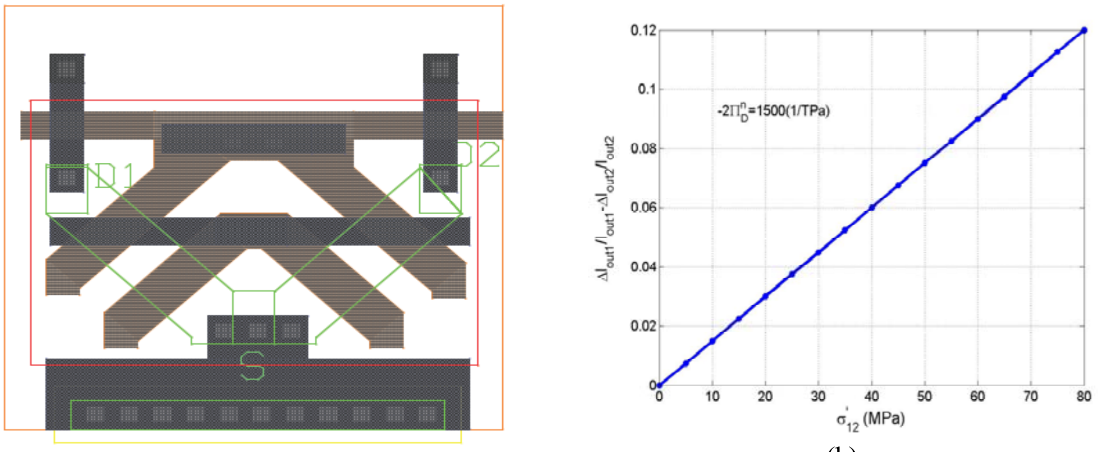


Fig. 4-9 Schematic of Shear Stress Sensitive NMOS Current Mirror Cell



(a)

(b)

Fig. 4-10 (a) Layout of Shear Stress Sensitive NMOS Current Mirror Cell; (b) Sample Plot of Output versus Shear Stress

4.3 Subtraction Circuit

An on-chip subtraction circuit was built so that any differences in the current can be measured directly. The schematic of the subtraction circuit is shown in Fig. 4-11. This subtraction circuit is composed of a cascode current mirror with four transistors placed close to each other and in the same orientation; hence the mismatch here is minimized. When two currents I_1 and I_2 are injected into the circuit, as in Fig. 4-11, the current I_1 is copied and drains the same amount of current from the output node, while the current I_2 is injected into the output node directly. In the equilibrium state, the voltage at the output node remains constant and the output current is equal to the difference of the two injected currents. The cascode current mirror is used here in order to eliminate possible errors that may be introduced by differences in the drain voltages.

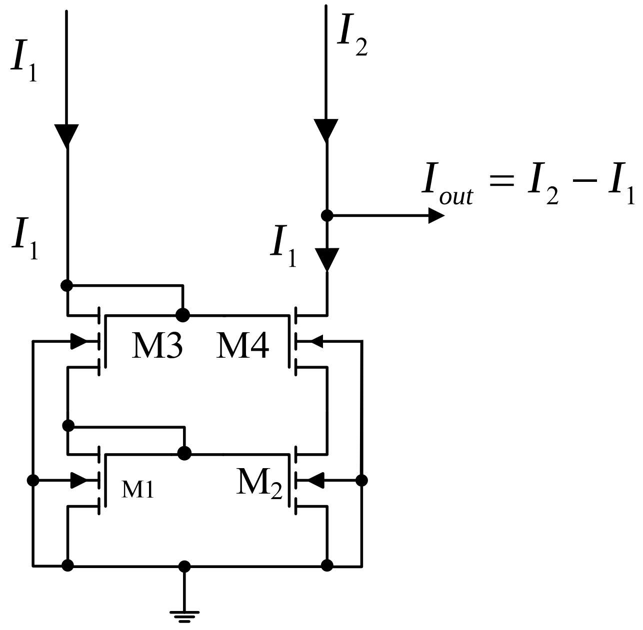


Fig. 4-11 Schematic of the Subtraction Circuit

4.4 Biasing Schematic and Array Design

4.4.1 PMOS Sensor Array

A PMOS sensor cell with biasing, subtraction and output circuitry is shown in Fig. 4-12. Everything in the dashed box represents a complete sensor cell. The five terminals are VDD, GND, Bias Current, Current Output and Current Difference Output. The PMOS sensor cell is composed of the four transistors in the crosshatched area, which is repeated 256 times to form the PMOS sensor array. The bias circuit is formed by the transistors Mb1 and Mb2, and shared by the cells in each row, so all the sensors in the same row are biased with the same gate voltages. The output current I_{out} is mirrored out by transistors Mo1 and Mo2. The subtraction circuit is composed of transistors M1-4, which provide the output of the current difference.

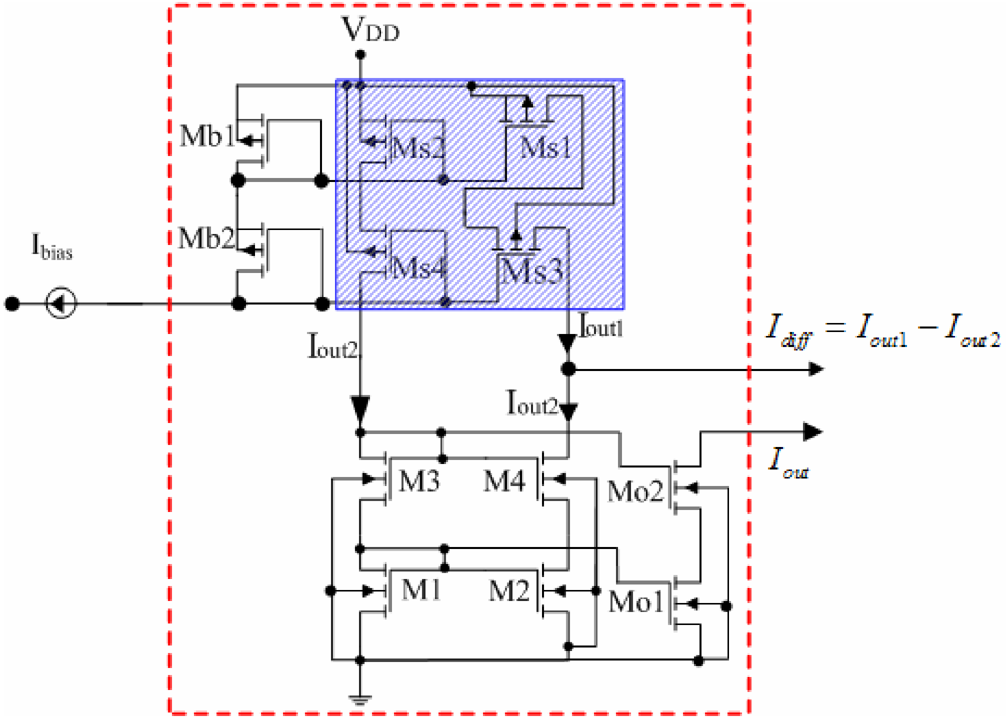


Fig. 4-12 PMOS Sensor Cell with Biasing, Subtraction and Output Circuitry

4.4.2 NMOS Sensor Array

Fig. 4-13 shows the NMOS sensor cell with biasing, subtraction and output circuitry. Again, everything in the dashed box can be regarded as part of the sensor. Applying a DC voltage VDD and a bias current I_{bias}, the current output and current difference output can be measured. As with the PMOS array, the current mirror type sensor cell in the crosshatched area of the figure is repeated 256 times to form the NMOS sensor array. The bias circuit is shared in each row and the subtraction circuit is shared by the sensors of the entire array.

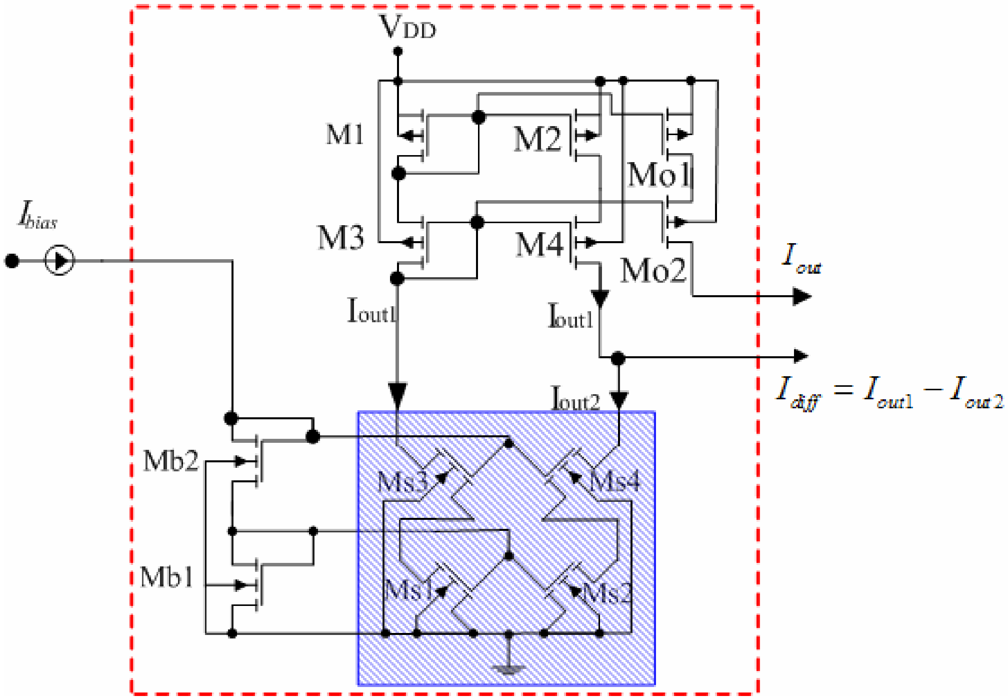


Fig. 4-13 NMOS Sensor Cell with Biasing, Subtraction and Output Circuitry

4.5 Multiplexer Schematic

4.5.1 NFET in Deep Triode Region

For an NMOS transistor, when $V_{GS} - V_{TH} > V_{DS}$, the transistor is operating in the linear region (or triode region) and the drain current can be expressed as

$$
\begin{aligned}
I_{DS} &= \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})[(V_{GS}-V_{TH})V_{DS}-\frac{1}{2}V_{DS}^2] \\
&= \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})[(V_{GS}-V_{TH})-\frac{1}{2}V_{DS}]V_{DS}
\end{aligned}
\tag{4.17}
$$

When $V_{GS}-V_{TH} >> V_{DS}$, the transistor is operating in the deep triode region, and Eq. (4.17) can be simplified to

$$
I_{DS} = \frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS}-V_{TH})V_{DS} \tag{4.18}
$$

The transistor works as a resistor, and its on-resistance can be written as

$$
R_{on} \cong \frac{V_{DS}}{I_{DS}} = \frac{1}{\frac{1}{2}\mu_n C_{ox}(\frac{W}{L})(V_{GS}-V_{TH})} \tag{4.19}
$$

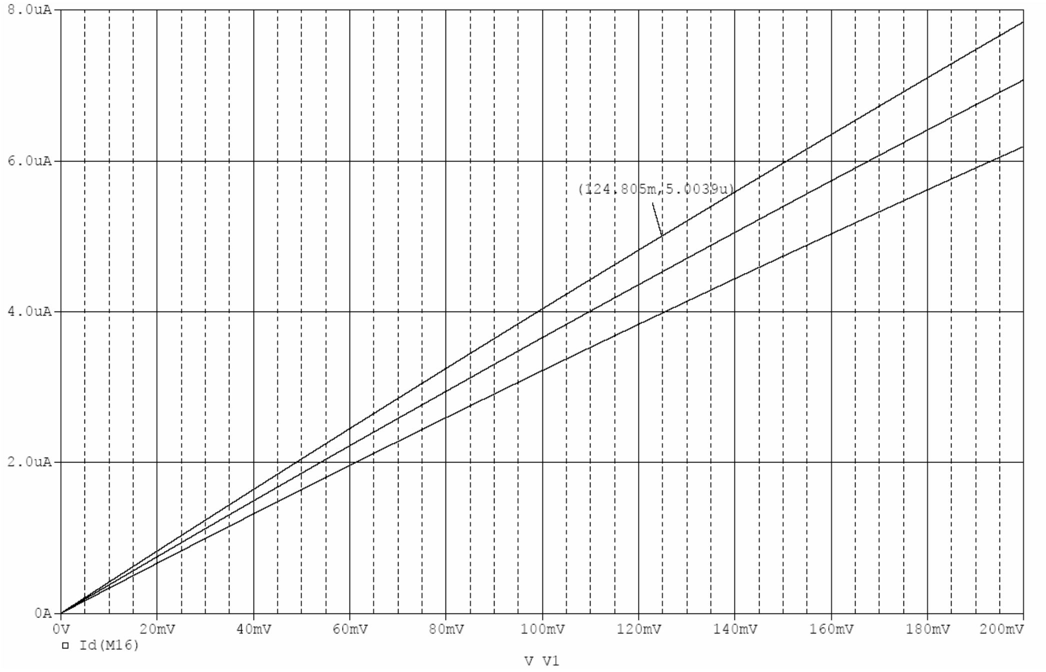


Fig. 4-14 Output Characteristics of NMOS Transistor in Deep Triode Region

The NMOS transistors can be used as switches, with control signals being applied to the gate to drive the transistor into the 'OFF' state (cut-off region) or 'ON' state (deep triode region). The family of logic circuits based on this principle is called pass transistor logic. An NMOS transistor with W/L=$1.6\mu m / 1.6\mu m$, and V_{GS} at 3V, 3.5V and 4V was simulated by PSPICE, and the results are plotted in Fig. 4-14. The plot shows a very linear relationship, with a resistance of 24.96 kΩ when V_{GS} is 4V.

4.5.2 NMOS Pass-transistor Multiplexer

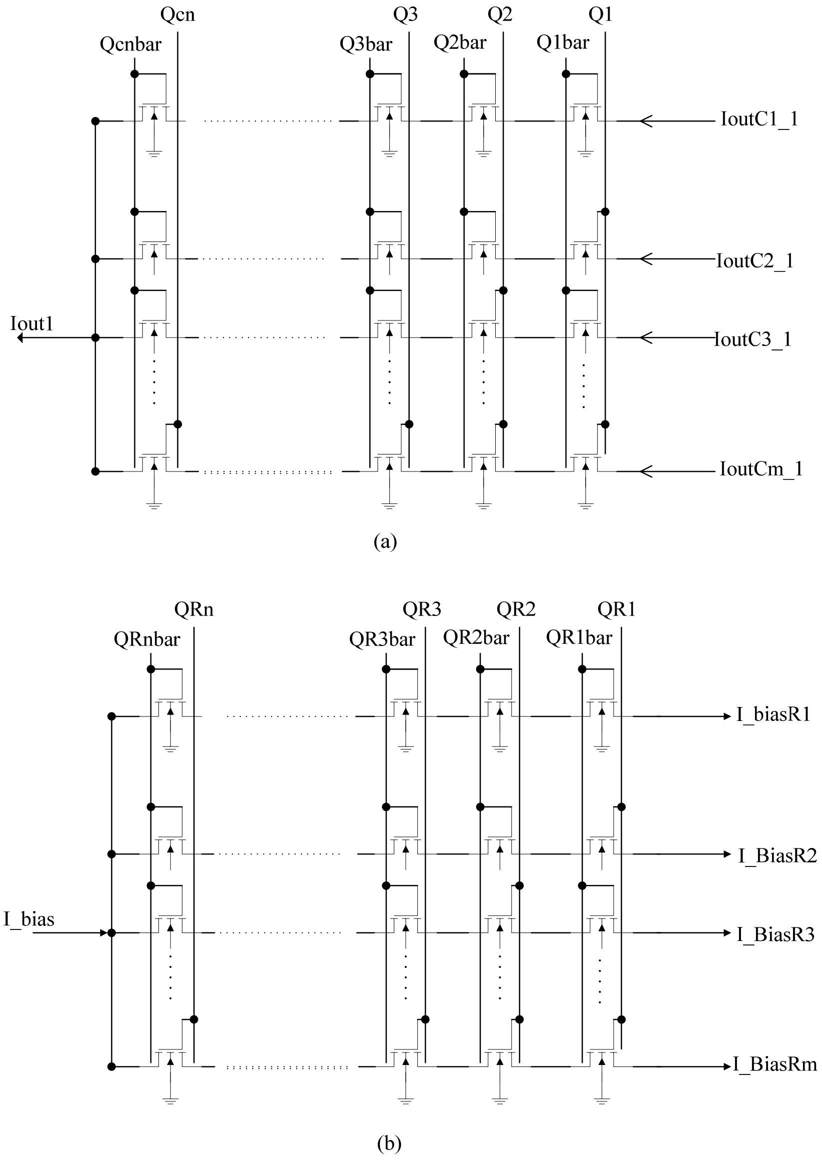


Fig. 4-15 Pass-transistor Multiplexers: (a) Column Select; (b) Row Select

Pass-transistor multiplexers are used in this design to selectively bias a row of sensors and to select a column as an output. Fig. 4-15 shows a row and column selection multiplexers based on pass transistors. Here, the row select multiplexer is 4-bit and the column select multiplexer is 5-bit, which means that the maximum transistor path is 5 transistors. Unit transistors with W/L=1.6um/1.6um are used, for a control signal of 4V; the on-resistance for one transistor is about 25 kΩ by Eq. (4.19). If a current of $5\mu A$ passes through the column selection multiplexer, the total voltage drop is about 0.625V. Thus, the voltage at the output node should be biased at least two overdrive voltages higher than this value in order to keep the stress sensitive transistor working in the saturation region. The voltage drop on the row selection multiplexer is not a concern because the current is biased by a current source which will adjust the voltage as necessary to maintain the current at the set point, which is $5\mu A$ here.

4.6 Counter for Sensor Scan

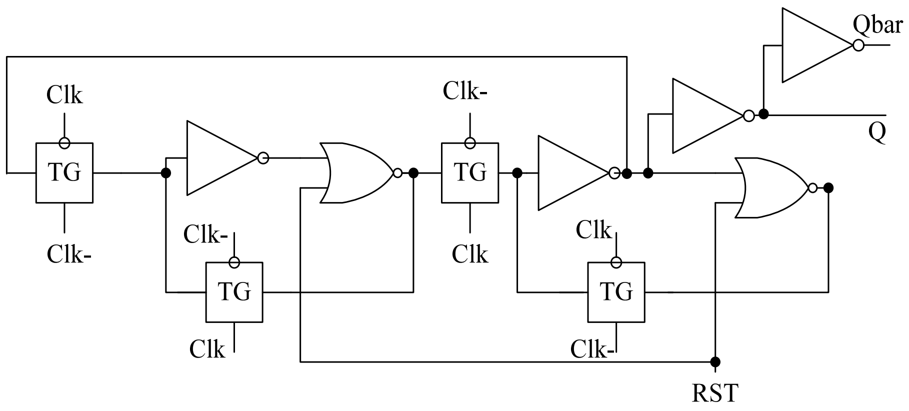
A counter was included in this design in order to generate a control signal to scan the sensors in arrays automatically and thus simplify the measurement procedure and save output pins. A ripple counter constructed from master-slave toggle flip-flops (T-FF) was used here, as shown in Fig. 4-16.

4.6.1 Master-slave T flip-flop

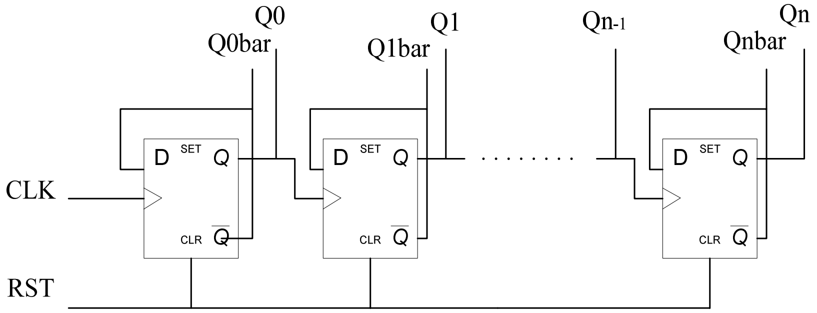
The schematic of a T-flip-flop with reset is shown in Fig. 4-16 (a) CMOS gates and transmission gates are involved. The T-FF is controlled by a complimentary clock signal. The output signal is buffered before it is sent out to drive the multiplexers.

4.6.2 Ripple Counter

A ripple counter is used in this design because the speed is not critical for this application. The schematic is shown in Fig. 4-16(b). When the reset signal RST is released, all outputs will be set to ‘1’. Then it counts down from all ones to all zeros and repeats continuously.



(a) T_FF



(b) Counter

Fig. 4-16 Schematic of an M-S T-flip-flop and a Ripple Counter

4.7 Estimated Minimum Chip Operating Voltage

As described in section 4.5, the power supply voltage for the sensor array should be high enough in order to assure the sensors to work in saturation region with relative high overdrive voltage. PSPICE was used to estimate the minimum voltage required for the chip. When external input current of 5μA is used to generate bias current for the sensor, the actual bias current for the sensors in NMOS array is about 2.7μA, and in PMOS array is about 5.1μA in this design. The row select multiplexer is in the path driven by the external current source and does not influence the work condition of the circuit, so it is ignored in the simulation. A fixed mismatch of approximately

3% is set by introducing a mismatch in W/L ratio. The schematics used to determine the minimum operating voltage in order to keep transistors working in saturation region are plotted in Fig. 4-17 for PMOS array and Fig. 4-19 for NMOS array. The output versus operating voltage for PMOS array is shown in Fig. 4-18, which indicates that the minimum operating voltage required is 5.7 V in order to make the output insensitive to the operating voltage. Similarly, the minimum operating voltage for NMOS array is determined by Fig. 4-20 as 4.5V. Thus, In order to make both NMOS array and PMOS array working properly, the minimum voltage required is 5.7V. The power supply of 6V was used in actual experiments for this project.

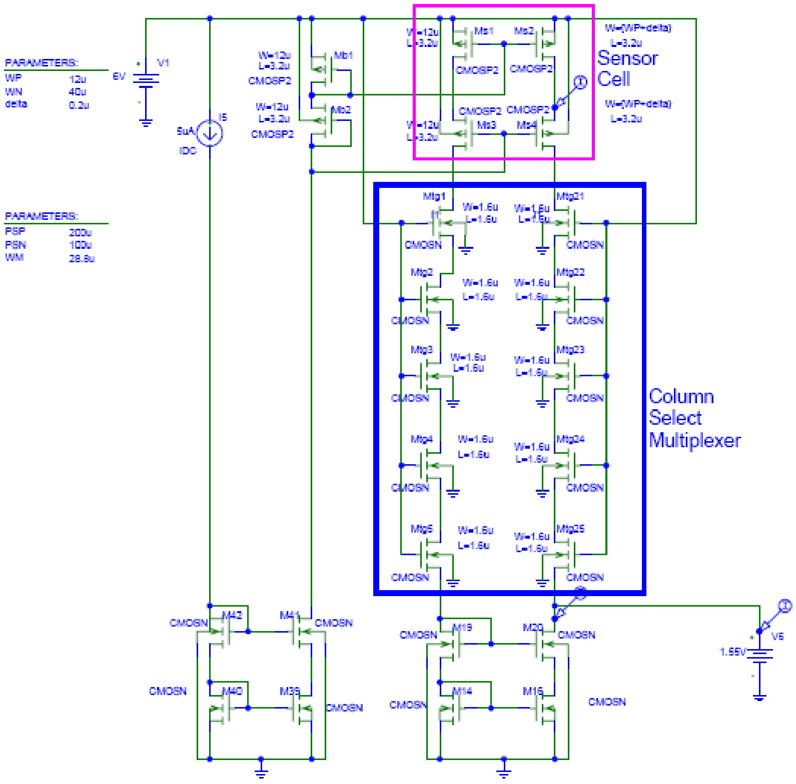


Fig. 4-17 Schematic to Estimate Operating Voltage for PMOS Array

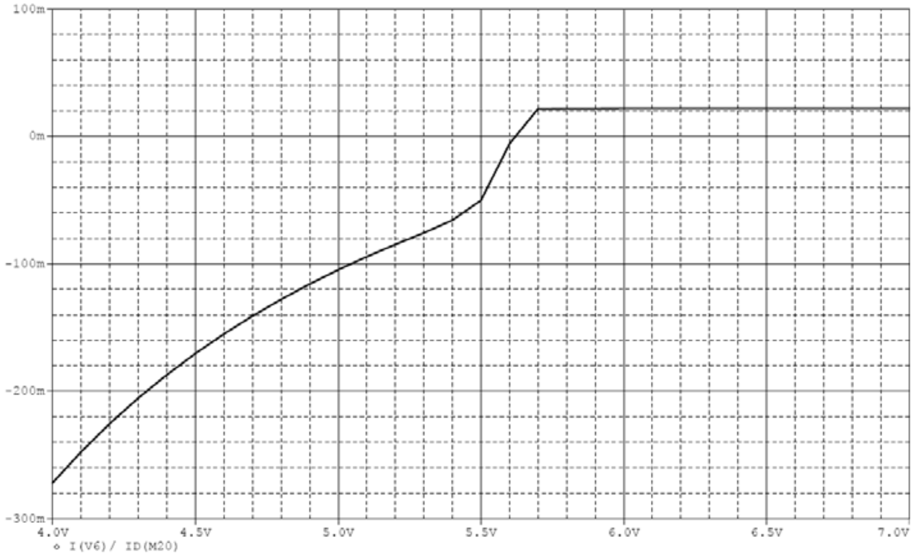


Fig. 4-18 PMOS Array Output versus Operating Voltage for a Fixed Mismatch

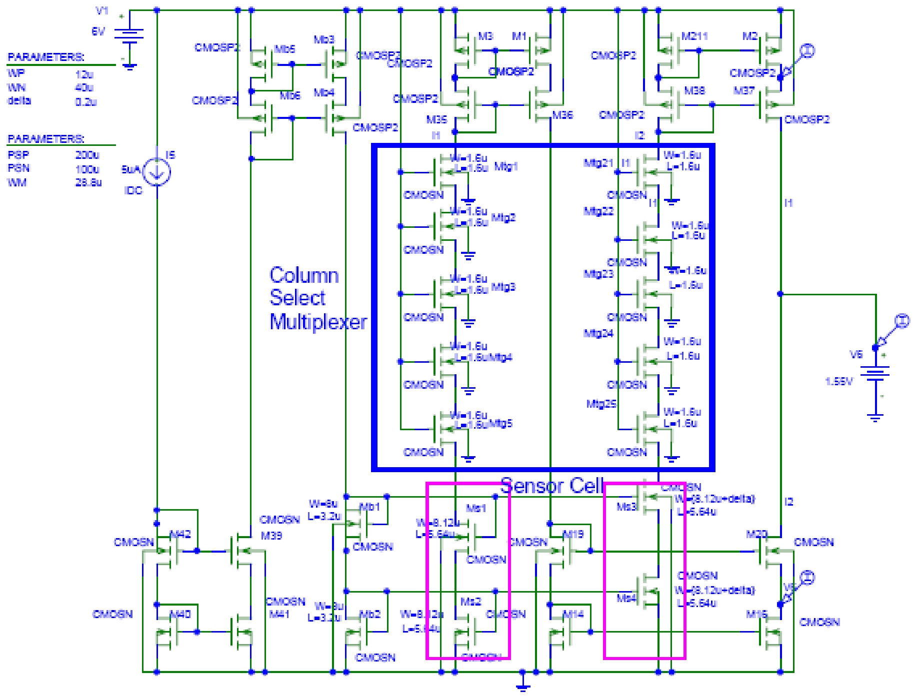


Fig. 4-19 Schematic to Estimate Operating Voltage for NMOS Array

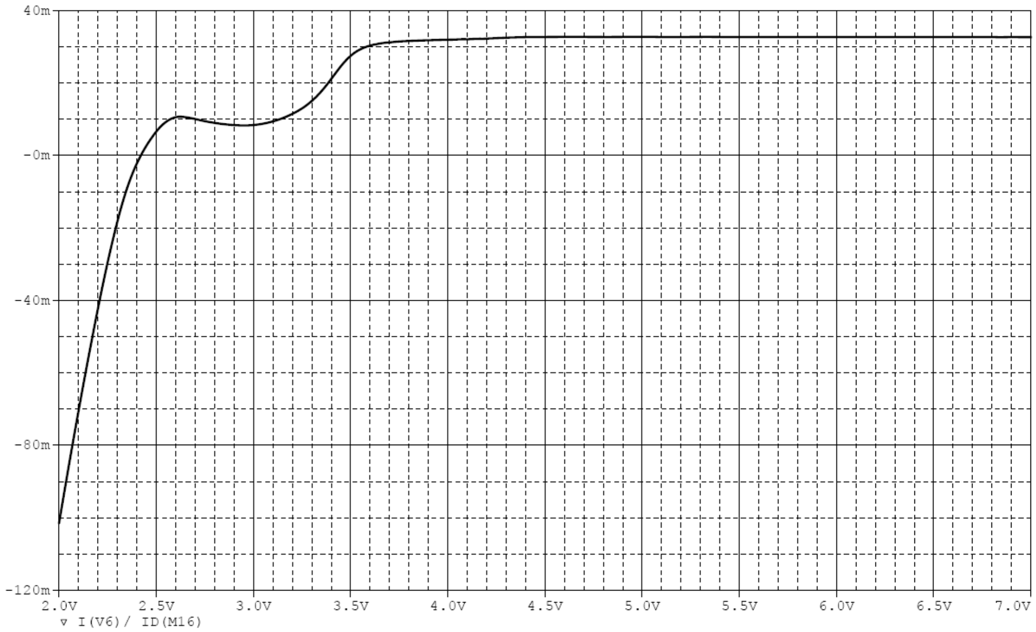


Fig. 4-20 NMOS Array Output versus Operating Voltage for a Fixed Mismatch

4.8 System Schematic

The system is organized as shown in Fig. 4-21 and Fig. 4-22. The bias circuit and subtraction circuit in the dashed-line boxes are shared by two arrays. Bias circuits and sensor cells for each array are shown in the respective figures. For the entire circuit to work, only one single power supply, one biasing current and one clock signal are needed, and two outputs can be measured. The row select multiplexers are implemented in a 4-bit 1-to-16 configuration and the column select multiplexers are in a 5-bit 32-to-1 configuration. Because each sensor array is composed of 16×16 sensors, only a 4-bit column select multiplexer is needed for each array and the extra bit of the column select multiplexer can be used as an array selector. A 9-bit counter with reset is sufficient to access every sensor in both arrays.

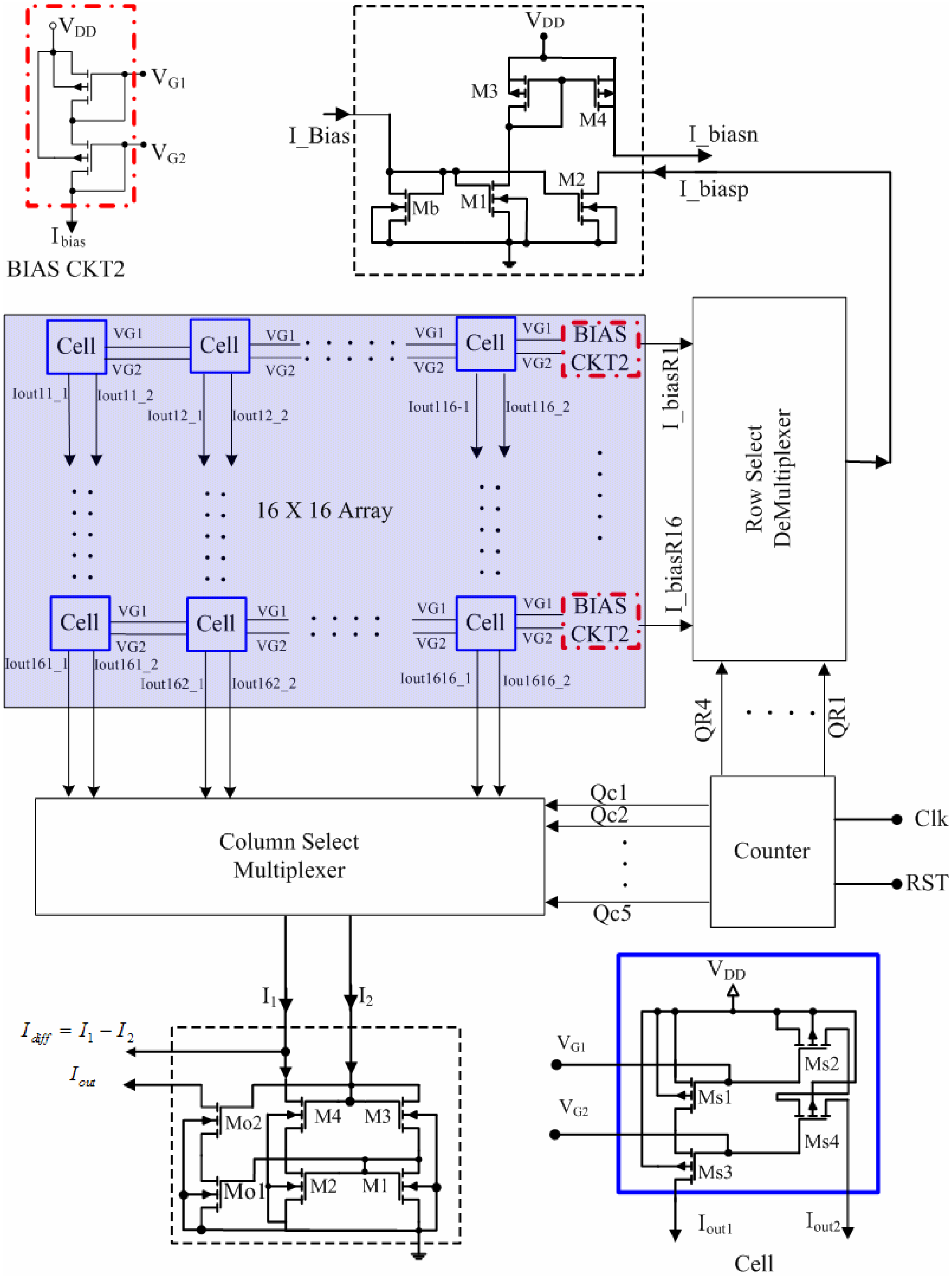


Fig. 4-21 System Schematic for PMOS Sensor Array

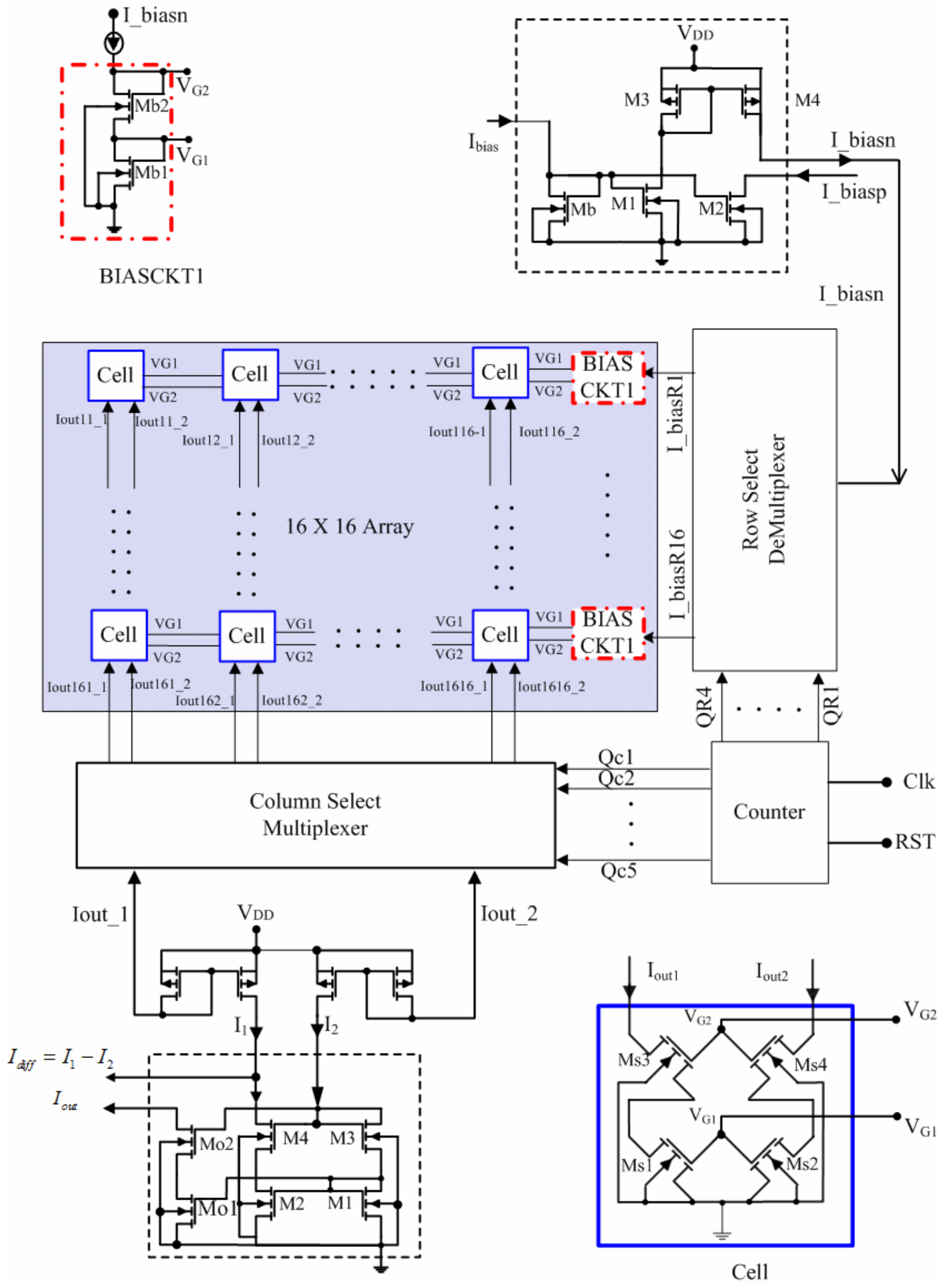


Fig. 4-22 System Schematic for NMOS Sensor Array

4.9 Chip Layout

Two designs are implemented in this work. The first is designed with a five-bit counter only to scan sensors in each row and column select are defined externally, and the other is designed with a nine-bit counter to scan every sensor in both NMOS and PMOS arrays automatically. The sensor array designs are the same for the two chips. With a subtraction circuit the current difference can be measured directly from the output, and two pins are used for outputs I_{diff} and I_{out}. The chips #1 (‘AU1’) are sensor arrays that include a five-bit counter for row selection, while the chips #2 (‘AU12’) have a built-in nine-bit counter for both row and column selection. Both sets of chips were fabricated using MOSIS AMI_ABN15 (feather size 1.5um) technology.

The pictures shown in Fig. 4-23 and Fig. 4-24 are taken from actual chips. One chip includes only a five-bit counter for row scan and the other chip includes a nine-bit counter to scan both row and column automatically. The function of each part is marked on the picture in Fig. 4-23 as an example.

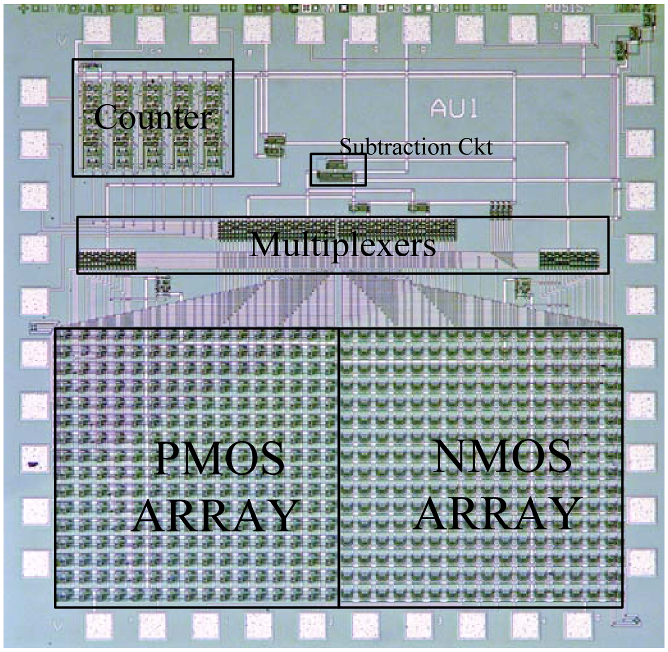


Fig. 4-23 Picture of Sensor Array Chip with a 5-bit Counter for Row Scan

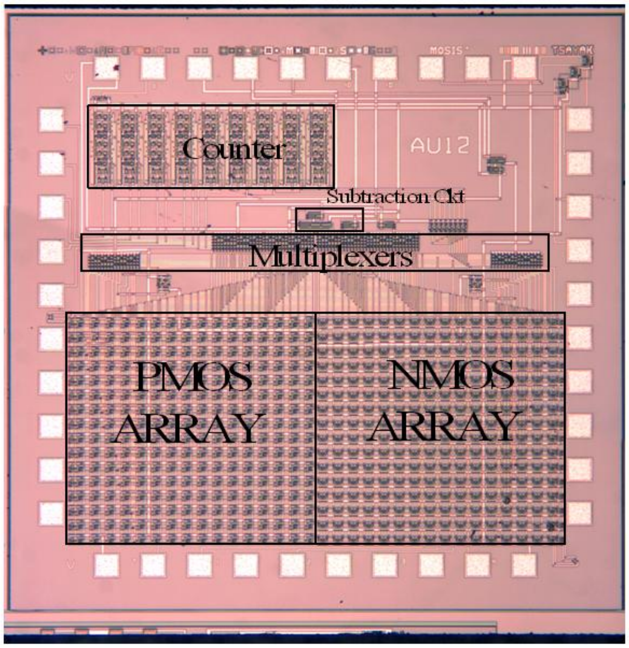


Fig. 4-24 Picture of Sensor Array Chip with 9-bit Counter for Row and Column Scan

CHAPTER 5. CHARACTERIZATION AND RESULTS

Chip-on-beam technology was used in this study to characterize the sensors. This characterization process employs a four-point-bending fixture (4PB), a PCB beam on which the chip is mounted, an HP 4155 semiconductor parameter analyzer, ANSYS simulation, DC power supply, and square wave generator. The basic calibration steps follow the procedure described in [136, 137]. The characterization flow chart for this work is shown in Fig. 5-1.

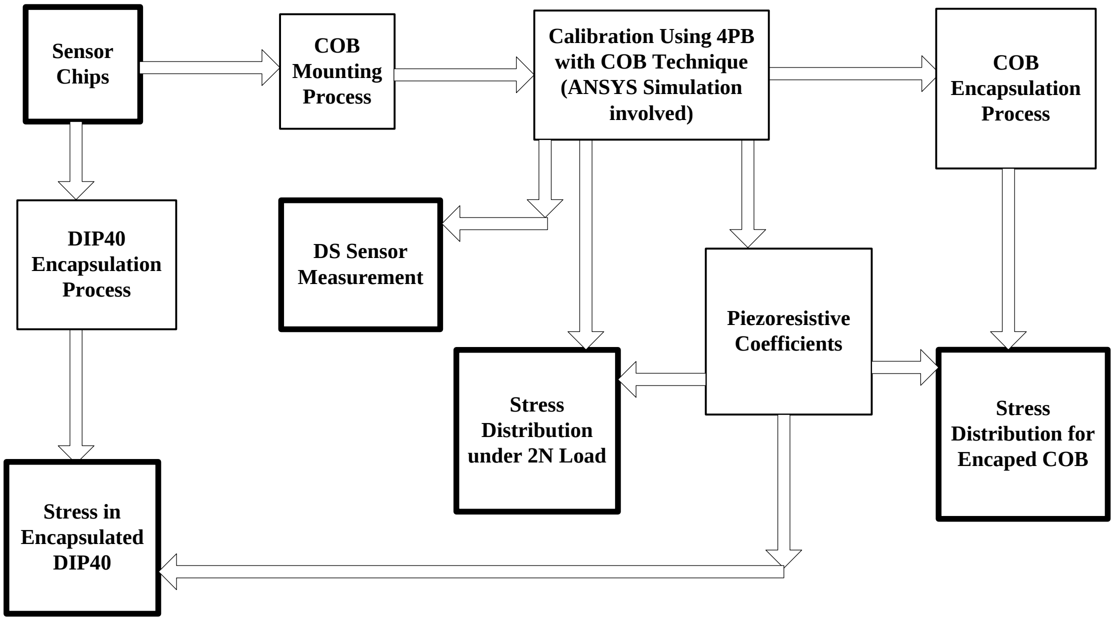


Fig. 5-1 Sensor Characterization Flow Chart

5.1 Experimental Setting

5.1.1 Four-point Bending Fixture

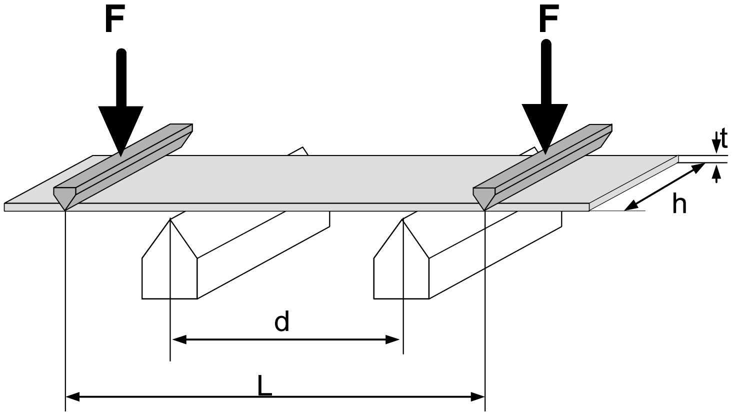


Fig. 5-2 Idealized Representation of a Four-Point-Bending Loading Fixture

A four-point-bending fixture is used to apply a known uniaxial stress to a silicon wafer strip with stress sensors integrated in it [138]. An idealized representation of a 4PB loading fixture is shown in Fig. 5-2. Using the classic strength of materials beam theory, it can be shown that a uniaxial stress σ is developed on the surface of the strip according to

$$\sigma = \frac{3F(L-d)}{t^2 h} \tag{5.1}$$

where ***F*** is the vertical force applied to the strip on the 4PB fixture, ***t*** is the thickness of the strip, ***L*** is the distance between the two outer points, ***d*** is the distance between the two inner supports, and ***h*** is the width of the silicon strip. This formula is accurate if the beam is not significantly deformed due to the applied forces, and dimensions ***t*** and ***h*** are small compared to ***d*** and ***L***. It was verified by three-dimensional finite element simulation using eight-node iso-parametric brick elements that the axial normal stress on the surface is constant between the two supports and that the transverse normal stress is virtually zero in those regions of the strip where the axial normal stress is uniform [138]. Also, the value of the constant axial stress is well predicted by Eq. (5.1).

5.1.2 Characterization System Setup for Sensor Array

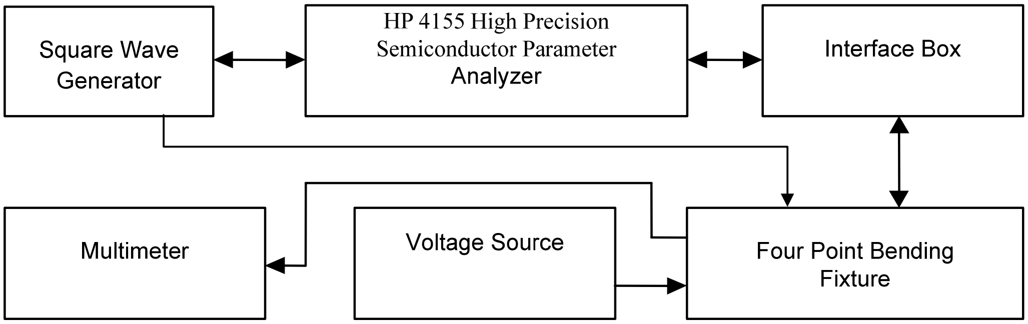


Fig. 5-3 Characterization System Setup for Sensor Array

The setup for the sensor characterization is shown in Fig. 5-3. In addition to the four-point-bending fixture, an HP4155 high precision semiconductor parameter analyzer is used to measure and collect data. This is connected to the 4PB fixture through an interface box, and a wave form generator is connected to the clock pin on the chip. A voltage source provides DC voltage to the chip and the load cell on the 4PB fixture, and a multi-meter is used to measure the output of the load cell in order to determine the force applied to the strip (or beam). The sensor response to the applied force is obtained by the measurements taken using this setup. If sensors are fabricated on the strip, the corresponding stress can be calculated using Eq. (5.1). If sensors are fabricated on a chip, and the chip is mounted on the beam, the stress on the chip surface corresponding to a given load becomes complicated and needs to be determined using finite element analysis (FEA), which will be described in Section 5.3.

5.1.3 Characterization System Setup for DSM Sensor

The characterization system setup for the DSM stress sensor is shown in Fig. 5-4. As with the setup for the sensor array 4PB fixture used to apply stresses to the chip-on-beam sample, a counter is used to measure the duty cycle or frequency ratio of the output signal to the clock under stress. Alternatively, a receiver can be used to measure the fundamental frequency of the output signal versus stress. The dashed line between the 4PB fixture and receiver indicates a wireless connection.

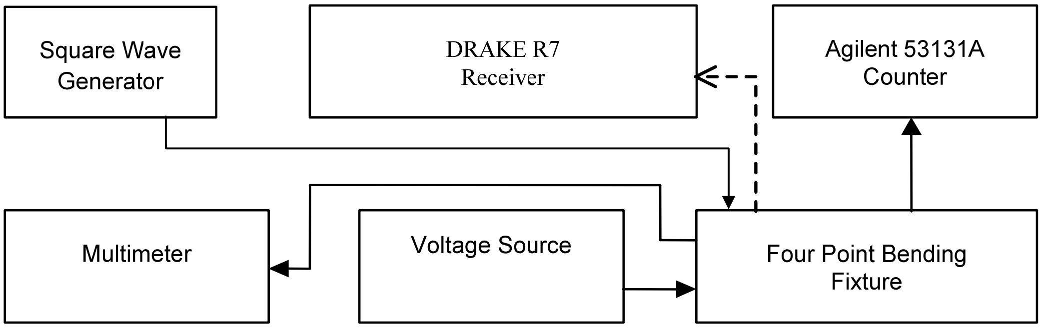


Fig. 5-4 Characterization System Setup for DSM Stress Sensor

5.2 Stress-Free Initial Results

Due to the mismatches of the transistors in sensor cells and bias circuits, some variations in the initial bias current and output from the sensor cells exist avoidably. This subsection shows the variations of bias current variation and sensor output variation when the die is in a stress-free state.

5.2.1 Stress-Free Bias Current Variation

5.2.1.1PMOS Array Stress-free Bias Current Distribution

The bias currents are measured before any load is applied. Fig. 5-5 shows bias current plotted on chip surface occupied by the PMOS sensor array, where each block represents the bias current for the sensor on the location respectively. Fig. 5-6 shows a histogram plot of bias current for a PMOS sensor array, the mean of the bias current is 5.169 μA with the standard deviation is 0.116 μA, or the relative variation is about 2.3%.

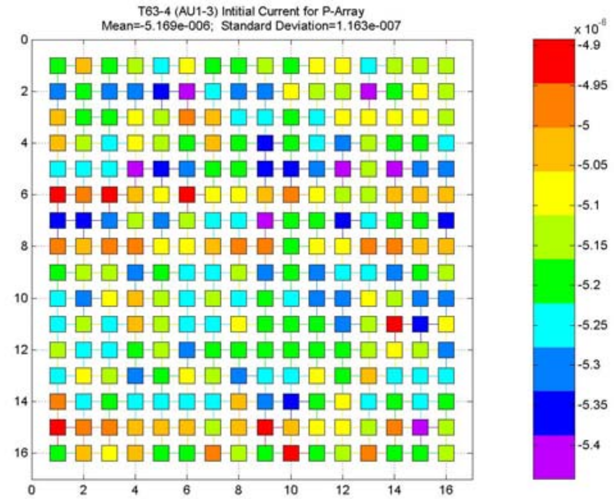


Fig. 5-5 Map of Stress-free Initial Bias Current for PMOS Sensor Array

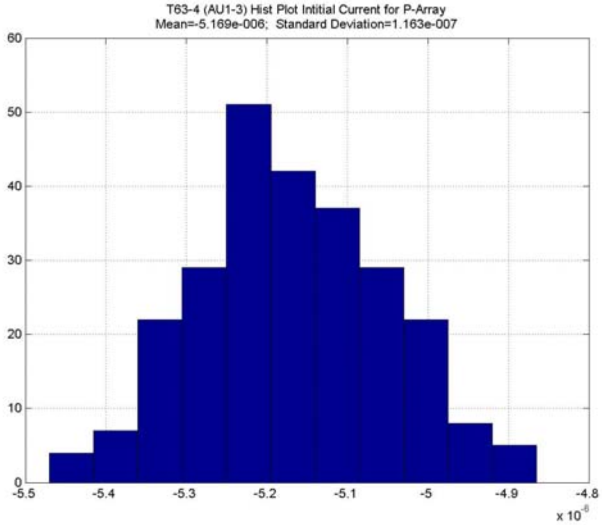


Fig. 5-6 Histogram Plot of Stress-free Initial Bias Current for PMOS Sensor Array

5.2.1.2 NMOS Array Stress-free Bias Current Distribution

Similar to the bias current for PMOS array, Fig. 5-7 and Fig. 5-8 show a map on chip and a histogram plot of stress-free bias current for each sensor cell in a NMOS sensor array, the mean of the bias current is 2.634 μA with the standard deviation is 0.0737 μA, or the relative variation is about 2.8%.

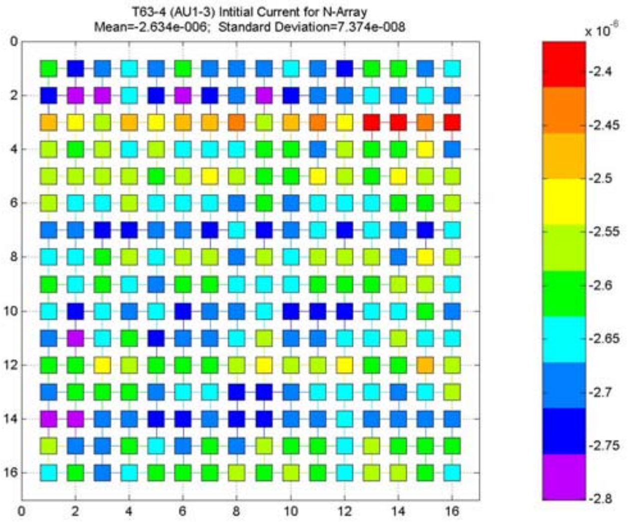


Fig. 5-7 Map of Stress-free Initial Bias Current for NMOS Sensor Array

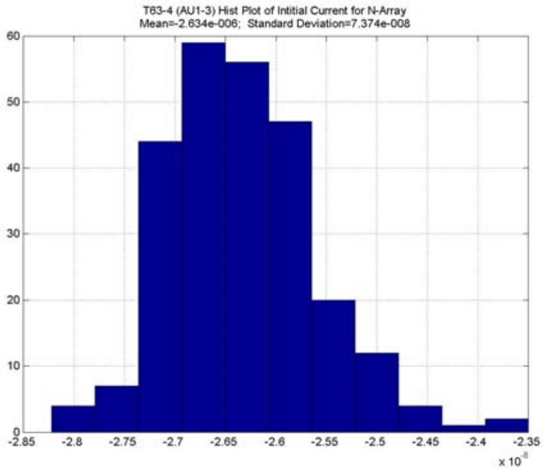


Fig. 5-8 Histogram Plot of Stress-free Initial Bias Current for PMOS Sensor Array

5.2.2 Stress-Free Sensor Output Variation

5.2.2.1 PMOS Array Stress-free Output Distribution

Ideally the output current for a sensor cell under stress-free condition is zero, mismatch always exits in reality. The output current form each sensor cell respect the initial mismatch between the transistor pairs in the sensor cell under the actual bias current. Fig. 5-9 and Fig. 5-10 show the distribution of the stress-free initial output current due to the initial mismatch in a PMOS array and corresponding histogram plot, the mean of the mismatch current is -0.0153 μA and the standard deviation is 0.0268 μA.

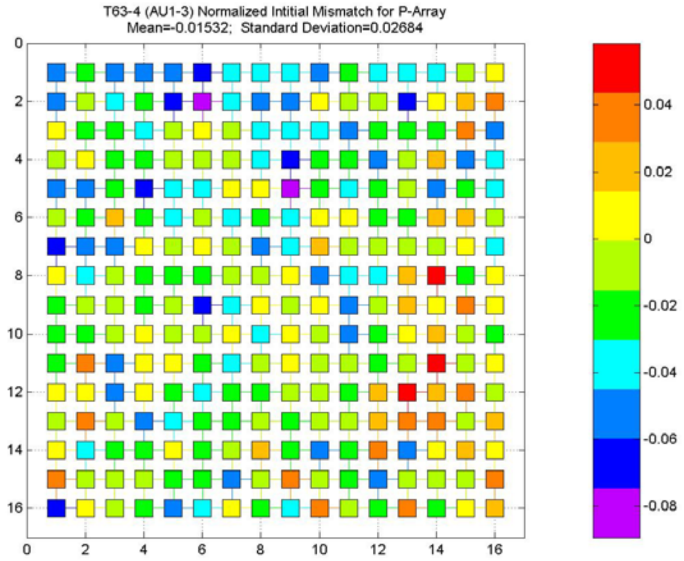


Fig. 5-9 Map of Stress-free Initial Mismatch Current for PMOS Sensor Array

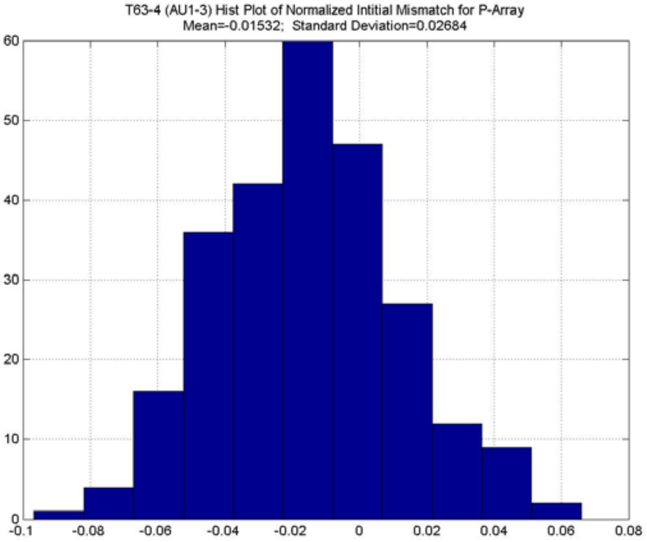


Fig. 5-10 Histogram Plot of Stress-free Initial Mismatch Current for PMOS Sensor Array

5.2.2.2 NMOS Array Stress-free Output Distribution

The distribution of the stress-free initial output current due to the initial mismatch in a NMOS array and corresponding histogram plot are shown in Fig. 5-11 and Fig. 5-12, where the mean of the mismatch current is 0.0145μA and the standard deviation is 0.0215μA.

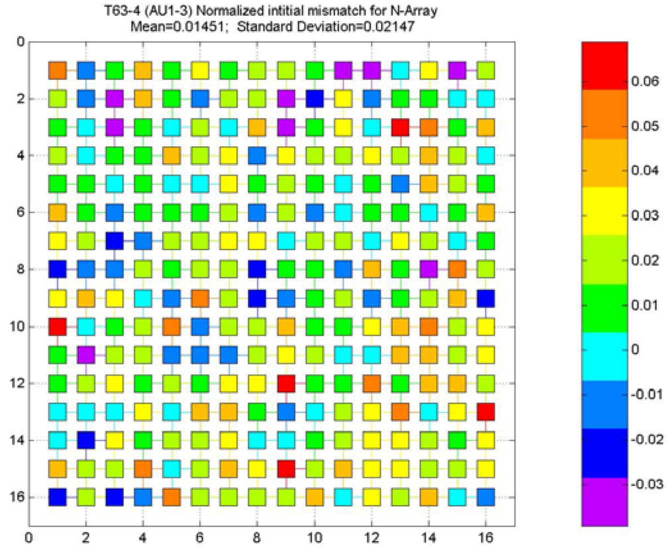


Fig. 5-11 Map of Stress-free Initial Mismatch Current for NMOS Sensor Array

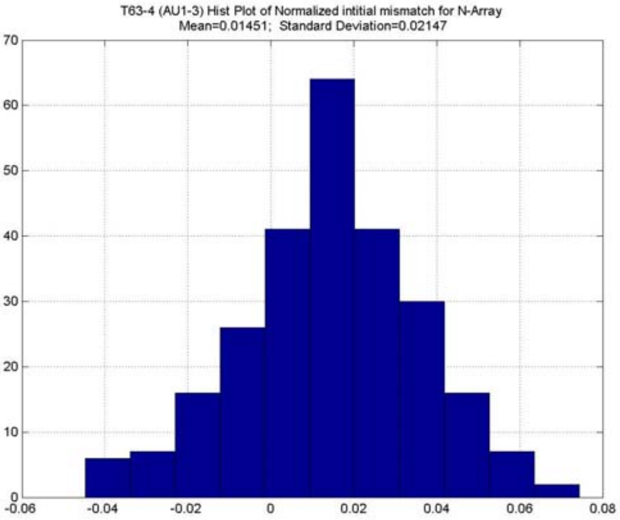


Fig. 5-12 Histogram Plot of Stress-free Initial Mismatch Current for NMOS Sensor Array

5.3 FEA Simulation for Stress Distribution

5.3.1 Die Stress for Chip-on-beam Sample

The sensors fabricated by MOSIS are only available in die form rather than the strips which are ideally used for stress experiments by 4PB. A PCB board is employed here to act both as a beam and a medium for connection. A die is mounted on the board with THERMOSET CircuitSAF™ ME525 underfill. The I/O pads of the die are then wire bonded to the board and the wires are soldered out from the pads on the board to make connections for measurement. Using this type of wiring connections offers advantages as it eliminates the possible stress introduced by probes and also makes good connections. The set up of a chip-on-beam sample in 4PB fixture is shown in Fig. 5-14.

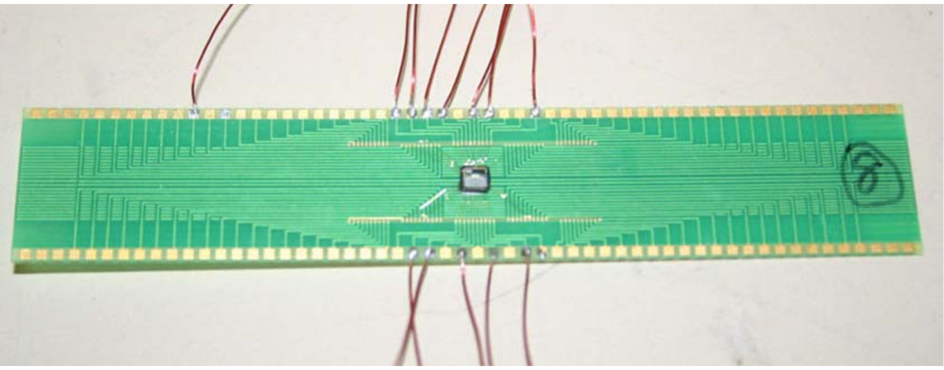


Fig. 5-13 Photograph of a Chip-on-Beam Sample

Table 5-1 Material Properties Used in ANSYS Simulation

Materials	Young's Modulus (GPa)	Poisson's Ratio	CTE (alpha1) (ppm/K)
Silicon	169	0.262	2.6
PCB (FR-406)	23.73	0.17	13
ME525	10.43	0.3	25
Ceramic	172	0.21	8.2

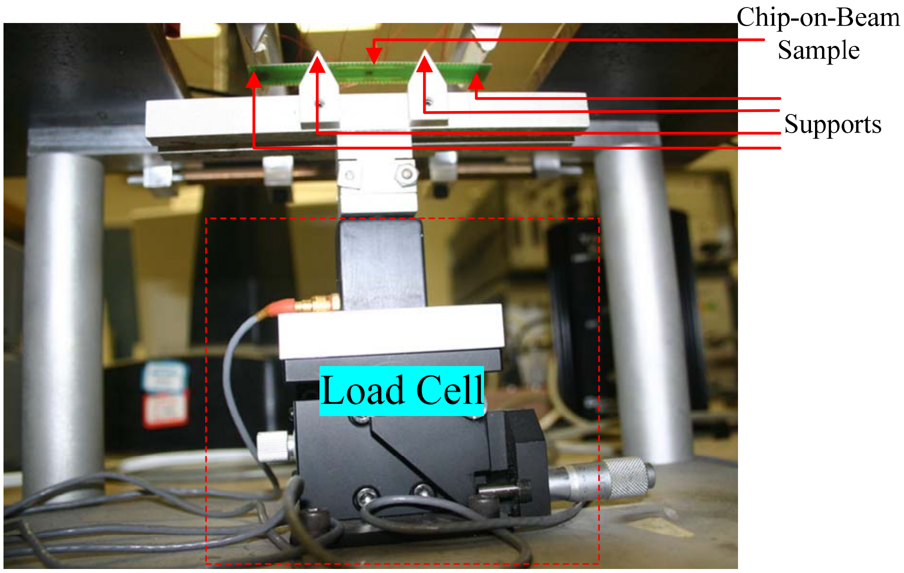
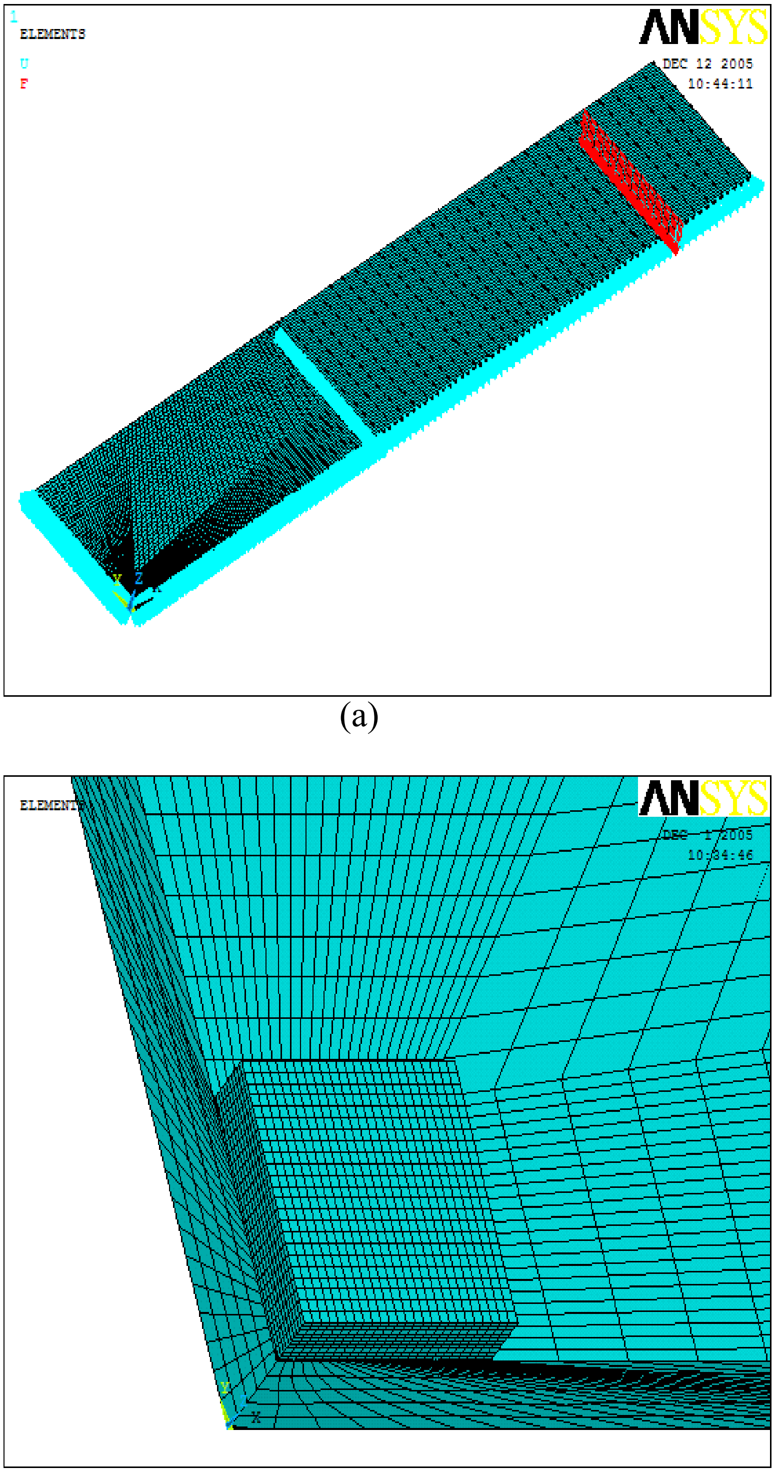


Fig. 5-14 Photograph of a Chip-on-Beam Sample in the 4PB fixture

ANSYS 9.0 was used to perform the finite element simulation in this work. Due to the high degree of symmetry of the configuration used, a quarter model is built to simulate the stress corresponding to the load on the beam. The model, along with its boundary conditions and load, are shown in Fig. 5-15. A 20-node brick element is used here (Solid95 in ANSYS). The material properties for each of the components used in this model are listed in Table 5-1. The dimensions that correspond to the variables used in Fig. 5-13 are $L = 80mm$, $d = 36mm$, $t = 0.5758mm$, and $h = 16.51mm$. The actual dimensions of the tiny chip used are $2.505mm$ in length, $2.565mm$ in width and $0.306mm$ in thickness. The thickness of the underfill layer is $41\mu m$.

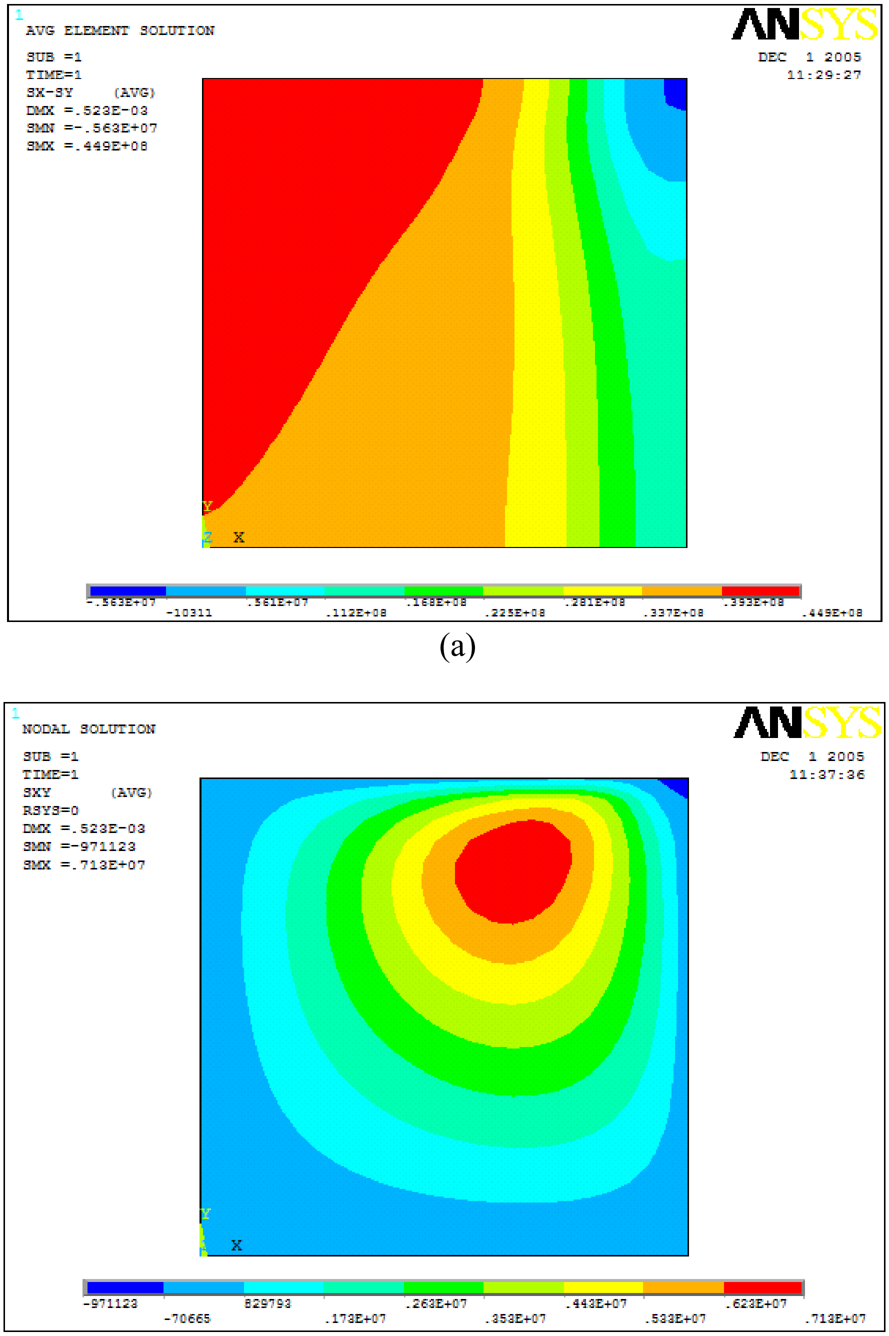
The simulation results are shown in Fig. 5-16. The chip shown represents only a quarter of the die; the lower left corner is actually the center of the chip and the upper right at the corner of the die. Fig. 5-16 (a) shows the in-plane normal stress difference on the die surface, and Fig. 5-16 (b) shows the in-plane shear stress on the die surface. These two stresses are the parameters that the sensors are designed to detect for this study.



(a)

(b)

Fig. 5-15 ANSYS Quarter Model for Chip-on-Beam



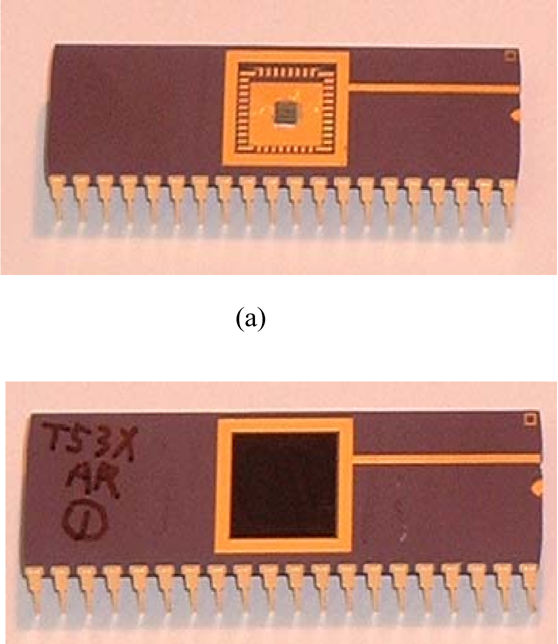
(a)

(b)

Fig. 5-16 ANSYS Quarter Model Simulation Results: (a) Normal Stress Difference on Chip, (b) In-plane Shear Stress on Chip (Lower Left is the Center of The Die)

5.3.2 Die Stress for DIP40 Encapsulated by ME525 Underfill

The DIP40 packages are supplied by MOSIS. The cavity is filled with ME525 underfill. The sample was heated to 95°C before the underfill was dispensed in the DIP40 package cavity, and after the underfill was filled the samples were cured in the box oven at 150°C for 30 minutes. The DIP40 package before and after encapsulated by ME525 are shown in Fig. 5-17. Due to the symmetry of the sample, only a quarter model is used here as in Fig. 5-18. Material properties used here are listed in Table 5-1 and Table 5-2. The curing temperature of 150°C is taken as the reference temperature, and the room temperature, 27°C, is used for final temperature. The die-attach material between the chip and the ceramic substrate is neglected. Due to the coefficients of thermal expansion (CTE) are different, when the package is cooled from 150°C to room temperature, stress will be generated. The simulated stresses on the die surface are plotted in Fig. 5-19.



(a)

(b)

Fig. 5-17 DIP40 Package before and after Encapsulated with ME525 Underfill

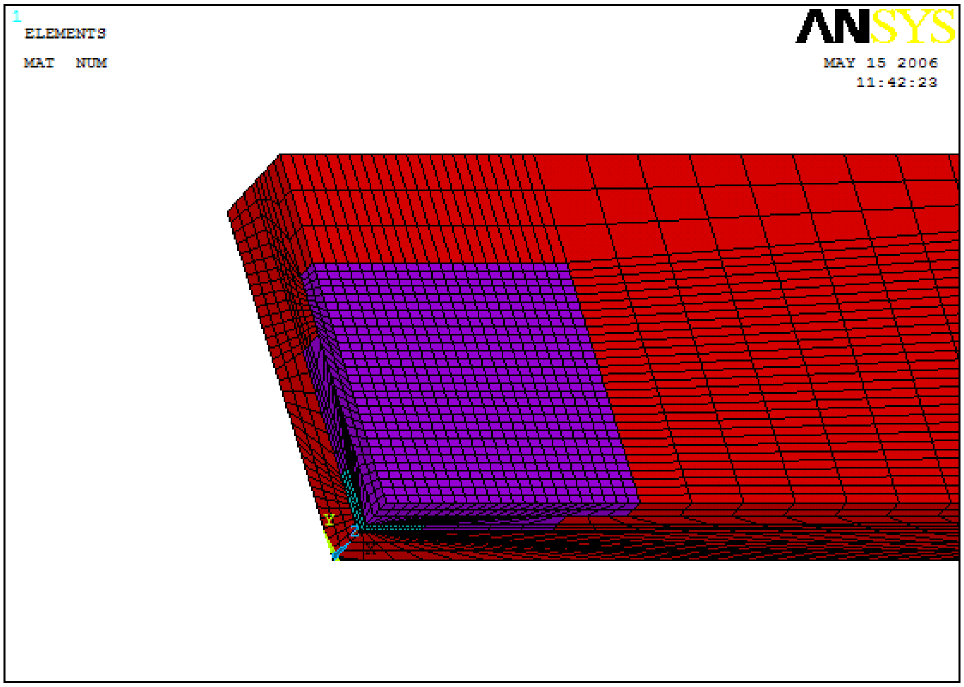
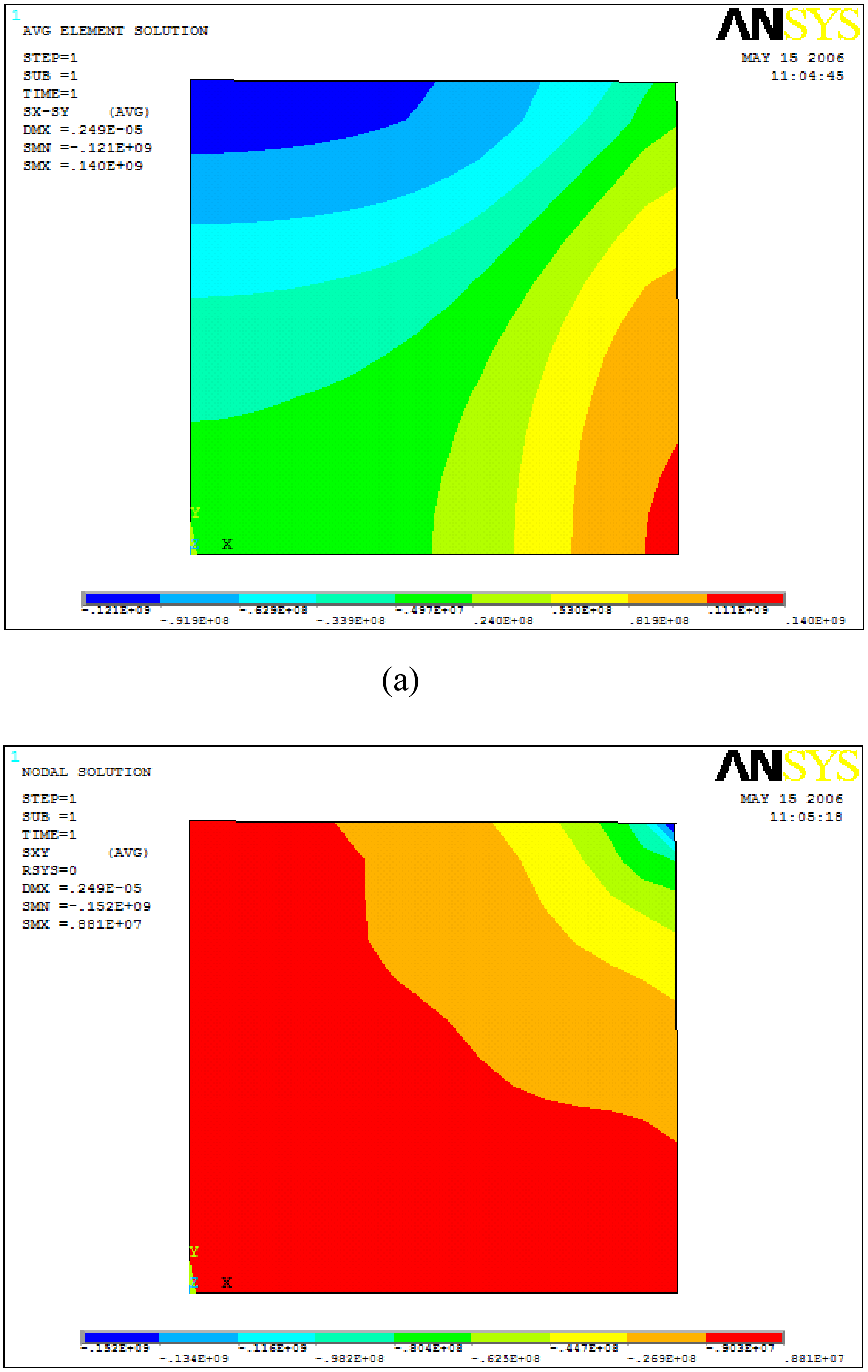


Fig. 5-18 Quarter Model for DIP40 Encapsulated with ME525

Table 5-2 Material Properties under Different Temperatures

T (^oC)	ME 525	Silicon[110]	FR-406
25.0	10.4	169.1	23.70
50	9.85	168.5	22.05
75	8.75	167.9	20.26
100	7.72	167.0	18.55
125	4.98	166.6	16.37
150	0.98	165.5	14.87



(a)

(b)

Fig. 5-19 Die Stress in DIP40 Encapsulated by ME525 Underfill: (a) In-plane Normal Stress Difference, (b) In-plane Shear Stress

5.3.3 Die Stress for Encapsulated Chip-on-beam Sample

Another setup for die surface stress testing in this work is take a chip-on-beam sample, as shown in Fig. 5-13, and encapsulated by ME525 underfill as shown in Fig. 5-20. Fig. 5-21 shows an ANSYS quarter model for the encapsulated chip-on-beam sample. Material properties used are listed in Table 5-1 and Table 5-2, the reference temperature is 150 ^{o}C which is the ME525 annealing temperature, and simulated normal stress difference and shear stress on the chip surface are plotted in Fig. 5-22 and Fig. 5-23.

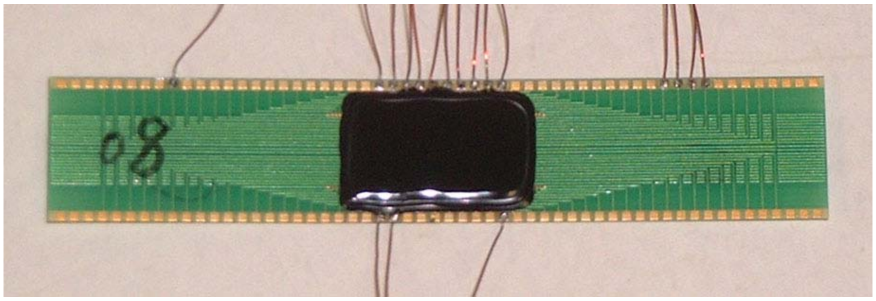


Fig. 5-20 Picture of an Encapsulated Chip-on-beam Sample

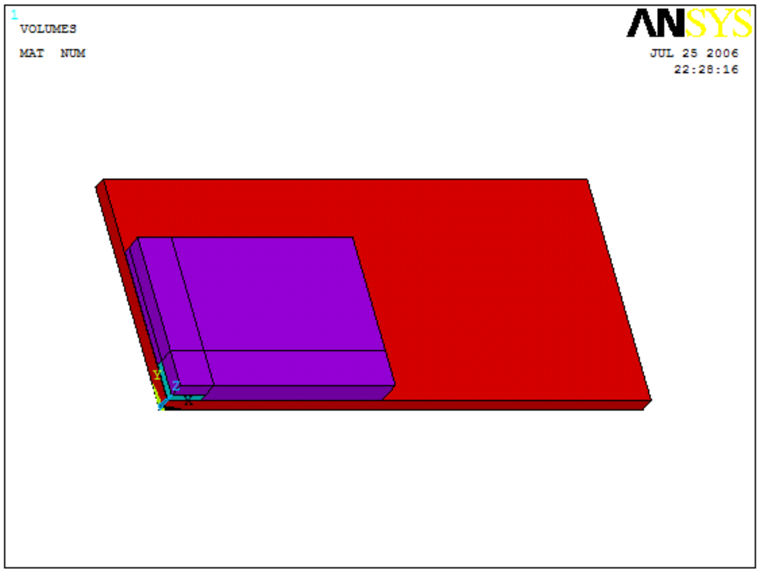


Fig. 5-21 ANSYS Quarter Model for Encapsulated Chip-on-beam Sample

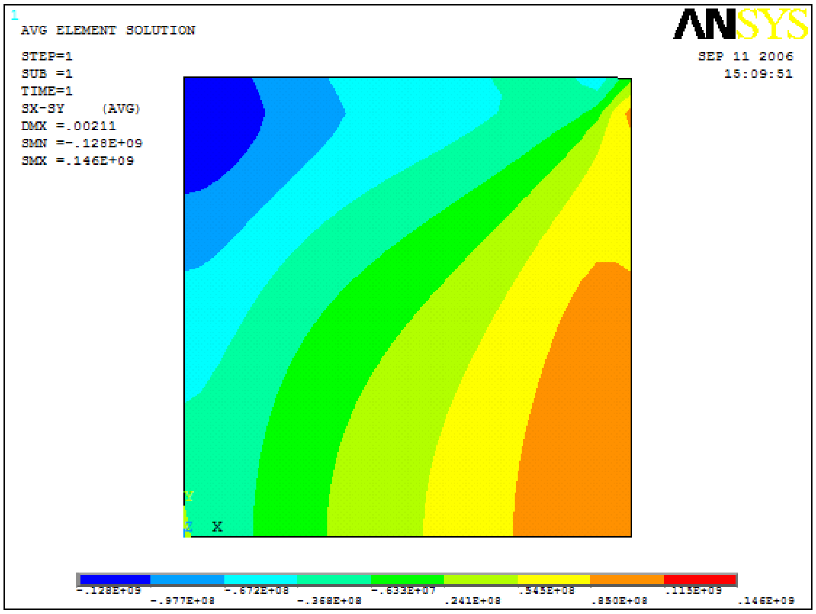


Fig. 5-22 Simulated Normal Stress Difference on Die Surface for Encapsulated Chip-on-beam Sample

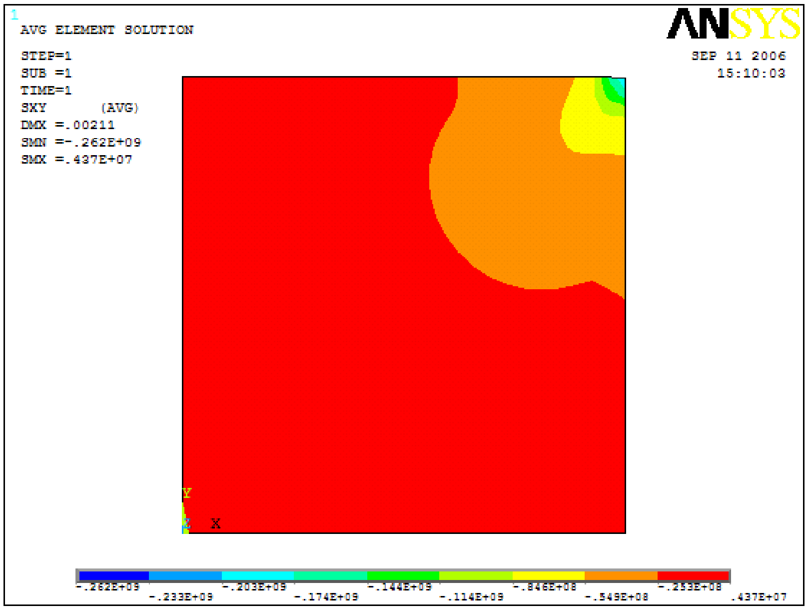


Fig. 5-23 Simulated Shear Stress on Die Surface for Encapsulated Chip-on-beam Sample

5.4 Calibration of Sensors

In order to measure the stress values using the piezoresistive sensors, the corresponding piezoresistive coefficient involved must be known values. The process used to determine these values is called calibration. Here, the only piezoresistive coefficients needed are Π_{44}^{p} and Π_{D}^{n}, so the objective of the calibration here is to determine these two coefficients. Fig. 5-24 and Fig. 5-25 show the simulated stress versus applied force by 4PB fixture, the corresponding stress increases linearly as the applied force increases, which indicates that the loaded force of less than 2N is in the safe range to avoid nonlinear effect due to large deflection of the PCB beam.

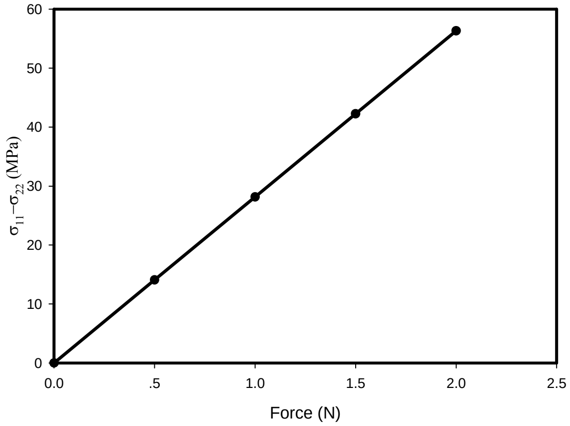


Fig. 5-24 Simulated Normal Stress Difference versus 4PB Load

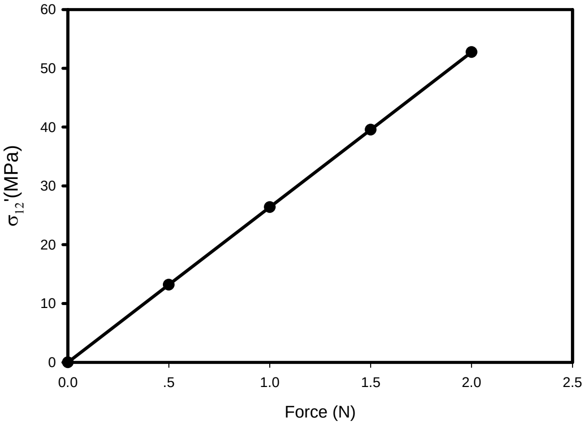


Fig. 5-25 Simulated Shear Stress versus 4PB Load

5.4.1 Coefficient Π_{44}^{p} Extraction

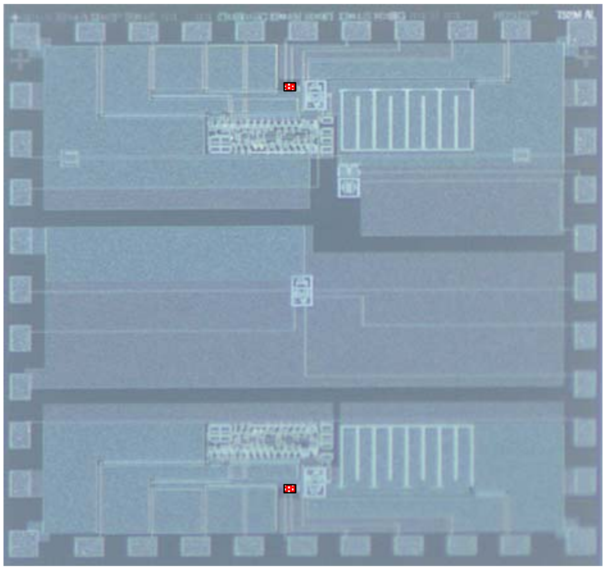


Fig. 5-26 Calibration Current Mirror on DSM Chip

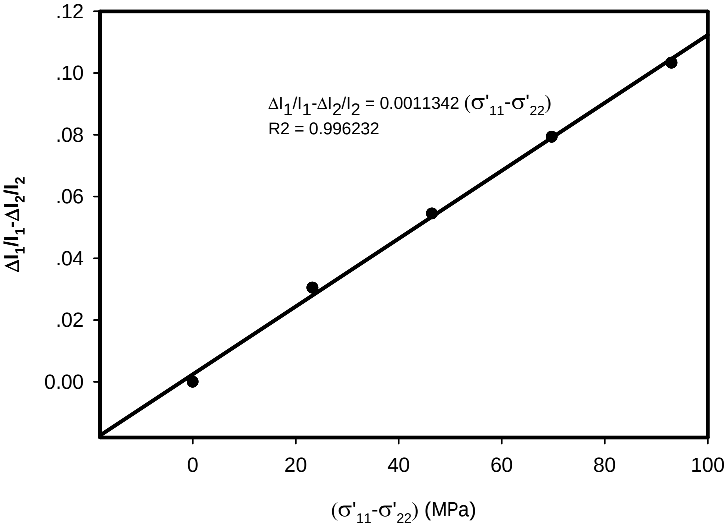


Fig. 5-27 Plot of PMOS Normalized Current Change in Current Mirror with Simulated In-plane Normal Stress Difference

The available sensors are on tiny chips from MOSIS, so use of a chip-on-beam technique is necessary to determine the piezoresistive coefficient Π_{44}^{p}. For a DSM sensor chip, separate current mirrors are available for calibration and these are shown as shaded blocks in Fig. 5-26. The stress values at the sensor sites are obtained from finite element simulation. A typical plot of a current mirror normalized current change versus the in-plane normal stress difference is shown in Fig. 5-27. According to Eq. (2.27), the Π_{44}^{p} value can be determined from the slope of the graph as $1134\,(TPa)^{-1}$, averaging Π_{44}^{p} values from same batch gives a value of $1139\,(TPa)^{-1}$.

For a sensor array chip, there is no separate cell provided for calibration, but many sensor cells are located in a region with relatively uniform stress, so these are good candidates for use in extracting piezoresistive coefficients. For the PMOS sensor cell, nine cells that lie in the shaded area on the die are shown in Fig. 5-28. The stress distribution and the sensor cell locations are shown in Fig. 5-29. The drawn black frame in the figure indicates the area on the die occupied by the sensor array, and the shaded black box indicates the area calibration sensor cell location. Fig. 5-30 shows a sample plot of normalized current change difference versus the in-plane normal stress difference for the nine sensor cells. The piezoresistive coefficient is determined to be 1186 $(TPa)^{-1}$ by Eq. (4.15). The average of determined Π_{44}^{p} value is $1139\,(TPa)^{-1}$, with a standard deviation of $32\,(TPa)^{-1}$ for sample from the batch with sensor chip #1, as shown in Table 5-3. Similarly the Π_{44}^{p} value was determined by six samples from sensor chip #2 and results are $1154\,(TPa)^{-1}$ with a standard deviation of $79\,(TPa)^{-1}$.

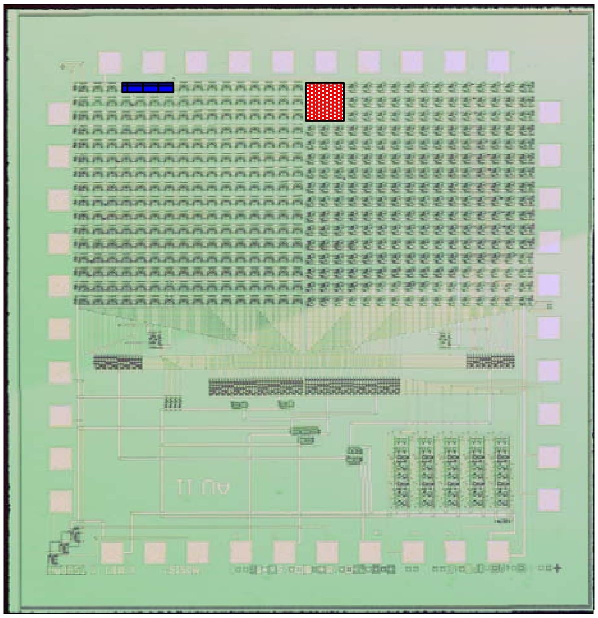


Fig. 5-28 Sensor Cells on Die Used for Calibration

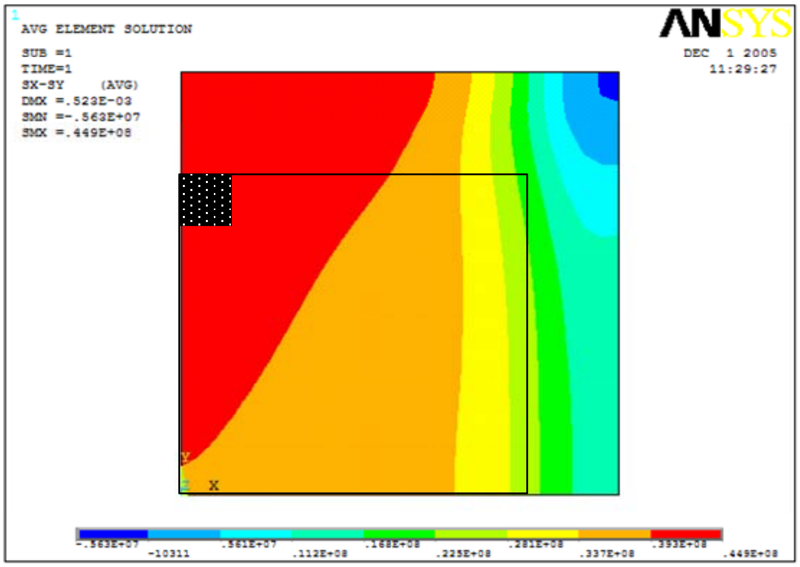


Fig. 5-29 Normal Stress Difference across Calibration Sensor Locations

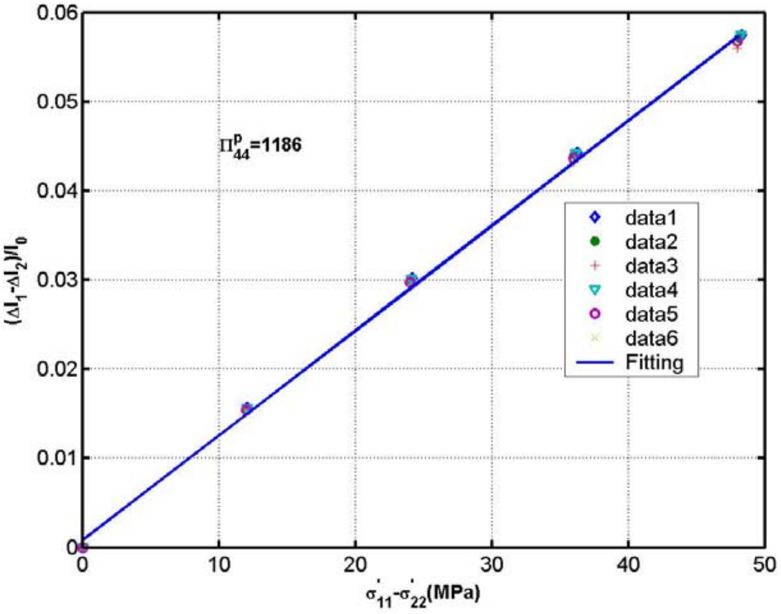


Fig. 5-30 Plot of PMOS Cell Normalized Current Change Data versus Simulated In-plane Normal Stress Difference

5.4.2 Coefficient Π^n_D Extraction

For the piezoresistive coefficient Π^n_D, the sensor used for calibration is shown in the shaded blue area in Fig. 5-31. The corresponding in-plane shear stress distribution at the sensor location indicated by the shadowed blue block is shown in Fig. 5-31. The stress values at the sensor sites are obtained from finite element simulation. The sample plot of normalized current change difference versus the in-plane shear stress is shown in Fig. 5-32. The piezoresistive coefficient $-2\Pi^n_D$ is determined in this measurement to be 1144 $(TPa)^{-1}$ with a standard deviation of 218 $(TPa)^{-1}$ by Eq. (4.16) from the sample with sensor chip #1, as shown in Table 5-3. The Π^n_D values extracted from the four sensors are averaged as -917 $(TPa)^{-1}$, and the piezoresistive coefficient $-2\Pi^n_D$ from samples with Sensor chip #2 is 1084 $(TPa)^{-1}$ with a standard deviation of 87 $(TPa)^{-1}$ or Π^n_D value of -542 $(TPa)^{-1}$ correspondingly.

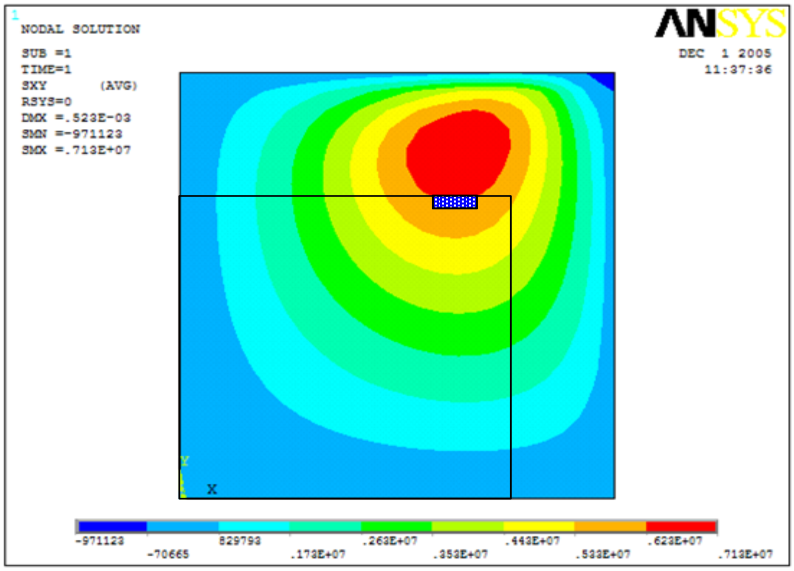


Fig. 5-31 Shear Stress across Calibration Sensor Locations

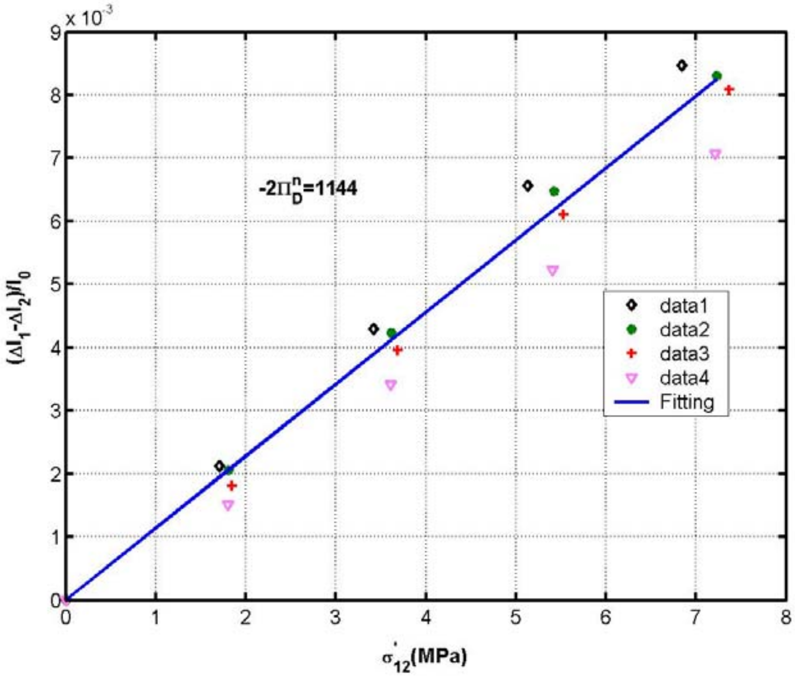


Fig. 5-32 Plot of Measured Normalized Current Change Difference versus Simulated In-plane Shear Stress

Table 5-3 Calibration Data for Sensors Chip1

Sensor Index	$\Pi 44^p$	Sensor Index	$-2\ \Pi D^n$
16-14	1142	16-26	1868
16-15	1148	16-27	1738
16-16	1121	16-28	2121
15-14	1167	16-29	1610
15-15	1178		
15-16	1137		
14-14	1062		
14-15	1163		
14-16	1136		
AVG	1139		1834
SDV	32		218

Table 5-4 Calibration Data for Sensors with MOSIS Fab ID T63Y

Sample Number	$\Pi 44^p$	$-2\ \Pi D^n$
1	1065	1018
3	1264	1184
5	1139	965
7	1231	1119
8	1145	1168
9	1081	1050
Average	1154	1084
SDV	79	87

5.5 Characterization Results

5.5.1 DSM Stress Sensor

Two experiments were performed on the DSM stress sensor. In order to investigate the properties of the DSM sensor over a wide range, a wide range of mismatch was simulated by injecting a constant current into the capacitor. Mismatches equivalent to $-100\% \sim 100\%$ were measured using this technique. Another measurement was performed to measure the actual response of the DSM stress sensor to applied stress.

5.5.1.1 Mismatch by Current Injection

Fig. 5-33 shows a schematic of the circuit used to inject a current into the DSM system to simulate the mismatches. On-chip current mirrors are included to inject a known amount of current without introducing a significant amount of extra capacitance at the current injection node inside the circuit. Positive and negative currents are injected via separate pins in this design.

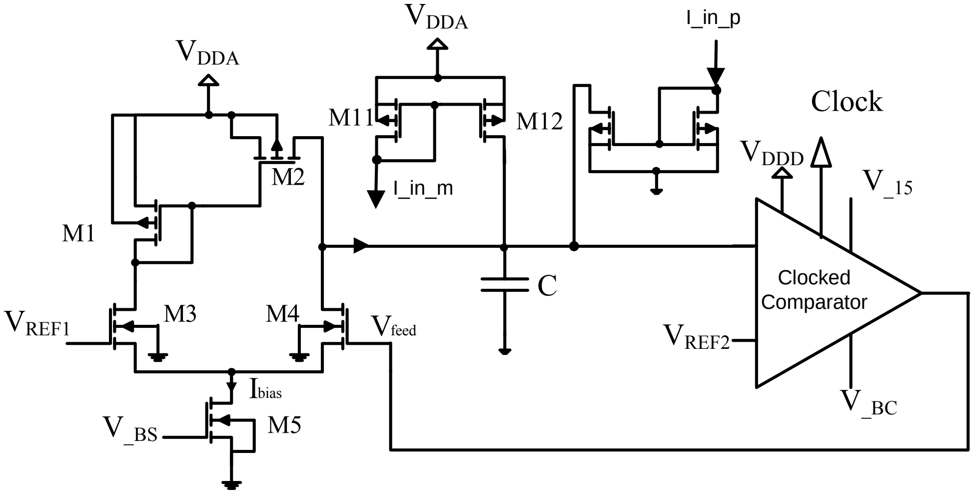


Fig. 5-33 DSM Current Injection Schematic

Ideally, the initial mismatch should be very small for a matched design. Besides the random mismatches that are always present, the two transistors that are used here to form a current mirror are orientated in different directions, which unavoidably generates some amount of mismatch due to the environmental differences between them during the fabrication process [104]. The actual bias conditions for this measurement are listed in Table 5-5. The pin assignment tables for the DSM sensor chips in this work are listed in Appendix C.

Table 5-5 Bias Condition for DSM Sensor

VDDD	VDDA	VREF1	VREF2	V_BC	V_15	Fclock
4V	4V	0.9V	2.0V	0.8V	2.0V	835kHz

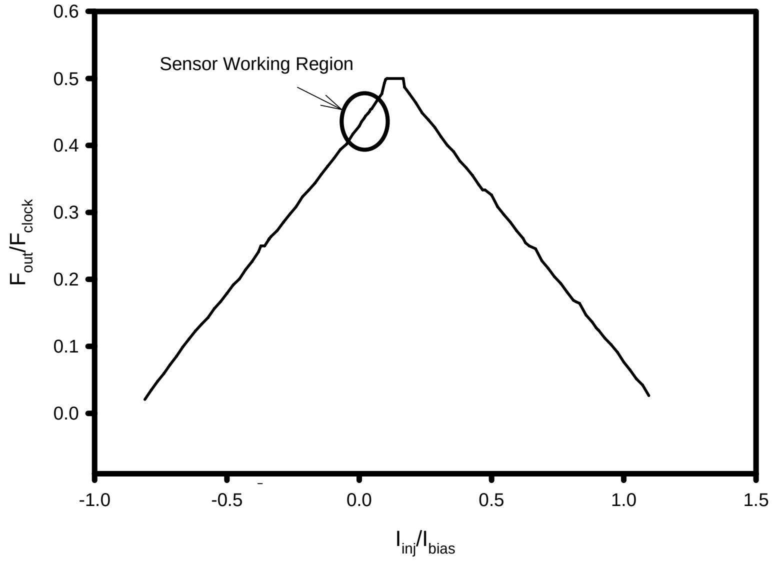


Fig. 5-34 Output Frequency Normalized by Clock Frequency versus Normalized Injected Current Mismatch

Instead of measuring the ratio of the output frequency to the clock frequency using a counter, as was done here, the output signal can be counted over a certain period of time, or fundamental frequency of the signal can be detected by a receiver. Where there is no mismatch, the output frequency is at half of the clock frequency. When the mismatch increases, two tones can be heard, one on either side of the half clock frequency. Here, the tone is split and the amount of the frequency shift from the center frequency is proportional to the mismatch between the two transistors in the current mirror, as shown in Fig. 3-16. The plots of the counter output, the frequency shift from the center frequency and the ratio of the output lower-side frequency over the clock frequency all have the same shape. If normalized correctly, the three plots merge into one, which indicates that any one of the three plots can be used to monitor the physical change.

Therefore, the ratio of the output lower-side frequency to the clock frequency is selected here to show the properties of the DSM sensor.

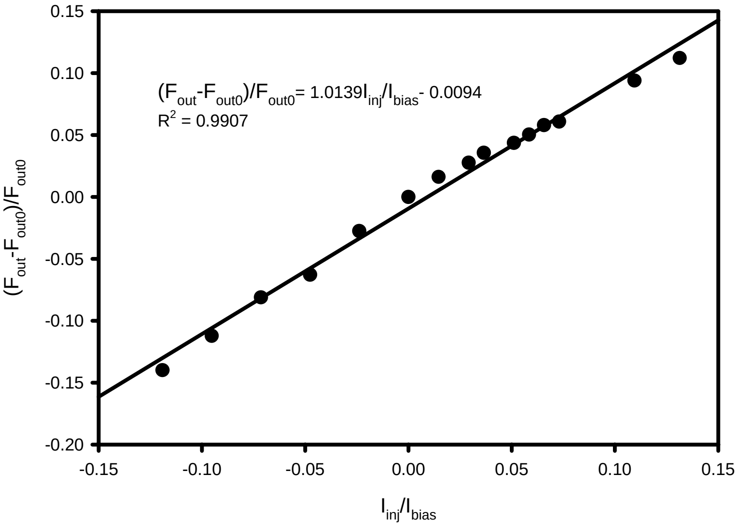


Fig. 5-35 Normalized Output Frequency Change versus Mismatch Injected In Sensor Operational Region

Fig. 5-34 shows the output lower-side frequency normalized by the clock frequency versus the normalized injected current. The bias current used here, $13.7\mu A$, is determined by averaging the currents extracted by extrapolating F_{out} / F_{clock} in both directions to zero. The injected current is read from the current source used to inject the current. The circled portion of the curve indicates the $\pm 10\%$ range, which is the range that covers the normal stress sensor response. Fig. 5-35 plots the normalized output frequency change versus the mismatch injected in the likely sensor operational region. The trend line fitting these data has an R^2 value of 0.9907 in this plot, which indicates a reasonable linear relationship between the normalized current injection and the output frequency change. This linear relationship is very desirable for the sensor's potential applications. The slope is approximately unity, which indicates that the normalized frequency shift is equal to the normalized mismatch. Based on this observation, for the DSM sensor Eq. (2.27) can be modified as

$$\frac{F_{out}-F_{out0}}{F_{out0}}=\Pi^{p}_{44}(\sigma'_{11}-\sigma'_{22}) \tag{5.2}$$

5.5.1.2 DSM Sensor Stress Response

Using the same biasing conditions as those listed in Table 5-5, a stress is applied by the 4PB fixture and the ratio of the output frequency to the clock frequency is measured. The stress value is estimated from the finite element simulation results. The frequency F_{out0} denotes the output frequency without stress, while F_{out} is the output frequency when a stress is applied. Fig. 5-36 shows the normalized output frequency change versus the in-plane normal stress difference. According to Eq. (5.2), the piezoresistive coefficient Π^{p}_{44} is determined to be 1179 $(TPa)^{-1}$, which agrees well with the value extracted directly from the separated current mirror cell, 1134 $(TPa)^{-1}$.

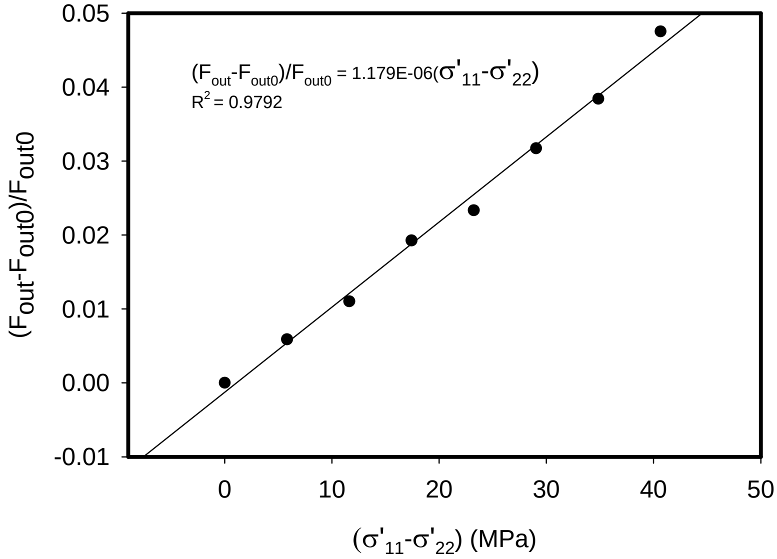


Fig. 5-36 Normalized Frequency Shift with Normalized In-plane Stress Difference

5.5.2 Sensor Array Stress Mapping Results

Die stresses were mapped under three setups, where one is die stress on chip-on-beam structure under 4PB load, the second is die stress change before and after the DIP40 packages were encapsulated with ME515 underfill, and the third is die stress when the chip on chip-on-beam sample was encapsulated with ME525 underfill.

5.5.2.1 Die Stress Mapping for Chip-on-Beam under 4PB Load

The reference currents to each cell were measured before the stress was applied and changes in the current were monitored as a load was applied. The calibrated piezoresistive coefficients were used to calculate the stress at all the sensor sites, and the stress distribution on the chip surface was fitted to a 2D surface in order to smooth the measurement data. The measurement was converted to corresponding stress. Fig. 5-37 and Fig. 5-38 show a 3D surface fitting using the TableCurve3D software, which offers many choices for using different functions to obtain a good surface fit. For the PMOS array and the NMOS array different functions were selected, and R-square values of 0.99 and 0.98 were obtained. These fitting results were exported into MATLAB functions which were then used to plot the stress mapping results. The normal stress difference and shear stress measured with a force load of 2N with mounting process #1 are plotted in Fig. 5-39 and Fig. 5-40. Each square on the picture indicates one sensor cell location. Another way to compare the measurement results with the simulated results is to overlap the measurement results on the simulated results directly without any fitting, as shown in Fig. 5-41 and Fig. 5-42 for the normal stress difference and shear stress respectively. Each box filled with color represents a result from one sensor cell in array. Fig. 5-43 and Fig. 5-44 show the averaged stress measurement results from eight samples with chip mounting process #2, the results from individual samples are listed in Appendix D. The difference between mounting process #1 and process #2 is the disense temperature, for process #1 the dispense temperature is room temperature while 90 ^{o}C for process #2. The measured normal stress difference and shear stress on the chip surface patterns compare well to the simulated stress distributions. Fig. 5-45 and Fig. 5-46 show example plots of normal stress difference and shear stress along four rows in sensor arrays, the slope gives the local stress gradient information.

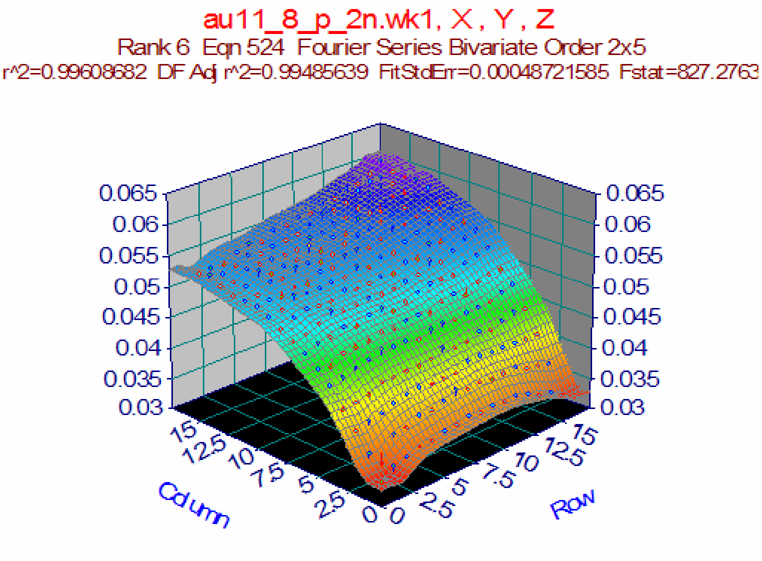


Fig. 5-37 Surface Fitting Based on Measured Data from PMOS Array on Sample #1 under 2N 4PB Load

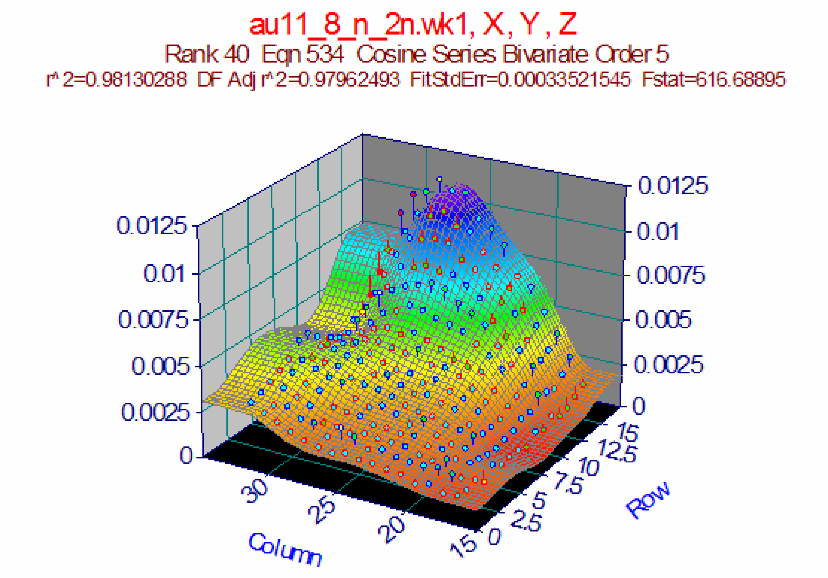
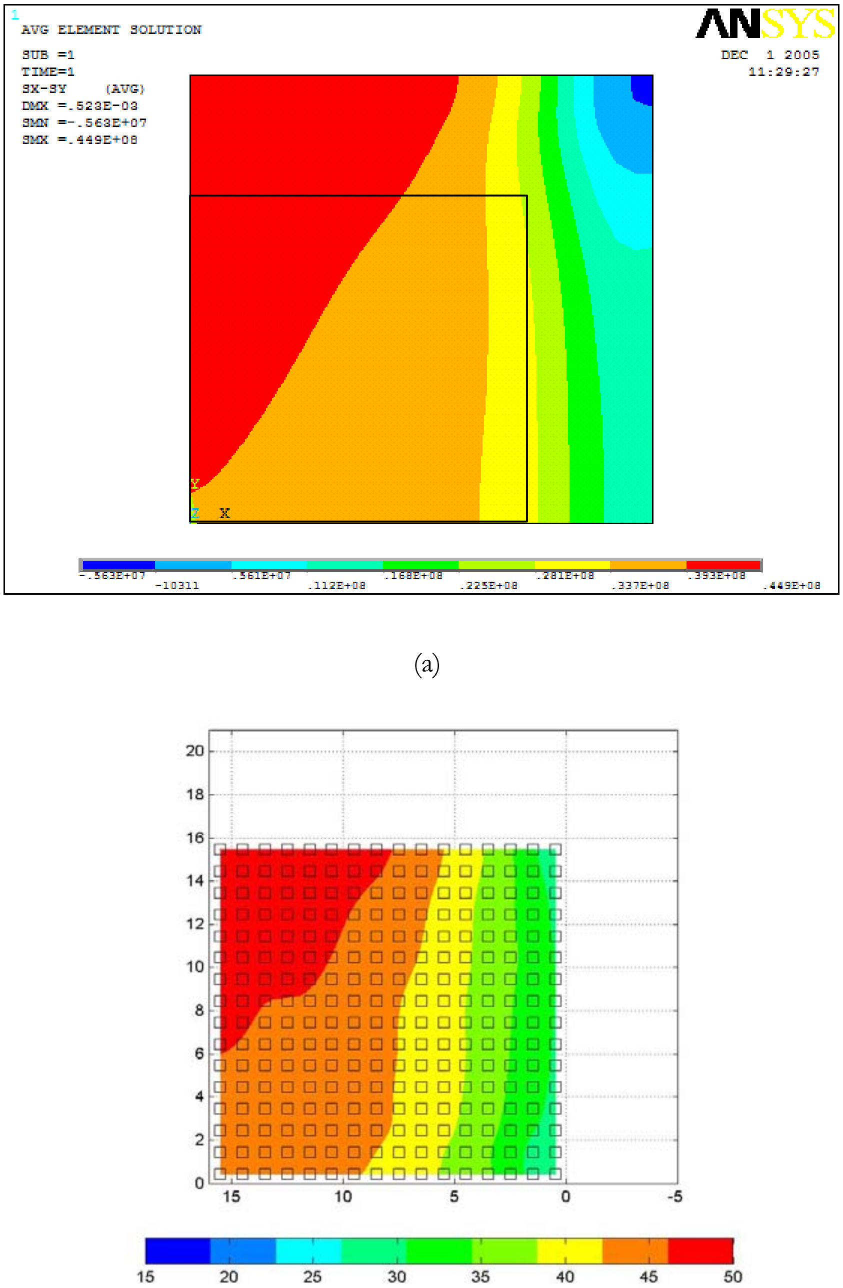


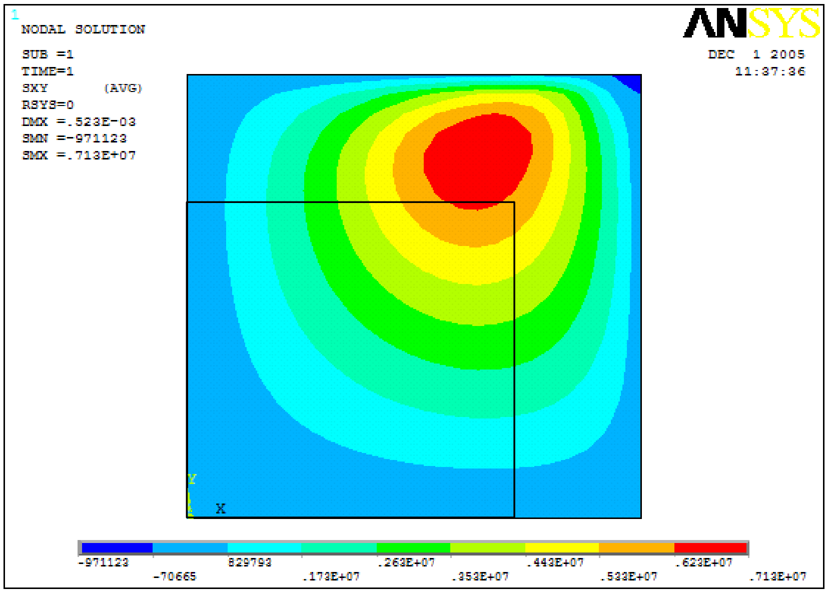
Fig. 5-38 3-D Surface Fitting Based on Measured Data from NMOS Array on Sample #1 under 2N 4PB Load



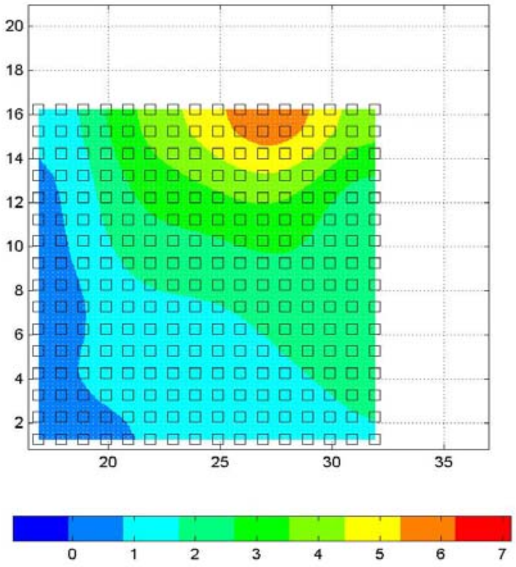
(a)

(b)

Fig. 5-39 Normal Stress Difference on Die Surface under 2N Load Sample #8: (a) Simulation Results; (b) Fitted Measurement Results



(a)



(b)

Fig. 5-40 Shear Stress on Die Surface under 2N 4PB Load Sample #8: (a) Simulation Results; (b) Fitted Measurement Results

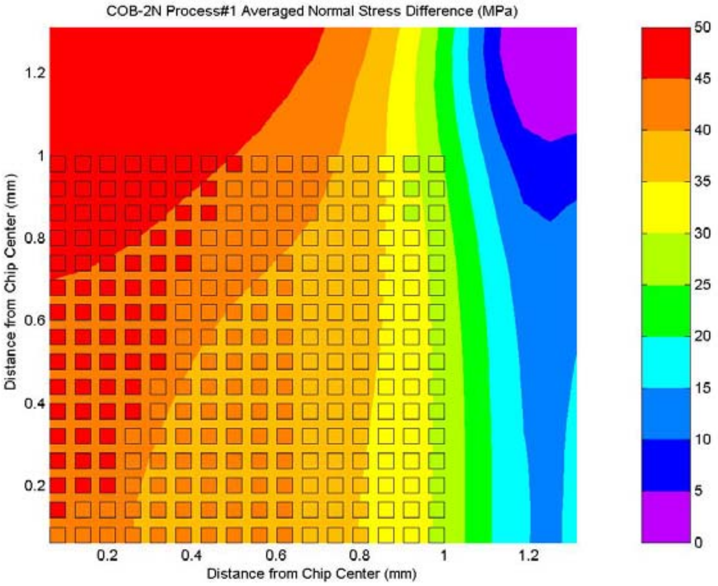


Fig. 5-41 Averaged Normal Stress Difference on Die Surface Measured Results under 2N Load with Mounting Process #1 Overlapped with Simulated Results

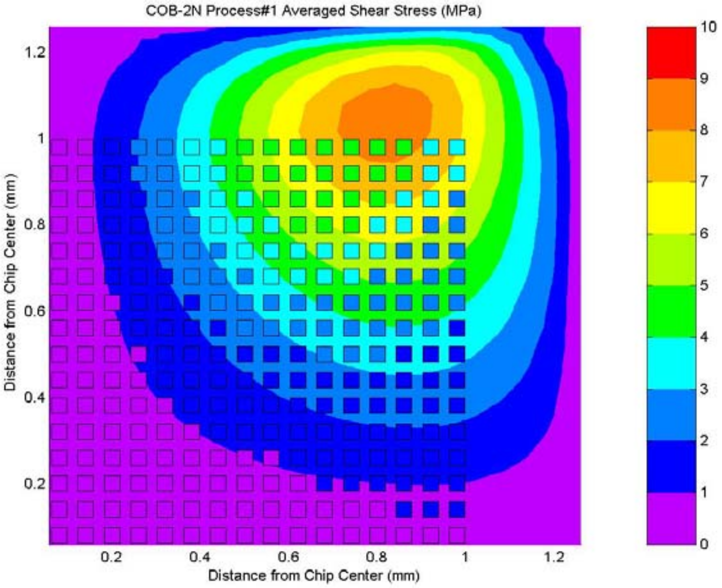


Fig. 5-42 Averaged Shear Stress on Die Surface Measured Results under 2N Load with Mounting Process #1 Overlapped with Simulated Stress

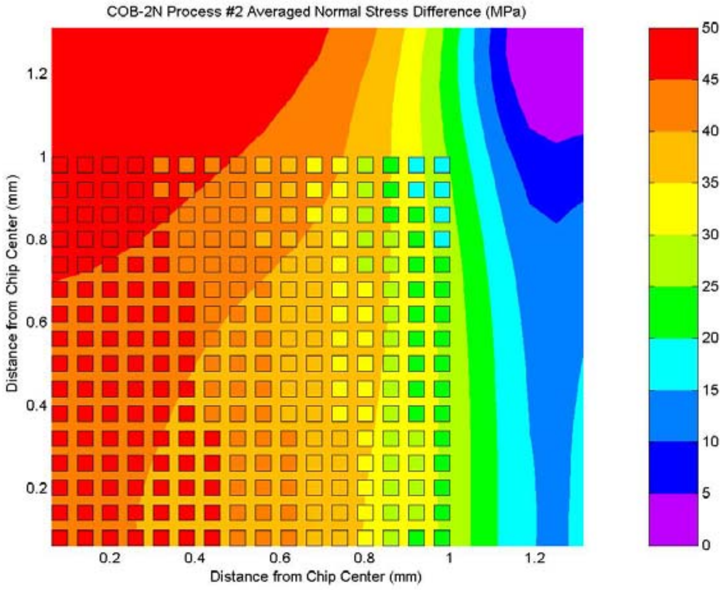


Fig. 5-43 Averaged Normal Stress Difference on Die Surface from Eight Samples with Mounting Process #2 under 2N Load

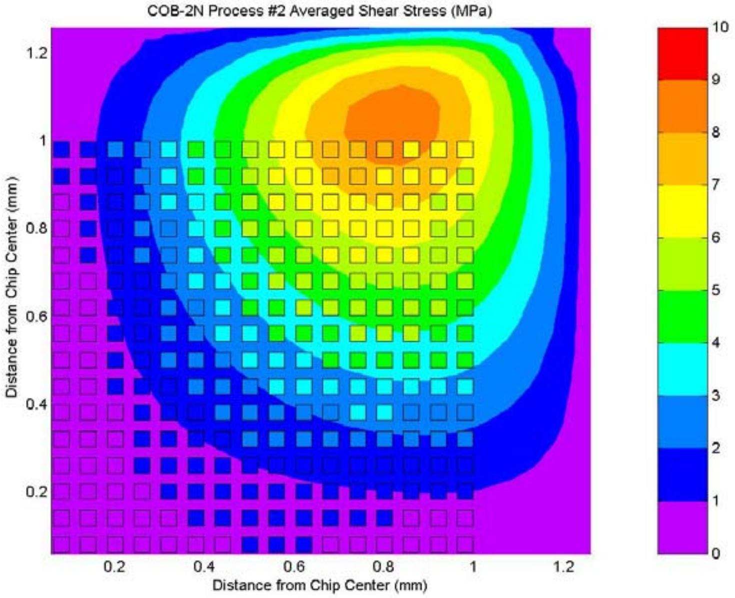


Fig. 5-44 Averaged Shear Stress on Die Surface from Eight Samples with Mounting Process #2 under 2N Load

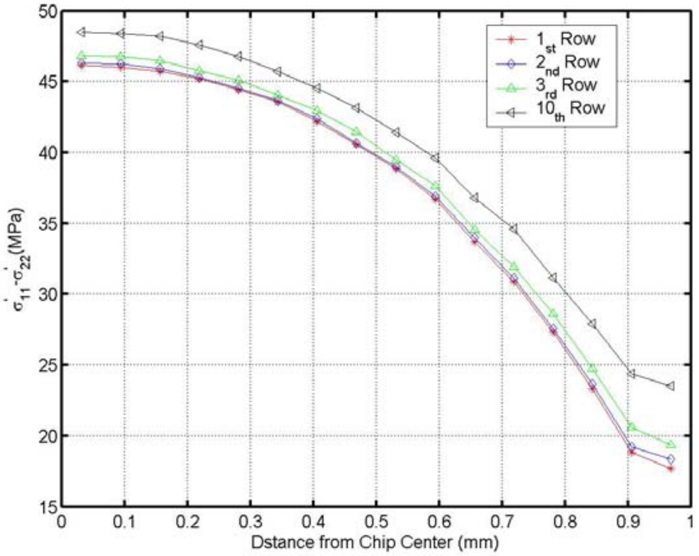


Fig. 5-45 Example Plots of Normal Stress Difference along Sensor Rows Based on Fig. 5-43

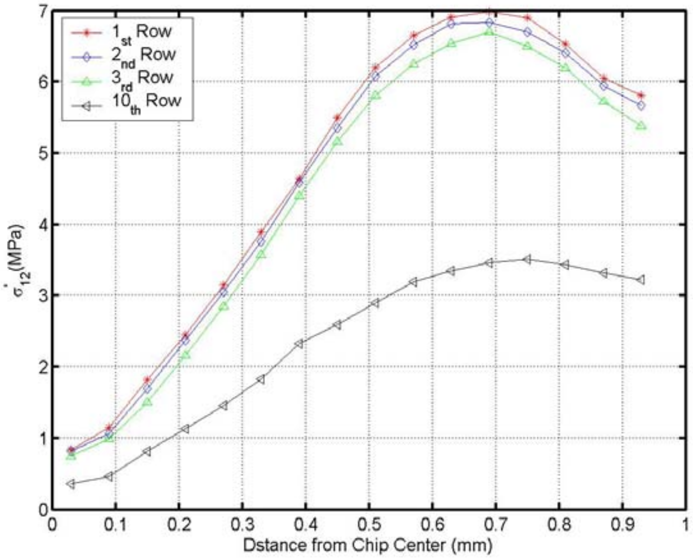


Fig. 5-46 Example Plots of Shear Stress along Sensor Rows Based on Fig. 5-44

5.5.2.2 Die Stress Mapping for Encapsulated Package

The sensor arrays were used to map the change of die stress before and after the DIP40 encapsulated with ME525 underfill. The current outputs before the package was encapsulated with ME525 underfill and the normalized current change are measured and converted to corresponding stress. Fig. 5-47 and Fig. 5-49 plot the raw stress data from measurement results. Fig. 5-48 and Fig. 5-50 show the measurement results from sensor array overlapped with simulation results correspondingly smoothed by taking the median of the stress value of nine neighbor sensors as the stress value. See Appendix H for measurement results for each sample. The measurement stress distribution patterns agree well to the ANSYS simulation even though the measurement stress values are lower than the simulation data.

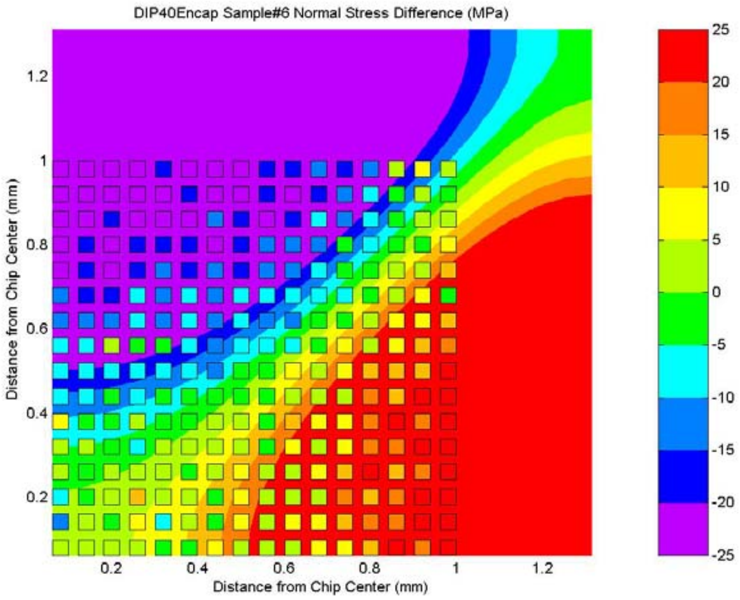


Fig. 5-47 Normal Stress Difference on Die Surface Measured Results Overlapped with Simulated Results for DIP40 Encapsulated with ME525

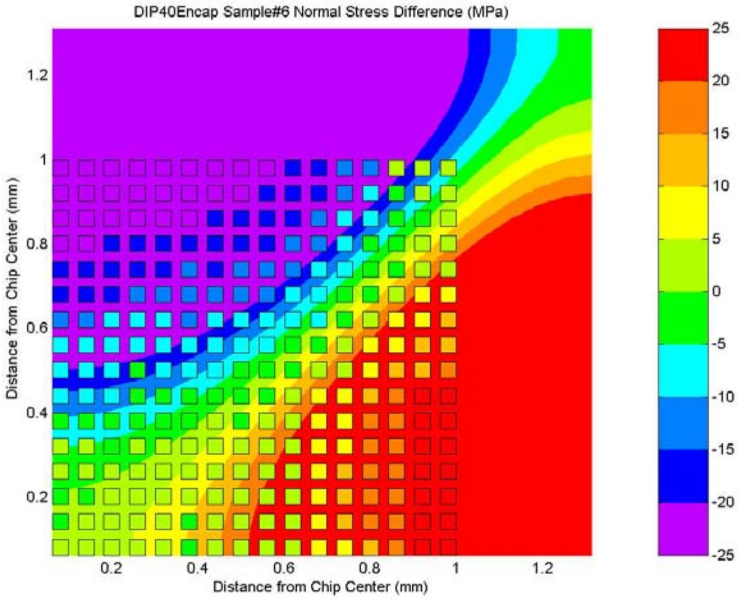


Fig. 5-48 Smoothed Normal Stress Difference on Die Surface Measured Results Overlapped with Simulated Results for DIP40 Encapsulated with ME525

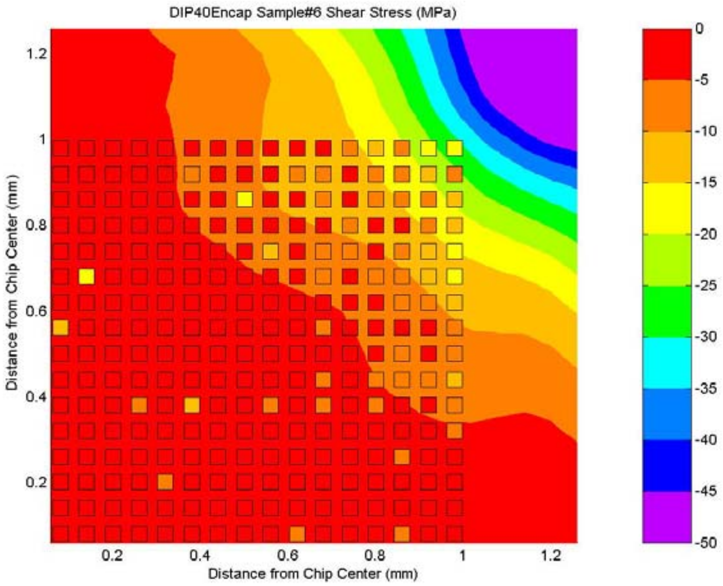


Fig. 5-49 Shear Stress on Die Surface Measured Results Overlapped with Simulated Results for DIP40 Encapsulated with ME525

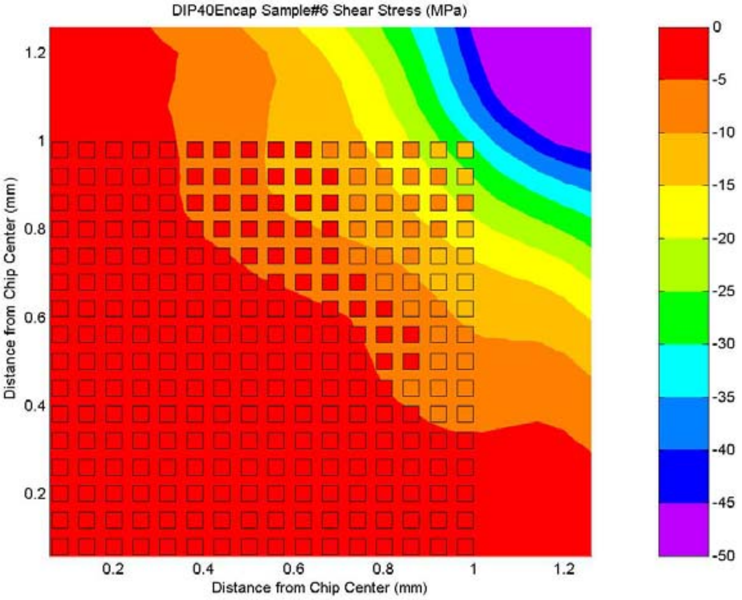


Fig. 5-50 Smoothed Shear Stress on Die Surface Measured Results Overlapped with Simulated Results for DIP40 Encapsulated with ME525

5.5.2.3 Die Stress Mapping for Encapsulated Chip-on-beam

The sensor array chips are used to measure the die stress in chip-on-beam sample encapsulated by ME525 underfill material. Loctite Hysol® globe top encapsulant FP4460 is used to make a dam on the beam around the die then the underfill ME525 is filled in order to encapsulate the chip. After being annealed in 150°C for 30 minutes, the encapsulated chip-on-beam sample is shown in Fig. 5-20. The original bias current and original mismatch current for each sensor are measured before chip-on-beam samples are encapsulated. The output of each sensor is measured after encapsulation, and the calibration piezoresistive coefficients are used to convert current change into corresponding stress. Fig. 5-51 and Fig. 5-53 show the normal stress difference and shear stress on die surface for encapsulated chip-on-beam sample #4 overlapped with the simulated stress distribution, see Appendix Ffor plots from other samples. Fig. 5-52 and Fig. 5-54 plot the averaged normal stress difference and shear stress on die surface from eight samples. All plots show the right patterns, which indicates the sensors in arrays measure the stress reasonably. It is found that there are some stress data for single sample stand out from their neighbors as shown in Fig. 5-51 and Fig. 5-53 which indicates non-uniform stresses exist locally, this may caused by different mechanical property of filler and resins in the glob top material.

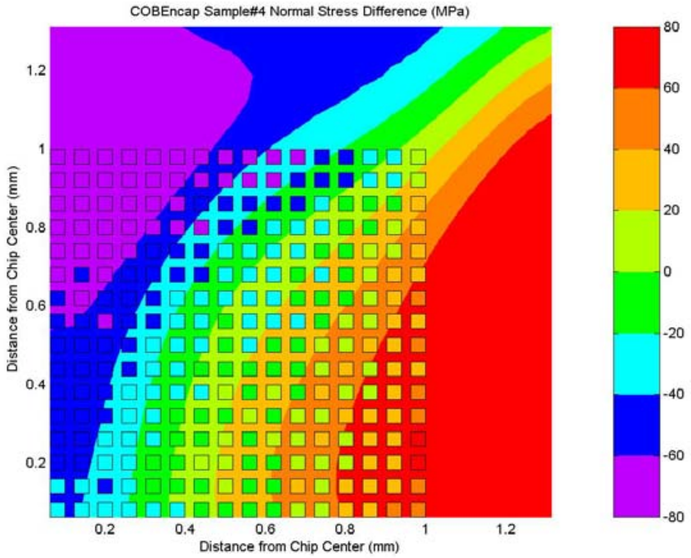


Fig. 5-51 Normal Stress Difference for Encapsulated Chip-on-beam Sample #4

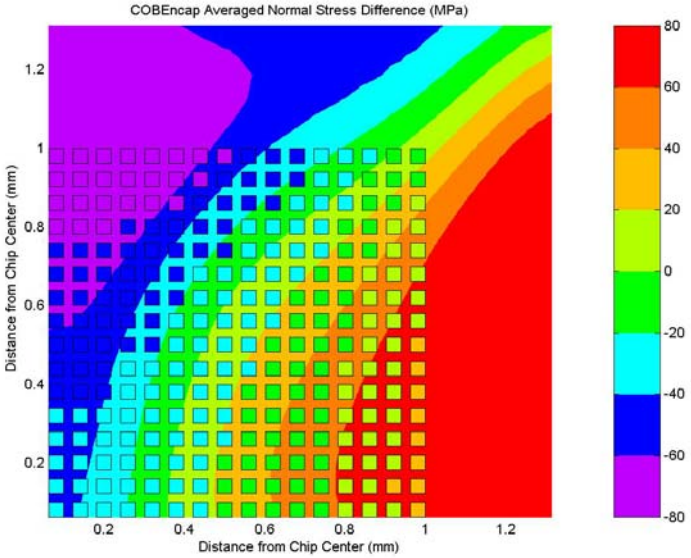


Fig. 5-52 Averaged Normal Stress Difference for Encapsulated Chip-on-beam

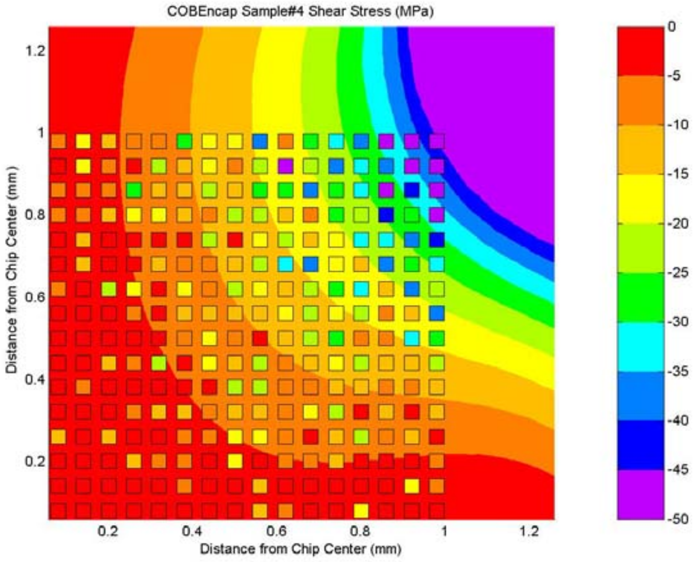


Fig. 5-53 Shear Stress for Encapsulated Chip-on-beam Sample #4

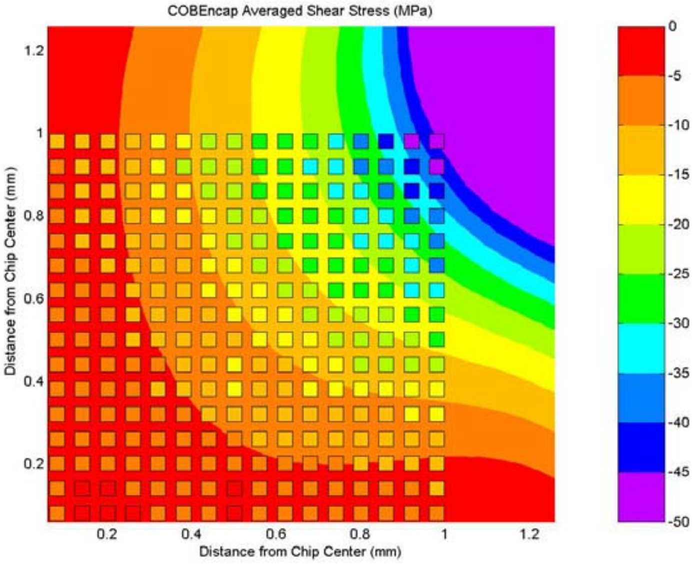


Fig. 5-54 Averaged Shear Stress for Encapsulated Chip-on-beam

CHAPTER 6. SUMMARY AND FUTURE WORK

6.1 Summary of the Work

A delta-sigma modulator based CMOS stress sensor with RF output was designed, implemented and characterized in this study. A CMOS current mirror formed by orthogonal oriented PMOS transistors is used as a stress sensor and integrated as part of a delta-sigma modulator in MOSIS 1.5 μm CMOS technology, which detects the in-plane normal stress on the die. The delta-sigma modulator functions as a transmitter whose output can be viewed as either a one-bit data stream or a double side-band suppressed carrier (DSBSC) signal. The output can be processed digitally, or remotely detected by a communication receiver. The results show that the magnitude of the normalized frequency shifts gives a precise measurement of the mismatch inside the current mirror, which is proportional to the stress. The proportionality factor is the piezoresistive coefficient for the corresponding MOSFET pair. This strategy provides a simple and convenient way to build a transmitter for a sensor. In this configuration, most of the circuits operate in the digital domain except for the sensor cell, so they are not sensitive to stress, temperature and other mismatches or variations. This technique can be developed further for many other applications.

Multiplexed CMOS sensor arrays for die stress mapping were studied. Cascode CMOS current mirrors are used as temperature compensated stress sensor cells with high sensitivities and small cell area. Sensor arrays with 256 sensor cells for in-plane normal stress difference and 256 sensor cells for in-plane shear stress were fabricated on a 2.2×2.2 mm2 MOSIS tiny chip. A chip-on-beam technique was used to calibrate the sensors, and the measured stresses on the chip surface agree well with the simulated stress distribution on the chip surface. The sensor array was also used to measure the stress on the die surface in a DIP40 package with the cavity filled with ME525 underfill, on chip-on-beam samples under 4PB load, and chip-on-beam samples encapsulated with ME525 underfill. The automatically scanned sensor chip provides the highest spatial resolution (number of data points per square millimeter) of die stress reported to date. The qualitative agreement between measured and simulated shear stress gives the first experimental verification that the PiFETs are actually measuring shear stress. The stress information obtained by the sensor arrays for the first time provides an experimental approach to measure the stress gradient along any path on chip surface with high resolution.

6.2 Future Work

The research reported in this dissertation showed a way to obtain a high resolution stress distribution map on a die and developed a simple but effective way to build a sensor transmitter separately, avoiding many of the difficulties involved in using high precision on-chip components. These two aspects can be combined to develop a sensor array with a digital output, which greatly simplifies the stress measurement process. The transmitter design reported here can be used for many other types of sensors and in other environments where it is necessary to detect a small mismatch.

An intentional mismatch for the transistors in the sensor cell may be designed in order to get the sign information of the stress by the delta-sigma modulator based stress sensor, and a cascode current mirror should be used to eliminate the current change due to drain voltage difference.

Further sensor cell size design should be considered in order to minimize the initial mismatches in sensor arrays. If the original mismatch among sensor cells in sensor array is much smaller than the mismatch induced by the stress, one bias current can be used to normalize the mismatch and simplify the data processing. Next versions of the sensor array may be designed using processes with smaller feature size, which may get even higher resolution for die surface stress, and expand the sensor array potential for the mechanical imaging applications such as tactile sensors.

Another observation in this work is that there are random local stress peaks on the die surface in every encapsulated sample. Further study should be performed to identify the exact reason and come up with some solution.

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APPENDICES

Appendix A. PSPICE Models for MOSFET Used in This Work

```
.MODEL CMOSP2 PMOS (                  LEVEL  = 7
+VERSION = 3.1     TNOM    = 27         TOX     = 3.2E-8
+ XJ      = 3E-7         NCH     = 2.4E16     VTH0    = -0.8476404
+ K1      = 0.4513608     K2      = 2.379699E-5 K3      = 13.3278347
+ K3B     = -2.2238332    W0      = 9.577236E-7 NLX     = 1E-6
+ DVT0W   = 0            DVT1W   = 0          DVT2W   = 0
+ DVT0    = 3.5725934     DVT1    = 0.703231    DVT2    = -3.694522E-3
+ U0      = 236.8923827   UA      = 3.833306E-9 UB      = 1.487688E-21
+ UC      = -1.08562E-10  VSAT    = 1.214242E5  A0      = 0.5102824
+ AGS     = 0.3008209     B0      = 4.14765E-6  B1      = 5E-6
+ KETA    = 0.0110152     A1      = 0           A2      = 0.364
+ RDSW    = 3E3           PRWG    = 0.1128791   PRWB    = -0.2328945
+ WR      = 1             WINT    = 7.565065E-7 LINT    = 1.130031E-7
+ XL      = 0             XW      = 0           DWG     = -2.13917E-8
+ DWB     = 3.857544E-8   VOFF    = -0.0877184  NFACTOR = 0.2508342
+ CIT     = 0             CDSC    = 2.924806E-5 CDSCD   = 1.497572E-4
+ CDSCB   = 1.091488E-4   ETA0    = 0.26103     ETAB    = -3.214696E-4
+ DSUB    = 0.2873        PCLM    = 1E-10       PDIBLC1 = 2.769509E-4
+ PDIBLC2 = 1.001142E-3   PDIBLCB = -1E-3       DROUT   = 9.990041E-4
+ PSCBE1  = 3.517926E9    PSCBE2  = 5.277956E-10 PVAG    = 15.0001499
+ DELTA   = 0.01          RSH     = 74.9        MOBMOD  = 1
+ PRT     = 0             UTE     = -1.5        KT1     = -0.11
+ KT1L    = 0             KT2     = 0.022       UA1     = 4.31E-9
+ UB1     = -7.61E-18     UC1     = -5.6E-11    AT      = 3.3E4
+ WL      = 0             WLN     = 1           WW      = 0
+ WWN     = 1             WWL     = 0           LL      = 0
+ LLN     = 1             LW      = 0           LWN     = 1
+ LWL     = 0             CAPMOD  = 2           XPART   = 0.5
```

```
+ CGDO    = 2.17E-10      CGSO    = 2.17E-10    CGBO    = 1E-9
+ CJ      = 3.087565E-4   PB      = 0.8         MJ      = 0.4476167
+ CJSW    = 1.667469E-10  PBSW    = 0.8         MJSW    = 0.1003324
+ CJSWG   = 3.9E-11       PBSWG   = 0.8         MJSWG   = 0.1003324
+ CF      = 0             )
*
*$

.MODEL CMOSN NMOS (                             LEVEL   = 7
+VERSION = 3.1            TNOM    = 27          TOX     = 3.2E-8
+XJ      = 3E-7           NCH     = 7.5E16      VTH0    = 0.5337484
+K1      = 0.9445837      K2      = -0.0753121  K3      = 7.077252
+K3B     = -3.0777492     W0      = 1.886279E-6 NLX     = 1E-8
+DVT0W   = 0              DVT1W   = 0           DVT2W   = 0
+DVT0    = 0.9888846      DVT1    = 0.4281615   DVT2    = -0.2561586
+U0      = 618.5828239    UA      = 6.54385E-10 UB      = 2.161262E-18
+UC      = -1.54758E-12   VSAT    = 1.081058E5  A0      = 0.6338864
+AGS     = 0.1095347      B0      = 2.0921E-6   B1      = 5E-6
+KETA    = -6.480023E-3   A1      = 0           A2      = 1
+RDSW    = 3E3            PRWG    = -5.879394E-4  PRWB    = -0.0256963
+WR      = 1              WINT    = 6.248667E-7   LINT    = 2.57154E-7
+XL      = 0              XW      = 0           DWG     = -4.22416E-10
+DWB     = 3.864446E-8    VOFF    = -0.034024   NFACTOR = 0.4346475
+CIT     = 0              CDSC    = 0           CDSCD   = 0
+CDSCB   = 2.152388E-5    ETA0    = -0.6149431  ETAB    = -0.3625863
+DSUB    = 1.0017134      PCLM    = 1.2971416   PDIBLC1 = 8.37923E-3
+PDIBLC2 = 2.05324E-3     PDIBLCB = -0.1        DROUT   = 0.0580928
+PSCBE1  = 2.181736E9     PSCBE2  = 5.050164E-10  PVAG    = 0.161873
+DELTA   = 0.01           RSH     = 53.5        MOBMOD  = 1
+PRT     = 0              UTE     = -1.5        KT1     = -0.11
+KT1L    = 0              KT2     = 0.022       UA1     = 4.31E-9
+UB1     = -7.61E-18      UC1     = -5.6E-11    AT      = 3.3E4
+WL      = 0              WLN     = 1           WW      = 0
```

```
+WWN    = 1             WWL    = 0             LL     = 0
+LLN    = 1             LW     = 0             LWN    = 1
+LWL    = 0             CAPMOD = 2             XPART  = 0.5
+CGDO   = 1.73E-10      CGSO   = 1.73E-10      CGBO   = 1E-9
+CJ     = 2.758084E-4   PB     = 0.9620726     MJ     = 0.5379993
+CJSW   = 1.526713E-10  PBSW   = 0.99          MJSW   = 0.1
+CJSWG  = 6.4E-11       PBSWG  = 0.99          MJSWG  = 0.1
+CF     = 0             )
*
*
```

Appendix B. MATLAB Code for Noise Simulation

```
close all; clear all;
%Initialize
I0=2.5e-6; %%%%%%%%%%%Current Value
t0=0;   Vref=1.5;   Vth=2;  Vtl=1;
ctrl=0; V0=1.5;     pc=0;   nc=0;
C=100e-12;  %%%%%%%%%Capacitor Value
fclk=0.5e6;   %%%%%%%%%Clock Frequency
delta=0.05;   %%%%%%%%%Delta is mismatch in percentage
An=5e-3;     %%%%%%%%%Peak amplitude of the noise
G=1e5;       %%%%%%%%%Gain

T=1/fclk/2;delta_I=delta*I0;

for n=1:2000        %%%%%%%%%%%1000 periods
   t(n)=t0+n*T;

% Determine Charge Current by Ctrl signal
   if ctrl==0
     I=I0+delta_I;  %%%%for Ctrl=0, I=I0+delta
   elseif ctrl==1
     I=-1*I0;          %%%%For Ctrl=1, I=-I0
   end;
V0=V0+I*T/C;       %%%Signal from capacitor
V1=V0+An*rand;    %%%Noise Added signal
V2=G*(V1-Vref);    %%%Amplified Signal

%%%%%%%%Determine Ctrl by comparing V2 and VTH and VTL
```

```
  if V2>=Vth
  ctrl=1;
  elseif V2<=Vtl
  ctrl=0;
  else ctrl=ctrl;
  end;

Vctrl(n)=ctrl;          %%%%%record the ctrl signal

% To generate Square waveform by adding more point during one period for ctrl signal
  for m=1:10
    if ctrl==1
    pc=pc+1;
    elseif ctrl==0
    nc=nc+1;
    end;
  Vc2(10*n+m)=V0+(0.1*m-1)*I*T/C;
  V12(10*n+m)=V1+(0.1*m-1)*I*T/C;
  Vout(10*n+m)=ctrl;
  end;
end;

%%%Plots%%%
subplot(3,1,1);
  plot(Vout,'b-');
  grid on;
  axis([2000 3000 -0.1 1.2]);
  title('Ctrl Signal vs time');
 hold on;

subplot(3,1,2);
  plot(V12,'b-');
  grid on;
```

```
    axis([2000 3000 1.45 1.55]);
    title('Voltage on capacitor with noise vs time');
  hold on;

%FFT to get signal spectrum
f=5000e3*(0:8191)/8192;
Voutfft=fft(Vout,8192);
pyy=Voutfft.*conj(Voutfft)/8192;

subplot(3,1,3);
    plot(f,pyy(1:8192),'g-')
    axis([2.2e5 2.8e5 0 300]);
    grid on;
    title('ctrl Voltage Power Spectrum');
  hold on;
    Vcfft=fft(V12,8192);
    pvc=Vcfft.*conj(Vcfft)/8192;
    nn=num2str(An);
 title('Ctrl Signal Power Spectrum with noise');
 xlabel('Frequency (Hz)')
 text(2.6e5,220,'noise=')
 text(2.65e5,220,nn)
```

Appendix C. Pin Assignments for Sensor Chips

Table A-1 Pin Assignments for DS_4 (T4AU-AG)

Pin Index	Pin Assignments	Pin Index	Pin Assignments
1	I_plus1	21	VGL
2	I_neg1	22	GND
3	V_151	23	OUT
4	GNDA1	24	GND2
5	VDDA1	25	VDDD2
6	V_C1	26	V_BC2
7	V_REF_1	27	V_REF22
8	V_BS1	28	GATE
9	D90	29	CLK2
10	D0	30	D0
11	CLK1	31	D90
12	Gate	32	V_BS
13	V_REF21	33	V_REF12
14	V_BC1	34	V_C2
15	VDDD1	35	VDDA2
16	GNDD1	36	GND2
17	OUT1	37	V_152
18	V_FEED1	38	V_BS
19	VDD	39	VGR
20	VDL	40	VDR

Table A-2 Pin Assignments for DS_5 (T56B-AF)

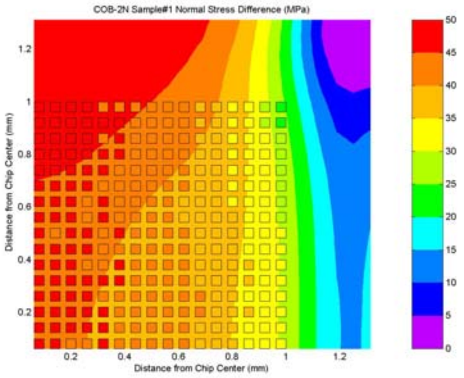
Pin Index	Pin Assignments	Pin Index	Pin Assignments
1		21	VGL
2		22	GND
3	I_Plus1	23	
4	I_Neg1	24	OUT2
5	VDDA1	25	VDDD2
6	V_C1	26	V_BC2
7	GNDA1	27	GND2
8	V_REF11	28	GATE
9	D90	29	CLK2
10	D0	30	D0
11	CLK1	31	D90
12	Gate	32	V_REF12
13	V_REF21	33	GNDA2
14	V_BC1	34	V_C2
15	VDDD1	35	VDDA2
16	GNDD1	36	V_REF22
17	OUT1	37	
18		38	V_BS
19	VDD	39	VGR
20	VDL	40	VDR

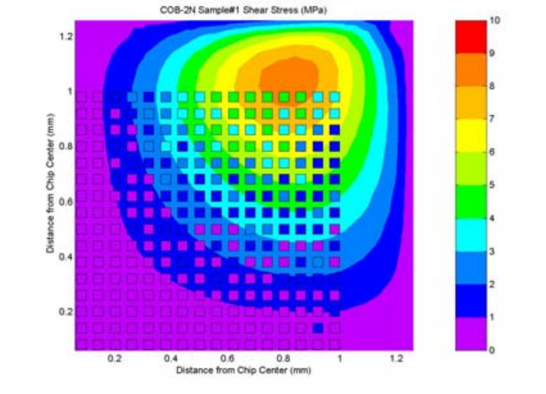
Table A-3 Pin Assignments for Sensor Array Chips

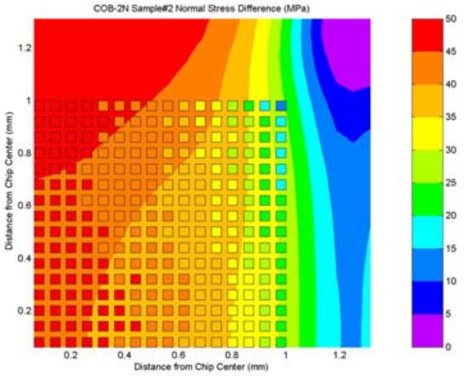
Pin Index	Pin Assignments	Pin Index	Pin Assignments
1		21	
2	3_1	22	VDPp_2
3	3_2	23	VDPp_1
4	2_2	24	VDPp_3
5	2_1	25	VDPp_4
6	GND	26	VDD
7	1_1	27	TEST
8	1_2	28	RQ1
9	I_D	29	
10	I	30	RQ2
11	I_b conner cells	31	
12	I_bias_Arrays	32	RQ3
13	RST	33	
14	CLK	34	RQ4
15	VDD	35	GND
16	CQ1	36	VDPn_2
17	CQ2	37	VDPn_1
18	CQ3	38	VDPn_4
19	CQ4	39	VDPn_3
20	CQ5	40	

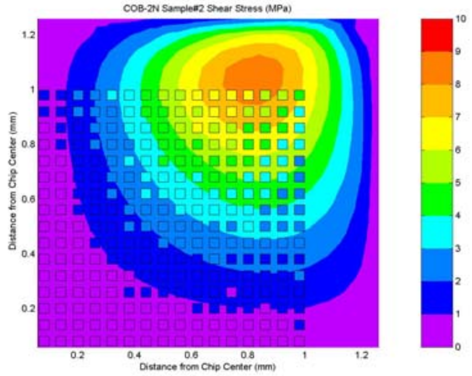
Appendix D. Stress Mapping for Individual Sample of Chip-on-beam under 2N 4PB Load (MPa)

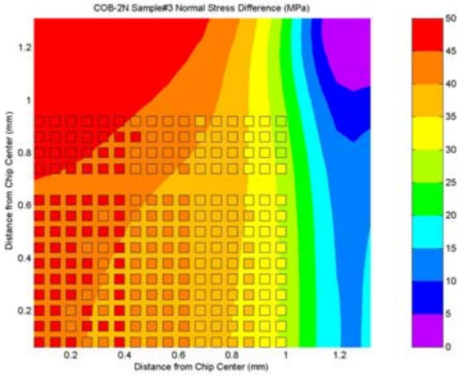
With Chip Mounting Process #1

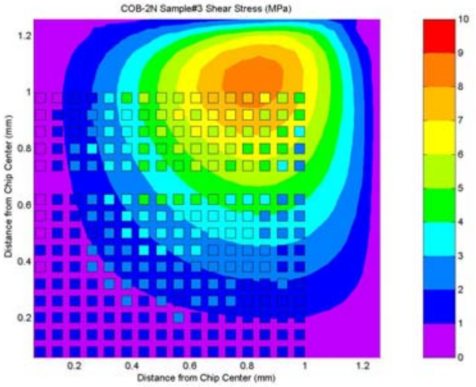

COB-2N Sample#1 Normal Stress Difference (MPa)


COB-2N Sample#1 Shear Stress (MPa)

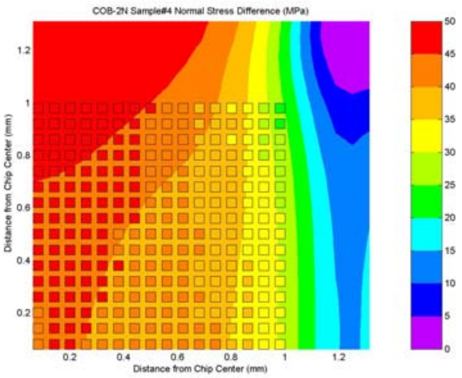

COB-2N Sample#2 Normal Stress Difference (MPa)

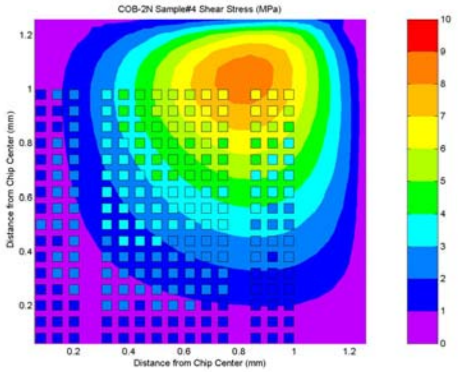

COB-2N Sample#2 Shear Stress (MPa)

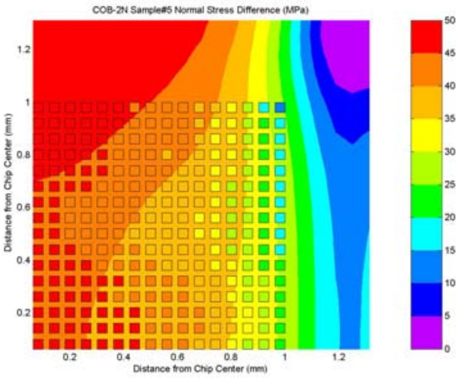

COB-2N Sample#3 Normal Stress Difference (MPa)

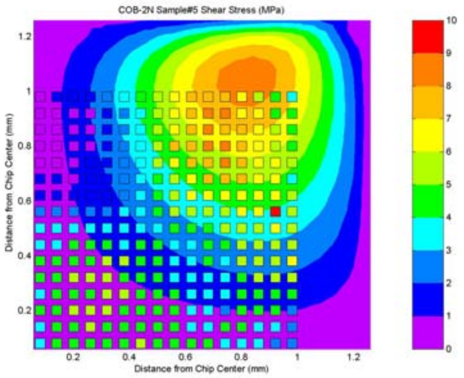

COB-2N Sample#3 Shear Stress (MPa)

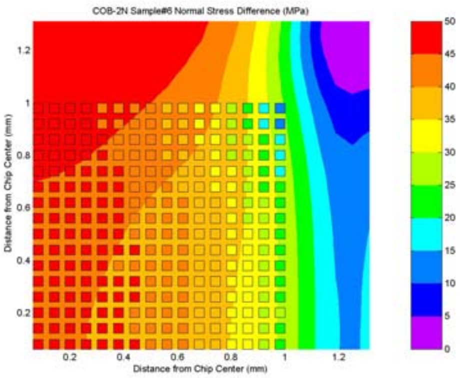
With Chip Mounting Process #2

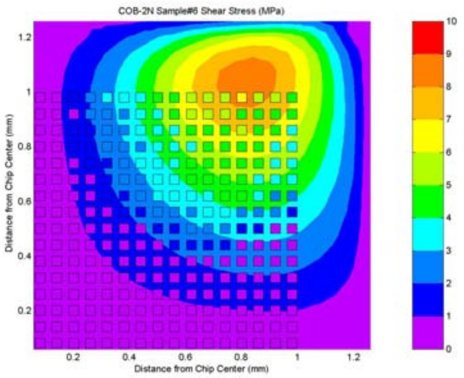




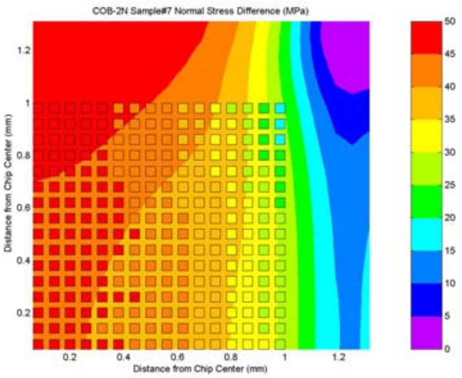


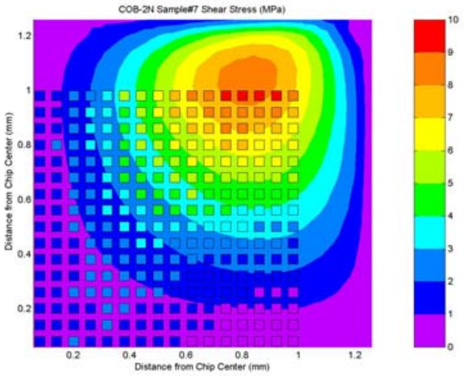


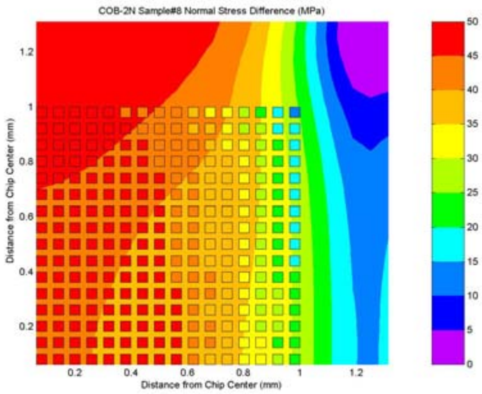


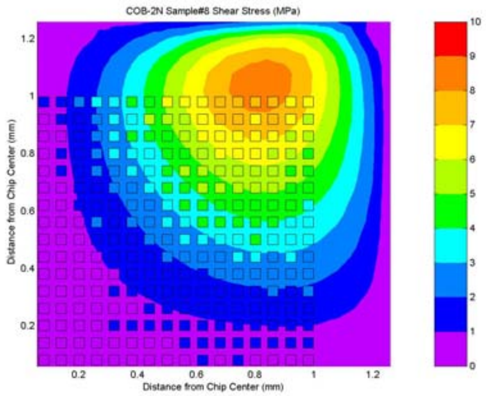


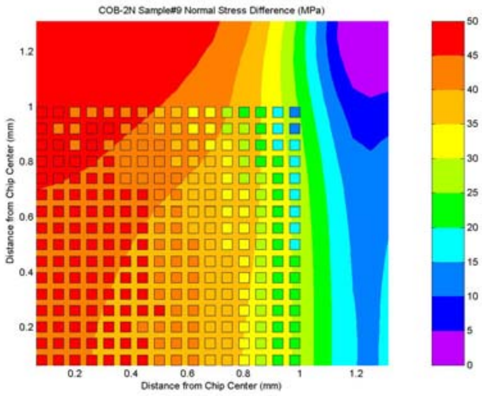
With Chip Mounting Process #2

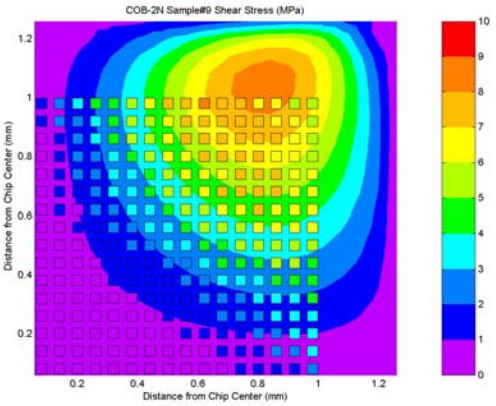












Appendix E. Measurement Stress Data for Chip-on-beam under 2 N 4PB Load (MPa)

$\sigma_x' - \sigma_y'$ COB2N Sample#1 Chip Mounting Process #1

47.20	46.42	46.55	47.42	47.08	47.69	45.85	46.36	46.25	46.07	45.68	46.51	45.87	45.91	46.40	45.97
46.35	47.07	46.85	47.64	46.16	46.48	47.29	46.36	44.88	45.67	45.96	45.52	45.83	45.50	46.84	45.96
46.71	47.21	46.71	46.27	46.67	45.70	46.13	45.83	45.69	45.96	45.89	45.49	45.67	46.52	46.97	44.99
45.26	46.47	47.33	46.47	45.15	45.14	44.90	44.97	45.08	45.42	44.95	45.50	45.58	46.03	45.49	44.56
44.83	45.58	44.44	45.05	46.14	44.79	45.26	45.10	44.69	44.64	44.69	45.22	44.88	45.28	45.10	45.52
44.22	45.34	45.47	45.41	44.95	44.79	44.14	44.32	45.31	44.91	45.70	45.02	44.71	44.45	44.25	43.36
43.19	43.14	43.92	44.19	43.83	43.33	43.02	42.61	42.35	43.67	43.17	44.10	44.13	43.51	43.99	43.98
42.77	42.39	42.41	42.42	43.53	42.46	43.43	43.23	43.20	43.95	43.33	43.44	42.52	42.90	43.14	42.79
40.47	41.49	42.20	42.49	42.23	41.91	41.28	42.27	41.89	41.72	41.84	42.27	42.80	42.56	42.53	42.14
40.19	40.09	40.15	40.25	40.41	40.90	39.66	39.93	40.13	40.26	41.01	41.27	40.71	41.48	41.97	40.11
37.01	38.69	38.37	37.88	38.47	37.60	38.06	38.83	38.63	38.57	39.50	39.28	40.42	40.71	39.55	39.02
36.37	36.27	37.00	36.38	36.95	37.69	37.22	37.51	37.97	38.01	38.03	39.19	38.97	38.59	38.72	38.68
34.88	34.38	33.95	34.98	33.25	34.70	34.43	35.53	35.29	35.83	36.47	36.74	37.02	36.38	36.06	36.67
30.62	31.79	32.59	33.16	33.42	32.72	33.50	33.47	34.10	34.11	35.17	35.13	34.39	35.87	34.67	34.57
27.97	28.40	30.21	30.26	30.41	31.58	32.13	31.20	32.81	32.48	32.93	32.75	32.45	31.96	31.35	32.48
23.70	24.97	25.51	27.59	28.57	29.11	28.62	29.78	30.01	30.17	30.76	30.58	30.67	31.77	30.72	30.66

σ_{xy}' COB2N Sample#1 Chip Mounting Process #1

3.44	3.05	1.77	1.24	1.59	1.12	2.12	1.40	0.90	1.10	0.86	1.04	0.60	1.00	-0.08	0.57
4.00	3.05	2.64	1.66	1.93	1.94	1.42	2.39	2.00	0.92	2.04	1.73	0.97	0.91	1.04	-0.29
4.83	4.10	3.65	2.01	2.42	3.18	1.91	1.70	1.78	0.86	1.74	1.19	0.96	0.47	0.37	0.23
4.32	3.99	3.98	4.21	3.03	1.49	2.34	1.48	1.02	0.93	0.96	1.08	0.27	0.59	0.09	0.38
4.63	4.78	4.20	3.43	3.08	2.70	1.84	1.78	2.09	1.19	0.76	0.72	0.85	0.65	0.82	-0.30
4.41	4.36	3.99	4.13	2.89	2.57	1.43	1.68	2.06	1.10	-0.01	0.76	0.26	-0.09	-0.44	0.07
4.30	4.14	3.86	4.13	2.96	1.60	2.31	1.52	0.91	0.95	1.44	0.33	0.02	0.56	-0.44	-0.36
4.08	3.62	4.01	3.76	2.57	2.92	1.24	1.43	0.88	1.09	0.76	1.27	0.63	-0.03	0.31	-0.90
3.90	3.66	3.16	2.59	2.19	1.69	1.03	1.40	0.19	0.98	-0.16	-0.00	-0.20	-0.00	-1.02	-1.27
3.36	3.02	2.61	1.84	2.97	1.23	1.30	1.19	1.24	0.67	1.07	-0.07	0.02	0.33	-0.16	-0.84
2.62	2.72	2.04	3.20	1.54	2.75	1.34	0.64	1.02	0.58	-0.23	0.15	0.12	0.04	-0.45	-1.07
1.98	2.21	1.32	2.97	1.06	0.43	0.55	0.58	-0.36	0.36	-0.46	-0.56	-0.74	-0.51	-1.35	-0.15
2.32	1.52	0.65	0.49	1.35	-0.14	0.19	0.40	1.07	-0.07	0.47	-0.39	0.10	-0.22	-1.08	-1.29
1.16	0.87	0.69	1.39	0.09	1.15	-0.26	0.01	-0.62	-0.25	-1.12	-0.74	-0.22	-1.35	-0.61	-0.84
0.47	0.46	-0.01	0.71	0.02	-0.96	0.03	-0.48	-0.86	-0.37	-0.29	-1.01	-1.14	-0.51	-1.03	-0.84
-0.39	-0.40	0.12	-0.22	0.06	-0.12	-0.39	-0.80	-1.25	-0.96	-0.43	-0.52	-0.63	-0.46	-0.56	-0.66

$\sigma_x' - \sigma_y'$ COB2N Sample#2 Chip Mounting Process #1

46.60	47.08	47.23	46.49	46.71	46.31	45.74	45.83	45.72	45.21	46.28	46.67	46.43	46.91	47.58	47.62
46.45	46.92	47.20	46.34	46.34	45.43	45.66	46.87	45.90	45.46	47.28	46.62	47.61	47.63	47.39	47.99
46.55	45.50	45.62	45.91	46.26	45.41	45.22	46.48	45.51	45.20	45.61	46.64	47.19	47.90	47.60	45.43
46.74	46.50	45.83	45.38	44.57	45.36	44.50	45.24	45.63	45.90	46.15	46.63	47.28	46.75	46.73	46.10
44.65	45.79	44.39	44.29	43.18	44.45	44.18	43.46	45.13	44.43	46.14	46.21	45.50	46.16	45.83	45.95
44.81	44.44	44.13	44.49	43.53	43.96	43.05	43.22	43.75	44.78	44.84	45.00	46.05	45.84	45.27	44.97
42.86	43.63	42.31	43.34	42.79	42.69	42.06	41.91	43.75	43.30	44.20	45.10	44.45	44.33	45.05	43.60
41.13	42.11	42.19	41.79	41.36	41.70	40.55	40.94	42.50	42.34	41.92	43.36	44.06	44.07	43.63	42.09
40.39	39.92	40.14	39.30	39.88	38.90	38.73	40.05	39.82	40.28	41.09	41.49	42.12	42.55	41.65	41.23
37.34	37.98	38.14	37.55	38.23	38.13	38.09	39.08	39.73	39.73	39.64	40.67	41.01	40.62	41.08	39.43
34.53	34.84	35.43	34.92	35.30	35.00	35.40	35.82	36.84	36.65	37.11	38.52	38.79	38.07	38.23	38.17
32.00	32.76	32.91	32.69	33.05	33.12	33.21	33.50	34.34	34.50	36.32	36.84	36.29	36.84	36.67	35.98
28.86	29.29	30.02	29.00	29.70	30.65	30.53	30.82	30.78	32.54	33.60	33.19	33.80	34.12	34.06	32.67
24.82	25.66	26.23	25.92	26.15	27.06	27.31	28.00	28.47	29.43	29.75	30.26	31.51	31.17	30.52	30.38
19.86	21.05	21.42	22.09	22.47	23.00	23.59	24.87	24.66	25.54	26.88	26.91	27.19	27.17	25.72	26.74
14.87	16.34	17.31	18.10	18.86	19.06	20.06	20.33	20.76	21.84	22.71	23.71	24.10	23.59	23.06	22.96

σ_{xy}' COB2N Sample#2 Chip Mounting Process #1

4.19	3.75	3.53	3.02	2.99	2.87	2.46	2.82	2.51	2.26	1.94	2.05	1.61	1.40	1.24	0.84
5.11	4.73	4.15	3.66	3.39	3.34	2.94	2.85	2.17	2.51	1.76	1.92	1.33	1.08	0.75	0.68
5.66	5.38	4.57	4.33	3.69	3.83	3.30	2.80	2.55	2.63	1.58	1.62	1.17	0.99	0.83	0.76
6.03	5.82	4.92	4.62	4.02	3.91	3.59	3.18	3.06	2.53	1.67	1.73	1.12	1.14	0.75	0.47
6.06	6.07	5.28	5.27	4.40	4.05	3.59	3.26	2.66	2.56	1.86	1.65	0.99	1.09	0.97	0.42
6.40	6.01	5.43	5.30	4.45	4.06	3.78	3.08	2.70	2.32	2.09	1.64	1.10	1.23	0.98	0.64
6.36	5.82	6.90	4.91	4.64	3.79	3.70	3.23	2.78	2.12	1.82	1.60	1.29	1.11	0.74	0.42
5.79	5.57	5.15	4.70	4.57	3.72	3.37	3.09	2.71	2.05	1.88	1.54	1.28	0.85	0.69	0.49
5.18	4.91	4.53	4.54	4.36	3.43	3.49	2.85	2.82	2.01	1.78	1.57	1.33	0.60	0.72	0.45
4.48	4.28	3.96	3.85	3.60	3.46	3.17	2.38	2.48	1.90	1.57	1.19	1.19	0.33	0.78	0.28
3.87	3.62	3.64	2.68	3.16	3.00	2.58	2.13	2.12	1.57	1.28	0.96	1.02	0.67	0.62	0.20
3.12	2.88	2.82	2.74	2.34	2.48	2.12	1.82	1.68	1.37	1.19	0.67	0.87	0.52	0.68	0.23
2.84	2.53	2.38	2.25	1.83	2.00	1.79	1.33	1.28	1.13	0.70	0.54	0.67	0.50	0.52	0.00
2.28	2.11	1.71	1.91	1.52	1.50	1.25	1.06	0.95	0.82	0.92	0.47	0.40	0.40	0.33	0.20
1.75	1.64	1.33	1.09	0.87	0.87	0.94	0.88	0.54	0.40	0.84	0.41	0.37	0.14	0.15	0.21
1.37	1.25	0.74	0.79	0.51	0.66	0.38	0.33	0.70	0.19	0.46	0.22	0.35	0.01	0.10	0.12

$\sigma_x' - \sigma_y'$ COB2N Sample#3 Chip Mounting Process #1

20.94	48.32	48.15	48.51	46.44	1.61	46.30	46.24	45.77	45.44	45.06	46.83	45.35	44.92	44.92	45.05
21.71	46.65	48.43	47.94	47.77	1.64	46.11	46.62	45.50	46.70	45.23	45.72	45.82	45.19	45.54	45.27
21.13	46.69	46.80	46.27	46.63	1.71	46.05	45.83	45.81	45.42	45.64	45.21	45.44	44.58	44.85	45.83
21.99	46.40	46.54	46.66	46.46	1.65	45.93	45.24	45.64	44.81	45.37	46.24	44.73	45.25	45.58	44.64
21.45	47.44	45.89	45.95	46.28	1.54	45.19	44.86	45.15	44.87	44.24	44.60	43.95	44.41	45.32	44.68
21.79	45.99	45.59	45.04	45.03	1.62	44.51	45.20	44.51	44.06	44.46	44.85	44.95	44.61	44.39	44.64
20.81	44.79	45.75	43.92	44.71	1.58	44.39	44.70	44.15	43.45	43.52	43.73	43.54	43.52	43.99	44.01
11.49	43.77	44.40	43.84	44.36	1.73	43.97	43.60	42.89	43.44	42.35	43.09	43.22	43.68	42.81	42.07
-11.99	42.66	43.01	42.29	43.01	1.53	42.54	42.08	41.61	42.06	42.47	42.09	42.59	41.94	42.13	42.00
-30.21	43.16	41.94	41.53	41.73	-0.42	41.23	41.24	41.28	41.33	41.09	40.71	41.49	40.99	41.76	42.15
-8.56	37.17	39.63	39.75	39.43	1.86	39.68	39.51	39.84	39.28	39.55	39.71	39.05	39.32	39.73	39.32
-10.63	38.16	37.85	38.28	38.62	1.46	39.03	39.28	38.50	38.64	38.97	38.38	39.22	39.19	38.61	38.92
-7.44	35.63	36.58	36.24	36.25	1.23	36.23	36.46	36.88	37.32	36.50	36.75	37.33	37.16	37.28	37.56
-9.28	33.22	33.80	34.89	34.45	1.15	34.97	35.33	34.93	35.58	35.37	35.65	35.42	35.76	36.11	35.65
-9.54	30.02	30.71	31.82	32.07	1.26	34.04	33.92	33.85	34.40	34.39	34.79	34.44	34.62	31.66	34.28
-19.67	26.67	27.72	29.14	30.22	0.92	31.58	31.94	32.39	32.85	32.92	33.32	33.14	33.19	33.00	31.94

σ_{xy}' COB2N Sample#3 Chip Mounting Process #1

4.72	4.12	3.49	2.98	2.85	-5.13	2.42	2.23	2.13	1.82	1.82	1.93	1.35	1.37	1.12	1.39
5.85	5.27	4.53	4.16	3.74	-5.21	2.39	2.45	2.06	1.94	1.94	2.04	1.86	1.75	1.58	1.73
6.51	5.78	5.51	4.81	4.08	-5.26	3.37	2.66	2.72	2.04	2.29	1.86	1.71	1.80	1.55	1.72
7.05	6.49	5.71	4.82	5.04	-5.18	3.66	3.18	3.02	2.90	2.44	1.82	1.82	1.87	1.68	1.52
7.07	6.52	5.62	5.61	4.83	-5.17	3.83	3.22	3.01	2.73	2.32	2.26	2.19	1.74	1.40	1.56
7.28	6.11	5.59	5.47	5.00	-5.22	4.25	3.59	3.54	2.72	2.71	2.49	2.10	1.69	1.66	1.54
6.36	5.96	6.01	5.47	5.19	-5.15	4.42	3.65	3.10	3.18	2.85	2.36	2.02	1.81	1.61	1.88
5.82	6.17	5.72	5.61	4.57	-5.08	4.14	3.96	3.23	3.18	2.51	2.27	1.89	2.05	1.77	1.51
5.47	5.25	5.53	4.80	4.72	-5.11	4.05	3.69	3.48	3.01	2.82	2.53	2.27	1.95	1.68	1.50
5.26	4.42	4.54	4.34	4.60	-5.16	4.04	3.33	3.02	3.00	2.44	2.40	1.90	1.79	1.39	1.64
4.09	3.94	3.82	4.00	3.54	-5.14	3.16	3.29	3.11	2.92	2.25	2.27	2.23	1.39	1.60	1.41
3.19	3.20	3.81	3.39	3.64	-5.13	3.03	2.75	2.34	2.44	2.16	2.16	1.76	1.46	1.55	1.46
1.99	2.31	2.25	3.00	2.68	-5.21	2.68	2.52	1.91	2.10	2.09	1.87	2.00	1.45	1.55	1.14
1.57	1.79	1.81	2.03	2.22	-5.14	1.82	1.81	1.54	1.56	1.46	1.76	1.62	1.39	1.63	1.58
0.54	1.11	1.26	1.18	1.66	-5.19	1.19	1.24	1.32	1.22	1.25	1.16	1.19	1.37	1.52	1.46
0.00	0.28	0.61	0.51	0.50	-5.23	0.79	0.94	0.92	1.25	0.72	1.10	1.50	1.40	1.38	1.33

$\sigma_x' - \sigma_y'$ COB2N Sample#4 Chip Mounting Process #2

47.38	48.34	48.35	48.66	47.90	47.23	47.58	46.68	46.59	45.74	46.22	45.54	45.49	44.87	44.78	44.31
48.75	48.22	47.83	47.93	47.49	47.31	46.73	46.36	46.89	47.28	45.96	46.28	45.52	45.59	45.70	45.27
47.19	47.85	48.57	47.28	46.92	47.74	46.96	46.63	46.82	46.91	45.67	45.70	45.47	45.48	45.05	45.50
48.40	46.76	47.89	48.22	47.67	47.56	45.90	46.68	46.90	46.17	46.22	45.76	45.71	45.07	45.44	44.55
48.31	47.22	47.45	46.85	45.65	46.70	46.51	46.67	46.35	46.37	45.58	45.76	45.15	44.93	44.37	43.70
46.00	46.10	47.30	45.39	46.10	45.59	45.44	45.69	44.61	44.61	45.68	44.88	44.30	43.77	44.38	44.68
45.58	45.61	45.74	45.19	45.02	45.05	45.25	45.16	44.56	44.96	44.76	44.89	44.51	44.52	44.62	44.11
45.35	44.70	44.66	44.42	44.17	44.76	44.26	44.12	44.63	44.27	43.58	43.91	42.21	43.92	44.03	43.47
43.39	42.97	42.91	42.88	42.99	43.46	42.81	43.04	42.86	42.76	42.73	42.89	42.89	42.55	43.00	42.74
41.54	41.27	42.31	41.55	42.21	41.61	42.12	41.19	41.76	41.15	41.67	41.80	41.77	42.25	42.97	41.31
39.39	39.92	38.72	39.44	39.45	39.19	39.90	39.55	40.16	40.12	39.00	39.63	40.70	39.83	40.14	40.75
36.77	37.59	36.83	37.82	37.75	38.51	37.86	38.35	38.24	38.89	39.25	39.33	38.97	39.46	40.38	40.12
34.57	35.29	34.42	35.11	35.24	35.99	35.40	35.86	36.55	36.61	37.20	36.86	36.29	37.72	37.77	37.39
30.63	31.56	32.30	32.40	33.03	33.82	34.05	34.31	34.47	34.50	35.17	35.34	35.58	35.52	36.29	36.16
27.20	28.36	28.68	30.00	30.65	31.69	31.97	32.70	32.73	33.27	33.89	33.05	34.15	33.72	31.57	34.32
23.32	24.25	25.68	27.17	28.08	28.96	29.35	30.08	31.21	31.44	31.23	31.70	32.02	32.48	32.37	32.18

σ_{xy}' COB2N Sample#4 Chip Mounting Process #2

6.03	5.38	4.53	3.76	3.26	3.16	3.13	2.54	2.48	2.19	2.06	1.63	1.53	1.45	1.31	1.24
6.92	6.08	5.11	4.29	3.83	3.55	3.38	2.82	2.53	2.33	1.94	1.74	1.72	1.62	1.57	1.41
6.98	6.02	5.60	4.62	4.19	3.77	3.67	3.09	2.78	2.41	2.13	1.98	1.91	1.62	1.70	1.61
NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN
6.33	6.27	5.53	4.96	4.76	4.26	3.75	3.51	3.11	2.86	2.40	2.15	2.01	1.69	1.74	1.59
6.40	6.10	5.44	5.05	4.52	4.23	3.73	3.61	3.09	2.85	2.37	2.15	2.11	1.99	1.80	1.63
5.62	5.94	5.50	4.72	4.66	4.04	3.67	3.53	3.43	2.99	2.59	2.47	2.09	2.11	1.66	1.72
5.42	5.26	5.23	4.89	4.65	4.18	3.84	3.61	3.42	3.00	2.65	2.53	2.36	2.32	1.77	1.66
5.05	5.09	4.96	4.44	4.43	4.14	3.84	3.64	3.44	3.23	2.77	2.54	2.25	2.16	1.81	1.66
4.88	4.69	4.37	4.13	4.35	3.74	3.78	3.67	3.09	3.04	2.88	2.50	2.31	1.98	1.70	1.69
4.19	4.14	4.01	3.81	3.83	3.69	3.31	3.43	3.09	3.01	2.74	2.45	2.37	2.37	1.95	1.76
3.24	3.88	3.42	3.48	3.47	3.57	3.43	3.09	3.09	2.96	2.66	2.39	2.27	2.08	1.80	1.57
NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN	NaN
2.36	2.44	2.54	2.66	2.57	2.82	2.67	2.82	2.57	2.40	2.29	2.30	2.15	1.92	1.84	1.59
2.08	1.87	1.81	2.42	2.36	2.30	2.00	2.08	2.28	1.98	2.02	2.32	1.74	1.75	1.71	1.51
1.48	1.26	1.72	1.79	1.65	1.73	1.73	1.91	2.07	1.92	1.75	1.87	1.60	1.68	1.63	1.69

$\sigma_x' - \sigma_y'$ COB2N Sample#5 Chip Mounting Process #2

50.08	49.93	49.79	48.79	47.55	47.91	45.58	45.77	45.40	46.54	47.99	50.17	50.23	51.70	51.34	50.03
50.59	51.35	49.45	48.43	48.40	47.17	46.93	46.15	46.21	45.85	47.56	48.61	51.38	50.64	51.33	50.57
49.25	49.67	49.42	48.58	47.94	47.04	44.86	44.86	44.69	46.03	47.04	48.12	49.55	50.89	50.36	50.76
48.35	47.40	47.28	47.19	46.93	45.15	44.91	43.70	44.77	44.42	45.89	47.36	49.35	50.85	50.06	49.53
46.48	46.37	46.90	45.64	46.22	44.25	43.36	42.32	42.32	43.17	44.89	46.30	47.52	47.19	48.08	47.35
45.70	45.36	44.66	44.60	43.10	43.01	42.71	41.21	41.30	41.44	43.53	45.21	42.23	46.66	47.52	46.62
43.36	43.74	43.91	43.33	43.12	41.55	40.86	40.53	39.95	40.71	42.51	44.14	44.10	46.33	45.97	45.65
43.98	43.45	42.39	42.58	41.38	40.67	39.73	38.80	38.83	39.60	41.29	43.66	43.25	44.90	44.84	43.85
42.00	40.94	41.44	38.37	40.31	39.52	39.06	38.33	37.67	38.85	39.87	41.74	42.43	43.43	42.90	42.39
40.14	40.58	40.76	40.02	38.75	37.83	36.56	36.25	36.62	37.51	39.48	40.68	41.52	42.45	42.86	42.11
37.62	37.09	37.53	36.95	36.54	35.58	35.54	34.07	34.18	35.25	36.35	37.63	39.31	40.40	41.07	39.58
35.12	34.71	34.70	34.47	33.25	33.57	32.15	32.28	31.88	33.23	34.38	36.01	37.84	38.78	38.77	37.41
30.34	30.65	30.45	30.66	30.19	29.65	28.88	28.37	28.59	29.90	31.07	32.12	34.38	35.24	35.23	34.28
26.13	26.51	26.84	26.15	26.56	25.96	25.60	25.12	26.03	27.20	28.05	29.11	29.46	31.64	31.04	29.82
19.96	21.07	22.19	22.38	22.61	22.39	21.89	21.85	22.41	23.15	24.57	25.81	26.88	28.45	25.46	26.51
14.81	16.46	16.94	17.94	18.32	17.79	18.02	18.23	18.29	19.53	21.01	21.86	23.41	23.92	23.09	22.46

σ_{xy}' COB2N Sample#5 Chip Mounting Process #2

3.80	4.39	4.49	4.88	5.48	3.58	5.60	5.98	5.89	5.68	6.16	5.02	4.55	2.66	2.86	2.30
4.82	4.80	5.42	5.91	6.60	6.08	6.16	10.98	6.48	5.80	5.24	5.36	4.92	4.37	3.42	2.87
5.61	6.11	6.31	6.83	6.76	6.75	6.72	6.09	5.51	5.44	5.45	5.14	4.63	4.19	3.56	3.49
6.20	6.96	7.32	7.74	7.32	7.13	6.26	6.24	5.40	5.22	5.03	4.77	4.55	4.86	4.35	3.76
7.22	8.13	7.93	8.40	8.11	7.42	6.30	5.48	5.15	4.90	4.00	3.98	3.96	2.99	4.02	3.77
7.27	8.25	8.03	8.22	7.91	7.21	6.16	5.64	4.59	4.17	4.19	3.77	3.87	3.96	3.85	4.28
7.04	7.60	7.60	7.76	7.17	6.62	6.03	5.45	4.48	3.32	3.82	3.40	3.78	3.86	3.97	4.24
6.80	6.74	6.92	7.20	6.28	5.71	5.43	5.12	4.16	3.97	3.75	4.00	4.40	4.66	4.14	4.41
5.76	5.53	5.35	5.17	5.13	4.82	4.59	4.55	3.86	4.25	4.05	4.38	4.75	4.68	4.26	4.94
4.25	3.94	3.99	3.90	3.42	3.85	3.11	3.98	3.90	4.63	4.67	4.99	4.87	4.88	4.04	5.06
3.33	2.94	2.73	2.56	2.52	2.65	2.96	3.13	3.73	3.89	5.14	4.87	5.19	4.95	4.57	4.90
2.06	1.68	1.25	1.34	1.48	1.64	1.96	2.82	3.36	4.12	5.18	5.27	5.48	5.10	4.69	5.00
1.24	0.85	0.53	0.61	1.06	1.12	1.58	2.40	3.25	4.35	4.73	5.44	4.22	5.40	5.15	4.98
1.11	0.78	0.33	0.14	0.59	0.95	1.40	2.40	3.38	4.16	4.84	5.04	4.65	5.09	4.54	4.32
1.13	0.39	0.45	0.25	0.76	1.07	1.39	2.54	3.48	3.77	4.71	4.86	4.51	4.36	4.08	4.89
0.11	0.00	0.30	0.67	0.91	1.47	1.82	2.84	3.62	3.96	4.55	4.02	3.90	4.41	3.93	3.81

$\sigma_x' - \sigma_y'$ COB2N Sample#6 Chip Mounting Process #2

46.16	46.54	47.16	46.34	47.28	48.67	47.89	48.41	49.36	49.05	48.43	48.39	47.57	48.19	48.25	48.30
45.76	47.30	47.65	48.29	46.83	49.00	47.98	48.56	48.91	48.29	48.47	47.77	48.32	49.19	48.05	49.65
46.47	45.71	47.89	47.87	47.20	47.61	47.86	49.09	47.80	48.22	48.00	47.48	48.68	48.08	49.01	49.34
45.99	45.84	46.21	47.12	46.74	46.83	46.23	47.47	48.09	47.46	47.17	47.16	47.94	47.76	48.31	47.15
44.87	44.76	45.61	45.60	46.36	46.31	46.39	46.72	46.03	46.80	46.95	47.26	47.36	47.63	46.49	46.83
44.20	44.16	44.95	44.37	45.95	45.75	45.21	45.29	45.61	46.30	44.87	45.90	46.23	46.34	47.06	46.71
42.48	43.27	43.94	43.49	44.59	44.85	44.75	43.80	44.87	45.33	44.96	45.14	45.03	44.55	44.97	45.98
40.36	41.17	42.33	42.00	42.99	42.79	43.36	43.32	43.33	42.83	43.55	43.49	43.43	44.30	43.75	43.89
38.90	39.46	39.83	39.94	41.03	41.89	41.73	41.61	42.45	41.11	41.29	42.98	41.27	41.81	42.10	43.31
36.83	37.05	37.73	38.68	39.77	39.65	40.15	40.26	40.37	40.18	41.46	40.50	41.08	41.19	40.77	41.63
33.22	33.70	34.74	35.29	35.74	36.06	37.19	38.25	37.61	38.66	39.03	39.26	39.08	38.84	39.52	39.26
30.13	30.66	32.51	32.57	33.47	34.45	35.39	35.78	35.94	35.87	36.60	37.52	36.54	37.01	37.21	37.92
26.17	27.16	29.42	28.95	30.35	30.93	31.96	32.02	32.98	33.41	33.77	33.68	33.84	34.32	33.73	34.10
21.75	23.85	25.54	26.10	27.95	28.64	28.41	28.62	30.03	30.26	30.89	31.00	30.54	31.43	31.58	32.09
17.69	19.24	21.04	22.28	23.37	24.56	25.07	25.55	26.75	27.11	27.94	27.50	27.83	27.99	26.35	28.09
13.06	14.92	16.69	17.98	19.43	20.52	21.74	22.84	23.07	23.36	24.46	24.67	24.73	25.21	24.73	24.50

σ_{xy}' COB2N Sample#6 Chip Mounting Process #2

4.70	4.07	3.63	3.29	3.09	3.05	2.25	1.70	0.31	-0.89	-1.63	-1.91	-2.25	-1.98	-1.44	-1.76
5.56	4.84	4.19	3.96	3.66	3.53	2.84	2.23	0.78	-0.18	-1.41	-1.78	-2.05	-1.99	-1.86	-1.84
5.82	4.94	4.71	4.56	4.51	3.99	3.60	2.50	1.34	0.20	-0.69	-1.37	-1.48	-1.60	-1.78	-1.71
6.11	4.84	5.06	4.70	4.74	4.63	4.02	2.71	1.95	0.80	-0.09	-0.60	-1.14	-1.25	-1.52	-1.59
5.82	5.36	4.83	4.95	4.96	4.30	4.15	3.08	2.24	1.23	0.42	-0.28	-0.47	-0.78	-1.15	-1.38
5.31	5.01	4.79	4.32	4.29	4.25	3.82	3.32	2.65	1.50	0.76	-0.08	-0.48	-0.44	-1.19	-1.90
5.05	5.06	4.82	3.93	4.49	4.25	3.69	2.91	2.06	1.46	0.38	0.16	-0.61	-0.58	-1.24	-1.82
4.66	4.08	3.83	3.63	3.95	3.78	3.30	2.72	1.72	1.55	0.58	0.23	-0.41	-1.01	-1.58	-1.84
4.39	3.96	3.96	3.49	3.37	3.32	3.36	2.22	1.17	0.85	0.58	-0.50	-1.23	-1.28	-1.67	-2.43
3.78	3.24	3.22	2.79	3.31	2.57	2.38	1.84	0.54	0.34	-0.54	-1.17	-1.37	-2.02	-2.02	-2.44
3.66	2.67	2.87	2.97	2.51	2.16	1.49	1.07	0.56	-0.51	-1.23	-1.42	-2.26	-2.11	-2.61	-2.84
3.19	2.25	2.55	2.43	1.55	1.40	1.24	0.21	-0.19	-0.49	-1.89	-2.16	-2.09	-2.31	-3.13	-3.10
2.97	2.42	1.88	1.84	1.13	0.58	0.16	-0.60	-1.21	-1.56	-1.83	-2.76	-2.83	-3.14	-3.59	-3.81
1.76	0.87	1.06	1.05	0.58	0.02	-0.45	-1.71	-1.36	-2.14	-2.82	-2.93	-3.43	-3.56	-4.08	-3.73
0.69	0.25	0.23	0.25	-0.27	-0.48	-0.87	-2.10	-2.22	-2.82	-3.12	-3.65	-3.94	-3.71	-4.13	-3.99
0.25	-0.25	-0.48	-0.93	-1.35	-1.86	-2.35	-2.47	-2.85	-3.23	-3.43	-3.39	-3.65	-4.54	-4.09	-4.38

$\sigma_x' - \sigma_y'$ COB2N Sample#7 Chip Mounting Process #2

46.30	46.27	45.68	47.07	46.50	48.11	47.82	47.53	47.84	46.11	46.86	46.70	46.20	46.20	46.43	45.32
46.13	45.78	46.39	46.85	48.08	47.47	47.68	47.38	47.58	47.76	47.25	48.15	46.16	46.81	46.72	46.71
45.21	45.22	46.31	47.22	45.99	47.37	47.20	46.88	47.71	47.71	47.31	47.40	46.91	46.67	47.45	45.62
45.37	45.84	46.96	46.64	47.07	46.08	47.35	47.21	46.64	47.20	47.00	46.78	46.38	45.62	47.03	45.81
45.09	45.39	45.20	45.84	45.35	45.00	46.43	47.32	46.05	46.26	46.50	46.84	45.86	45.11	44.91	45.39
43.85	44.16	44.18	44.34	44.74	46.05	45.77	46.63	46.71	45.68	44.88	44.86	45.31	44.59	44.76	45.23
43.06	43.84	43.02	44.47	44.35	45.00	44.86	44.24	45.16	44.73	44.43	44.58	45.06	44.43	44.47	43.81
42.38	42.35	41.95	42.44	42.69	42.86	43.07	44.27	44.08	43.86	44.06	42.54	43.37	43.06	42.88	43.25
41.02	40.12	41.56	40.83	41.35	41.11	41.37	41.93	41.93	41.82	42.28	42.14	42.66	41.01	41.76	42.25
38.65	39.01	39.61	38.65	39.16	39.07	39.65	40.01	40.53	40.45	40.67	40.53	40.31	40.77	40.93	40.74
35.21	36.28	36.55	36.27	36.60	37.27	36.85	37.93	37.86	38.11	37.97	37.53	39.13	38.48	38.75	39.03
32.16	33.24	33.39	34.22	34.93	35.40	35.05	35.66	35.88	36.28	35.98	36.98	36.46	36.48	36.23	36.81
29.57	30.52	30.89	31.08	31.84	31.47	32.88	33.47	33.67	33.94	34.02	33.63	34.12	34.47	34.25	34.84
25.90	26.55	27.71	28.56	28.97	29.96	30.74	30.70	30.93	31.31	31.11	31.56	32.25	32.92	32.90	32.28
21.08	22.46	23.95	24.99	26.43	26.71	27.69	27.94	28.97	28.94	28.89	29.39	29.47	29.98	28.08	30.74
16.59	18.26	19.53	21.36	22.71	23.27	24.65	25.59	25.80	26.36	27.09	27.41	27.02	27.82	27.97	27.21

σ_{xy}' COB2N Sample#7 Chip Mounting Process #2

8.56	7.97	6.90	6.18	5.70	5.26	4.54	3.78	2.96	1.98	1.46	1.16	0.86	0.65	0.76	0.30
9.80	8.46	7.58	6.89	6.39	5.51	4.61	3.76	2.95	2.14	1.46	1.03	0.69	0.53	0.50	0.11
10.04	8.82	7.99	6.97	6.56	5.64	4.88	3.84	2.96	2.17	1.52	1.04	0.81	0.71	0.44	0.00
9.71	8.89	8.18	7.05	6.60	5.90	4.98	3.99	3.05	2.37	1.65	1.25	1.02	0.81	0.41	0.41
9.54	8.46	8.13	7.16	6.52	5.74	4.88	4.14	3.46	2.58	1.73	1.48	1.22	0.94	0.89	0.59
8.57	8.42	7.59	6.97	6.19	5.27	4.80	4.19	3.19	2.61	2.00	1.56	1.45	1.40	1.04	0.61
8.24	7.83	7.06	6.57	6.01	5.39	5.08	4.14	3.27	2.86	2.29	1.92	1.60	1.31	1.24	0.77
7.55	7.17	6.67	6.41	5.53	5.12	4.62	4.04	3.27	2.86	2.44	2.15	1.68	1.70	1.38	1.07
6.69	6.14	5.95	5.79	5.49	4.75	4.49	4.28	3.54	3.12	2.36	2.51	2.00	1.97	1.48	1.29
5.62	5.70	5.46	5.24	4.51	4.52	4.21	3.66	3.28	3.10	2.68	2.07	2.35	1.93	1.80	1.42
5.11	4.64	4.57	4.23	4.29	4.28	3.57	3.35	3.13	2.76	2.62	2.57	2.35	2.35	1.83	1.78
3.96	3.81	3.72	3.68	3.61	3.14	3.37	3.31	2.76	2.69	2.44	2.49	2.44	2.19	2.07	1.57
2.71	3.17	3.04	3.04	2.98	2.75	2.98	2.60	2.47	2.33	2.32	2.49	2.16	1.96	1.94	1.47
2.35	2.37	2.25	2.33	2.12	2.24	2.24	2.06	2.30	1.93	1.91	1.90	2.48	1.86	1.86	2.12
1.85	1.87	1.99	2.04	1.71	1.76	1.72	1.56	1.63	1.87	1.57	1.78	1.99	1.59	1.47	1.55
1.46	1.44	1.19	1.31	1.54	1.45	1.31	1.29	1.49	1.26	1.44	1.66	1.60	1.46	1.40	1.51

$\sigma_x' - \sigma_y'$ COB2N Sample#8 Chip Mounting Process #2

47.56	48.63	49.52	49.14	49.89	51.03	50.96	51.52	50.63	51.96	53.18	52.50	52.72	51.75	52.39	52.37
48.48	49.23	49.77	49.67	49.96	50.13	50.07	51.69	51.96	50.36	51.68	53.03	51.99	53.05	52.62	53.21
46.84	47.51	49.55	49.67	49.39	49.68	49.70	50.69	51.58	51.24	52.32	52.01	51.98	51.07	52.59	50.93
46.34	47.37	48.89	49.02	49.11	49.86	49.97	49.79	49.85	49.68	50.93	51.48	51.77	51.39	52.14	51.65
46.41	46.06	47.17	48.01	48.58	49.40	49.89	49.78	49.79	49.37	50.45	51.56	50.71	50.13	51.30	51.28
43.88	47.05	46.56	46.71	47.81	48.94	49.15	48.28	49.70	48.97	48.73	50.30	49.70	50.27	49.72	49.25
43.33	44.67	45.51	46.11	46.63	48.43	46.78	46.90	47.74	47.95	47.78	49.20	49.59	48.69	48.61	49.89
42.34	42.89	44.32	44.93	45.78	46.14	45.98	46.79	46.81	45.72	47.59	47.05	46.96	47.29	47.95	47.39
40.47	41.39	42.70	43.10	43.54	44.44	44.87	43.96	44.00	44.54	44.88	45.27	45.48	45.58	46.13	45.40
37.82	39.35	41.00	41.05	42.45	41.98	42.44	42.56	42.12	42.58	42.75	43.92	43.71	43.35	43.47	44.06
34.31	36.52	37.61	38.12	39.17	39.05	38.74	38.79	38.89	38.47	40.34	40.33	39.99	41.18	40.18	39.97
31.53	33.85	34.64	36.03	36.39	36.13	36.15	36.39	36.23	36.55	37.02	37.27	38.52	38.87	38.43	38.33
28.49	29.17	30.91	30.93	31.81	32.53	33.09	32.73	32.51	32.53	33.24	33.21	33.83	34.13	34.25	34.29
23.76	25.08	26.25	27.66	28.44	28.97	28.74	28.60	28.39	28.73	29.05	29.87	29.63	29.85	30.74	30.41
18.67	19.97	21.60	22.76	23.69	24.27	24.18	24.41	24.47	24.75	24.67	25.19	25.84	26.02	24.36	25.52
13.72	15.10	16.51	17.58	18.53	19.24	19.40	19.81	19.81	19.98	20.14	21.06	21.21	21.61	21.33	20.68

σ_{xy}' COB2N Sample#8 Chip Mounting Process #2

6.17	5.79	5.11	4.61	4.33	4.22	3.75	3.66	3.25	2.87	2.45	2.16	1.61	1.76	1.53	0.87
6.77	6.40	5.86	5.31	4.96	4.58	4.19	3.89	3.47	3.01	2.46	1.93	1.73	1.62	1.17	0.79
7.17	7.05	6.49	5.83	5.33	5.04	4.53	4.27	3.66	3.00	2.55	2.04	1.68	1.52	1.34	0.56
7.45	6.82	6.61	6.04	5.69	5.52	4.70	4.29	4.07	3.24	2.40	1.81	1.70	1.35	1.10	0.84
7.84	7.20	6.99	6.23	5.93	5.49	4.93	4.25	3.71	3.08	2.31	1.88	1.64	1.40	1.25	1.01
7.43	7.15	6.62	6.12	5.69	5.14	4.72	4.14	3.64	2.99	2.25	1.99	1.56	1.42	1.17	0.97
6.96	6.67	6.22	5.76	5.26	5.02	4.54	4.07	3.40	2.54	1.95	1.94	1.39	1.49	1.27	1.13
6.29	5.99	5.70	5.00	5.14	4.63	4.02	3.57	3.09	2.55	1.94	1.73	1.48	1.27	1.27	0.91
6.03	5.16	4.68	4.85	4.38	4.01	3.34	3.30	2.52	2.49	1.78	1.60	1.18	1.17	0.93	0.66
4.69	5.02	4.51	3.95	3.90	3.36	3.00	2.29	2.19	1.79	1.46	1.26	1.30	1.08	0.85	0.72
4.40	3.99	4.17	3.03	3.03	2.97	2.53	2.28	1.88	1.83	1.26	1.41	0.90	1.09	0.70	0.53
3.48	3.71	3.10	3.10	2.48	2.11	1.85	1.98	1.44	1.23	0.78	1.11	0.81	1.03	0.59	0.71
3.16	2.57	2.40	2.07	2.24	1.71	1.54	2.00	1.45	0.92	0.87	0.88	0.43	0.79	0.47	0.74
2.37	1.88	1.59	1.54	1.38	1.41	1.18	0.96	0.85	0.64	0.90	0.35	0.81	0.72	0.66	0.58
1.44	1.25	0.98	1.07	1.04	0.74	0.51	0.53	0.41	0.60	0.63	0.19	0.52	0.63	0.46	0.93
1.00	0.08	0.46	0.61	0.00	0.47	0.44	0.28	0.55	0.29	0.21	0.29	0.49	0.61	0.52	0.61

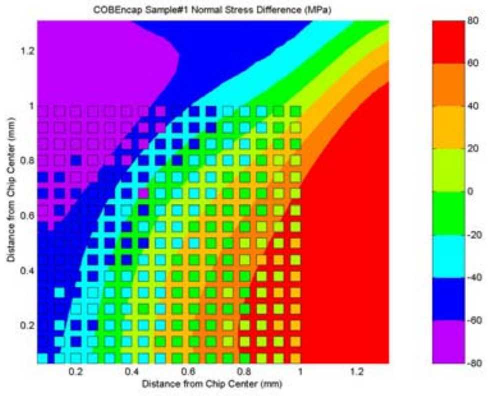
$\sigma_x' - \sigma_y'$ COB2N Sample#9 Chip Mounting Process #2

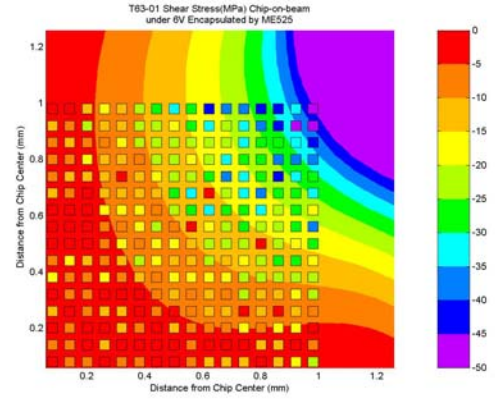
45.34	45.44	46.08	46.74	47.90	47.82	48.58	48.80	49.07	49.51	48.97	49.82	50.32	49.89	48.78	49.13
45.39	44.54	45.84	47.53	47.84	47.58	48.17	49.68	49.99	49.64	48.65	49.33	50.24	49.41	49.64	49.54
43.87	44.98	44.97	46.13	47.24	48.09	48.24	48.79	49.40	49.31	49.73	48.99	48.98	49.34	49.60	49.85
44.33	45.31	45.41	45.63	46.26	47.57	48.11	49.23	48.09	48.32	48.34	48.52	48.91	48.29	48.41	48.49
42.84	45.28	44.57	45.15	45.96	46.96	47.08	47.79	47.04	47.63	48.40	47.85	47.72	46.02	47.90	48.37
42.67	43.09	43.79	43.97	44.80	45.82	46.64	46.29	47.10	46.81	47.39	46.62	46.24	47.06	47.66	46.75
40.90	41.75	42.64	42.92	44.21	45.36	45.04	45.18	45.84	45.51	45.23	45.55	45.84	44.95	45.68	45.65
39.39	39.44	41.47	42.54	42.95	42.15	43.36	43.79	43.60	43.88	44.13	44.10	45.09	44.80	44.04	43.54
36.45	37.53	38.86	39.31	40.20	40.72	41.51	41.72	42.08	42.69	42.18	42.05	42.46	41.07	42.54	43.02
33.58	34.76	35.73	37.38	38.04	38.87	38.82	39.79	40.43	40.53	40.81	40.78	40.85	41.06	40.92	40.81
30.55	32.08	32.76	35.40	35.34	36.73	37.15	36.33	37.65	37.68	37.20	37.43	37.83	37.90	37.48	37.67
27.79	29.01	30.81	31.58	32.73	33.77	34.62	34.66	34.78	35.18	35.36	35.50	35.95	35.91	35.41	36.30
24.59	26.27	27.17	28.11	29.17	30.26	30.97	30.83	31.15	31.79	31.87	31.87	32.18	32.08	32.43	31.58
20.48	21.93	24.06	24.82	26.23	26.86	26.92	27.62	27.41	28.08	28.25	28.57	28.79	29.10	28.85	29.12
16.57	18.21	19.50	21.03	21.92	22.97	23.77	23.95	24.11	24.24	24.27	24.61	24.87	24.98	23.76	24.86
12.30	13.97	15.21	16.55	17.50	18.42	19.16	19.36	19.72	20.20	20.74	20.89	20.73	21.26	20.71	20.29

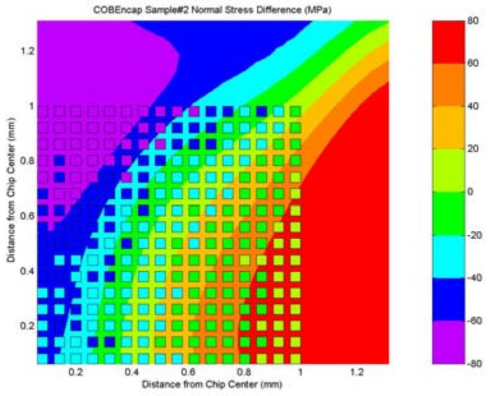
σ_{xy}' COB2N Sample#9 Chip Mounting Process #2

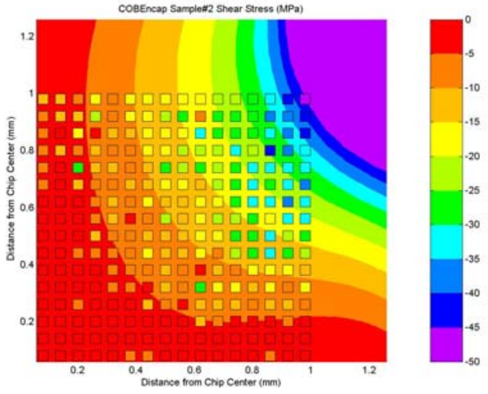
5.36	5.84	5.85	5.88	6.32	6.64	6.33	6.20	5.64	4.93	4.59	4.10	3.80	3.40	3.25	2.42
5.93	6.39	6.33	6.78	6.55	6.97	6.82	6.33	5.60	5.08	4.31	3.77	3.52	3.02	2.47	1.80
6.28	6.50	7.14	6.97	7.09	7.34	6.99	6.43	5.61	5.17	4.25	3.52	3.29	2.72	2.17	1.47
6.83	7.12	7.37	7.05	7.63	7.31	7.01	6.65	5.83	4.77	3.94	3.15	2.70	2.26	1.70	1.17
7.32	7.90	7.50	7.29	7.11	7.06	6.56	5.91	5.33	4.18	3.53	2.98	2.61	1.98	1.52	1.12
7.57	7.66	7.70	7.31	6.70	7.09	6.41	5.53	4.85	4.03	3.15	2.53	2.20	1.75	1.39	0.91
8.13	7.55	7.41	7.39	6.71	6.12	5.95	5.14	4.25	3.47	2.78	2.25	1.63	1.59	0.97	0.73
7.90	7.19	7.56	6.77	6.34	5.67	5.14	4.37	3.72	2.84	2.20	1.86	1.47	1.29	0.77	0.64
7.07	6.81	6.86	6.75	5.46	5.24	4.34	3.71	3.12	2.59	1.89	1.23	1.03	0.78	0.83	0.52
6.11	5.88	5.68	5.51	4.85	4.49	3.77	3.56	2.35	1.90	1.33	1.08	0.80	0.65	0.53	0.15
5.44	5.51	5.05	4.56	3.98	3.85	3.11	2.59	2.28	1.41	1.09	0.53	0.49	0.57	0.33	0.18
4.85	4.63	4.37	3.78	3.08	3.06	2.51	2.19	1.54	1.16	1.04	0.63	0.47	0.44	0.03	0.10
4.09	3.86	3.57	2.93	2.77	2.42	2.11	1.57	1.11	0.92	0.49	0.24	0.45	0.30	0.00	0.04
3.53	2.75	2.79	2.75	2.36	1.56	0.97	1.23	0.86	0.91	0.31	0.28	0.20	0.32	0.25	0.06
2.46	2.05	1.59	1.76	1.14	1.34	1.40	0.66	0.44	0.56	0.65	0.34	0.04	0.14	0.19	0.40
1.25	1.14	0.93	0.73	0.96	0.96	0.42	0.36	0.36	0.48	0.47	0.36	0.23	0.49	0.34	0.12

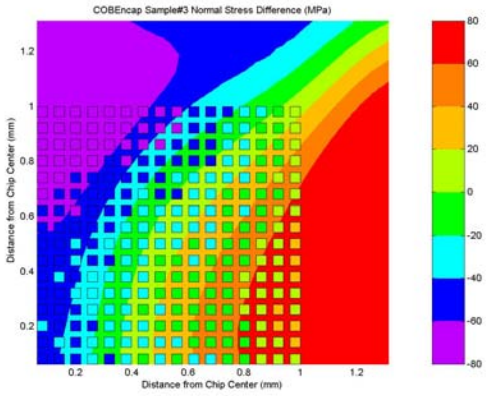
Appendix F. Stress Mapping for Individual Chip-on-beam Encapsulated Samples (MPa)

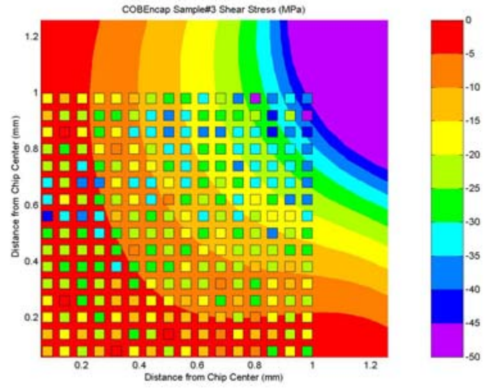

COBEncap Sample#1 Normal Stress Difference (MPa)

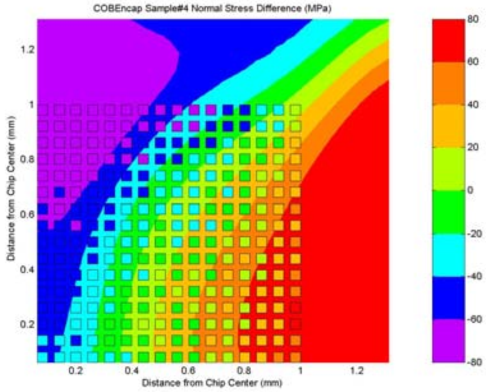

T63-01 Shear Stress(MPa) Chip-on-beam under 6V Encapsulated by ME525

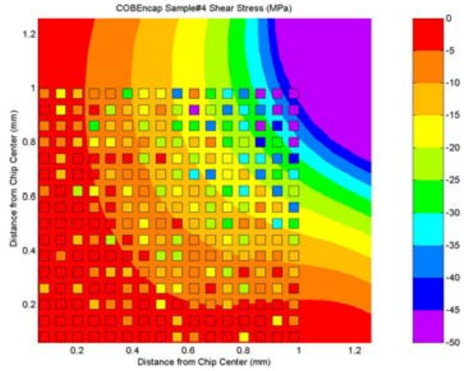

COBEncap Sample#2 Normal Stress Difference (MPa)

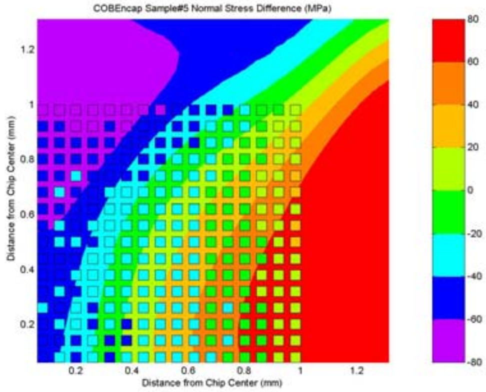

COBEncap Sample#2 Shear Stress (MPa)

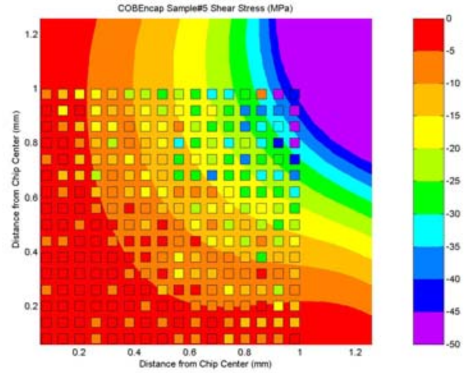

COBEncap Sample#3 Normal Stress Difference (MPa)

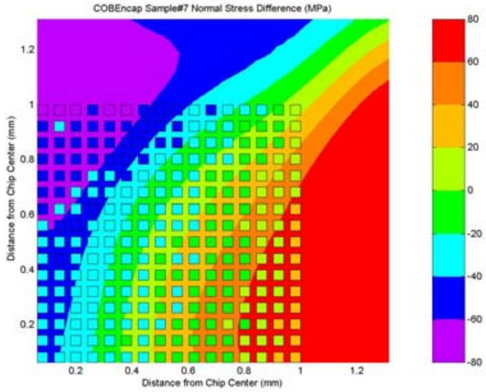

COBEncap Sample#3 Shear Stress (MPa)

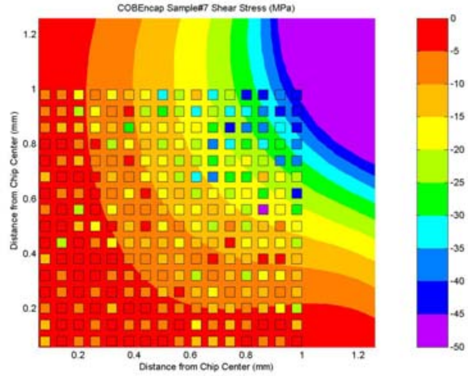

COBEncap Sample#4 Normal Stress Difference (MPa)

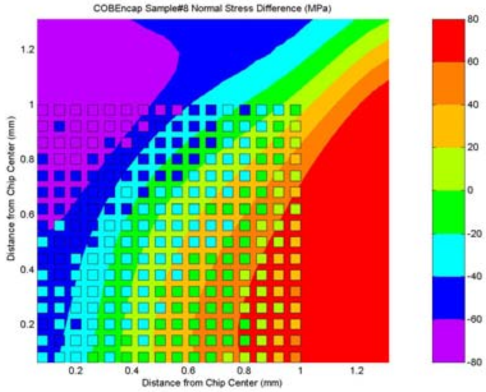

COBEncap Sample#4 Shear Stress (MPa)

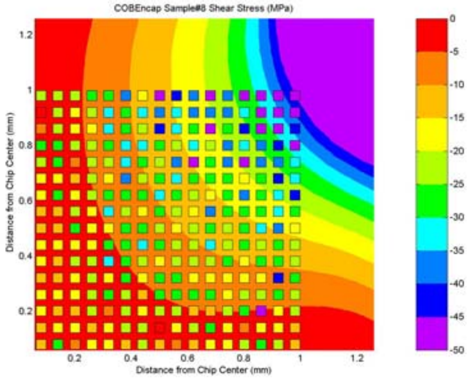

COBEncap Sample#5 Normal Stress Difference (MPa)


COBEncap Sample#5 Shear Stress (MPa)


COBEncap Sample#7 Normal Stress Difference (MPa)


COBEncap Sample#7 Shear Stress (MPa)


COBEncap Sample#8 Normal Stress Difference (MPa)


COBEncap Sample#8 Shear Stress (MPa)

Appendix G. Stress Measurement Data for Individual Chip-on-beam Encapsulated Samples (MPa)

$\sigma_x' - \sigma_y'$ COBEncap Sample#1

22.38	15.30	12.20	-0.86	-6.68	-14.75	-10.15	-5.61	-26.98	-25.92	-28.27	-39.07	-36.57	-24.74	-33.00	-31.23
26.59	15.45	15.21	7.00	3.29	-4.50	-12.85	-16.18	-17.95	-26.47	-31.62	-38.56	-36.05	-40.02	-35.43	-42.66
29.60	20.85	8.88	2.01	2.60	-12.86	-12.69	-17.30	-25.83	-31.58	-33.99	-36.67	-40.55	-47.69	-29.98	-45.64
24.54	10.89	10.73	-1.78	-4.51	-8.08	-10.36	-10.49	-27.34	-19.83	-36.84	-22.04	-30.11	-37.40	-41.40	-40.78
29.90	20.31	10.44	-1.55	0.56	-9.23	-6.76	-16.53	-22.47	-30.27	-30.42	-26.89	-39.35	-40.20	-38.17	-42.13
25.46	12.26	11.73	-5.07	-6.13	-5.45	-12.72	-17.57	-27.85	-32.32	-28.28	-38.79	-45.00	-51.22	-43.35	-40.14
18.51	20.49	21.42	5.17	-1.56	-10.03	-16.48	-16.74	-31.32	-31.84	-40.14	-40.89	-46.75	-40.96	-49.05	-51.79
23.76	11.67	6.75	0.79	-1.09	-10.20	-25.36	-24.65	-32.02	-40.63	-43.16	-49.56	-41.53	-41.84	-48.06	-49.28
14.85	20.00	6.63	-6.57	-14.25	-12.98	-19.49	-30.11	-33.75	-39.34	-44.77	-40.56	-51.85	-55.54	-42.29	-51.07
14.71	10.15	-0.30	-1.62	-10.12	-15.98	-20.56	-21.34	-29.57	-44.02	-33.61	-51.82	-45.98	-45.26	-53.72	-61.26
18.33	1.38	-4.91	-10.44	-16.59	-23.81	-30.44	-37.64	-35.76	-61.94	-50.35	-52.99	-55.22	-56.40	-58.74	-55.41
14.73	3.74	-0.34	-12.56	-18.85	-20.88	-31.73	-38.95	-33.84	-47.92	-56.06	-56.61	-62.38	-62.68	-58.12	-53.69
4.80	8.77	-11.86	-21.63	-22.54	-31.95	-32.80	-44.00	-57.94	-56.67	-61.51	-60.84	-68.58	-55.51	-60.87	-62.71
-2.79	-4.07	-17.91	-21.76	-28.14	-33.33	-40.90	-50.05	-59.81	-61.87	-61.68	-60.58	-73.67	-65.59	-68.62	-65.28
0.59	-12.67	-22.47	-29.50	-30.43	-50.32	-50.72	-51.69	-62.18	-64.90	-77.86	-77.45	-69.30	-84.81	-70.08	-76.89
-7.51	-12.73	-23.12	-32.00	-24.87	-48.17	-52.83	-59.06	-76.56	-69.42	-78.75	-77.42	-79.61	-76.49	-83.43	-86.99

σ_{xy}' COBEncap Sample#1

-50.73	-48.53	-42.75	-38.57	-29.71	-31.26	-16.67	-39.56	-26.54	-19.35	-22.87	-21.32	-9.72	-4.71	-8.51	-23.07
-30.87	-53.08	-33.51	-36.01	-34.02	-29.79	-29.96	-28.89	-17.77	-26.74	-24.22	-17.72	-13.50	-16.76	-3.71	-19.43
-40.07	-43.94	-29.25	-39.70	-43.45	-28.64	-22.49	-24.80	-20.70	-26.96	-23.49	-13.90	3.51	-18.25	-14.42	-11.89
-44.16	-37.93	-29.35	-28.31	-26.77	-36.46	-31.37	-20.65	-2.57	-20.08	-22.35	-14.45	-14.79	-9.42	-12.50	-4.49
-38.98	-32.71	-31.07	-26.18	-32.90	-30.15	-29.87	-27.02	-22.12	-15.48	-20.46	-20.00	-4.45	-17.20	-2.95	-12.04
-37.19	-24.29	-22.91	-31.96	-35.48	-24.47	-26.48	-20.92	-24.50	-14.18	-17.70	-9.97	-11.21	-8.83	-2.85	-12.12
-43.28	-34.34	-24.73	-21.64	-28.96	-4.60	-34.96	-18.70	-21.19	-22.81	-15.27	-13.48	-13.78	-6.54	-4.67	-12.57
-29.99	-26.71	-22.56	-19.37	-21.29	-33.13	-29.37	12.28	-14.21	-13.75	-17.35	-5.58	-7.89	-6.78	-6.59	-8.72
-31.84	-16.04	-24.58	-22.21	-20.22	-27.31	-20.12	-6.31	-15.11	-12.59	-15.61	-14.01	0.84	-11.44	-2.22	-0.31
-27.75	-22.99	-20.82	-24.53	-15.05	-14.07	-8.22	-24.64	-17.63	-16.42	-7.27	-8.24	-7.42	-4.16	-3.06	1.18
-23.24	-22.91	-21.89	-6.68	-13.96	-11.37	-19.16	-16.95	-9.10	-21.95	-10.56	-3.86	21.11	-8.56	-1.57	-6.92
-11.57	-10.77	-16.27	-13.03	-0.83	-12.30	-17.13	-9.49	-16.27	-14.95	-6.68	-0.47	-13.18	-13.64	4.67	-7.64
-16.02	-12.10	-9.08	-12.97	-14.18	-11.33	-18.69	-8.62	-7.96	-6.19	-15.81	-0.77	-10.20	-0.61	-12.35	2.56
-13.39	-23.43	-5.57	-18.71	-14.09	-3.48	-3.92	-3.94	1.95	-14.99	-5.93	-9.61	-9.83	-4.77	-3.48	-8.98
2.01	-5.56	-10.43	-5.49	-14.88	-5.78	-1.78	-3.10	4.69	-16.37	-6.09	-6.03	-3.08	-9.04	-9.87	-6.91
9.14	-14.08	-8.85	-7.83	-7.21	-12.09	4.09	-4.53	4.03	-6.29	-18.83	6.61	-14.47	-2.73	-8.04	8.03

$\sigma_x' - \sigma_y'$ COBEncap Sample#2

16.64	15.23	2.69	-3.27	-10.92	-11.50	-6.99	-21.11	-24.60	-28.53	-30.26	-35.10	-38.82	-27.02	-35.56	-36.69
18.46	5.09	-0.60	-0.68	-10.12	-8.76	-15.96	-12.20	-19.60	-22.58	-33.49	-44.51	-47.09	-33.39	-39.60	-35.41
10.63	8.88	4.90	-7.16	-15.96	-10.30	-14.88	-15.71	-20.82	-27.21	-36.19	-35.37	-37.90	-40.47	-40.02	-37.68
14.35	6.86	-2.95	-9.28	-8.10	-17.59	-13.66	-9.85	-27.86	-25.04	-34.06	-25.65	-36.39	-45.07	-35.65	-33.15
15.30	9.79	-1.08	-8.68	-10.73	-19.71	-16.12	-23.61	-22.90	-28.49	-35.42	-36.34	-35.05	-40.24	-37.79	-39.85
11.14	6.64	-5.80	-3.43	-7.57	-9.17	-15.61	-15.65	-24.09	-23.83	-37.42	-40.63	-43.75	-38.57	-40.35	-44.10
9.83	7.59	3.74	1.04	-9.36	-10.69	-16.27	-16.37	-26.12	-32.09	-35.73	-47.49	-34.92	-38.75	-39.68	-44.48
15.18	0.47	-7.07	-9.50	-12.00	-8.57	-23.07	-17.15	-31.44	-39.82	-47.19	-32.24	-52.04	-53.88	-47.62	-51.23
11.20	0.93	-9.63	-4.73	-13.27	-16.44	-23.70	-22.79	-28.24	-38.00	-39.49	-50.59	-49.66	-53.37	-46.15	-49.64
0.74	-0.09	-4.71	-7.61	-17.29	-22.21	-18.09	-29.14	-32.69	-42.16	-28.31	-46.62	-54.98	-54.13	-58.62	-48.99
2.97	-4.56	-14.71	-13.06	-22.44	-30.37	-26.72	-30.18	-35.68	-45.73	-44.43	-55.90	-57.24	-60.67	-61.58	-50.77
3.71	-4.19	-14.72	-17.08	-23.47	-20.65	-29.04	-33.29	-37.09	-44.37	-60.30	-41.54	-61.00	-60.18	-57.72	-60.72
-5.74	-6.27	-19.05	-23.40	-29.64	-32.77	-39.59	-39.10	-44.90	-52.52	-62.63	-62.86	-67.62	-62.47	-59.98	-64.99
-3.44	-10.95	-23.95	-28.57	-34.57	-40.51	-45.65	-44.98	-62.06	-63.78	-68.85	-64.73	-70.62	-73.13	-75.06	-74.17
-8.73	-21.12	-25.06	-33.81	-34.24	-48.94	-49.65	-55.13	-64.04	-62.48	-68.20	-73.17	-81.05	-80.64	-60.51	-76.20
-12.99	-27.35	-45.80	-36.37	-46.10	-58.16	-63.30	-69.14	-72.73	-77.59	-85.75	-84.75	-86.60	-84.82	-87.14	-83.07

σ_{xy}' COBEncap Sample#2

-53.88	-42.82	-44.51	-31.73	-30.41	-39.09	-30.01	-34.95	-27.63	-22.58	-14.05	-18.45	-5.37	-2.69	2.79	7.58
-43.49	-38.24	-37.68	-35.95	-34.27	-33.83	-36.31	-34.13	-23.67	-29.67	-18.26	-9.05	-13.65	-8.98	1.40	-2.38
-34.39	-39.05	-32.44	-43.74	-30.63	-28.30	-32.45	-18.21	-31.06	-30.38	-16.67	-16.41	-12.31	-4.00	0.70	-6.93
-27.02	-29.05	-25.74	-24.22	-31.47	-32.84	-30.99	-27.00	-28.03	-26.99	-19.63	-13.81	-5.63	2.79	-0.31	4.60
-22.84	-28.49	-26.81	-31.59	-26.00	-26.22	-27.64	-21.23	-26.36	-23.04	-5.79	-15.41	-12.17	-1.05	0.82	1.33
-24.94	-26.85	-26.11	-21.77	-21.62	-24.37	-18.18	-24.25	-16.71	-7.04	-13.20	-17.11	-13.91	-5.92	9.90	-3.27
-16.76	-9.84	-31.55	-24.67	-28.29	-13.55	-17.42	-19.30	-18.33	-15.29	-4.77	-27.11	-14.08	-11.09	6.88	3.31
-16.80	-26.46	-18.70	-21.87	-23.01	-15.47	-14.74	-10.39	-11.51	-10.04	-6.23	-8.27	-1.79	-0.61	0.40	4.53
-17.15	-24.86	-17.24	-19.20	-27.51	-16.35	-13.94	-20.05	-11.73	-12.11	-10.11	-10.60	-9.65	0.93	0.83	0.61
-17.56	-19.83	-18.92	-17.53	-11.73	-10.21	-15.15	-9.90	-14.11	-15.11	-9.77	-1.08	-14.19	3.99	1.09	-5.01
-16.54	-15.59	-10.93	-7.61	-9.71	-13.25	-9.59	-0.71	-8.20	-8.54	-7.70	-8.39	-2.52	1.85	0.02	-8.64
-7.81	-8.03	-12.02	-8.70	-11.93	-8.46	-14.04	-10.33	-6.86	-6.03	-9.70	-9.46	-2.97	2.44	-0.07	-4.64
-19.58	-20.35	1.27	-13.39	-12.23	-9.71	-8.91	-6.23	-10.81	-5.31	0.13	-0.44	1.45	-4.36	-4.33	3.77
-8.16	-13.48	-19.75	-6.24	-29.50	-12.95	4.02	-1.17	-1.53	-5.22	-3.13	7.06	-8.56	8.80	5.20	5.11
-10.27	-10.02	-1.89	-10.22	-1.75	-0.92	0.82	-2.92	0.62	3.40	-4.79	0.84	3.96	-0.82	-1.74	8.16
-10.63	-5.03	-8.18	-6.38	-6.64	-5.99	-0.66	-0.40	0.26	0.27	-1.74	0.17	1.98	-3.99	-4.91	7.15

Sx-Sy COBEncap Sample#3

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   19.76   10.50    0.27  -15.38  -10.35  -21.10  -21.16  -18.59  -23.04  -19.13  -26.09  -42.18  -37.09  -43.30  -55.40  -40.82
   20.17   12.16    5.28   -1.14  -11.23  -13.39  -18.33  -20.97  -22.05  -21.21  -34.43  -34.84  -39.75  -42.28  -37.22  -48.63
   27.08   21.69    0.41   -0.65   -5.98  -13.92  -11.16   -9.90  -12.71  -23.80  -32.57  -29.61  -40.55  -43.36  -46.51  -36.29
   18.00   24.30   16.74    0.09   -8.34   -0.65  -15.54  -12.14  -23.26  -16.99  -25.18  -38.85  -32.09  -42.31  -49.98  -46.97
   14.97   14.37    3.53    0.18  -10.34  -10.50  -13.12  -18.83  -19.64  -21.34  -26.50  -35.55  -36.07  -33.11  -40.34  -40.20
   21.89   13.70    4.94    0.75   -9.83   -7.24  -17.30  -16.36  -18.42  -30.69  -31.87  -36.24  -35.84  -48.34  -39.88  -49.53
   31.28   11.02    1.47   -7.28   -7.59  -10.10  -21.54  -19.29  -16.89  -32.70  -31.43  -43.92  -48.03  -34.16  -48.16  -47.28
   23.76    8.85    2.44  -12.84  -10.22  -23.13  -19.20  -26.75  -32.99  -25.85  -23.67  -32.23  -43.17  -38.63  -54.91  -47.65
   20.99   15.12   -5.94  -11.24  -19.56  -25.31  -26.67  -39.93  -31.65  -36.71  -33.14  -40.66  -43.08  -51.78  -57.98  -52.58
   16.81    3.74   -2.39  -24.28  -12.48  -20.85  -34.52  -30.68  -37.56  -39.74  -40.39  -44.25  -46.06  -61.83  -55.83  -55.69
    9.22   -0.22   -3.11  -17.50  -12.98  -30.49  -29.25  -40.41  -51.68  -38.61  -49.97  -58.66  -51.92  -52.39  -57.88  -64.81
   13.43    4.24  -12.40  -25.24  -28.18  -35.03  -36.83  -35.09  -48.20  -58.94  -51.45  -55.45  -52.94  -57.74  -60.97  -64.92
   14.43   -2.41  -10.65  -25.16  -36.83  -41.59  -46.69  -44.96  -56.44  -55.82  -69.93  -59.04  -60.24  -67.77  -77.78  -71.07
    9.87   -2.97  -13.18  -23.01  -32.14  -40.39  -42.07  -43.49  -60.60  -66.56  -70.01  -70.10  -73.55  -70.43  -80.94  -83.19
    1.52   -7.38  -19.09  -38.76  -26.93  -54.75  -57.16  -62.52  -76.24  -74.93  -71.64  -83.69  -90.71  -80.26  -72.10  -91.28
    8.77   -9.10  -22.47  -31.72  -41.81  -49.52  -54.32  -68.89  -74.27  -78.01  -81.65  -83.67  -80.89  -88.03  -90.31  -86.43
```

σ_{xy}' COBEncap Sample#3

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  -38.11  -48.03  -41.96  -35.77  -37.18  -38.18  -35.60  -30.70  -26.13  -25.77  -20.81  -19.56  -22.78  -18.29  -19.07  -28.10
  -33.83  -22.28  -38.15  -33.28  -32.22  -34.49  -37.33  -19.43  -22.23  -25.97  -13.15  -13.71  -21.10  -20.96  -23.13  -16.86
  -39.19  -42.92  -40.07  -32.57  -31.84  -34.31  -28.23  -19.86  -35.59  -24.33  -22.17  -17.01  -18.34  -16.97  -14.45  -26.46
  -54.91  -22.32  -33.38  -30.66  -30.56  -34.99  -19.71  -21.66  -20.30  -20.88  -13.27  -26.57  -26.51   -9.69  -13.84   -7.98
  -39.13  -26.91  -34.30  -33.68  -38.85  -27.93  -33.30  -33.64  -26.37  -22.62  -21.65  -20.14  -12.45  -20.19  -18.47  -11.53
  -20.77  -27.13  -37.23  -25.93  -28.91  -21.99  -28.15  -22.70  -17.76  -18.14  -21.89   -8.14  -26.63  -14.56   -6.36   -9.63
  -34.96  -29.97  -37.86  -26.67  -27.14  -27.10  -22.63  -32.91  -25.51  -18.84  -20.12  -20.32  -19.13  -11.06  -13.65  -14.84
  -26.54  -34.11  -33.40  -33.78  -32.28  -33.11  -28.13  -15.80  -18.76  -26.82  -18.34  -23.62  -10.38  -14.81  -12.97  -17.18
  -27.17  -39.30  -37.17  -32.21  -28.29  -19.35   -9.68  -20.46  -23.45  -23.35  -25.95  -22.19  -16.65  -11.06    4.25  -24.14
  -24.86  -32.01  -32.05  -22.50  -18.24  -34.52  -34.50  -26.48  -23.69  -25.95  -27.13  -17.31  -15.47  -16.21  -23.06  -12.53
  -13.24  -20.57  -34.65  -15.32  -19.61  -34.46  -18.88  -23.92  -20.26   -9.07  -27.28  -25.82  -13.58  -11.82  -29.87  -16.99
  -19.15  -28.96  -16.00   -5.00  -22.12  -16.89  -24.23  -14.89  -26.23  -29.30  -30.93  -14.31  -11.89  -17.34  -13.20   -3.05
  -17.04  -29.44  -27.43  -15.46  -25.49  -36.64  -27.56  -34.72  -33.01  -23.11  -27.86  -20.68  -20.56  -27.35  -24.76  -13.24
  -16.34  -20.57  -16.50  -24.39  -32.41  -36.14  -24.25  -38.28  -28.90  -24.07  -27.36  -25.21  -28.98  -15.27  -14.38  -24.57
  -11.89  -22.10    1.13  -28.04  -23.34  -23.66  -17.55  -30.30  -24.88  -24.93  -26.28  -22.41    2.75  -22.12  -17.88  -16.87
  -17.29  -14.18  -15.81  -24.01  -24.50  -33.17  -32.65  -43.40  -27.96  -24.47  -23.18  -24.04  -16.81  -19.32  -13.72  -14.07
```

$\sigma_x' - \sigma_y'$ COBEncap Sample#4

```
   54.27   40.57   37.39   29.78   17.57   11.04   -8.42  -12.47   -2.98   -8.91  -20.20  -34.04  -32.91  -35.85  -23.80  -33.59
   49.75   31.53   21.34   20.95    5.91   21.80   -6.94   -5.29    4.32   -6.00  -14.77  -19.49  -29.38  -40.23  -34.34  -37.58
   60.99   39.31   30.75   17.80    6.29    7.43   -0.66   -2.65    2.35    1.22   -9.25  -18.48  -31.31  -29.08  -46.40  -45.06
   67.51   38.00   32.41   13.45   25.31    8.31   10.07   -9.24    1.21   -7.32  -12.23  -30.02  -28.15  -39.75  -49.63  -43.42
   57.54   29.22   21.98   23.13    5.79    4.05   -1.43    1.55  -18.46   -9.06  -16.61  -28.45  -31.34  -47.68  -40.15  -46.88
   43.36   36.94   19.84    8.17   28.17   -0.37    3.87  -12.32    0.24  -20.13  -25.60  -34.86  -33.81  -50.01  -50.52  -45.11
   39.96   32.77   17.75   20.51    7.62   -6.07   -1.75  -13.22   -1.25  -15.87  -25.72  -35.67  -54.07  -52.24  -44.17  -53.54
   45.16   37.77   22.60    1.67    8.41  -14.29  -19.31  -24.53  -16.39  -25.68  -39.17  -38.50  -56.73  -43.07  -47.25  -59.23
   38.33   26.82    3.61    3.18   -9.60  -23.42  -33.71  -27.87   -2.28  -28.06  -31.10  -42.86  -49.98  -60.30  -59.24  -55.74
   49.76   36.67   15.37   -2.15   -5.63  -13.11  -22.36  -25.77  -27.25  -34.03  -35.15  -44.20  -48.11  -58.41  -60.28  -59.59
   34.02   30.20    7.51   -4.06  -21.02  -17.54  -33.17  -34.76  -28.35  -52.15  -54.17  -52.60  -48.87  -67.10  -57.03  -74.64
   30.94   12.05    1.81  -16.03  -10.50  -27.89  -31.68  -33.09  -33.60  -40.85  -55.06  -55.30  -63.93  -64.51  -62.71  -83.22
   20.45    8.26   -0.96  -19.23  -24.58  -39.19  -38.50  -46.98  -40.96  -62.65  -68.69  -77.36  -73.77  -74.63  -85.77  -80.01
   24.19  -14.49  -19.74  -19.21  -36.15  -54.74  -55.69  -57.78  -56.32  -54.14  -66.03  -80.23  -83.52  -79.70  -97.17  -91.53
   15.68  -20.00  -20.71  -41.23  -54.04  -55.05  -71.28  -71.18  -64.62  -74.22  -83.70  -86.50  -86.58 -104.88  -73.27 -107.67
   11.81  -27.38  -38.92  -48.65  -54.83  -62.39  -86.99  -84.67  -76.51  -89.88  -91.57  -96.40 -107.18  -91.29  -94.69 -124.13
```

σ_{xy}' COBEncap Sample#4

```
  -52.72  -49.66  -54.32  -46.95  -40.63  -31.58  -22.84  -35.82  -26.59  -22.63  -14.28  -11.61    6.07   -6.06   -5.34   16.19
  -51.09  -49.58  -40.50  -27.73  -38.99  -25.17  -37.82  -10.10  -33.05  -13.74   -9.59   -2.83  -11.32   -4.45  -16.51   -2.33
  -48.29  -39.95  -48.88  -41.30  -30.24  -36.85  -11.47   -7.86   -6.67  -14.35   -8.16  -14.03   -6.32   -1.49   -3.69   -0.83
  -36.62  -32.21  -34.17  -23.90  -31.59  -10.44  -30.82  -24.63   -9.05  -24.23  -13.50   -0.44  -20.55   -1.81   -0.13  -17.66
  -31.36  -36.53  -26.37  -29.78  -19.74  -19.64  -27.20  -17.26  -29.87  -19.59  -11.81  -20.77  -13.07  -14.11   -0.31    1.80
  -29.09  -20.86  -36.78   -5.99  -13.67  -37.80  -24.82  -24.91  -20.63  -14.78   -6.31  -15.68    2.41   -6.69    9.41    1.24
   -9.70  -45.93  -26.40  -14.01  -23.12  -30.51  -13.82  -19.49  -11.78   -9.02   -6.76   -6.95   -8.68   -7.29   -1.55   -8.86
  -35.39  -23.21  -26.40  -23.76  -17.19  -24.89  -17.53  -12.97   -4.38  -21.52  -20.03  -12.99  -16.25    9.17  -12.81  -13.30
  -18.29   -9.36  -13.38  -23.44   -2.87  -14.20  -24.31  -13.83   -6.85  -10.42  -21.31  -10.10  -19.44  -16.17    2.51   11.66
  -17.99  -19.90  -24.07   -8.74  -20.71   -8.72   -8.16  -10.06  -19.10  -19.18    3.33   -7.13   -6.73   -4.71    6.32   10.56
  -28.13  -14.93  -13.68  -14.95    5.24   -9.29  -16.01  -13.22   -6.92   -1.82   -1.82  -14.10   -8.94   -7.63   -5.88   -1.12
   -7.14  -22.02  -12.81  -16.50   -3.13  -14.26   -4.64   10.44    4.03  -20.91   -1.12  -12.69    1.52   -5.33   -1.00   -1.15
   -6.02   14.14  -28.02  -17.81   -4.66    5.49  -18.71   -5.17   -3.12   -6.52   -4.24   -5.11   -3.22  -10.29    5.16    7.85
  -10.69   -7.58   -8.32  -10.02   12.67   -4.91  -20.07    2.29   -2.60  -10.23   21.64   -1.01  -10.41    3.52   -3.11    5.62
  -17.86  -15.71   -6.67   -7.03  -11.81  -10.01   -0.63    4.43    5.73   -2.21   -5.42    2.35   19.48    7.43    1.81    5.22
   -7.83   -0.70   -6.20   -5.85    8.82    6.66   -7.14    4.72   14.73   10.54   -1.82   11.15  -10.60    0.82    6.00   -1.55
```

$\sigma_x' - \sigma_y'$ COBEncap Sample#5

```
   12.32    4.48   -5.90   -4.24  -18.49  -23.29  -28.85  -32.60  -30.92  -35.62  -36.59  -46.67  -38.93  -43.08  -39.18  -48.07
   13.02   13.13   -0.69   -6.23  -22.37  -19.67  -24.35  -28.16  -29.57  -22.73  -44.39  -40.29  -35.33  -43.53  -43.35  -47.37
    9.40   11.59   -2.62   -3.99  -14.63  -13.92  -27.95  -31.87  -33.19  -34.46  -40.99  -37.81  -40.12  -33.14  -38.40  -43.58
   19.16    4.15   -1.37   -6.20  -21.59  -19.69  -21.45  -26.08  -34.11  -37.29  -30.94  -34.10  -41.60  -39.01  -47.58  -37.12
   17.26    5.56    1.63   -7.87  -18.14  -15.16  -25.35  -20.50  -30.71  -34.45  -33.84  -28.83  -37.79  -40.15  -36.86  -40.10
   18.15    5.26    7.28   -7.20  -13.30  -18.18  -25.36  -20.91  -36.22  -29.22  -35.16  -26.93  -32.30  -37.26  -40.81  -44.86
   16.58    5.91   -0.57   -4.75   -9.11  -13.78  -23.48  -25.29  -29.08  -29.07  -34.78  -37.16  -39.65  -40.93  -45.35  -44.84
   22.28    7.03   -2.09   -5.03   -8.69  -19.16  -23.81  -29.75  -31.79  -37.23  -39.83  -33.84  -42.28  -37.35  -38.25  -41.14
   36.62    9.25    2.79   -0.85  -12.48  -16.79  -24.97  -24.68  -31.64  -26.99  -38.39  -38.66  -28.39  -46.23  -36.56  -40.12
   19.00   11.02    6.45   -4.54  -12.84  -17.23  -24.00  -31.88  -33.02  -36.61  -37.74  -36.58  -42.55  -46.40  -43.06  -44.18
   20.69   10.97    6.19   -8.67  -16.18  -13.88  -24.30  -32.05  -34.61  -36.88  -36.80  -38.73  -40.15  -43.23  -38.79  -49.63
   25.48   11.71    2.35   -8.72  -18.53  -20.88  -26.21  -35.67  -34.69  -46.90  -41.96  -41.09  -41.87  -37.27  -49.28  -41.40
   19.96    5.96   -1.33   -9.38  -15.96  -21.39  -34.34  -37.94  -45.95  -45.12  -45.83  -49.98  -54.46  -48.94  -52.44  -54.16
   17.87    2.34   -2.61  -12.38  -27.85  -28.11  -40.79  -42.06  -52.45  -54.10  -56.45  -55.12  -51.66  -57.79  -54.75  -58.22
   11.60    5.82  -13.75  -23.61  -30.79  -35.19  -46.59  -43.12  -59.51  -57.33  -62.35  -57.91  -66.13  -63.86  -48.97  -57.44
    0.23   -3.80  -19.67  -21.51  -41.87  -49.97  -51.90  -55.63  -62.25  -68.86  -63.87  -64.04  -69.56  -67.73  -70.72  -70.16
```

σ_{xy}' COBEncap Sample#5

-44.26	-45.37	-45.53	-46.65	-42.29	-35.34	-33.65	-29.94	-20.29	-17.81	-13.95	-14.85	-8.03	-13.76	-14.17	3.76
-49.66	-36.63	-31.41	-40.99	-27.33	-33.47	-25.54	-22.54	-27.01	-21.26	-12.16	-6.85	-20.15	-19.18	-14.39	-8.71
-6.26	-38.04	-33.71	-34.02	-28.59	-33.17	-28.24	-15.60	-20.63	-9.27	-26.85	-1.21	-12.57	-3.95	-11.90	-7.64
-25.61	-36.97	-35.38	-23.43	-35.36	-27.09	-28.60	-24.28	-12.49	-23.02	-11.78	-6.20	-13.25	-7.01	-11.00	-8.78
-32.52	-25.18	-29.21	-31.29	-26.44	-25.39	-19.99	-17.46	-21.32	-16.98	-5.30	-6.40	-19.74	-6.51	-5.51	-11.21
-30.89	-17.55	-28.41	-23.13	-24.60	-35.03	-6.61	-15.10	-9.08	-18.28	-8.66	-11.13	-6.20	-7.61	-3.70	-2.72
-25.96	-26.79	-24.84	-27.77	-18.23	-28.58	-9.51	-20.84	-19.88	2.66	-13.70	-11.09	-1.45	-6.78	-7.53	-8.53
-23.41	-17.72	-9.16	-33.17	-25.83	-28.78	-7.65	-14.87	-8.21	-8.26	-17.07	-17.74	1.31	0.22	6.12	-6.44
-27.33	-23.75	-19.82	-18.81	-11.33	-14.75	-19.75	-11.39	-4.42	13.21	-8.89	2.82	-10.28	-1.43	-8.78	1.67
-22.35	-18.51	-19.09	-10.78	-12.72	-19.23	-15.25	-7.86	-14.58	-4.03	-2.42	-9.17	-2.07	-6.42	0.26	6.70
-24.68	-13.38	-7.86	-8.91	-19.03	-10.58	-14.00	-0.93	-9.53	-5.00	-0.01	-6.33	4.81	-3.46	-7.31	-3.91
-12.41	-10.30	-16.77	-21.84	-10.22	-6.96	-5.15	-8.19	3.49	-7.91	4.45	-3.14	-6.76	-2.88	-1.78	-4.83
-15.40	-17.35	-16.19	-11.97	-10.05	-20.93	-11.96	-5.87	15.46	2.56	0.31	-0.75	-1.52	2.77	-8.36	-8.06
-16.95	0.91	-10.76	-8.05	-10.75	-12.06	-2.07	-4.24	-8.11	4.20	-0.35	7.09	7.19	3.77	10.00	1.55
-13.44	-15.36	-8.67	-1.99	-4.35	-12.90	-5.44	-4.73	-1.63	-8.96	14.38	-1.45	11.90	18.11	-3.67	5.75
-8.03	-1.25	-2.31	-3.56	-5.81	6.44	5.92	6.36	9.95	-5.65	-0.38	3.86	-7.88	2.46	0.16	-0.48

$\sigma_x' - \sigma_y'$ COBEncap Sample#7

27.92	23.78	12.79	4.41	-6.17	-2.43	-7.42	-16.02	-17.89	-20.54	-27.70	-23.99	-32.16	-28.91	-25.50	-24.88
33.47	18.09	7.40	2.61	-11.02	-5.33	-9.27	-16.45	-16.87	-20.88	-19.98	-24.89	-30.32	-27.13	-33.88	-39.28
23.69	26.21	6.00	-1.99	6.60	-5.82	-12.93	-9.95	-24.43	-23.13	-24.78	-28.92	-25.68	-28.62	-34.35	-31.53
29.74	17.06	6.34	1.64	-3.95	-7.28	-9.22	-21.03	-11.16	-30.55	-28.62	-26.38	-27.65	-30.47	-31.52	-36.96
28.93	10.52	8.81	3.11	-4.99	-1.65	-14.97	-20.01	-19.02	-22.87	-25.17	-28.83	-26.18	-33.86	-29.83	-25.43
29.22	4.77	11.53	-6.67	-1.57	-12.40	-13.41	-19.50	-14.51	-21.82	-33.07	-25.50	-36.78	-35.67	-36.64	-28.71
22.48	10.08	7.21	-0.65	-3.85	-10.61	-21.80	-20.95	-15.80	-23.53	-26.12	-26.84	-33.30	-38.12	-42.55	-34.68
32.67	15.78	0.84	-0.10	-9.14	-12.38	-16.22	-17.46	-22.29	-30.79	-35.83	-33.41	-37.38	-36.83	-35.53	-34.71
27.25	18.17	2.54	0.49	-8.15	-9.15	-23.46	-28.44	-30.34	-26.11	-38.05	-35.69	-36.21	-43.63	-40.32	-35.02
24.77	12.72	7.48	-7.30	-13.77	-13.20	-20.17	-28.55	-31.53	-25.56	-30.31	-32.55	-44.75	-31.66	-39.02	-43.50
16.48	8.86	1.81	-7.04	-14.99	-15.65	-27.96	-28.96	-26.73	-32.65	-37.15	-32.76	-35.65	-36.88	-42.07	-40.81
19.78	13.14	2.32	-6.72	-19.19	-17.71	-24.07	-33.43	-34.67	-34.55	-48.14	-37.24	-35.59	-46.25	-48.49	-42.56
16.96	4.24	-1.53	-8.20	-20.33	-24.35	-30.96	-32.81	-35.97	-46.07	-53.44	-40.74	-50.60	-51.96	-52.38	-54.10
13.83	-2.54	-10.60	-9.59	-21.62	-26.46	-31.83	-41.58	-41.19	-50.44	-43.60	-49.73	-50.05	-51.83	-49.67	-58.09
8.18	-3.90	-6.69	-18.78	-27.81	-30.22	-33.41	-43.31	-44.05	-48.97	-54.62	-51.69	-57.08	-52.28	-35.61	-59.51
6.76	-3.06	-27.33	-25.62	-34.42	-41.30	-39.28	-50.44	-45.65	-55.00	-60.24	-62.64	-56.84	-68.16	-75.60	-61.21

σ_{xy}' COBEncap Sample#7

-41.32	-42.13	-44.29	-36.56	-37.37	-24.37	-41.31	-25.15	-18.95	-20.94	-14.31	-13.89	-12.00	-23.50	-12.58	3.15
-37.67	-40.93	-31.64	-28.49	-39.63	-16.67	-19.22	-17.78	-9.92	-17.75	-3.64	-17.80	-8.48	-16.92	-2.44	-9.66
-42.84	-39.07	-36.64	-31.82	-24.52	-11.38	-25.32	-49.38	-13.22	-15.78	-4.27	-17.68	-13.84	-10.30	-4.59	-7.83
-40.69	-33.34	-39.53	-27.87	-16.86	-26.31	-17.03	-20.38	-20.72	-17.33	-13.60	-21.18	-11.24	-6.21	-9.09	5.50
-24.67	-30.37	-41.69	-31.01	-24.05	-25.19	-24.16	-18.69	-9.93	-0.98	-11.02	-12.62	-8.31	-11.21	-10.87	-10.47
-34.76	-20.99	-29.19	-35.10	-25.25	-35.68	-17.97	-10.32	-21.45	-11.62	-0.96	-9.73	-16.63	-10.32	-7.99	-13.94
-13.59	-33.63	-19.66	-21.25	-23.54	-30.33	-20.03	-17.08	-17.80	-11.38	-6.92	-20.47	-12.22	-5.23	-15.67	-12.77
-20.32	-20.87	-19.02	-19.03	-24.06	-20.25	-14.30	-16.95	-6.06	-18.99	-14.57	-11.77	-2.18	-7.35	-1.57	-5.44
-32.20	-25.14	-18.91	-21.09	-16.21	-18.99	-18.17	-14.68	-15.51	-11.55	-12.09	-9.43	-14.99	-6.67	-9.22	-3.80
-18.37	-20.75	-18.22	-12.81	-17.32	-18.18	3.53	-5.39	-2.04	-12.97	-8.66	-7.88	-8.79	-3.83	-8.05	-4.89
-14.17	-3.75	-27.05	-19.74	-3.44	-6.39	-15.51	-5.35	-11.44	-13.89	-8.38	-8.54	-7.25	-3.90	-5.07	-2.92
-18.43	-8.11	-14.53	-20.62	-9.83	-13.71	-8.52	-16.85	-4.15	-19.98	-2.17	-9.41	-1.79	-13.08	-1.23	-0.35
-7.82	-16.06	-17.63	0.58	-8.13	-4.47	7.07	-1.09	-16.79	-5.16	-1.86	-3.80	-7.71	-1.23	-9.03	-9.78
-15.90	-23.70	-13.22	-8.41	-13.71	13.42	-7.39	-20.76	-10.03	1.06	-1.33	-3.65	13.16	-8.22	-2.50	-6.77
-5.28	-8.11	-11.02	-3.44	-8.63	-3.25	-7.44	5.04	7.42	-22.25	-4.68	-6.85	-6.61	0.54	-1.55	38.59
-7.12	-5.73	-5.13	-0.76	12.29	-12.02	0.69	-6.02	-3.90	-0.17	-11.07	-4.61	0.86	-9.33	-13.53	-12.31

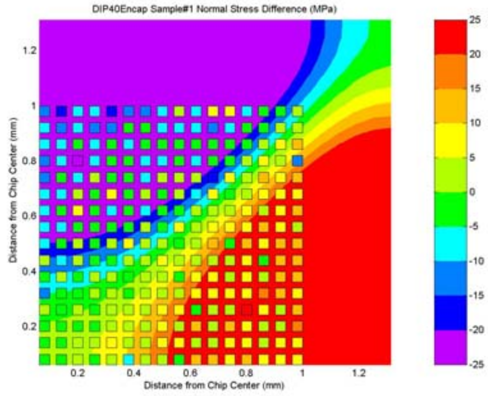
$\sigma_x' - \sigma_y'$ COBEncap Sample#8

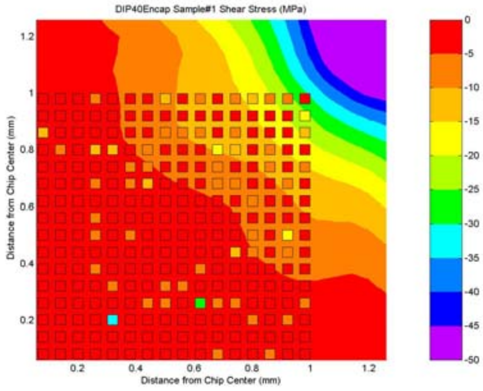
44.83	31.36	12.28	1.78	0.61	-5.75	-8.81	-19.87	-13.46	-15.71	-14.00	-28.91	-18.96	-34.69	-26.37	-24.85
41.94	30.10	9.34	-3.49	-9.07	-4.20	-16.27	-16.31	-15.54	-21.49	-12.00	-24.46	-30.58	-37.38	-40.58	-33.64
35.17	23.23	8.04	-1.17	-1.42	-10.66	-11.34	-10.24	-19.72	-28.07	-23.94	-32.68	-32.22	-40.04	-29.46	-41.36
36.82	16.90	14.54	1.51	-5.72	-6.81	-12.60	-17.65	-26.39	-31.61	-25.85	-30.60	-34.67	-33.10	-38.83	-33.73
40.36	22.52	9.65	1.41	-6.90	-14.75	-12.46	-15.44	-11.48	-25.50	-23.68	-30.39	-28.84	-38.82	-34.60	-38.26
30.31	20.49	4.30	6.51	-11.69	-8.70	-17.79	-28.44	-24.11	-29.02	-28.43	-33.94	-38.33	-37.03	-50.68	-37.60
31.19	23.35	8.83	-1.86	-9.10	-19.42	-16.70	-26.81	-24.24	-34.01	-35.71	-29.68	-39.18	-39.66	-43.40	-49.24
32.98	16.20	1.10	-6.37	-13.84	-24.64	-25.25	-25.40	-29.00	-31.79	-27.78	-32.89	-45.07	-49.99	-43.59	-36.38
24.64	14.78	9.95	-4.11	-22.36	-24.43	-20.16	-21.09	-33.11	-37.87	-37.52	-37.06	-41.83	-46.66	-38.93	-44.28
18.56	13.96	-0.08	-5.86	-14.04	-14.46	-30.49	-26.69	-29.95	-35.33	-44.38	-47.21	-44.16	-45.67	-52.92	-46.95
22.41	2.75	-2.55	-16.91	-21.76	-25.65	-35.31	-32.58	-32.24	-44.57	-39.40	-44.25	-49.59	-50.46	-56.07	-54.07
13.85	3.16	-9.28	-21.31	-27.67	-38.32	-28.28	-41.17	-40.47	-50.83	-46.11	-48.79	-55.76	-58.78	-57.59	-56.09
22.65	-3.17	-11.73	-27.91	-36.53	-22.65	-42.77	-48.66	-49.68	-49.50	-52.82	-58.58	-49.28	-64.86	-66.85	-55.92
0.72	-8.96	-16.61	-33.26	-34.12	-43.04	-43.29	-49.34	-54.16	-58.13	-60.14	-56.54	-63.70	-60.03	-63.15	-69.79
3.97	-17.43	-24.52	-36.37	-38.90	-48.44	-48.76	-49.75	-54.30	-65.69	-66.28	-62.56	-71.34	-78.34	-59.84	-71.04
-1.43	-23.49	-34.46	-40.49	-37.53	-48.57	-56.00	-69.28	-61.03	-63.35	-67.74	-71.80	-74.54	-74.73	-84.95	-77.22

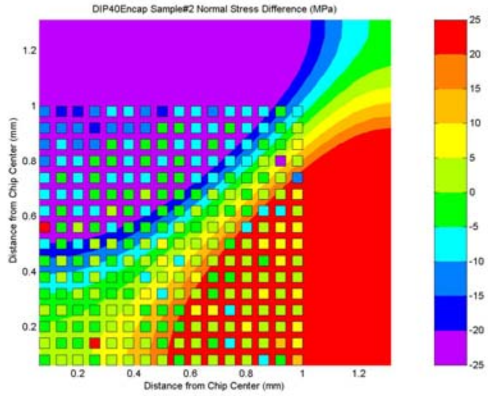
σ_{xy}' COBEncap Sample#8

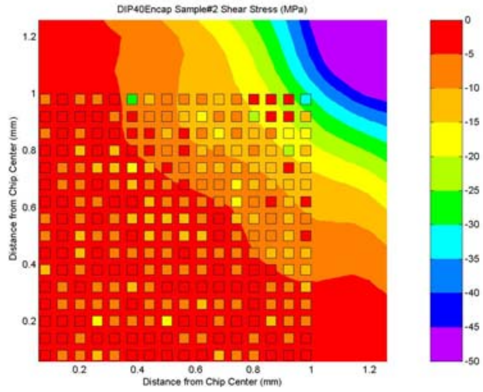
-63.52	-64.01	-43.48	-46.78	-34.86	-34.92	-42.50	-28.32	-19.51	-24.09	-24.76	-28.93	-21.36	-22.31	-10.55	-12.38
-54.45	-56.51	-52.57	-44.37	-39.39	-43.41	-30.88	-31.35	-35.33	-29.28	-27.01	-42.47	-29.19	-15.96	-16.07	-20.28
-59.40	-48.22	-48.85	-39.93	-37.08	-27.87	-27.52	-29.17	-34.26	-23.55	-25.51	-16.32	-20.63	-60.24	-19.31	-27.23
-50.46	-33.29	-41.17	-32.58	-48.43	-15.97	-39.30	-26.60	-25.41	-25.15	-15.70	-18.28	-23.99	-29.17	-8.08	-20.04
-37.06	-39.45	-28.83	-35.58	-37.30	-28.18	-25.41	-27.79	-24.30	-23.32	-26.15	-19.85	-17.45	-23.68	-17.38	-19.33
-48.29	-35.89	-51.02	-24.68	-29.29	-27.81	-15.61	-35.48	-25.03	-31.82	-22.44	-15.76	-28.35	-12.68	-25.60	-17.11
-36.50	-36.72	-29.47	-30.19	-48.32	-26.59	-23.11	-16.50	-21.14	-23.71	-24.58	-19.55	-28.59	-13.11	-23.39	-12.77
-40.37	-33.24	-32.64	-23.29	-36.50	-31.04	-25.10	-24.77	-17.56	-20.20	-24.67	-25.04	-27.31	-23.18	-17.89	-7.03
-50.78	-39.17	-44.55	-25.23	-22.19	-26.36	-33.93	-29.57	-20.73	-29.38	-15.29	-27.63	-28.08	-22.47	0.16	-10.84
-15.57	-31.33	-21.46	-34.68	-26.83	-23.79	-25.05	-17.46	-29.01	-32.18	-21.43	-16.40	-12.19	-16.18	-20.57	-21.00
-35.16	-25.47	-27.52	-31.95	-33.82	-36.99	-28.16	-21.10	-25.35	-28.05	-27.69	-27.08	-20.70	-23.45	-20.68	-14.37
-26.81	-33.16	-33.25	-25.81	-21.47	-18.23	-29.06	-33.65	-18.04	-29.00	-31.96	-18.78	-28.12	-7.40	-19.64	-18.41
-29.47	-22.51	-15.11	-20.47	-24.91	-21.44	-24.52	-18.16	-20.00	-19.72	-21.22	-22.85	-24.13	-24.79	-11.63	-18.26
-22.09	-16.54	-18.00	-20.80	-8.71	-13.10	-18.75	-20.79	-29.37	-17.04	-22.67	-16.68	-16.97	-11.98	-16.59	-9.59
-23.18	-22.06	-21.48	-27.89	-27.21	-16.76	-28.01	-10.96	-11.65	-16.61	-11.98	-11.55	-19.06	-14.22	-15.96	-25.66
-21.89	-4.64	-8.28	-27.84	-20.06	-18.77	-16.03	-12.99	-12.58	-18.12	-18.57	-11.10	-15.67	-19.04	-11.16	-10.91

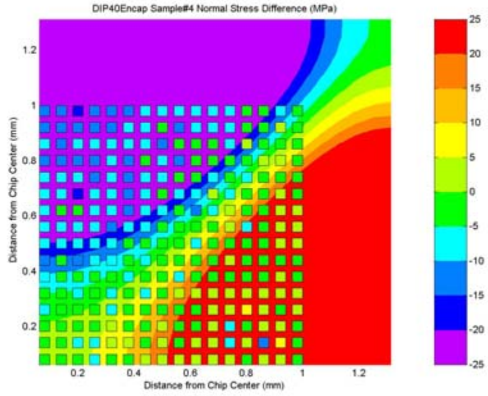
Appendix H. Individual Stress Mapping for DIP40 Encapsulated Samples (MPa)

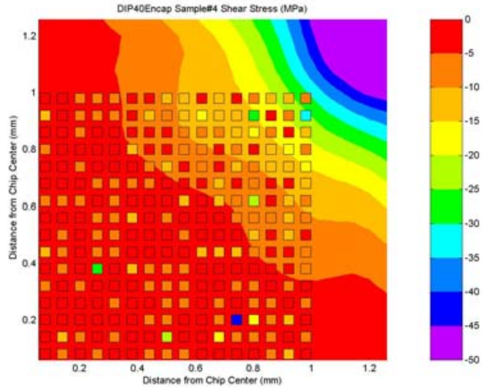


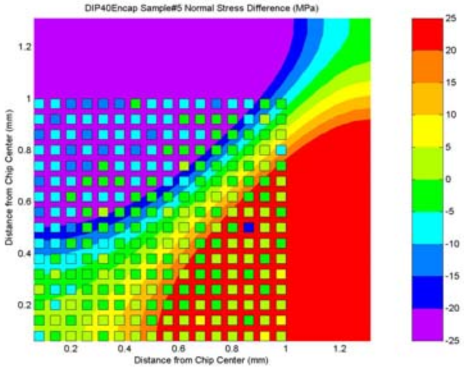


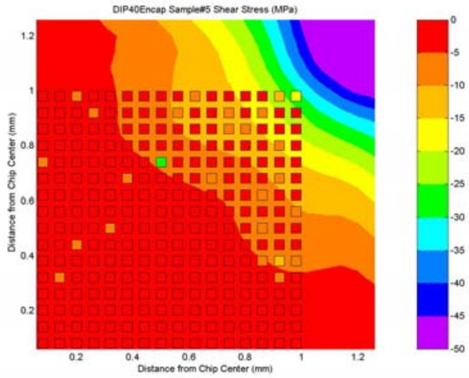


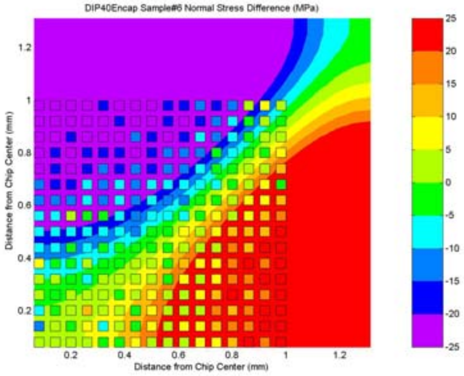


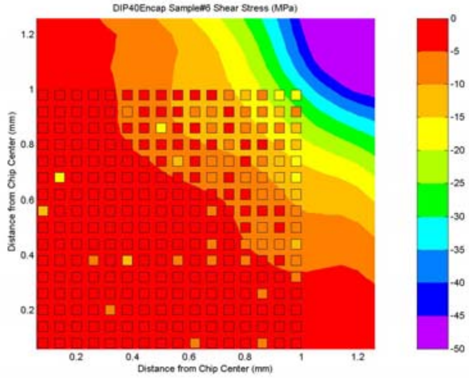


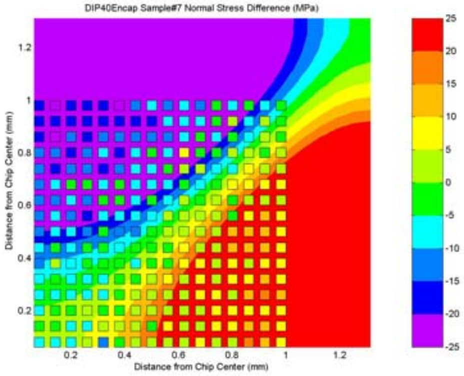


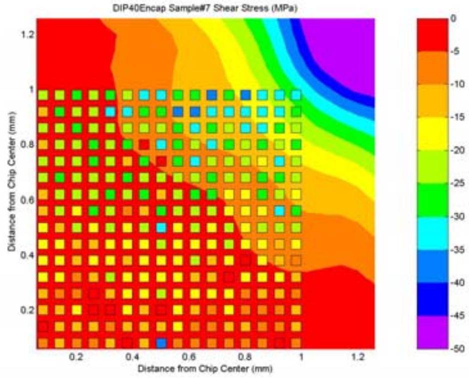

DIP40Encap Sample#5 Normal Stress Difference (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
25
20
15
10
5
0
-5
-10
-15
-20
-25

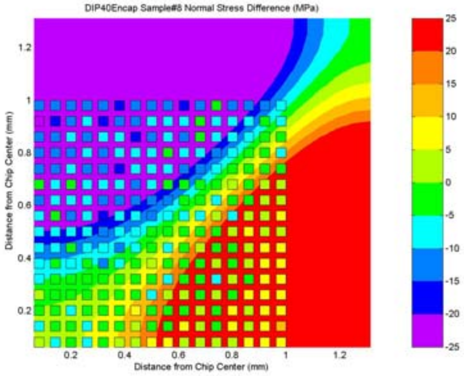

DIP40Encap Sample#5 Shear Stress (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50

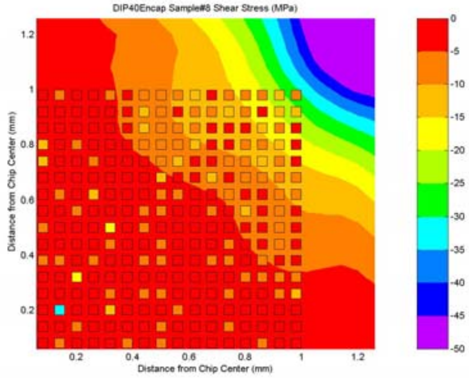

DIP40Encap Sample#6 Normal Stress Difference (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
25
20
15
10
5
0
-5
-10
-15
-20
-25


DIP40Encap Sample#6 Shear Stress (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50


DIP40Encap Sample#7 Normal Stress Difference (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
25
20
15
10
5
0
-5
-10
-15
-20
-25


DIP40Encap Sample#7 Shear Stress (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50


DIP40Encap Sample#8 Normal Stress Difference (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
25
20
15
10
5
0
-5
-10
-15
-20
-25


DIP40Encap Sample#8 Shear Stress (MPa)
Distance from Chip Center (mm)
Distance from Chip Center (mm)
0.2
0.4
0.6
0.8
1
1.2
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50

Appendix I. Individual Stress Mapping Data for DIP40 Encapsulated Samples (MPa)

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#1

9.20	7.07	8.22	12.83	7.01	10.64	12.30	-0.66	4.67	4.00	-5.44	1.01	-2.39	4.21	-2.44	-4.83
8.04	9.95	4.66	9.06	5.87	3.35	0.31	5.17	8.24	4.46	0.10	5.32	2.47	1.40	-2.23	-2.49
15.73	4.04	4.08	7.20	10.34	4.50	11.26	3.01	6.65	2.03	4.29	2.44	-1.01	-1.85	-0.91	-2.01
13.33	4.79	9.51	22.72	3.38	3.86	-1.26	8.28	9.23	1.13	3.80	3.35	-0.84	1.27	-4.56	3.66
9.81	14.73	16.48	5.59	8.85	8.77	6.86	3.23	3.28	1.48	-3.78	1.17	0.30	-2.86	-2.28	-10.65
13.35	10.50	3.40	5.56	1.49	7.11	6.10	-0.97	3.27	2.83	-0.75	2.22	2.15	-2.32	2.82	-2.87
10.52	11.78	-2.06	5.02	0.47	2.59	0.83	1.80	5.46	2.45	0.68	-0.85	-0.73	1.98	-5.87	1.33
12.42	12.14	7.13	13.72	-1.94	10.78	1.81	-2.79	0.77	0.80	5.52	2.00	-3.00	1.94	-1.73	-5.81
3.94	7.02	12.48	9.90	8.54	6.47	2.57	7.41	-0.32	3.07	-3.54	-0.27	-4.29	-1.98	-8.16	-9.28
12.63	9.56	1.80	5.74	4.07	0.04	2.34	-0.03	-2.43	-5.60	-0.91	-5.33	-4.96	5.98	-2.55	-5.62
6.67	8.12	6.56	2.91	-0.17	9.05	-5.90	2.63	-3.78	0.44	-2.62	6.57	-4.48	1.55	-8.91	-6.32
11.21	6.71	11.19	4.39	9.97	-15.89	1.22	2.20	3.43	-6.99	-2.15	-4.23	0.39	-6.11	-4.58	-12.48
-13.02	0.92	9.06	1.03	-4.38	-1.81	-5.25	-2.03	-6.73	-8.41	-3.02	-4.87	-7.57	-37.61	-8.72	-14.40
14.85	6.63	2.34	-2.10	-1.43	-4.48	-4.29	-3.21	-2.86	-4.25	-7.06	-4.04	-5.37	-3.84	-9.18	-5.30
3.31	3.31	-2.88	-3.20	-5.01	-14.60	-7.39	-7.08	-8.70	-2.48	-2.06	-11.80	-11.01	-8.42	-11.17	-9.80
1.94	-1.67	-3.75	-5.96	9.47	8.98	-9.00	2.53	-9.57	-12.05	-14.63	-19.02	-9.74	-8.51	-15.23	-12.75

σ_{xy}' DIP40Encap Sample#1

5.20	-18.19	-10.39	-4.26	-5.77	0.36	-4.56	-4.36	1.44	-1.60	0.26	-3.96	-8.45	-3.45	0.25	1.98
-8.36	0.18	-2.44	-3.89	0.20	-6.60	-4.15	3.75	-19.22	-7.00	15.73	5.22	-2.39	-5.50	-2.18	2.29
-6.75	1.03	-0.29	-7.33	-5.37	1.18	-4.51	0.30	-0.35	-2.21	-0.03	-1.65	-0.30	-4.02	-1.19	-5.97
-13.91	3.16	-0.46	-1.03	0.26	1.95	-7.77	5.41	-7.71	-5.46	-4.99	0.14	-1.54	-9.36	1.03	4.37
-8.50	-3.94	-6.18	-11.41	3.37	-6.77	-2.51	-1.04	-3.79	-11.73	1.53	-3.58	-6.89	-3.31	0.72	1.08
-3.74	-1.60	2.65	-15.33	-6.76	-8.35	-1.15	2.01	-4.70	8.06	-1.73	0.14	-6.18	-1.24	2.34	-5.15
-5.47	0.26	-5.21	-4.30	-0.61	-1.81	4.33	-4.67	-3.69	-4.96	-5.04	-0.49	-25.99	-3.49	-4.49	-1.94
6.40	-3.61	-9.10	9.18	3.10	-1.95	1.18	-0.93	1.82	-1.89	-1.71	-6.10	-3.51	21.44	-4.42	-1.79
-13.82	-4.65	-5.95	-2.12	-4.73	-0.83	1.05	4.44	-4.41	2.56	3.29	-6.65	-5.63	5.51	2.46	3.03
2.96	3.90	2.10	-6.56	-6.52	-11.53	-1.06	-2.16	0.11	1.78	-2.43	-1.63	-6.39	3.31	-1.66	2.22
-3.63	1.95	3.93	1.88	-9.76	-8.77	-1.22	0.26	-6.91	-0.72	3.38	3.41	6.60	3.29	4.15	1.55
0.82	-1.18	-4.95	-10.79	6.15	4.41	6.58	-1.77	3.99	0.82	6.01	-6.67	3.19	-31.74	4.58	1.63
-8.44	1.28	-3.10	-13.85	13.71	-5.50	-0.92	-7.55	-8.45	-1.24	-8.46	10.36	7.32	4.09	4.94	-0.70
1.60	2.71	0.31	-1.25	-4.26	4.81	2.96	2.39	-1.66	-3.60	-3.97	0.73	-3.46	5.27	20.11	4.91
1.37	9.76	4.78	-9.56	-1.76	-0.01	4.12	2.29	2.94	9.15	-1.82	1.60	-4.85	8.17	2.60	4.02
-4.52	8.63	-13.02	-1.12	-0.92	13.77	3.03	-0.25	-2.09	-2.43	7.34	-1.79	5.37	2.23	6.18	9.09

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#2

10.64	-1.01	-5.30	1.04	2.23	1.54	4.45	-0.64	3.71	3.19	0.31	2.10	-1.34	0.35	1.61	-1.37
8.34	10.85	0.17	3.62	-6.18	-2.60	1.84	3.49	-1.00	1.70	1.08	2.73	54.68	-0.38	-0.02	2.63
8.35	0.16	1.27	9.24	4.93	4.74	2.55	-0.68	-0.51	-2.31	2.02	0.30	-1.02	-3.17	-2.44	-2.18
1.64	0.66	1.62	1.60	-5.30	5.77	5.94	-1.40	-2.10	-2.10	3.17	1.97	-2.99	-2.99	3.01	1.59
8.09	2.92	7.87	2.59	3.87	-2.47	1.88	0.63	-5.02	7.68	-4.92	-1.14	3.06	2.25	-2.63	-3.31
3.56	2.47	2.24	1.73	-0.83	-1.44	7.84	0.10	0.79	-5.57	-4.13	-4.86	0.72	-2.93	0.12	-4.26
3.67	7.14	-0.96	0.88	0.33	2.31	1.38	-5.08	5.58	1.27	0.16	-3.17	4.37	-2.36	2.66	-1.59
6.77	8.28	6.10	2.39	-0.73	1.17	2.11	3.21	5.26	3.07	-0.72	0.16	2.95	-6.92	-0.79	-8.75
7.58	5.68	1.91	-5.46	1.05	4.66	-1.31	1.34	-2.39	-3.32	-1.45	-7.02	-1.84	1.19	-4.97	36.02
2.89	-9.08	-5.94	-0.25	-2.32	-1.27	0.82	-3.24	-1.39	-5.74	-2.48	1.54	-9.48	-6.02	-2.00	-8.35
7.81	1.46	1.45	-0.84	1.11	2.58	-0.11	-3.09	-2.23	0.13	-3.35	-1.86	-4.13	-9.17	-5.86	-5.02
-12.97	1.56	-0.97	-4.75	-4.01	-6.85	-6.41	-4.75	-3.30	-5.51	-7.25	-8.10	-3.21	-8.32	-3.09	-6.51
3.91	-22.68	1.98	-5.22	-5.55	-8.13	-5.98	-2.12	-5.45	-4.69	-6.81	-3.24	-4.25	-9.05	-6.82	-10.68
5.15	-1.83	-2.98	-5.36	-8.57	-3.98	-7.67	-9.36	-3.25	-2.98	-7.98	-4.79	-10.49	-10.83	-7.28	-10.18
3.83	-1.29	-5.31	-8.08	-3.88	-8.61	-8.87	-3.34	-2.91	-12.27	-10.70	-10.02	-17.78	-11.74	-10.85	-11.52
-6.73	-3.67	-9.96	-5.62	-7.17	-10.22	-9.54	-9.10	-16.20	-12.49	-9.61	-7.37	-11.56	-16.96	-16.04	-11.89

σ_{xy}' DIP40Encap Sample#2

-4.85	-6.17	-5.02	-11.08	-5.93	-1.32	-5.00	-4.46	-4.82	0.79	-13.95	-5.61	-7.63	-2.74	-0.18	1.65
0.63	-4.83	-7.53	-2.32	-4.39	-4.04	6.53	0.95	-5.58	-9.22	-3.16	-4.30	-9.19	-4.37	-5.27	-4.83
-2.98	-4.91	-2.68	-15.75	-7.33	-9.81	-6.41	-15.32	-3.74	-3.77	-6.34	-0.57	-3.18	-11.01	-8.21	-5.89
-3.03	-8.10	-9.25	-6.64	-6.15	-0.20	-6.30	-6.11	-6.18	-13.21	-6.17	-7.88	-3.45	-5.65	-8.19	-9.66
-0.91	-5.60	-0.85	-9.16	-6.80	-11.21	-7.36	9.88	-0.40	-4.17	2.72	-2.32	-1.79	-9.65	-6.60	-14.31
-14.38	-0.33	-7.24	0.05	-2.75	-3.71	-5.03	-7.62	-7.59	-9.94	-1.79	-5.36	-2.58	-3.89	-12.12	-10.64
-3.97	-2.02	-10.53	8.72	-6.32	-8.19	-6.08	-5.62	-4.76	-8.00	-6.10	-6.94	-9.96	-12.37	-10.69	-10.25
-9.12	-4.84	-10.72	-7.78	-9.77	-4.83	-13.68	-9.34	-12.62	-13.94	0.31	-6.84	-6.63	-6.81	-13.01	8.81
-6.65	1.16	-7.98	-4.50	-6.15	-10.71	-12.66	-10.27	-11.73	-8.63	-2.48	-11.34	-13.41	-5.76	-11.89	-7.07
3.50	-0.89	-9.54	-9.07	-3.10	-2.54	-11.08	-5.56	-7.13	-6.91	-6.97	-16.52	-8.95	-3.93	-11.79	7.29
0.64	-6.00	-8.22	-3.66	-5.95	-14.71	-8.25	-5.71	-4.69	-8.11	-7.37	-16.68	-14.41	-11.38	-10.29	-10.57
-4.25	-5.23	-9.12	-11.74	-11.34	-17.70	-11.80	-1.07	-9.90	-12.33	-11.56	-11.89	-11.15	-13.33	-0.56	-13.47
-3.31	-3.39	-11.77	-4.65	-10.57	-3.32	-4.30	-8.67	0.78	-10.06	-9.85	-14.70	-6.16	-10.12	-20.04	-13.22
-6.74	-4.38	-8.04	-0.43	0.89	-0.34	-2.01	-10.04	-4.79	-8.77	-18.69	-7.41	-11.80	-9.72	-15.94	-15.38
-3.67	-2.62	-3.51	-3.67	-5.82	-3.01	-9.97	-9.14	-13.74	-15.50	-5.26	-5.00	-20.67	-4.45	-0.24	-10.61
-6.01	-0.00	-6.22	-5.52	17.20	-26.23	-11.67	-9.39	-9.14	-7.28	-12.54	-7.62	6.79	11.50	-2.88	-32.64

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#4

-0.61	0.06	1.97	-3.58	3.60	1.16	0.61	0.11	0.45	0.42	-2.14	-0.70	-6.12	-1.71	-3.60	-0.83
-0.09	8.01	-13.16	0.55	-5.73	0.87	3.00	-1.67	0.40	-3.06	1.45	1.19	-8.47	-5.02	-1.07	-3.93
-0.16	1.35	0.84	-0.04	-5.69	1.23	-0.57	-1.21	3.80	-1.63	-3.55	1.79	-0.89	-4.00	-4.65	-3.81
1.95	-0.93	4.20	5.16	2.11	0.32	-2.11	-2.34	-3.11	-0.63	-0.91	-6.78	-2.51	-1.73	-4.18	-9.81
1.87	1.69	2.05	3.65	0.15	4.76	0.57	0.14	-4.04	-7.92	-4.02	-5.84	-4.26	-6.18	-2.50	-4.95
-2.51	2.74	-0.92	-0.39	-3.02	-3.03	-3.45	-5.76	-1.42	-2.64	-5.20	-4.20	-1.14	-3.76	-4.84	-5.23
-0.06	-4.18	-4.13	-1.46	2.65	-2.39	-1.48	-1.04	-0.41	-6.15	-1.55	-6.43	-5.79	-11.85	-4.23	-10.18
0.04	0.43	-2.05	-2.91	-2.03	-4.47	-7.11	-0.45	-4.36	-3.93	-3.12	-8.76	-8.23	-8.17	-5.93	-5.98
0.67	1.84	-1.39	-5.80	0.50	-2.34	-0.10	-2.83	-3.23	-6.81	-6.48	-11.16	-5.22	-6.64	-7.46	-6.29
2.60	1.58	-1.07	-0.88	1.20	-5.37	-11.48	-1.20	-8.40	-5.57	-10.72	-7.16	-6.03	-2.40	-4.50	-7.65
-2.99	0.25	-2.40	-2.65	-5.03	0.28	-5.74	-8.02	-3.13	-8.68	-11.29	-7.24	-5.49	-15.43	-9.10	-7.09
-0.43	-1.48	-1.84	-8.11	-3.98	-6.18	-2.72	-4.23	-8.05	-7.59	-10.73	-7.63	-11.14	-9.20	-8.25	-8.54
-4.34	2.52	0.54	-2.98	-1.52	-2.67	-3.05	-10.23	-8.40	-2.14	-10.77	-9.79	-12.10	-13.31	-11.56	-12.22
-2.59	-1.81	-0.21	0.34	-7.64	-4.74	-2.90	-3.27	-13.16	-6.07	-9.66	-8.66	-7.92	-7.17	-13.30	-7.82
-3.29	0.46	-4.36	-3.38	-8.05	-5.90	-8.49	-11.20	-1.78	-9.65	-8.77	-10.98	-11.56	-11.85	-13.40	-10.41
-3.54	-7.42	-0.41	-1.37	-8.77	-7.33	-9.73	-6.03	-7.22	-5.16	-12.65	-11.69	-13.98	-16.56	-13.50	-11.80

σ_{xy}' DIP40Encap Sample#4

-6.16	-30.35	-13.13	-6.51	-18.17	-10.18	-8.02	-9.56	-0.01	-7.19	-5.59	-1.87	-6.93	-2.72	-7.50	-2.48
-13.27	-9.01	5.68	-15.01	-10.89	-3.41	-11.85	-10.31	-10.61	-3.86	-2.27	-6.35	-1.05	-13.14	-4.45	-10.14
-14.31	-4.45	-7.40	-11.16	-12.67	-3.79	-3.54	-9.73	-1.35	-3.93	-4.84	-4.45	-5.37	-7.91	-9.50	-7.55
-9.78	-25.39	-16.68	-2.91	-6.54	-8.51	-22.25	-9.52	-12.78	-5.32	-1.05	-5.25	-7.16	-17.33	-8.00	0.23
-4.74	-10.23	-13.31	-7.11	-10.19	-2.16	-7.21	-7.00	-0.69	-11.01	9.90	-9.09	-3.40	-44.64	-7.30	-1.80
-13.97	-10.43	-9.21	2.79	-4.26	-12.97	-12.55	-3.11	-0.66	-12.66	-2.64	-1.49	-7.12	-8.41	-15.53	0.07
-2.38	-17.32	-8.09	-8.94	-7.44	-1.52	6.90	-3.94	-2.18	-10.24	-2.79	-4.28	-1.97	7.14	-1.98	-4.83
-11.40	-10.28	-8.47	-7.94	-3.77	6.94	-13.77	-1.40	-5.64	1.73	-5.13	-9.21	-8.65	-3.41	-4.17	-5.36
-10.27	-7.22	2.01	-3.50	-12.65	-3.44	-2.28	-7.98	-0.93	0.12	-9.61	-5.57	-9.69	-5.51	-20.72	-5.11
-4.82	-10.96	-2.82	4.14	-6.96	-7.03	-3.14	-2.99	3.25	-1.71	-7.61	-9.25	-1.67	-7.00	4.16	-8.51
-3.80	8.42	-4.86	-14.14	-0.99	-8.37	4.92	-10.83	-4.39	-4.18	-10.21	-4.42	-4.16	-4.15	-4.25	-3.75
-6.81	-8.14	0.77	-4.67	-3.02	-5.13	-9.21	-5.08	-7.65	-9.06	-4.47	-1.91	-6.17	-4.30	-8.26	0.14
-9.06	-6.88	-2.42	2.65	-1.44	-8.02	0.71	-6.05	-6.02	-6.01	-29.44	3.53	-4.74	3.56	-0.36	-6.46
-6.89	-6.02	-8.18	-3.79	-9.43	5.41	-6.36	-3.40	-1.48	1.77	-3.71	-6.56	0.40	0.12	-8.38	-1.75
-4.01	9.30	3.29	-2.10	-0.30	-4.84	-5.92	-3.30	-8.87	-7.55	-6.77	-3.31	12.05	-3.69	-12.99	-9.10
-0.38	-11.57	1.77	-7.62	-1.35	-1.60	-8.42	-0.63	-2.05	-11.88	8.53	-9.43	-0.67	-3.91	-2.92	21.90

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#5

0.79	7.82	3.39	1.23	2.59	2.90	0.64	3.72	3.14	3.79	3.69	-1.95	0.94	1.53	-2.61	-5.60
5.30	4.13	-0.26	1.64	2.45	7.38	2.66	3.94	-2.23	1.92	1.09	1.38	1.45	-1.72	0.19	-2.36
2.99	2.22	0.87	1.71	-0.42	1.02	-1.26	-3.65	-4.49	3.31	-3.16	-1.53	-2.58	0.52	-5.01	-2.41
4.84	-0.29	3.90	1.51	-0.19	-1.20	-0.96	-1.99	1.39	3.14	-2.08	-0.78	-2.19	-5.18	-8.79	0.09
5.06	2.59	-0.96	3.44	-0.39	-0.35	1.44	-3.01	-2.32	-1.42	-0.41	0.97	-3.76	-1.36	1.58	-4.54
4.18	-0.33	4.61	2.44	3.18	-2.59	2.46	-2.23	-1.57	-1.50	-3.42	1.05	-3.09	-5.82	-4.51	-6.03
-0.08	4.05	1.79	2.16	-4.80	-1.69	2.14	1.24	-1.54	-4.43	-4.57	-6.22	-0.19	-2.88	-5.15	-5.26
4.53	3.23	-16.97	-2.89	2.97	-1.85	1.45	-0.83	-0.91	-4.21	-0.36	-3.14	-4.84	-10.29	-8.31	-8.93
-2.14	2.14	2.98	1.12	-0.95	-3.08	0.51	2.31	-1.41	-0.23	-0.11	1.01	-3.63	-6.18	-6.56	-10.80
1.70	-1.93	-0.64	1.96	2.48	-4.40	-3.04	-3.86	-1.83	-1.46	-8.22	-5.32	-6.94	-3.94	-8.38	-9.39
2.89	-3.08	-3.48	-3.36	-0.48	-4.49	-7.92	-5.07	-4.69	-6.79	-4.61	-4.40	-4.33	-7.61	-7.81	-10.28
-2.67	3.09	-1.25	-3.18	-4.80	-3.95	2.34	-6.78	-7.29	-6.43	-6.71	-3.70	-11.07	-11.45	-9.51	-9.78
-7.37	0.30	-1.46	-2.81	-3.03	-1.74	-4.11	-3.19	-7.34	-11.58	-8.92	-11.89	-6.55	-12.09	-9.97	-7.98
0.73	-0.38	-2.10	-0.99	-2.74	-5.78	-5.81	-8.22	-10.07	-7.48	-6.11	-7.85	-10.98	-9.38	-5.12	-10.26
-0.88	3.37	-5.08	-0.72	-2.91	-4.18	-2.71	-7.29	-7.09	-7.75	-6.64	-9.14	-8.84	-8.17	-11.11	-7.01
-1.97	-3.37	-7.41	-7.66	-10.99	-6.82	-5.21	-6.33	-5.94	-3.61	-12.10	-11.13	-11.17	-12.78	-8.46	-8.12

σ_{xy}' DIP40Encap Sample#5

-15.86	-4.95	-4.13	-2.87	-2.86	-2.22	1.85	-7.91	-1.49	-2.93	-8.04	-1.71	-3.95	8.48	3.33	-4.43
-14.25	-2.57	-3.34	-6.61	-4.66	-6.05	0.07	-0.05	-2.22	4.54	-12.55	-7.12	-0.92	-0.34	2.93	-2.93
-2.81	-9.18	-2.04	0.47	-4.53	7.10	-5.45	3.52	-6.27	1.53	-5.36	6.57	3.44	5.00	9.05	0.20
-2.92	1.57	-6.13	-2.50	1.92	-0.01	3.62	-4.58	1.22	0.77	0.34	-1.57	2.65	8.15	3.18	11.03
3.51	-7.36	-9.89	4.36	7.89	-1.41	2.38	-0.14	-1.58	1.74	-0.75	1.64	4.19	2.23	12.46	2.82
4.36	0.14	0.08	-0.92	-0.37	-7.12	2.21	1.43	4.79	-2.88	11.29	5.61	-3.66	0.82	-0.28	0.25
-7.92	-0.51	-2.23	-0.48	-4.88	3.36	-1.40	-1.07	-4.54	4.87	1.38	0.18	-1.14	4.30	2.57	4.18
4.41	-5.78	14.40	4.00	4.24	4.34	2.15	6.79	1.96	0.21	9.29	4.12	3.77	1.94	-2.48	4.17
0.59	-1.47	5.22	-1.27	-28.67	4.13	2.26	-1.72	1.92	-3.41	5.96	5.90	0.80	7.15	7.35	7.86
7.20	6.30	2.19	-0.20	-1.22	-0.35	-1.22	7.22	2.42	-0.60	12.62	5.84	3.05	1.91	0.05	-2.96
-3.55	3.26	1.16	0.64	-3.32	-5.43	1.40	-4.57	2.29	4.28	2.81	1.48	1.49	2.88	1.78	0.31
-1.77	2.40	-3.22	-1.01	4.82	-3.05	-1.26	4.73	-7.82	0.19	0.84	0.86	5.89	1.17	-0.60	6.29
18.19	-7.42	6.28	2.24	2.81	1.60	-0.61	2.67	1.80	2.54	-4.47	-0.49	5.49	-0.91	-0.75	4.12
-6.86	-3.60	-0.08	-3.65	4.76	0.89	9.37	0.32	0.43	-5.11	4.42	1.67	3.19	-0.51	1.33	4.59
6.19	1.73	3.00	0.84	4.42	-0.09	4.41	1.91	0.97	7.95	3.27	-5.94	-1.29	9.28	-1.55	3.29
0.75	0.02	3.56	3.30	-7.15	8.15	1.53	7.31	15.40	8.46	-0.91	-1.90	8.12	-0.97	2.97	0.74

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#6

26.92	17.35	26.54	10.55	9.40	7.83	3.19	3.94	2.58	5.72	-3.28	-1.91	3.37	3.34	2.07	0.85
24.89	20.03	19.40	15.09	13.34	8.39	5.96	1.21	6.03	-1.94	4.06	-5.53	6.22	-1.37	3.26	-11.43
34.56	24.70	15.83	13.72	17.83	4.66	3.59	3.59	7.59	-0.59	1.94	2.29	11.40	0.22	-1.05	-5.13
25.48	19.45	14.07	21.89	10.12	5.57	5.00	1.20	5.85	0.95	-2.58	4.84	4.19	3.40	-0.24	1.56
23.10	20.56	16.36	15.06	8.80	1.59	5.56	-1.38	1.01	3.19	4.45	3.64	-5.13	-1.56	0.97	2.10
26.30	15.40	26.20	15.70	7.33	5.65	10.40	-3.00	4.84	1.90	-3.68	-3.18	1.05	-3.69	-2.58	6.67
23.49	21.70	11.52	15.96	4.52	3.60	4.55	-2.52	-3.93	-2.58	-1.91	-4.39	-7.72	-2.89	-5.84	-5.99
23.05	13.82	13.98	10.54	9.24	0.15	6.82	-3.54	-1.56	-12.66	-6.80	-5.46	-5.33	-5.24	-5.31	-5.03
17.79	14.34	6.32	4.97	8.58	-0.31	-6.25	-9.56	-6.24	-13.31	-8.67	-4.57	-0.89	3.59	-6.47	-9.73
14.70	9.67	6.57	1.26	-0.47	-0.66	-10.38	-14.68	-5.04	-10.82	-8.37	-10.39	-6.90	-12.89	-11.14	-10.06
-1.61	8.85	2.03	-0.35	-5.92	-9.01	-6.55	-9.20	-9.52	-13.31	-7.17	-13.66	-9.28	-15.80	-18.52	-12.22
10.34	3.83	3.19	-4.85	-4.20	-7.00	-12.70	-11.83	-18.68	-13.93	-18.42	-14.83	-16.01	-23.24	-18.95	-20.41
5.17	-0.86	-3.94	-6.59	-2.88	-14.15	-14.96	-12.88	-16.08	-22.54	-16.86	-17.64	-18.73	-21.87	-18.20	-24.62
3.94	0.85	-1.23	-9.78	-12.02	-8.00	-18.75	-20.80	-19.40	-14.96	-21.00	-22.15	-28.53	-17.40	-30.60	-27.53
-1.97	0.79	-0.09	-9.58	-11.34	-19.10	-26.15	-19.80	-23.85	-25.36	-16.56	-28.00	-24.53	-25.75	-30.60	-33.73
4.88	8.29	0.82	-13.67	-18.76	-12.40	-17.88	-18.53	-21.55	-20.81	-24.95	-17.14	-26.26	-27.07	-28.35	-30.55

σ_{xy}' DIP40Encap Sample#6

```
 -16.83   -8.57  -14.18  -10.25  -15.07  -19.08  -14.38   -7.87   -7.16  -12.72   -6.48   -6.06   -4.70   -3.71   -3.35    4.23
 -15.85  -13.30   -6.48   -8.12  -11.77  -11.27   -8.79   -4.94   -4.58   -5.28   -4.95    0.85   -0.17    1.75   -4.71   -1.83
  -9.10   -9.51   -8.03   13.91   -9.96   -7.01   -7.84    2.89   -7.77   -8.24   -1.20    0.39   -6.96   -4.56    0.99   -9.06
 -10.07   -9.18   -6.29   -2.93   -2.85   -9.63   -2.51   -4.12   -4.84   -9.24   -8.61   -4.27   -1.54   -2.50   -3.74   -2.21
  -5.97   -1.17    1.17   -5.96   -5.42   -4.16   -3.59   -2.24   -4.85    3.22   -4.02   -2.84   -1.26   -2.97   -3.61    1.46
  -2.06   -7.21   -7.01    1.46   -7.24   -8.15   -2.90   -5.89    0.51   -6.03   -6.26   -0.00   -3.32    0.38   -2.84   -2.32
  -4.99   -5.93   -0.11   -0.37   -2.86    5.51    0.87   -1.98   -1.51    4.83    1.79    2.33    2.64   -3.62    4.23   -5.79
   1.65   -2.52    0.62   -0.34  -13.80   -0.72   -1.86    2.04    1.11   -1.69   -8.99    0.29    0.66   -0.08   -1.71   -2.55
  -3.67    3.00  -18.23   -2.46    2.41   -0.69   -0.50   -1.07    3.55    1.89    1.81    4.02    4.57   -3.60    0.28   -1.72
   4.57   -4.46   -3.31    0.41   -2.05    1.25    0.35    1.03    0.15   -3.37   -0.55    0.76   -2.36    1.90    1.22   -2.73
  -1.35   -7.38    5.26   -3.01    0.38    3.02   -1.47   -2.73    2.83   -0.14  -10.14   -3.27   -1.29   -0.40    3.96    4.51
   2.97    4.68    0.60    2.09    6.04   -2.68    9.39   -4.08    2.89    2.75    3.29   -5.00   -0.23   -6.33    2.83   -2.40
   4.83    3.52   -0.82   -1.83    0.01   -0.16    3.61    0.26   -3.74   -1.88   -5.44    4.77    2.46    5.04    5.34    6.99
   7.08    6.27    5.36    3.71   -1.47   -1.29    5.03    8.43    4.76    8.67    1.82   -1.67   -2.55   -0.59    0.26    5.91
   5.87    2.67    7.99    8.17    3.35  -19.99    3.22    0.30    2.93   11.34   -4.99    2.48   -1.91    2.60    7.60    0.59
   4.68    4.41    3.23    0.70    2.58    2.27    4.79  -10.68    7.01    2.74    8.11    6.33    2.32    0.78    0.59    3.04
```

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#7

```
   6.11   14.31   17.32    3.32    1.05    9.85    1.61    1.34    0.09    1.56   -0.14  -11.37    2.17   -5.71   -7.38   -9.50
   6.45   11.35   10.24    5.10    8.56    3.42    4.86    8.15   -0.53    0.56    2.13    3.08   -5.21   -7.12   -3.42   -0.47
   6.30    9.73    5.68    9.18    9.67    4.09    4.50    4.09    2.85    0.14   -1.95   -2.54    0.44   -0.22   -3.90   -6.62
  14.66   15.75   10.50    2.48    9.87    6.40    1.19    3.60    2.89    2.09   -1.46   -9.98   -8.62   -6.55   -5.47   -5.73
   5.79   10.55    8.36    8.38    4.70    5.35    1.70    5.65    0.33   -2.31   -1.71   -5.66   -6.75   -6.09   -2.83   -9.35
   6.57    6.16    4.81    7.02    4.94    7.67    6.28   -1.79   -1.33   -9.10   -3.71   -4.08   -4.32   -5.65    0.82  -12.26
   5.67   10.33   10.44   11.97    2.49    4.42    6.03   -0.77   -1.60   -4.57   -6.66   -4.15   -1.69   -5.89   -3.60   -8.43
   5.79   13.28   10.87   10.27    4.98    2.64    2.02    3.32   -1.81  -10.29  -11.89   -4.81  -12.35   -8.76   -8.60  -14.96
   9.42   11.70    8.06   -3.11    4.60    1.10    2.87    1.86   -5.59   -9.26   -9.26   -5.46  -15.91  -11.41   -9.11  -11.15
   3.31    4.94    0.80   -1.22    2.78   -2.88    0.32   -5.93   -1.16   -6.01   -1.58   -3.82  -12.48   -8.60  -12.69  -14.19
   5.88    5.79    6.85    8.00   -4.49   -5.23   -4.30   -7.51   -5.56   -8.43   -4.99   -7.85   -4.39   -4.87   -8.87  -13.62
   1.87    2.72    6.37   -7.77   -6.62    3.49    0.07   -2.85   -9.34   -9.85  -11.98  -15.42  -13.63  -11.77  -15.33  -12.58
   3.10   -2.34    0.68    1.51   -0.88   -4.90    6.88   -8.15   -2.09   -5.87  -17.43   -5.85  -11.41  -15.63  -13.94  -13.79
  -3.99    2.27   -8.21   -2.53   -5.98   -4.57   -7.27  -11.09  -10.16  -14.94  -14.54  -14.93  -15.68  -11.88  -22.05  -16.32
  -1.66    4.11   -8.31    0.07   -4.84   -6.61   -6.18   -7.18  -16.70  -15.14  -19.03  -17.66  -16.74  -19.56  -17.38  -15.59
  -1.30   -7.99   -2.21   -7.68   -1.17  -12.74   -8.07  -10.43   -5.95  -14.74  -21.72  -15.78  -17.41  -18.21  -25.57  -16.79
```

σ_{xy}' DIP40Encap Sample#7

```
 -33.77  -28.27  -24.64  -26.66  -21.72  -23.14  -16.80  -25.22  -21.77  -16.12   -9.77  -14.60   -9.72  -11.24  -10.64   -5.33
 -34.02  -34.11  -28.12  -21.73  -31.01  -27.36  -24.74  -30.96  -20.80  -13.89  -11.61  -17.35  -11.02   -6.66   -9.51   -0.06
 -31.76  -30.99  -31.60  -26.35  -19.91  -28.91  -26.86  -18.54  -22.69  -16.88  -16.54  -16.37  -12.11   -9.04   -7.43   -6.22
 -38.26  -34.53  -31.24  -24.24  -22.37  -21.75  -18.11  -17.27  -19.23  -15.47   -4.33  -19.02   -8.49   -9.14  -10.09   -8.30
 -26.20  -30.25  -22.02  -25.81  -22.47  -22.00  -16.96  -19.61  -21.64  -21.63  -18.85   -4.93  -19.76  -15.22  -10.13   -9.17
 -35.85  -31.89  -27.23  -32.97  -24.23  -27.31  -28.03  -21.77  -17.39  -15.67  -13.24  -13.24  -16.28   -9.78   -5.31   -5.52
 -28.50  -37.01  -32.25  -23.32  -32.73  -24.02  -29.16  -23.54  -20.37  -19.41  -21.33  -13.93  -15.25  -11.50   -7.53   -6.32
 -28.74  -38.19  -27.90  -26.92  -29.21  -22.93  -21.40  -23.69  -18.44  -17.84  -19.64  -16.51  -16.32  -15.28  -16.34   -9.06
 -30.38  -27.24  -24.35  -32.04   10.55  -23.61  -13.96  -25.95  -34.89  -20.95  -17.71  -15.12  -21.86   -2.92  -11.52  -36.14
 -31.05  -26.93  -23.06   -3.51  -27.88  -21.62  -25.16  -12.74  -21.56  -15.16  -18.40  -16.13  -16.25  -14.97  -13.62  -10.07
 -23.37  -31.41  -22.43  -28.28  -11.44  -27.51  -22.68   -9.82  -19.83  -16.22  -14.52  -15.14  -15.35  -15.01  -13.41   22.63
 -26.68  -34.07  -21.43  -23.73  -21.82  -23.38  -26.46  -23.23  -21.34  -15.69  -15.57  -22.11  -11.86    0.58   -7.43  -12.53
 -24.10  -24.66  -22.58  -27.44  -27.16  -21.41  -21.28  -26.17  -16.02  -14.70  -16.38  -10.83    1.92   -2.13  -11.55   -7.51
 -29.85  -22.31  -26.42  -24.78  -21.71  -20.96  -22.52  -19.87  -22.05  -12.22  -13.13   -9.54   -5.47  -18.77  -12.14   -7.08
 -24.60  -30.00  -24.14  -23.23  -22.67  -26.32  -22.19  -20.76  -14.86  -19.03  -18.40  -16.54   -7.81  -10.86  -12.12  -14.65
 -23.68  -14.35  -24.74  -11.67  -23.74  -20.28  -14.78  -13.15  -19.22  -15.56  -16.44  -17.43  -12.64  -13.58    1.26   -8.75
```

$\sigma_x' - \sigma_y'$ DIP40Encap Sample#8

```
   5.34    8.22    9.56    3.38    1.81    1.80    4.97    6.85    5.46    4.20    1.17   -3.55   -5.72   -4.35   -5.09    1.36
  10.64    8.32    4.88    5.82   -0.02    1.51    9.58   -0.89   -0.56    0.40   -4.05   -4.95   -5.97   -2.66   -0.14   -8.32
   6.33    9.44    2.05    6.25   -0.98    1.93   -1.52   -0.51   -1.93    6.58   -4.16   -1.10   -3.05   -7.16   -3.89   -2.22
   5.20    8.73    6.83   -4.13    3.19   -1.14    1.81    3.26   -5.73   -1.77   -1.88   -4.87   -2.50   -4.22   -0.92    4.06
   5.94    6.01   -2.23    4.63   -7.67   -2.91   -3.27   -6.98   -0.88   -2.75   -1.82   -0.89   -4.19   -2.13   -4.07   -7.52
   6.05    7.81    2.58   -1.42    1.12   -0.99   -4.70   -3.43    1.91   -3.91   -9.55  -11.97   -3.65   -8.99   -4.36   -6.87
   8.96    5.84    3.21   -1.54   -1.06    0.05   -1.75   -6.92   -0.61   -5.05  -11.29   -5.35   -6.70   -1.69   -8.43   -6.38
   3.25    3.07    7.34    0.67   -1.54   -3.37   -3.49   -4.49   -4.30   -9.91   -8.97  -11.17   -8.54   -6.39   -8.57   -9.47
   6.36    3.62    0.09   -8.31    1.89   -6.96   -7.03   -7.17  -12.37   -5.88   -7.58  -15.73   -9.09  -10.20   -4.46   -5.13
   3.73    2.28   -4.10   -2.09   -8.98   -4.77   -3.42  -10.25  -10.36  -10.19  -10.36  -10.41   -7.75   -8.26   -7.17  -12.35
   1.61    2.55   -0.22    4.57   -3.71   -4.50   -4.04   -4.43   -7.60  -11.90   -7.88   -7.63   -8.14   -4.63   -5.46   -4.03
  -0.34   -0.37   -0.48   -3.29   -8.10  -12.08  -11.69   -6.16   -6.81   -8.70  -15.38  -12.91  -12.34   -9.05  -14.68  -11.90
  -9.05   -2.08   -3.96   -5.23  -10.44   -8.36   -7.31   -4.77   -9.70   -7.40   -8.33  -10.74   -7.71  -13.89  -11.21  -12.93
  -2.95   -1.00   -6.97   -7.21   -6.40   -4.47  -11.26   -7.38  -12.02  -15.63   -9.43   -9.19  -13.41   -7.68  -12.26  -10.79
  -5.91   -1.78   -9.33   -8.83   -8.37   -4.90   -9.87   -7.50   -7.43  -11.98  -10.81  -15.35   -6.36  -13.84  -16.32  -20.49
  -7.38  -10.00  -14.39  -11.31   -4.84  -13.33  -15.12  -13.99  -12.65  -10.74  -15.47  -10.80  -11.45  -11.03  -12.36  -14.19
```

σ_{xy}' DIP40Encap Sample#8

```
  -8.99  -14.44   -0.27   -3.16   -3.37   -7.28   -5.80   -2.99   -3.25    2.18   -1.02   -9.25  -10.73    0.61   -3.34    1.13
 -11.35  -10.78   -5.44  -10.26   -5.92   -6.72   -7.46   -6.71   -5.65   -8.76   -2.50   -6.91   -9.91    0.26    4.16   -2.50
  -6.13   -1.85  -12.29   -5.51  -10.65   -8.34    2.51    0.14   -2.40   -2.08   -7.13   -7.33   -3.45    1.15    1.76   -5.40
  -7.61   -7.12   -2.87   -6.17   -7.37   -9.75   -4.01  -10.78   -2.17   -1.48   -4.00   -5.10   -4.04   -3.14    8.61    8.98
  -9.15  -11.07   -2.46   -0.44   -7.44   -3.05   -7.64   -4.89   -0.98   -5.51   -6.17   -3.28   -6.61    0.10   -7.88   -0.42
  -0.86   -8.99    3.84   -3.70   -3.85  -11.67   -3.26   -7.62   -1.47   -4.72   -6.52   -3.73   -3.49   -1.60   -3.79    2.70
 -14.68   -7.21   -6.42  -12.12   -2.91   -2.64   -3.04   -4.01   -3.35    1.23    2.95   -4.61    7.68    2.45   -1.61   -0.10
  -7.03    1.18   -9.53   -5.13  -12.32   -4.36   -5.54    1.53   -2.36   -2.83   -0.08   -4.31    2.11   -6.31    5.87   -2.34
  -6.46   -9.32   -6.55   -8.73   -8.13  -10.72   -5.62   -6.53   -2.13   -7.40   -9.51   -2.84   -5.86    3.43   -6.55   -8.64
  -5.17  -10.72  -10.47   -7.88    0.48   -0.69   -2.94   -6.97   -7.74    1.94   -6.42   -0.99   -7.96   -2.94   -4.17    0.75
  -1.08    4.45    0.71   -1.19   -4.26   -4.68    0.08   -4.52    8.72   -1.29    1.94    1.26   -3.16   -0.05   -0.16   -5.35
  -5.70   -1.80    1.11   -0.63    5.57    2.78   -0.41    3.13  -16.75   -6.76   -4.32   -3.29   -6.21  -14.39    1.18   -3.11
   1.72   -3.77   -3.17   -4.48   -5.37    1.57  -11.95    5.48   -2.78    7.72   -7.33   -0.17    3.75    0.51    3.31   -1.03
  -1.32    1.03   -1.35   -5.30   -4.45   -2.38   -0.13   -5.47   -1.76    2.87    1.54  -15.13   -2.07   -3.80   -6.12   -3.31
  -5.59    7.41    0.91    1.85   -1.37    4.59   -5.07   16.77   -1.56    2.18   -6.42    0.05    1.22  -33.72   -0.73   -7.00
   0.13   -3.26    4.15  -10.50  -13.30   -0.08   -2.04   -2.06   -5.43    2.88   -5.52   -3.03   -3.47    0.44   -1.98   -4.37
```