FLIP CHIP AND LID ATTACHMENT ASSEMBLY PROCESS DEVELOPMENT

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DISSERTATION ABSTRACT

FLIP CHIP AND LID ATTACHMENT ASSEMBLY PROCESS DEVELOPMENT

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Flip chip technology offers numerous advantages over conventional packages by virtue of its electrical performance, greater input/output (I/O) flexibility and small size. This study focuses on two flip chip assembly process developments: large size, fine pitch lead-free capillary flow flip chip and wafer-applied bulk coated flip chip. The assembly process for a lid attached on the backside of the die was also investigated.

Large size, fine pitch lead-free flip chips are highly desirable for many industrial applications. In this research, the 20.5 millimeters square dies with pitches down to 6 mils were assembled on ceramic substrates. The solder bumps were 97.5Sn2.5Ag. Many process parameters, including reflow profile, flux dispensing and die cleaning, were optimized for the best assembly and reliability performance. The assemblies were

subjected to air-to-air thermal cycle testing in the final stage. The assemblies exhibited greater than 2700 cycles of thermal fatigue characteristic life.

The wafer-applied bulk coated assembly process is a novel technique used in flip chip assemblies. A successful assembly process was implemented in this study. PCB dehydration prior to assembly, dispensing volume, reflow profile and placement parameters have been examined. The optimized assembly process is presented. Good solder wetting and void free underfill were achieved. Liquid-to-liquid thermal shock reliability tests were performed. The results of failure analysis also provided valuable information for future process and material development.

Flip chips with high thermal conductivity lids are currently being used in a flip chip package designed for high power applications due to its enhanced ability to dissipate heat. Here, attaching the lid to the backside of the die was investigated. Pure indium was used to solder attach the lid to the die. This study presents an overall lid assembly methodology, along with a report on the reliability testing of assembled parts.

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TABLE OF CONTENTS

LIST OF TABLES ……..……..…… xv

LIST OF FIGURES……... xvii

CHAPTER 1 INTRODUCTION……... 1

1.1 Flip Chip Technology……... 1

1.2 History of Flip Chip Technology……..... 4

1.3 Introduction to Underfill……... 5

1.3.1 Role of Underfill…….. 5

1.3.2 Desirable Properties for Underfill……. . 7

1.4 Flip Chip Assembly Process Overview……..... 7

1.5 Capillary Flow Underfill Process…….. 8

1.5.1 Capillary Underfill Materials…….. 9

1.5.2 Underfill Dispensing……..... 10

1.6 Fluxing Underfill Dispensing…… 11

1.6.1 Fluxing Underfill Materials……..... 12

1.6.2 Fluxing Underfill Materials Development……... 13

1.7 Wafer-Applied Underfill Materials……... 15

1.7.1 Wafer-Applied Underfill Materials…….. 15

1.7.2 Wafer-Applied Materials Development…….. 18

1.8 Lid Attachment Technology……. 19

1.8.1 The Role of Lid……. 19

1.8.2 Description of Lid Physical Structure……... 19

1.8.3 Lid Attachment Materials……. 20

1.8.4 Lid Attachment Process……..... 21

1.9 Lead-Free Technology…….. 22

1.10 Research Objectives...……. 23

CHAPTER 2 LARGE SIZE, FINE PITCH LEAD-FREE FLIP CHIP ASSEMBLY... 25

2.1 Introduction……... 25

2.2 Test Vehicle…….. 26

2.3 Description of Assembly Process Flow……..... 28

2.4 Solder Wetting Study……..... 28

2.4.1 Flux Materials…….. 28

2.4.2 Reflow Profile…….. 30

2.5 Underfill Void Study…… 33

2.5.1 Underfill Materials…….. 34

2.5.2 Fishbone Diagram for Underfill Voids……... 34

2.5.3 Effect of Dispensing Process…….. 35

2.5.4 Flux Residue……... 38

2.5.5 Die Condition…….. 40

2.6 Reliability Test……..... 42

2.7 Failure Analysis……... 45

2.8 Summary…….. 47

CHPTER 3 WAFER-APPLIED BULK COATED FLIP CHIP ASSEMBLY…….. 48

3.1 Introduction…….. 48

3.2 Test Vehicle Description…….. 49

3.2.1 Test Die……... 49

3.2.2 Test Board……... 50

3.3 Wafer Coating Process……. 52

3.3.1 Wafer Dicing……... 52

3.3.2 Bulk Material Coating……. 53

3.3.3 B-staging……. 54

3.3.4 Die Release and Loading…… 55

3.4 Overview of Assembly Process……... 55

3.5 Dehydration of the Test Board……. 56

3.6 Fluxing Underfill Dispensing Volume……. 56

3.7 Reflow Profile Development……... 57

3.8 Placement Speed and Force……. 60

3.9 Reliability Tests……... 61

3.10 Failure Analysis……. 63

3.11 Summary…… 65

CHAPTER 4 LID ATTACHMENT…….. 66

4.1 Introduction…….. 66

4.2 Test Vehicle……. 67

4.3 Overview of the Assembly Process……. 67

4.4 Lid Shear Testing……. 69

4.5 Assembly Equipment Selection……... 70

4.6 SST Thermal Profile Optimization…….. 72

4.7 Copper Lid Assembly…….. 78

4.8 Reliability Test: Multiple Reflows……... 80

4.8.1 Test Profile…….. 80

4.8.2 Shear Test Results……... 81

4.8.3 IMC Analysis…….. 82

4.9 Reliability Test: High Temperature Storage…… 84

4.9.1 Shear Test Results……... 84

4.9.2 Growth Kinetics of IMC……. 85

4.10 Reliability Test: Thermal Shock…… 88

4.10.1 Shear Test Results……. 89

4.10.2 Test Analysis……. 89

4.11 Summary…… 93

CHAPTER 5 CONCLUSIONS……. 94

5.1 Large Size, Fine Pitch Lead-Free Flip Chip Assembly……... 94

5.2 Wafer-Applied Bulk Coated Flip Chip Assembly……... 95

5.3 Lid Attachment…… 96

5.4 Recommendation for Future Work…….. 97

BIBLIOGRPHY……..... 99

LIST OF TABLES

Table 1.1 Current flip chip consumption and forecasts …… 3

Table 1.2 Properties of typical capillary underfill and fluxing underfill……... 13

Table 1.3 Comparison of solder and conductive adhesive junctions, typical values…. 21

Table 2.1 Summary of assembly results…… 30

Table 2.2 Material properties of Ablefill MB1502 underfill……. 33

Table 2.3 Effect of cleaning process on underfill voiding……. 40

Table 2.4 Wetting angle measurements……. 41

Table 2.5 Optimum parameters……. 42

Table 2.6 Reliability test results……. 43

Table 3.1 Properties of Bulk Materials…….. 54

Table 3.2 Effect of fluxing underfill dispensing weight…… 57

Table 3.3 Reflow parameters for profiles A and B…… 58

Table 3.4 Results of assembly for two profiles…….. 59

Table 3.5 Reliability test results……. 62

Table 4.1 Controllable factors…… 73

Table 4.2 The design layout and experimental results……... 74

Table 4.3 Response table for mean…… 75

Table 4.4 Reflow profile measurement…….. 79

Table 4.5 Growth constants and linear correlation coefficients……. 87

LIST OF FIGURES

Figure 1.1 Structure of a flip chip on board …….. 2

Figure 1.2 Structure of a flip chip BGA …… 2

Figure 1.3 Comparison of stress on individual solder joint with and without underfill used ……..... 6

Figure 1.4 Capillary underfill process flow …….. 9

Figure 1.5 Fluxing underfill process flow ……. 12

Figure 1.6 Current wafer-applied underfill approaches……. 16

Figure 1.7 Cross section of lid attachment structure (drawing is not to scale) ……. 20

Figure 2.1 Test die and its solder ball pattern ……... 27

Figure 2.2 Ceramic substrate …… 27

Figure 2.3 Assembly process flow …… 28

Figure 2.4 Reflow profile for flux TF38 with Sn2.5Ag solder ……. 31

Figure 2.5 Self-alignment ability, showing good solder joint formation …….. 32

Figure 2.6 Cross-sectioning picture, showing good solder joint formation ……. 34

Figure 2.7 Fishbone diagram for underfill voids …….. 34

Figure 2.8 Different dispensing patterns ……... 36

Figure 2.9 Assembled parts cleaning process ……... 39

Figure 2.10 Comparison of underfill voiding level with and without cleaning process 41

Figure 2.11 Weibull plot of the AATC ……. 44

Figure 2.12 C-SAM images……... 45

Figure 2.13 Die cracking at 1700 cycles …….. 46

Figure 2.14 Solder fatigue cracking at 2500 cycles …….. 46

Figure 3.1 Underfill dispensed on a conventional board and placed with a glass slide 49

Figure 3.2 FA10 test die …… 50

Figure 3.3 Auburn FA10 test board …….. 51

Figure 3.4 Wafer coating process flow ……. 52

Figure 3.5 Assembly process flow …… 56

Figure 3.6 Reflow profiles …… 58

Figure 3.7 Cross-section shows good solder wetting …… 60

Figure 3.8 C-SAM picture of assembly with CNB 946-04 fluxing underfill and WABU bulk underfill …… 61

Figure 3.9 Weibull plot of cycles to failure …….. 63

Figure 3.10 Delamination progression with LLTS ……... 64

Figure 3.11 An example of underfill fillet cracking ……. 64

Figure 3.12 A solder crack, which occurred near the UBM ……. 65

Figure 4.1 Schematic of lid attach process ……..... 68

Figure 4.2 Shear test ……. 69

Figure 4.3 Shear test failure mode …… 70

Figure 4.4 Examples of bonding voids visible in X-ray images……..….. 71

Figure 4.5 Fracture surface after shear test ……... 72

Figure 4.6 Heating profile…….. 73

Figure 4.7 The prediction profile for mean underfill voids and S/N ratio……. 76

Figure 4.8 2-factor interaction plots …….. 77

Figure 4.9 Assembly with optimized placement parameters, X-ray image showing only tiny voids ……... 78

Figure 4.10 An example of C-SAM image showing good wetting and void free…… 79

Figure 4.11 Reflow profile for multiple reflow test ……. 81

Figure 4.12 Shear test results for multiple reflows ……... 82

Figure 4.13 SEM images showing the IMC growing after reflow …… 83

Figure 4.14 Shear test results …… 85

Figure 4.15 The IMC layer thickness increase during high temperature storage ……. 87

Figure 4.16 Arrhenius plot for the IMC growth …… 88

Figure 4.17 Shear test results for AATS ……... 89

Figure 4.18 C-SAM images during AAATC …… 90

Figure 4.19 Side views of parts showing indium loss after 2000 cycles……... 90

CHAPTER 1

INTRODUCTION

1.1 Flip Chip Technology

With the continued proliferation of low cost, portable consumer electronic products with greater functionality, there is increasing demand for electronic packaging that is smaller, lighter and less expensive. Flip chip is an essential enabling technology for these products.

The term “Flip Chip” is commonly used to refer to an assembly method used to make a direct electrical connection by placing the chip face down onto a substrate, circuit board, or carrier. The electrical connection between the chip I/O and substrate is achieved using conductive materials, such as solder, conductive epoxy, metallurgy bump (e.g., gold) and anisotropic conductive adhesives. Among these materials, solder is the most commonly used in flip chip assemblies.

Flip chip can be categorized as either flip chip on board (FCOB) or flip chip in package (FCIP) [1]. When the bare chip is directly connected to a printed circuit board (PCB) with other components to form the final electronic product, the technique is referred to as FCOB, or direct chip attach (DCA). Figure 1.1 shows an illustration of FCOB. The chip is directly attached onto a conventional PCB by solder. Underfill is added between the chip and the PCB. FCIP is the mounting of a flip chip in a package, such as a ball grid array (BGA) or chip scale package (CSP). An example of a flip chip

BGA is shown in Figure 1.2. This package is subsequently assembled onto a PCB to build the final product.

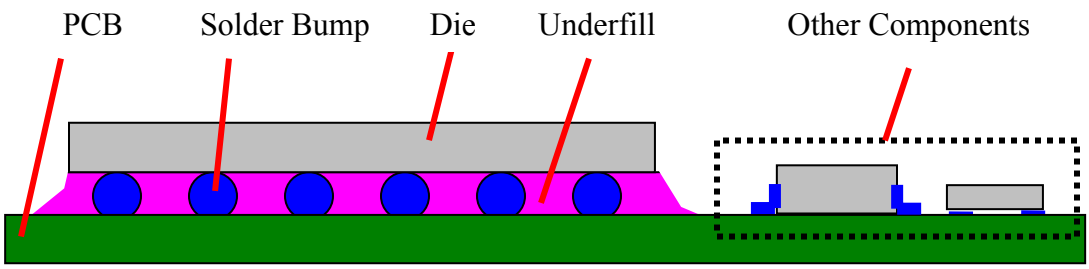


Figure 1.1 Structure of a flip chip on board

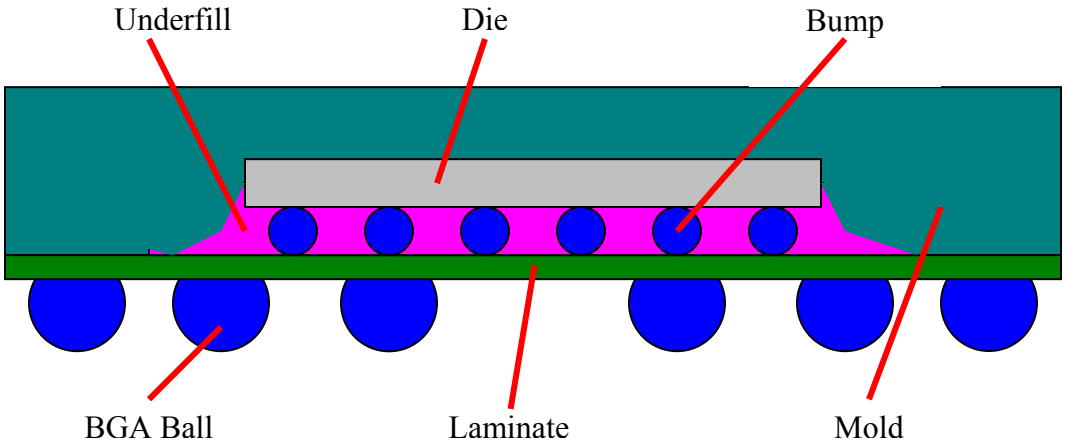


Figure 1.2 Structure of a flip chip BGA

In comparison to conventional wire bonding, flip chip technology has a number of advantages, including superior electrical performance, larger number of input/outputs (I/Os), and smaller size. First, by eliminating bonding wires, the electrical path length and inductance of the connections are reduced in flip chip assemblies. The inductance of the connection has been reported to be reduced by a factor of 10, and the path shortened by a factor of 25 to 100 [2]. This considerably enhances the electrical speed performance. Second, for wire bonding the connections are limited to the die perimeter, so increasing the number of I/O will also drive the die size up. In contrast, flip chip connections can use the whole area of the die and accommodate more connections. Third, eliminating bond wires reduces the required board area and requires far less height.

Flip chip technology has been implemented in a wide variety of applications. Today, flip chips are widely used in watches, disk drives, hearing aids, portable communicators and LCD displays. Table 1.1 provides information on the global flip chip consumption, along with forecasts for the future [3].

Table1.1 Current flip chip consumption and forecasts [3]

Total Flip Chip Demand (in Million Units)					
	2004	2005	2006	2007	2008
Flip Chip in Package	1,763	2,578	3,993	6,147	8,079
Flip Chip on Board	4,053	4,323	5,077	6,200	7,271
Total	5,816	6,901	9,069	12,347	15,350

1.2 History of Flip Chip Technology

The history of flip chip may be dated from the invention of IBM's solid logic technology (SLT) in 1961. In the original SLT packaging, solder-covered copper balls were used as connections between the chip pads and the substrate. This package went into production in 1964 in the IBM System 360 [4]. Gilleo [5] has correctly pointed out that the SLT package was the world's first BGA, the first DCA, the first surface mount technology (SMT) and the first CSP. IBM continued their efforts and introduced the second major development in flip chip technology, Controlled Collapse Chip Connection (C4), in 1965 [6]. IBM's C4 used evaporation to deposit 95/5 PbSn solder through a metal mask. Then the chip was heated, and a solder ball formed on the chip pad. After testing, the chips were placed face down on a ceramic substrate. Through reflow, the chips were directly bonded to the substrate. This technique could form hundreds of solder joints simultaneously, and enabled C4 to become a fundamental technique for flip chip fabrication. Later, Delco Electronics introduced its first flip chip generation, which was used in the Pontiac automobile in 1969 [7].

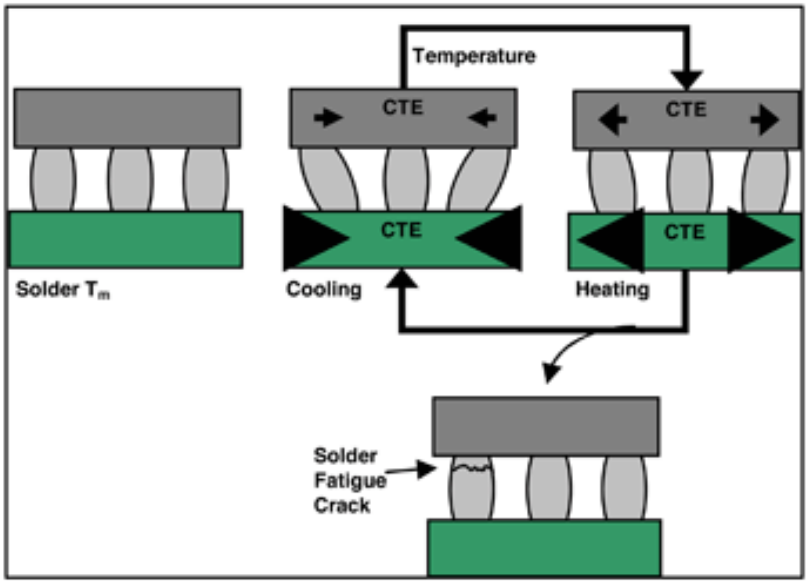
Until the late 1980s, flip chips were predominately mounted onto silicon or ceramic substrates without underfill. Hitachi introduced a resin-inserted flip chip device on an alumina substrate in 1987 [8]. This was a great step forward for flip chip development. Late in 1990, IBM took a further step in assembling flip chips on organic printed circuit boards, using a polymer encapsulation to enhance the reliability of the package [9].

1.3 Introduction to Underfill

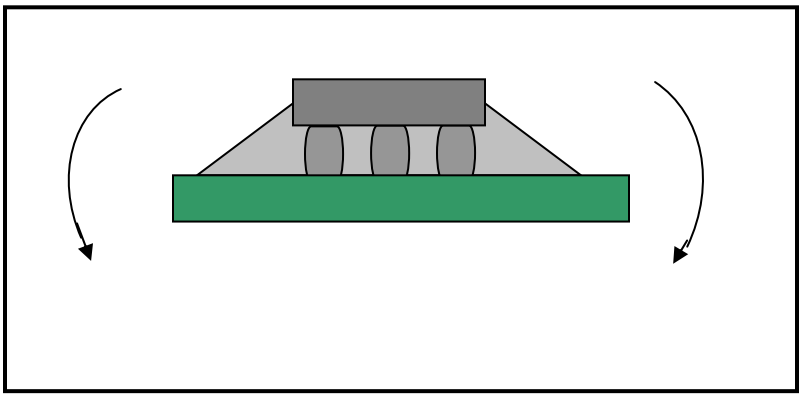
1.3.1 Role of Underfill

The underfill plays an important role in increasing the reliability of flip chip assemblies. In the earlier flip chip assemblies, small dies were assembled on silicon or ceramic substrates. The coefficient of thermal expansion (CTE) mismatch between the silicon die (~2.5 ppm/°C) and the ceramic substrate (~7.0 ppm/°C) was not significantly large to cause early thermal fatigue failure of the interconnection with small silicon die. However, when the substrate switched from ceramic to laminate, the CTE mismatch between the silicon die and the laminate (~ 16 ppm/°C) became larger. The strain imposed on the solder joints increases during cooling of the package (Figure 1.3 a) [10]. The strain results in early failure of the solder joint during thermal cycling.

To improve the reliability, underfill was added to the flip chip assembly process. An underfill encapsulant is usually a polymer material that fills the space between the chip and substrate after the chip is soldered. The underfill usually contains filler particles such as silica to modify the underfill properties, such as rheology, strength, toughness, modulus, CTE and thermal conductivity. The underfill bonds the die and the substrate together. Since the die, underfill and substrate deform together as a unit, the relative deformation between the die and the substrate becomes very small and the shear deformation of the solder joint becomes very small. In other words, underfill reduces the shear stress in the solder joints by spreading the localized stress into the underfill layer and subsequently improves the reliability (Figure 1.3 b). In comparison to unencapsulated assembly, a factor of ten to one hundred enhancement in fatigue life can be achieved by underfilling a flip chip [9].



(a) Stress on the solder joints during heating or cooling of the package



(b) Stress on the whole package when underfilled structure is cooled down

Figure 1.3 Comparison of stress on individual solder joint with and without underfill used [10]

1.3.2 Desirable Properties for Underfill

Epoxies are the dominate polymer used for underfills because of their balanced properties, long-established safety record, wide availability, high versatility and general characteristics that are desired in this product area [11]. The desirable properties for an underfill include [12]:

- Low coefficient of thermal expansion
- High modulus of elasticity
- High glass transition temperature
- Good adhesion characteristics
- Low dielectric constant
- Good flowability
- Short curing time

1.4 Flip Chip Assembly Process Overview

The application and cure of the underfill are primary steps that have an impact on the flip chip assembly process flow [13]. Based on the underfill application and cure, flip chip underfill can be categorized as capillary, fluxing and wafer-applied. Capillary flow underfill is applied after the flip chip is placed and reflowed. Fluxing underfill is applied prior to die placement and cures during the reflow process. Wafer-applied underfill assembly is a new process where the underfill is pre-applied on the whole wafer prior to singulating the wafer into individual dies. The wafer-applied underfill can be cured during the solder reflow process. These processes will be discussed in detail in the following sections.

1.5 Capillary Flow Underfill Process

Flip chips assembled with the capillary flow process have been in manufacturing for many years. So far, capillary flow remains the most common method of underfilling. This mature technique produces good reliability and good product yield for flip chips.

Figure 1.4 illustrates a typical capillary flow assembly process. The overall process flow begins with die placement. The bare die is picked, and flux is applied using a flux dipping station on the pick and place system. Alternately, flux can be sprayed onto the substrate prior to die placement. The bare die is then aligned using the pick and place machine's vision system to orient the die to the substrate. Next, the assembly is sent to the reflow oven. The tacky flux holds the die in place during part transfer and before the solder melts in the reflow oven. As the temperature increases in the reflow oven, the flux becomes active and removes the surface oxide on the solder. Then the solder melts on the substrate pads and forms solder joints between the die and the substrate. After soldering, some assembles may need cleaning to remove flux residue that may affect the subsequent underfill dispensing step and reliability. If a low residue or no clean flux is used, the cleaning process may not be required. Electrical test or inspection may also be performed prior to dispensing the underfill but can be eliminated based on throughput requirements and assembly yield results. Following soldering, the underfill is dispensed along the edge of the die. Capillary force pulls the underfill into the gap between the die and the substrate. For some underfills, a second dispense may be required to form a fillet around the edge of the die. Finally, the assembly is subjected to high temperature to cure the underfill.

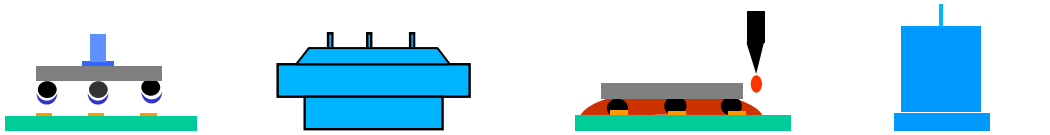


Figure 1.4 Capillary underfill process flow

1.5.1 Capillary Underfill Materials

For capillary flip chip assembly, most underfills contain about 70% filler particles. The fraction of filler particles together with its properties such as size, shape and size distribution can affect the underfill viscosity and, hence, underfill dispensing [14]. IBM introduced underfills in 1990, which greatly improved chip reliability [3]. However, the first underfills suffered from high viscosity, slow flow rates and long curing times, none of which were conductive to high volume production. Later, Motorola, an IBM flip chip licensee, began to seek a better underfill material with a quick flow rate and short cure time. New fast flow, snap cure underfills [15-17] were developed by several researchers. Compared with standard underfill, fast flow, snap cure underfill can reduce the cure time from 30-90 minutes to 5-10 minutes, and cut flow time under a 0.5'' square die from 1-5 minutes to 5-60 seconds [18].

1.5.2 Underfill Dispensing

Underfill is dispensed along the edge of a die using a dispense system. Dispensing may create underfill voids or a non-uniform fillet if not properly controlled. To obtain good dispensing, it is important to understand the characteristics of underfill flow.

Schwiebert and Leong [19] presented an equation that can be used to estimate underfill flow time. Their model assumed viscous flow between two parallel plates. The flow time, T, can be calculated as

$$T = (3\mu L^2)/(h\gamma\cos\theta) \qquad (1.1)$$

Where, μ is the absolute viscosity of the fluid, L is the flow distance, h is the separation distance between the two plates, γ is the surface tension of the liquid-vapor interface, and θ is the wetting angle of the fluid on the plate. This equation ignores the effect of solder bumps, surface roughness, flux residue and other flow obstructions. This equation indicates that the flow time is inversely proportional to the surface tension, separation distance, and the cosine of the wetting angle, and directly proportional to the viscosity and the square of the flow distance.

For a real underfill dispensing process, many factors may affect the underfill flow, such as dispensing pattern [20], substrate temperature [21] and needle temperature. The dispensing pattern is largely determined by the number of solder bumps, bump pattern, die size and underfill viscosity. The underfill viscosity changes with temperature and a higher temperature will lower the underfill viscosity and thus accelerate the flow speed. On the other hand, too high a temperature may result in partially underfill cure, causing

the underfill to stop flowing. The temperature must be carefully controlled to properly underfill the die. The underfilling process is usually conducted at an elevated temperature through heating of the substrate.

As noted previously, the flow of the capillary underfill is based on the capillary mechanism, which is time-consuming. The flow time increases with the square of the chip size and the inverse of the standoff height. Based on semiconductor and packaging roadmaps, it is clear that trends for larger devices and high packaging densities will continue to increase [22]. The trend is also to finer pitch bumps which results in smaller bumps, and hence results in lower gap heights which will reduce flow speed. This will inhibit cost-effective and high throughput production with the conventional underfill process. New and innovative technologies are required. Fluxing underfill and wafer-applied underfill technologies are two approaches being pursued.

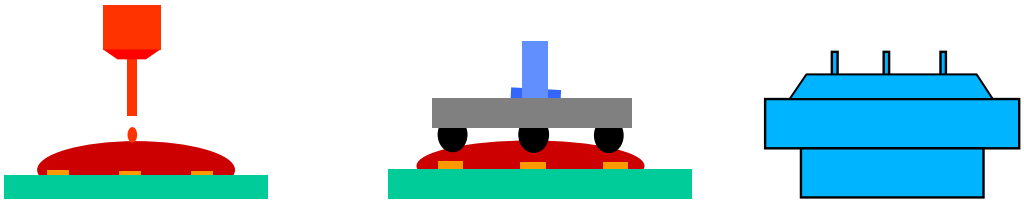
1.6 Fluxing Underfill Process

The concept of the fluxing underfill process was first presented by Pennisi and Papageorge in 1992 [23]. Fluxing underfills are polymer systems that incorporate fluxing activity into the underfill. The assembly process integrates the solder reflow and underfill cure together. There is no separate underfill flow process, and so this is often referred to as a “no flow” process.

Compared with the capillary flow process, the fluxing underfill process needs less equipment and has higher assembly throughput. However, there are several issues and concerns related to this process. The PCBs must be dehydrated to remove the absorbed moisture prior to assembly. Placement may induce underfill voids, and assembly yield is

sensitivity to the reflow profile [24]. The fluxing underfill cannot contain a high level of filler, as it may interfere with the solder joint formation [25, 26]. A low level of filler in the underfill results in a high CTE of the underfill, so the CTE mismatch between the underfill and solder joints is large. This will decrease the assembly reliability.

The fluxing underfill process is shown in Figure 1.5. It consists of three main processes. First, a controlled amount of fluxing underfill is dispensed onto the die site on the substrate. Then, the bare die is placed into the underfill. A placement force on the bare die is needed to squeeze the underfill until the solder bumps contact the substrate pads. Finally, the assembly passes through the reflow oven to make the solder connection and cure the underfill. A post reflow cure may be required depending on the material.



Fluxing Underfill Dispense Die Placement Solder Reflow & Underfill Cure

Figure 1.5 Fluxing underfill process flow

1.6.1 Fluxing Underfill Materials

Most fluxing underfills consist of epoxy resin, fluxing agent, hardener and catalyst [27]. The material properties of the fluxing underfill are very different than those of the capillary underfill due to the process difference. In comparison to capillary underfill, typical fluxing underfills have higher CTE, lower modulus and lower filler

content. Yan [28] summarized typical material properties for both capillary underfill and fluxing underfill for comparison, as listed in Table1.2.

Table 1.2 Properties of typical capillary underfill and fluxing underfill [28]

	Conventional Capillary Underfill	Fluxing Underfill
Curing Temperature	< 150 °C	Compatible with solder reflow
Curing Time	< 30 min	
Tg	> 125 °C	Usually lower
Working Life	> 16 hours	Similar
CTE	22-27 ppm/°C	60-80 ppm/°C
Modulus	8-10 GPa	2-3 GPa
Fracture Toughness	> 1.3 MPa·$m^{0.5}$	Typical lower
Moisture Absorption	< 0.25 %	Typical higher
Filler Content	< 70 wt%	None or very low

1.6.2 Fluxing Underfill Materials Development

In order to achieve a successful assembly, it is necessary to study the fluxing underfill material properties and to optimize the assembly process. Lu et al [29] characterized the underfill adhesion strength to the die passivation and found that the adhesion directly related to underfill delamination. Underfill delamination is the phenomena of underfill losing adhesion to the silicon die under thermal cycling loading.

It is usually initiated at the corner of dies, and will spread over the chip surface toward the center of die. This will degrade the reliability of the assembly. The underfill delamination was detected using C-mode scanning acoustic microscopy (C-SAM) in Lu's paper. Wong et al [30] analyzed the effect of the concentration of the hardener and catalyst on the physical properties of the cured underfills. Morganelli [31] investigated and reported the effect of toughening agents on fillet cracking of fluxing underfills. Zhang [26] studied the effect of incorporating fillers and presented a novel approach to incorporate silica fillers into the fluxing underfill. In this approach, two layers of underfill were applied onto the substrate prior to the die placement. The bottom underfill layer facing the substrate was fluxing and unfilled; the upper layer facing the chip was filled with 65 wt% silica fillers. A 100% yield of solder interconnect was achieved with this two-layer filled fluxing underfill system.

In the fluxing underfill assembly process, a die is directly placed onto the substrate pad site covered with pre-dispensed fluxing underfill. The forced motion of die placement causes a convex flow front to pass over the pad and solder mask-opening features promoting void capture. Milner et al [32] investigated the effects of substrate parameters such as pad height, solder mask opening height, pad/solder mask opening separation, and pad pitch on void formation. Colella et al [33] further showed that placement speed, force and dwell time had an impact on interconnect yield and void formation.

The reflow profile is very important for high yield assembly. The profile should allow chip collapse before the beginning of underfill gelation. Otherwise, failure of the chip to collapse will result in poor or open solder joints [34, 35]. Many companies have

invested considerable effort to develop fluxing underfill materials and processes for flip chip. No flow, fluxing underfills are commercial available from many companies.

1.7 Wafer-Applied Underfill Process

The concept of wafer-applied underfill was presented by Shi et al [36], Johnson and Baldwin [37], and Crane and Gamota [38] in 1999. The underfill is applied to the die at the wafer level. This pre-application moves underfill handing and application to the chip supplier, and allows for cost-effective application to hundreds or thousands of dies at once, instead of individually. The goal of the pre-applied materials is to provide the necessary fluxing activity during soldering and also serve as the underfill, curing during the reflow process. This creative process allows coated dies to be loaded into tape and reel, and to be handled just as any other surface mount part. Labor costs, facility costs and floor space are thus greatly reduced, a considerable benefit for SMT assemblers.

1.7.1 Wafer-Applied Underfill Materials

Researchers have been working on two wafer level underfill systems, single layer and two-layer materials [39]. Figure 1.6 shows some wafer-applied underfill approaches.

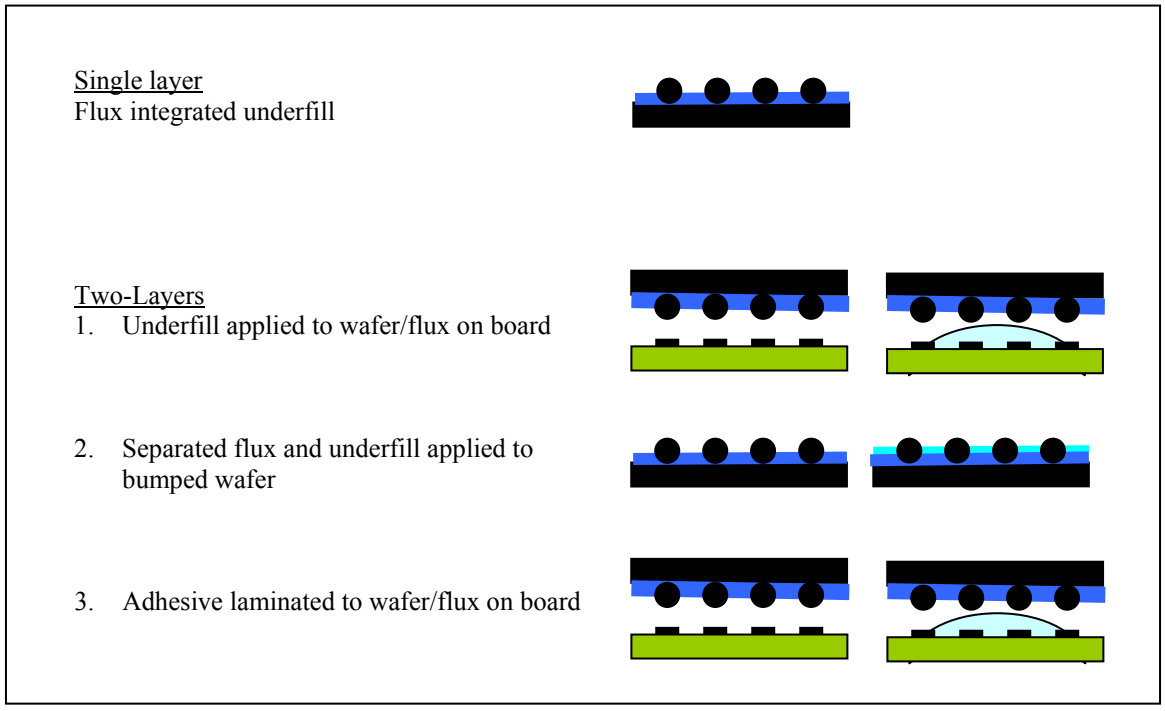


Figure 1.6 Current wafer-applied underfill approaches [39]

Single layer material serves as both flux and underfill. This material is usually not filled. The epoxy based, no flow underfills are a good candidate to build the single layer material since the flux agents such as carboxylic acids can serve as hardeners [39]. Pennisi and Papageorge [23] reported that a thermoset material including a fluxing agent and a curing agent was formulated and applied to a chip. The chip was positioned on the substrate and the thermoset material was heated to achieve tack that can hold the chip in place after placement. At the reflow temperature, the fluxing agent removed oxide from the solder and the substrate pad, and the curing agent reacted with and cured the thermoset resin. Since there is no dispensing process, the single material system has low assembly costs. However, short shelf-life limits its application.

The two-layer material systems consist of separate fluxing and bulk underfill layers [40]. The fluxing layer contains no filler that may affect solder joint formation between the solder bumps and pads on the substrate, but the bulk underfill layer in the two-layer system can be highly filled to reduce CTE to enhance reliability.

In two-layer systems, option 1 is to pre-apply a bulk underfill as a liquid to the wafer, then B-stage the resin to form a solid, tack free bulk underfill layer. The flux or fluxing underfill is dispensed onto the substrate prior to die placement. Johnson et al [41] developed a process where the liquid bulk underfill material was applied on the bumped die and then B-staged. The liquid fluxing underfill was dispensed onto the die site of the board. Aguila [42] has done some work on coating the underfill before bumping. An epoxy resin was screen printed, cured and then laser drilled to form openings for solder bumps. The solder bumps were formed by stencil printing solder paste into the openings and reflowing. For assembly a polymer flux was dispensed on the board, the die placement, and reflow then a post cure was used to complete the underfill cure. The assemblies were subjected to a liquid-to-liquid thermal shock test at -40 °C to + 125 °C. The assemblies passed as many as 7170 cycles.

In option 2, underfill and flux are sequentially applied as liquids and B-staged to form two solid layers. Since no dispensing step is required during assembly, the flip chip assembly can thus become truly transparent to a standard SMT assembly line [38]. The final coated die is tack free. However, some degree of tack is necessary to hold the die in place on the board after placement. In a normal SMT line, this tacky function is provided using the flux or solder paste. In the option 2 wafer-applied underfill assembly process, tack may be achieved by applying heat to the die and softening the coatings prior to

placement. The most efficient way to do this is to provide heat directly to the coated die. Commercial, high volume pick and place systems with die heating stations are already available [41]. Johnson [43] et al at Auburn University developed a method that used a heat sink to provide heat and soften the coated underfill in a pick and place machine without a heating system.

Option 3 is to pre-apply a bulk underfill in a solid form as a thermoplastic or thermoset film onto the wafer. This solid film can be high filled, and the flux is applied at the die site on the substrate prior to die placement. Capote and Zhu proposed the use of a pre-applied laminated film on the die and a liquid flux layer on the substrate [44].

1.7.2 Wafer-Applied Material Development

Wafer-applied underfill technology is still under development. Many research groups, such as Auburn-Loctite-Motorola, Georgia Tech-National Starch & Chemicals-National Semiconductor, and Aguila, have demonstrated the feasibility of wafer-applied underfills through a variety of approaches.

Several papers have been published on the development of wafer-applied underfill flip chip assembly [45-51]. However, most of these studies have been on underfill material formulations, characterization, processability and the wafer coating process. The materials and processing issues are complex. So far, no wafer-applied underfill materials for flip chip have been commercialized.

1.8 Lid Attachment Technology

1.8.1 The Role of a Lid

As clock speeds continue to increase, microprocessors face their biggest operational challenge ever, namely heat. More and more heat is being produced, and this heat must be dissipated in a way that will not hinder the device's functionality or reliability [52]. Traditional system thermal management solutions such as fan cooling are no longer sufficient. Integrated thermal management solutions are necessary for both current and future generations of microprocessors. These solutions are usually provided in the form of a lid that is integrated into the flip chip package. The lid provides a path for heat transfer from the device to a heat sink and offers mechanical protection of the device from the end user's heat sink attachment.

1.8.2 Description of Lid Physical Structure

Figure 1.7 illustrates a cross section of a typical lid attachment structure. The bottom unit in the figure represents the device (silicon die) that is a flip chip attached to a substrate. The lid is attached on the backside of the device using solder or some other thermally conductive material. Typically lids can be made from many materials, such as AlSiC, Al, Cu, CuMo, CuW and Silicon [53]. A heat sink is attached on the top surface of the lid.

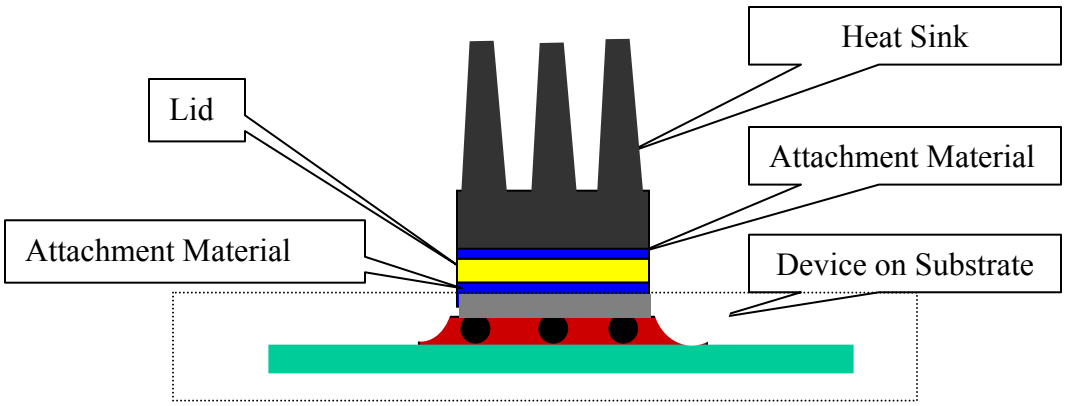


Figure 1.7 Cross section of lid attachment structure (drawing is not to scale)

1.8.3 Lid Attachment Materials

The basic requirements for lid attachment materials are that they should have high thermal conductivity, high strength, and good adhesion to the joining surface. They should also address any CTE mismatch between the lid and the silicon die. Conventional attachment materials include filled polymers and solder alloys. Polymer adhesives offer good strength and adhesive properties, and may be easily bonded to silicon, metal, ceramic, or ceramic composite materials without the need for flux and metallization of the joining surface. However, they cannot provide the same level of thermal conductivity as the completely metal bond formed by solder. Since high thermal conductivity is the most desirable property for lid attachment materials, soldering is an attractive joining method to form highly effective thermal bonds. Solder bonds also offer additional advantages such as reworkability compared to polymer adhesives. Table 1.3 shows the typical properties of solder and conductive adhesive approaches [54].

Table 1.3 Comparison of solder and conductive adhesive junctions, typical values [54]

Characteristic	Tin-lead solder	Conductive adhesive
Volume electrical resistivity	0.00015 Ω·cm	0.00006 Ω·cm
Junction electrical resistivity	10-15 mΩ	< 25 mΩ
Thermal conductivity	30 W/m·K	3-5 W/m·K
Shear strength	100%	40-110% (solder as 100%)
Mechanical shock performance	Good	Poor
Temperature and humidity (85%/85°C)	No change	Product specific
Minimum process temperature	210 to 220 °C	25-150 °C
Environment impact	Negative (Lead)	Minor
Thermal fatigue	Yes	Can be minimal

1.8.4 Lid Attachment Process

When a thermally conductive adhesive is used as the attachment material, the process begins with applying the adhesive on the back of the die using dispersing or printing. Then, the lid is placed into the adhesive using a pick and place machine. The final step is to cure the adhesive in a box oven or through a conveyor oven. The adhesive can also be coated onto the lid and dried. The precoated lids, as would be expected, offer a very manufacturing-friendly format, and the method has gained popularity [55]. A third option is the use of preforms. Preforms are extruded, stamped, compacted or formed

pieces of adhesive or pure soft solder alloys. A wide variety of preform shapes such as washers, discs, pellets, collars, ribbon forms, rings, and wire forms can be created for different applications. The preform can be manually placed over the backside of the die, and then the lid is placed on top of the preform. After the lid placement, the assembly is heated to cure the adhesive.

For solder attachment, solder paste can be screen printed or dispensed on the backside of the die. The lid is then placed onto the paste, and the connection forms in a solder reflow process. Solder preforms can also be used to attach the lid to the die. They provide an extremely repeatable solder volume. Preforms can also be handled easily by automated equipment, allowing high production capacity.

1.9 Lead-Free Technology

Environmental concerns have led to regulations requiring lead-free electronics packaging in many countries. The Waste Electrical and Electronic Equipment (WEEE) Directive in Europe banned lead in many electronic assemblies and products beginning July 1, 2006, and although only 7% of the total Pb consumption in the United State is from the electronics industry, there is pressure to remove Pb from all electronic manufacturing processes.

The most common electronic solders are 63Sn/37Pb and 62Sn/36Pb/2Ag. As an alternative to these alloys, several Sn based lead-free solder alloys have been studied and shown to have acceptable mechanical properties [56]. SnAgCu alloy (SAC) is considered to be the most promising candidate for replacing eutectic SnPb solder in reflow applications. In general, different variations of the SnAgCu alloy (SAC), with Ag content

from 3.0% to 4.0% and 0.5% to 0.7% Cu, are all acceptable compositions for lead-free soldering. For binary lead-free solder, Lin et al [57] showed that 99.3Sn0.7Cu has superior thermal and isothermal mechanical fatigue properties compared to 63Sn37Pb. Flip chip assemblies with this solder alloy on Cu under bump metallurgy (UBM) bumps exhibited excellent fatigue life performance.

1.10 Research Objectives

This project focused on the development of flip chip assembly processes. One objective of this research was to develop an assembly process for fine pitch flip chip array packages with lead-free solder, and included the development and characterization of an improved process for flip chip array package assembly. Another objective was to implement flip chip technology on a conventional SMT assembly line by developing a suitable flip chip assembly process with a wafer-applied underfill. The third objective was a lid attachment study. Lid attachment was performed using multiple assembly methods.

The development of lead-free solder assembly of a fine pitch flip chip is described in Chapter 2. Large die with fine pitch were assembled on ceramic substrates. Process parameters were optimized to achieve a low level of underfill voiding. Reliability of the assemblies and failure analysis were also studied.

Chapter 3 presents the development of a new wafer-applied bulk layer assembly process. The assembly process is similar to that used with fluxing underfill. The liquid flux was dispensed onto the board prior to placement, while the bulk underfill material

was applied at the wafer level. The material evaluation, coating evaluation, reflow profile development, reliability testing and failure analysis are described in detail.

Chapter 4 describes the lid attachment process for flip chip in package. Assembly methods and reliability testing results are presented.

Chapter 5 concludes the dissertation. The findings of this dissertation are summarized and suggestions for future work are given.

CHAPTER 2

LARGE SIZE, FINE PITCH LEAD-FREE FLIP CHIP ASSEMBLY

2.1 Introduction

As flip chip die become larger in size, finer in pitch and lead-free, technical challenges such as poor solder wetting and underfill voiding need to be addressed. These problems may decrease flip chip reliability, and limit the use of this technique for many applications.

For large dies, the underfill will take a longer time to flow under the whole die. A finer pitch die usually has smaller solder ball diameters, and hence may result in a small gap between the die and substrate after reflow. The longer underfill flow time and lower gap between the die and substrate may affect underfill flow and result in voids or other underfill defects.

In this chapter, the capillary flow assembly process for large, fine pitch lead-free flip chip die is investigated. Assemblies were subjected to an air-to-air thermal cycle test (AATC) to evaluate their reliability. Failure analysis was conducted to identify failure modes using C-SAM, cross-sectioning and scanning electronic microscopy (SEM) techniques.

2.2 Test Vehicle

The test vehicle consisted of bumped test dies (X1740) mounted on a ceramic substrate. The test die was 20.5 mm square and 0.67 mm thick (Figure 2.1). There were 4330 solder balls arranged in a nonsymmetrical array on the die. The solder balls were 85 μm in diameter and the bump pitch ranged from 150 μm to 275 μm. The solder alloy was 97.5Sn2.5Ag. A 16 μm Cu stud was used as the UBM. The substrate shown in Figure 2.2 was a 49 mm × 49 mm × 1.7 mm ceramic substrate (Kyocera A440) with 6 perimeter rows of pins on one side. The substrate pads were 80 μm in diameter with an electroless nickel/electroless gold finish.

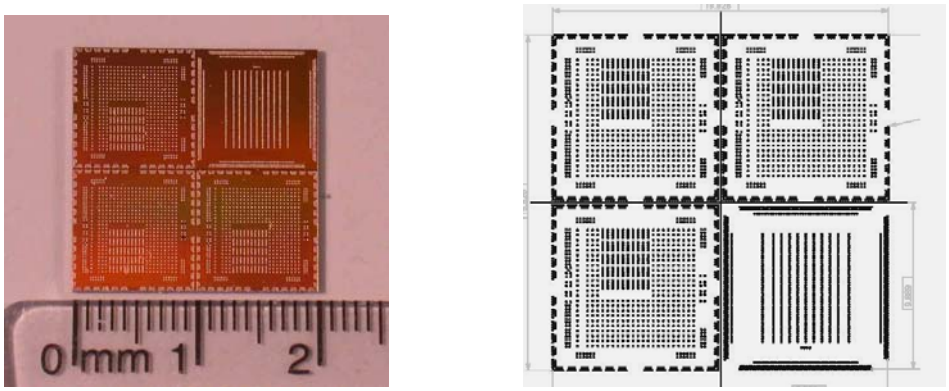


Figure 2.1 Test die and its solder ball pattern

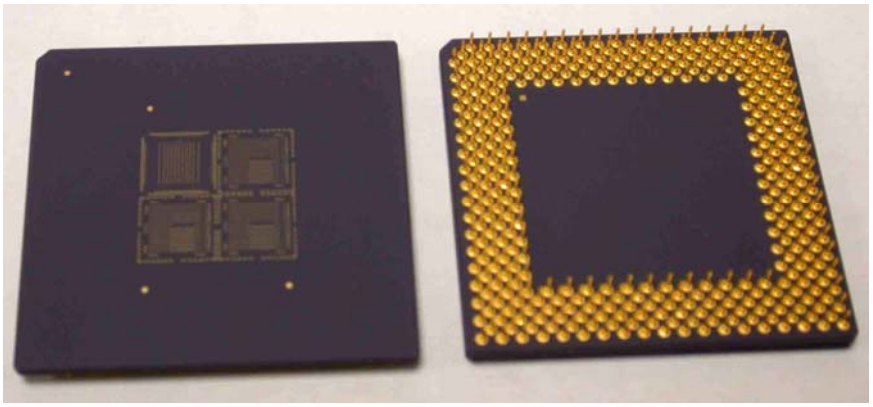


Figure 2.2 Ceramic substrate

2.3 Description of the Assembly Process Flow

The test vehicles were assembled on an automated SMT line at Auburn University. A standard capillary flow assembly process was used, as shown in Figure 2.3. A Siemens F5 pick and place system was used for flux dipping and die placement. Assemblies were then sent through a Heller 1800 reflow oven for solder reflow. After soldering, underfill was dispensed using a Camalot 3700 dispensing system and then cured in a Blue M box oven.

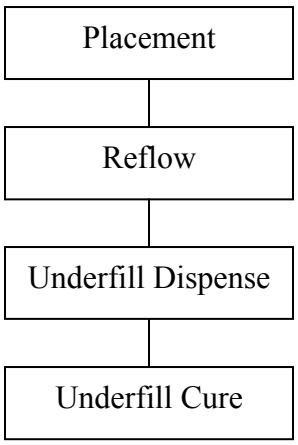


Figure 2.3 Assembly process flow

2.4 Solder Wetting Study

2.4.1 Flux Materials

The flux provides two main functions: to hold the chip in place and to remove oxides from the solder bumps and the substrate pads, enabling the solder to flow and wet the substrate pad surface. The higher soldering temperature needed for lead free solder requires greater stability of the flux at high temperature. Two fluxes were evaluated for

use with the 97.5Sn2.5Ag solder bumps. One flux was TF38 from Heraeus. TF38 is a low residue, no clean tack flux designed for use in the attachment of bumped chips to various substrates. This tack flux is based on a synthetic oligamer and rheology modifier, and provides for a higher tolerance to thermal cycling and compatibility with most underfill compounds [58]. TF38 has sufficient activity to tolerate 0.1% O_2 in the reflow oven. Another flux was TSF 6502 from Kester. TSF 6502 is a no-clean tacky soldering flux formula that possesses a high activity level, and was designed for a wide range of temperature and humidity conditions [59].

The fluxes were applied using a rotating flux station on the Siemens F5 pick and place system. The flux transfer volume was controlled by the depth of the flux on the rotating station and the dip time. With the dip time held constant, the flux depth was varied to study the role of flux on solder wetting and underfill voids. Table 2.1 summarizes the assembly results. All of the assemblies exhibited good solder wetting. Slightly fewer underfill voids were observed when TF38 was used. There was no significant effect on the solder wetting or the underfill voids when the depth of flux was increased from 25 μm to 35 μm. Flux TF38 with a flux depth of 25 μm was used for the remaining studies.

Table 2.1 Summary of assembly results

	Depth of Flux: 25 μm		Depth of Flux: 35 μm	
	Solder wetting	Underfill voids	Solder wetting	Underfill voids
TF 38	Good	Small void (less than TSF 6502)	Good	Small voids (less than TSF 6502)
TSF 6502	Good	Small voids	-	-

2.4.2 Reflow Profile

A reflow profile was developed for the 97.5Sn2.5Ag solder using a Slim KIC profiling system. The profile is shown in Figure 2.4. Assemblies were heated from room temperature to 150 °C at a maximum rate of 2.0 °C/sec. The assemblies were then maintained within a temperature range from 150 °C to 170 °C for 72 seconds to allow for solvent evaporation and flux activation to occur, and then heating continued to a peak temperature of 249 °C. This profile resulted in a time above the melting point (225 °C) of approximately 63 seconds, and required a total of 5 minutes to complete the reflow. A nitrogen atmosphere was used throughout the reflow operation. The oxygen content was below 60 ppm.

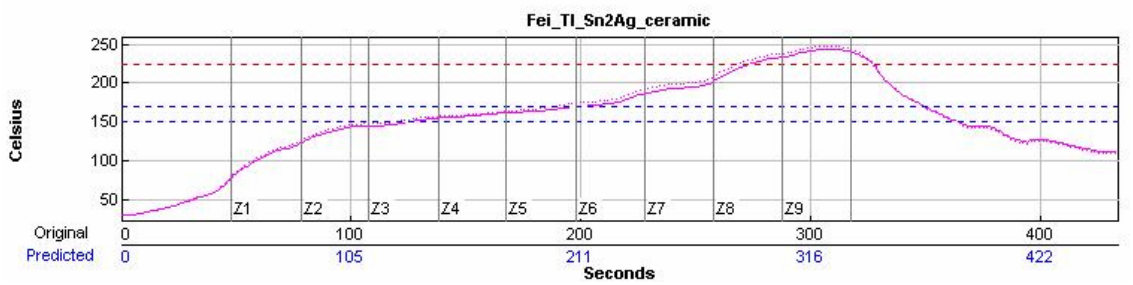
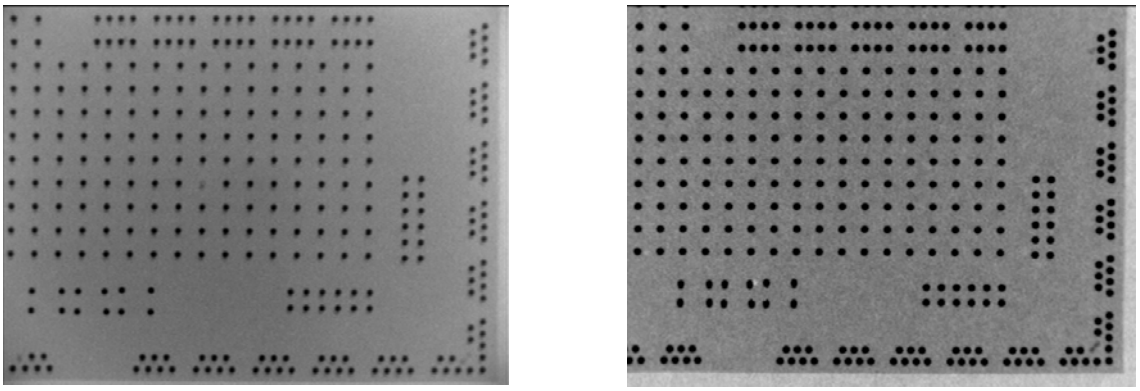


Figure 2.4 Reflow profile for flux TF38 with Sn2.5Ag solder

A variety of evaluation methods were used to assess the results after soldering, including die shear, X-ray inspection and cross-sectioning for direct joint observation. Die shear was tested using a Dage die shear machine. The results showed that all pads on substrate were sheared off. This indicates that solder joints were formed between the die and substrate. The X-ray images in Figure 2.5 show that the assemblies had the ability to self-align. The surface tension of the molten solder pulled the die into alignment with the substrate pads. This self-alignment ability also indicated that good solder wetting was achieved. Cross-sectioning was performed to verify the quality of the solder joint formation. Figure 2.6 shows that high quality solder joints were formed between the die and substrate.



(a) As-placed (b) After reflow

Figure 2.5 Self-alignment ability showing good solder joint formation

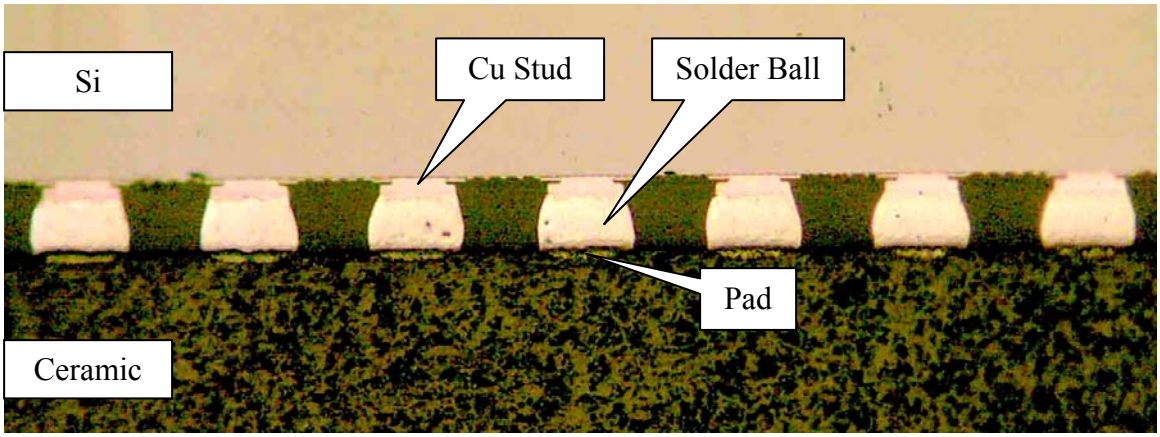


Figure 2.6 Cross-sectioning picture, showing good solder joint formation

2.5 Underfill Voiding Study

The use of an underfill can minimize the shear stress generated by the CTE mismatch between the die and substrate. This shear stress is well known to lead to early fatigue failure in the solder joints. It is also known that underfill voiding is a common problem for flip chip assembly especially for large dies. These voids can adversely affect reliability [60].

Void detection was conducted using the C-SAM technique. C-SAM is a powerful tool that allows the user to detect voids in the underfill material on the actual production parts. It is also useful in reliability testing to detect underfill delamination.

2.5.1 Underfill Materials

Ablestik Ablefill MB1502 was selected as the underfill material. This underfill has a fast flow rate and good self-filleting properties to eliminate the need for a secondary fillet dispense process. The recommended cure condition is 90 minutes at 150 °C. Material properties are given in Table 2.2. Other underfills, such as CNB944-15, FP4547FC and FP4549SI from Loctite, were only used for the flux residue study in Section 2.5.4.

Table 2.2 Material properties of Ablefill MB1502 underfill

Viscosity	Tg	Modulus	CTE
20,000 cP	114 °C	3.4 GPa	50 ppm/°C

2.5.2 Fishbone Diagram for Underfill Voids

Eliminating underfill voids requires careful optimization of many process parameters. The fishbone diagram summarizes the factors affecting underfill voids in the flip chip assembly process, as shown in Figure 2.7.

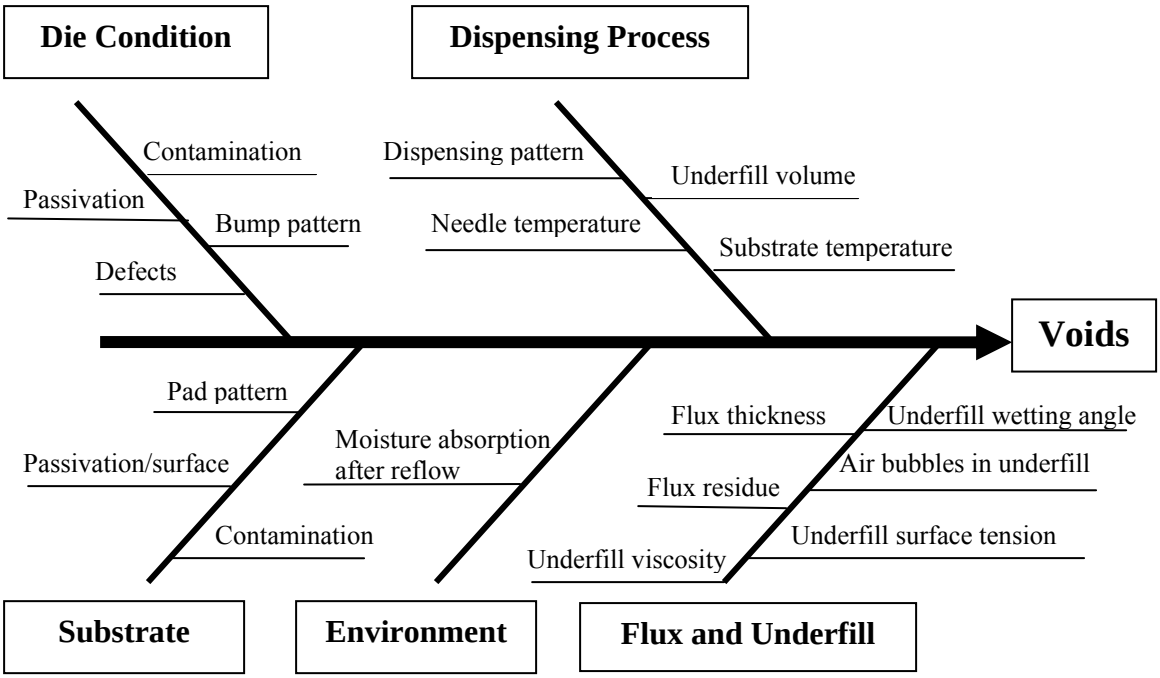


Figure 2.7 Fishbone diagram for underfill voids

Based on the fishbone diagram above, three main process factors were investigated: dispensing process, flux residue and die condition. These are discussed in turn below.

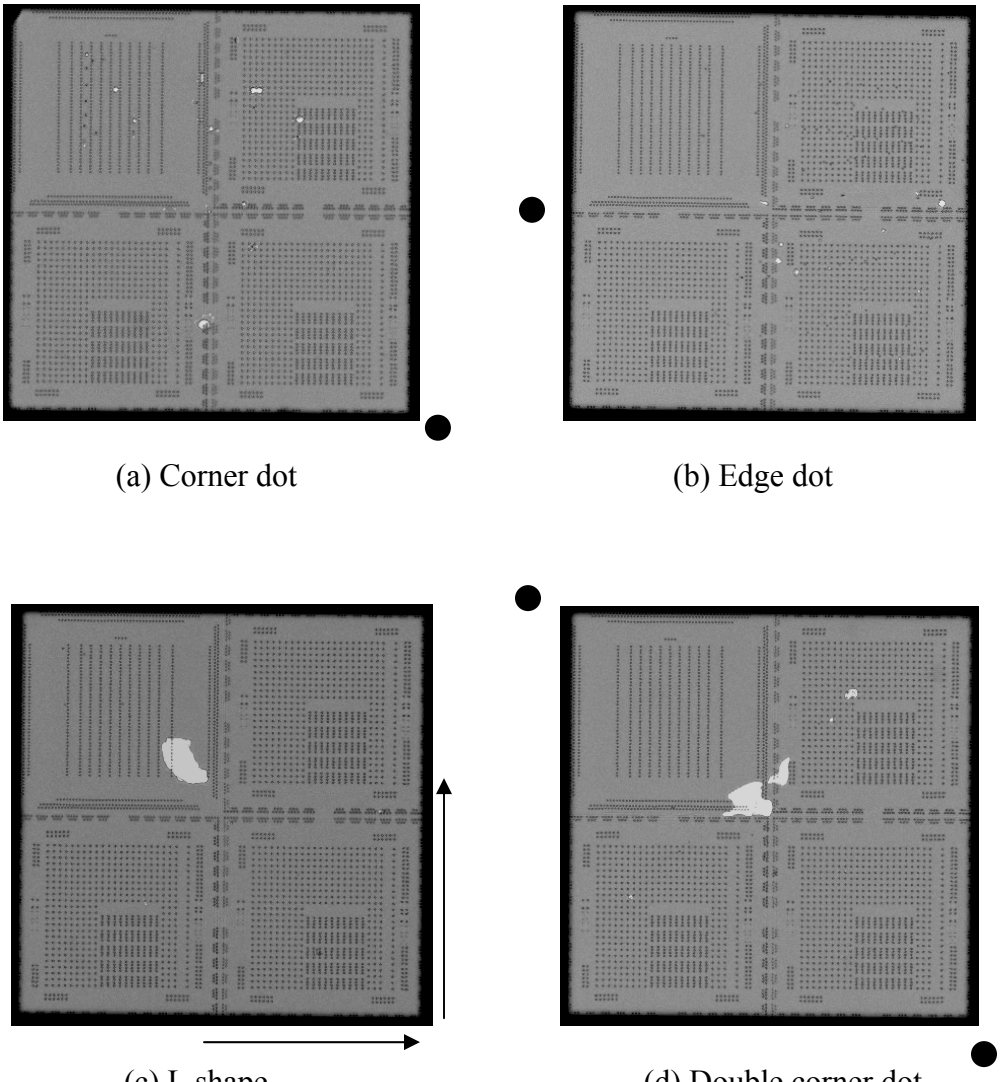
2.5.3 Effect of Dispensing Process

Underfill dispensing was performed with a Camalot dispensing system using an 18-gauge needle. Factors in the dispensing process that may affect voiding include dispensing pattern, underfill volume, needle temperature, and substrate temperature.

2.5.3.1 Dispensing Pattern

The underfill dispensing pattern is a critical factor that affects underfill flow and, hence, voiding. Several dispensing patterns were developed for the parts with asymmetric area array solder joints. The dispensing patterns and assembly results were shown in Figure 2.8.

The simplest dispensing pattern tested was a single drop at the corner (a) or at the middle of one side (b). The single dot pattern eliminated big voids and produced assemblies with a few small voids. At the same time, big voids were observed using an L-shaped dispensing pattern (c) because the material tended to spread too fast along the die edge, surrounding a big void in the die center. A non-continuous dispensing pattern such as the double dot (d) was also prone to causing voids since the underfill flow fronts easily trap a pocket of air after they rejoin. Since the die had an asymmetric bump pattern, dispensing on different die sides was also examined. No significant effect on underfill voids was observed when dispensing on the different die sides. The corner dot and edge dot pattern were thus determined to be the optimum dispensing patterns.



(a) Corner dot (b) Edge dot

(c) L shape (d) Double corner dot

Figure 2.8 Different dispensing patterns

2.5.3.2 Underfill Volume

An excessive dispensing volume can result in the underfill fillet climbing over the top of the die. Insufficient underfill could increase the flow time and form non-uniform fillets or in the extreme case not completely underfill the die. Various underfill amounts were tested and 50 mg was found to be the optimum amount that produced good fillets without big underfill voids.

2.5.3.3 Needle Temperature

The underfill temperature could be increased by heating the dispensing needle. Higher temperatures decrease the viscosity of the underfill. This prevents the underfill from forming a "tail" as the needle retracts, especially for high viscosity underfills. Needle set-point temperatures at: ambient and 43 °C were evaluated. It was found that the level of voids was not affected by needle temperature. No needle heating was used in this study.

2.5.3.4 Substrate Temperature

The most common way to increase the underfill flow is to heat the substrate during the dispensing process. Measured substrate temperatures of 85 °C, 90 °C, 95 °C, 100 °C and 107 °C were evaluated in an attempt to lower the underfill voiding level. However, temperature was found to have no significant effect on voiding level in this study. 90 °C was used as the substrate temperature.

2.5.4 Flux Residue

No clean flux leaves inert residue after reflow. These residues do not pose a long term risk for corrosion. However, they may impede the flow of underfill, and cause voids. In addition, flux residue in the assemblies may also degrade the reliability of the component due to chemical interactions with the underfill or degraded adhesion. Therefore, it is necessary to investigate a cleaning process after reflow.

After solder reflow, the assembled parts were cleaned using a 10% concentration of HYDREX DX aqueous cleaner to remove the flux residue. HYDREX DX is a VOC (Volatile Organic Compound) free, high performance alkaline cleaner with exceptional wetting properties and detergency, which can be used to remove water soluble flux and paste residues as well as rosin and many no-clean flux and paste residues after reflow [61]. The diluted HYDREX DX solution bath was kept at 72 °C during the cleaning process. The parts were submerged into the bath for 30 minutes, and then dipped in DI water at 70 °C for 30 minutes. For sufficient cleaning, an ultrasonic bath was used for both the HYDREX DX and DI water. After rinsing in DI water for 5 minutes, compressed air was used to blow out the water from underneath the dies; the parts were dipped into DI water, then blown again, 5 times. The parts were submerged in Ethanol in the ultrasonic bath for 5 minutes, and again blown dry. Finally, the parts were dried at 125 °C for 6 hours prior to underfill dispensing. The cleaning process is illustrated in Figure 2.9.

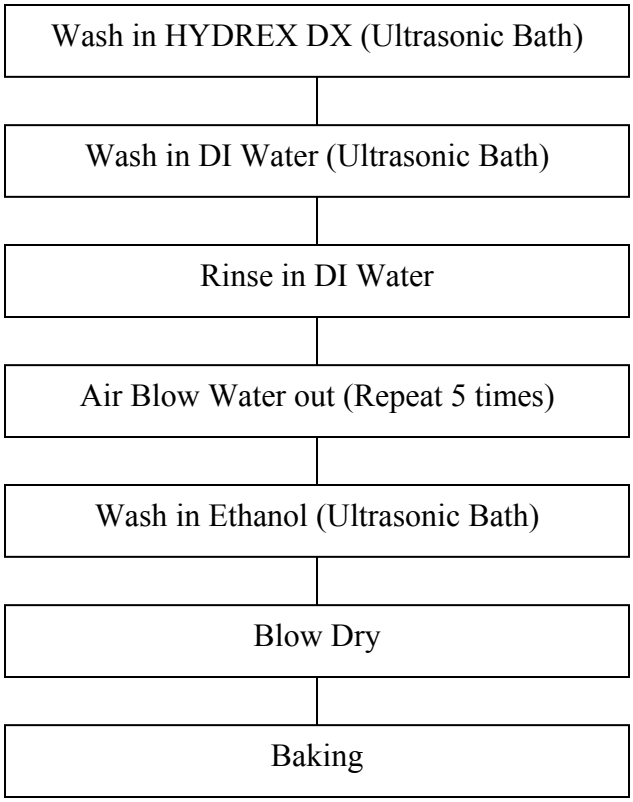


Figure 2.9 Assembled parts cleaning process

After cleaning, the assembled parts were dispensed with underfill and then cured. MB 1502 and three underfills from Loctite were used to evaluate this cleaning process. Parts without cleaning were also dispensed with the same underfill for comparison purposes. All parts were examined using C-SAM. The results are listed in Table 2.3. Voiding was slightly decreased after flux residue cleaning for one of the underfills (CNB944-15). In the other three cases, no change in voiding was observed. This cleaning process had little or no impact on underfill voiding. The suspected reason was insufficient cleaning of the parts. The HYDREX solution might not completely go under the whole part because of the large die size and small gap of the assemblies. To help the

HYDREX go through the part, water gun was used to blow the HYDREX during the cleaning process. However, no improvement was observed.

Table 2.3 Effect of cleaning process on underfill voiding

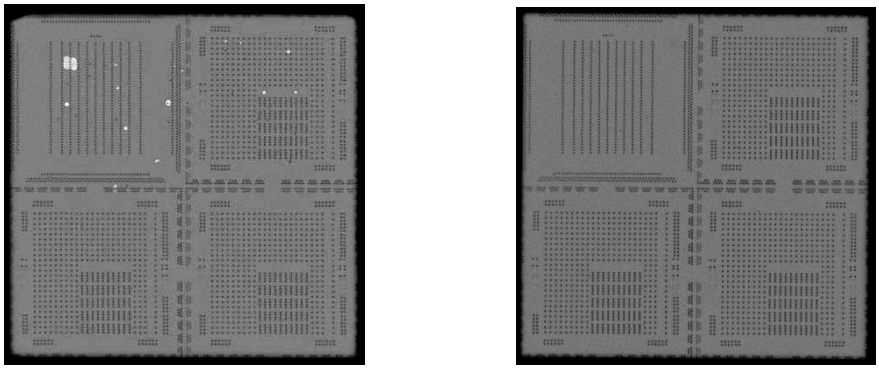
Flux	Underfill	Parts without Cleaning	Parts with Cleaning
TF38	CNB944-15	Small voids	Tiny voids
TF38	FP4547FC	Void free	Void free
TF38	MB1502	Small voids	Small voids
TF38	FP4549SI	Small voids	Small voids

2.5.5 Die Condition

Die contamination was considered as a factor that might cause underfill voids. In order to examine the effect of the die condition, dies cleaned prior to assembly were assembled onto boards utilizing Ablefill MB1502 underfill. No cleaning process was performed on the assemblies after reflow. For comparison purposes, as-received dies were also assembled onto boards with the same underfill.

A 10% concentration of HYDREX DX solution was used to clean the dies. The dies were submerged in this solution at 72 °C for 3 minutes, followed by dipping in DI water at 70 °C for 3 minutes. Then they were rinsed in DI water and ethanol, and then blown dry with nitrogen. Finally, all cleaned dies were baked at 125 °C for 5 minutes.

All assemblies were examined using C-SAM. Figure 2.10 shows the assembly results. Void free assemblies were achieved with cleaned dies.



(a) No cleaning process (b) with cleaning process

Figure 2.10 Comparison of underfill voiding level with and without cleaning process

The die surface was checked before and after cleaning using an optical microscope. No contamination on the dies as-received was observed. However, further study showed that the cleaning process changed the die surface condition. The wetting angle between the underfill and the die was measured using a specially designed optical microscope. The die-to-underfill wetting angle became smaller after the cleaning process, as shown in Table 2.4. From equation 1.1 in Chapter 1, the underfill flow time is inversely proportional to the cosine of the wetting angle. The liquid material with a low wetting angle has better flow properties, and hence better flow. The cleaning process thus benefited the underfill flow and thus contributed to a void free assembly.

Table 2.4 Wetting angle measurements

Underfill	Dies as received	Dies after cleaning process
Ablestik MB1502	22°	14°

2.6 Reliability Test

32 parts were assembled for reliability testing using optimum parameters as shown in Table 2.5. Flux TF 38 and Ablefill MB1502 were used, and all of the dies were cleaned prior to assembly. The reliability test was a 90 minutes -55/125 °C air-to-air thermal cycle consisting of 20 minutes of dwell time at each temperature extreme and 25 minutes transition between the temperature extremes. The test parts were inspected every 100 cycles. A Keithly 2001 multimeter was employed to perform 4–wire resistance measurements. The failure of an assembled die was defined to occur when its resistance increased by 10% over its initial resistance. To confirm the failure, the failed part was returned to the chamber and the resistance measurement repeated after an additional 100 cycles. If the two measurements were the same, failures were removed from the thermal cycle chamber and failure analysis was performed. The reliability test results are listed in Table 2.6.

Table 2.5 Optimum parameters

Dispensing pattern	Underfill Volume	Needle Temperature	Substrate Temperature
Edge dot	50 mg	Ambient	90 °C

Table 2.6 Reliability test results

Number of Failed Dies	Cumulative Number of Failed Dies	Cycles to Failure
1	1	300
1	2	1700
2	4	2400
11	15	2500
5	20	2600
4	24	2700
6	30	2800 (Test stopped)

The Weibull distribution is a widely used lifetime distribution function in reliability engineering. After AATC testing, the failure data was characterized using Weibull analysis. Figure 2.11 shows the Weibull plot. One plot (All Data) is for all of the data, while another plot (Censored Data) includes the data without the part that failed at 300 cycles. The parameters for both plots were summarized in Table 2.7. The characteristic life of assembly is the number of cycles at which 63.2% of the parts have failed.

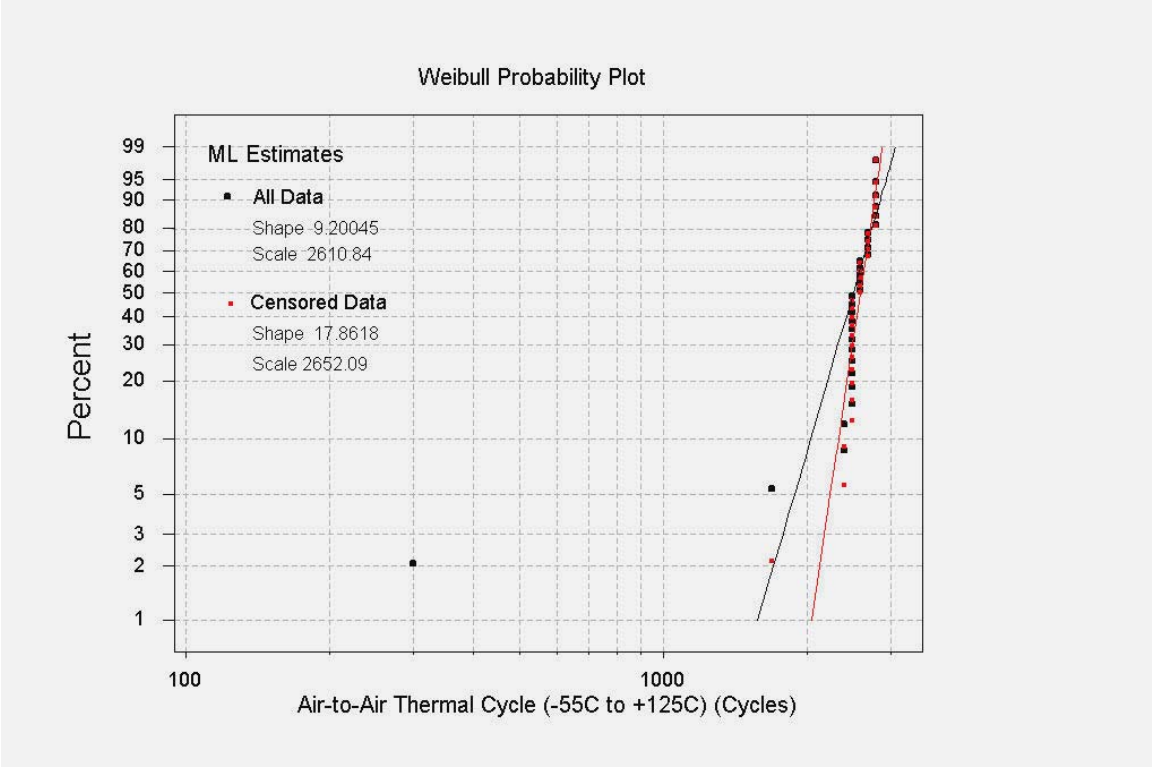


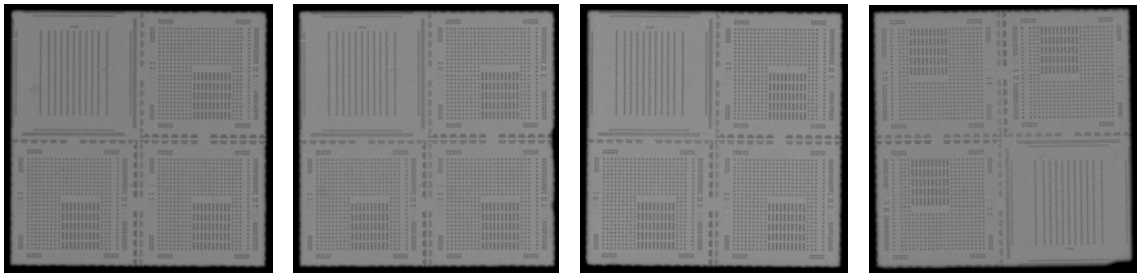
Figure 2.11 Weibull plot of the AATC

Table 2.7 Summary of AATC test results

	First Failure	Characteristic Life	Slope
All data points	300	2611	9.200
Censored	1700	2652	17.86

2.7 Failure Analysis

All of the tested assemblies were examined using C-SAM during the air-to-air thermal cycles testing. However, no underfill delamination was observed in the C-SAM pictures, as shown in the Figure 2.12.



0 cycle 300 cycles 1700 cycles 2400 cycles

Figure 2.12 C-SAM images

In order to analyze the failure mode, the related solder balls in the failed parts were cross-sectioned and inspected using a SEM. One part failed at 300 cycles and was considered an infant mortality. The suspected reason for this failure was the edge of the die was damaged during the assembly process. Unfortunately, the failure mode was not determined due to over polishing of the cross-section.

Die cracking was observed for the die that failed at 1700 cycles as shown in Figure 2.13. The cracks were located near the edge of the chip. From SEM analysis, the major observed failure mode was solder fatigue cracking as shown in Figure 2.14, where the crack propagation path is along the top solder joint, below the Cu stud. This is a common failure mode for flip chip assembly [62, 63].

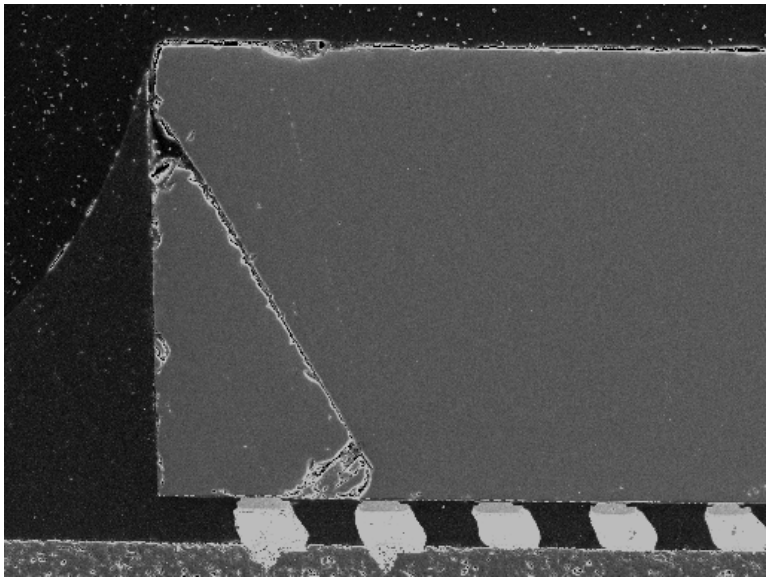


Figure 2.13 Die cracking at 1700 cycles

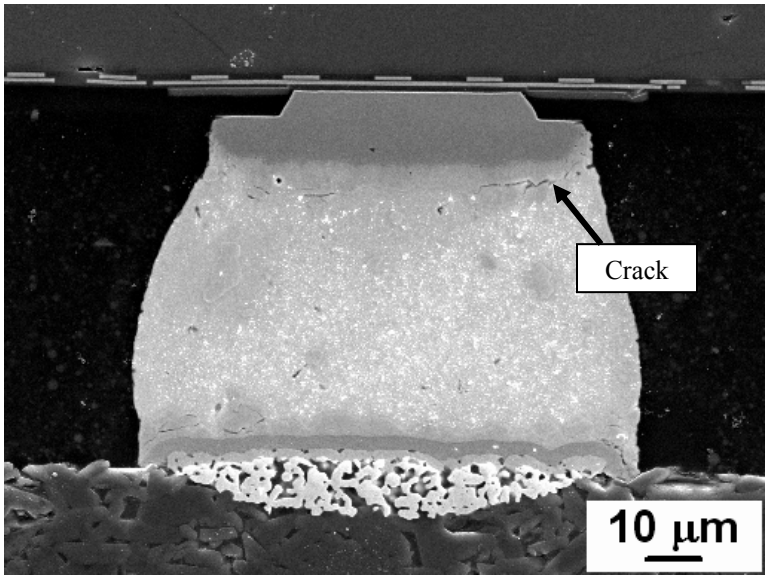


Figure 2.14 Solder fatigue cracking at 2500 cycles

2.8 Summary

This study focused on large size, fine pitch lead-free flip chip assembly process development. The combination of underfill Ablefill MB 1502 and flux TF38 was used as the assembly materials. The reflow profile was tested for the solder wetting. Dispensing parameters such as the dispensing pattern, underfill volume, underfill temperature and substrate temperature were optimized. The assemblies cleaned after reflow and the dies cleaned before assembly was also studied. The successful assembles were then tested in an air-to-air thermal cycling test. The great majority of assemblies survived for at least 2400 cycles and exhibited good reliability.

CHAPTER 3

WAFER-APPLIED BULK COATED FLIP CHIP ASSEMBLY

3.1 Introduction

To overcome some of the drawbacks of fluxing underfill described in Chapter 1, the use of wafer-applied bulk coated die was investigated in this study. A bulk material was coated at the wafer level prior to assembly. The assembly process then followed a conventional fluxing underfill process.

Compared to a conventional fluxing underfill, the bulk coated layer contained a high level of filler. This bulk material offers lower CTE, and hence potentially higher reliability. In addition, the flip chip coated with bulk material can be assembled on the PCB without a solder mask on the die site. Although this is not possible for a traditional flip chip assembly, it can be achieved for a wafer-applied bulk layer underfill assembly. The bulk layer that is coated prior to assembly limits the controlled collapse of the solder balls during reflow.

Assembly on the PCB board with no solder mask on the die site is a promising method that offers many advantages. The fluxing underfill dispensed on a conventional PCB may have air bubbles trapped in the solder mask openings during the placement process, as shown in Figure 3.1. The voids can only be minimized by minimizing the depth of the solder mask opening, and the separation distance between the copper pad

and the solder mask opening edge [64]. Obviously, there is no such problem when no solder mask is used. In addition, the registration requirements of the solder mask become tighter for very fine pitch of flip chip die. No solder mask at the die site is definitely welcomed by the PCB manufacturing company.

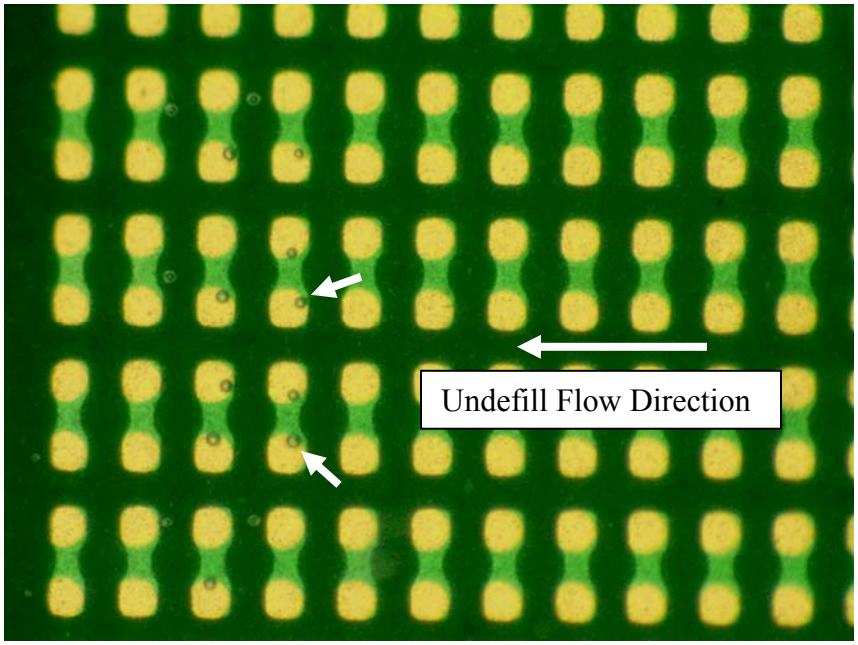


Figure 3.1 Underfill dispensed on a conventional board and placed with a glass slide.

3.2 Test Vehicle Description

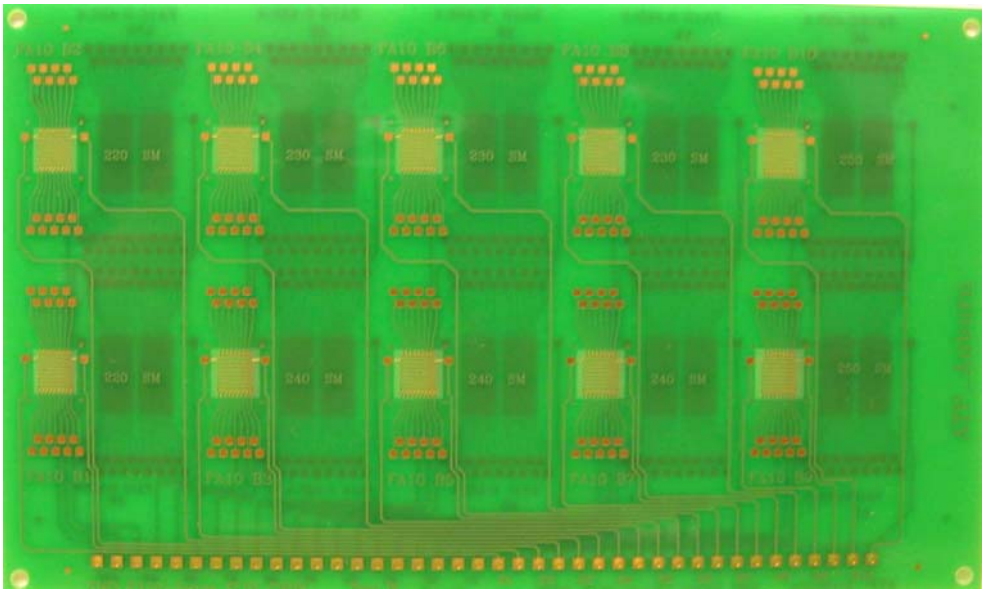
3.2.1 Test Die

The FA10 die is a commercial available test die and is shown in Figure 3.2. The die is 5 mm square with 250 μm pitch solder bumps in a full area 18 × 18 array (except 3 corners). The dies used in this study had eutectic Sn/Pb solder bumps.

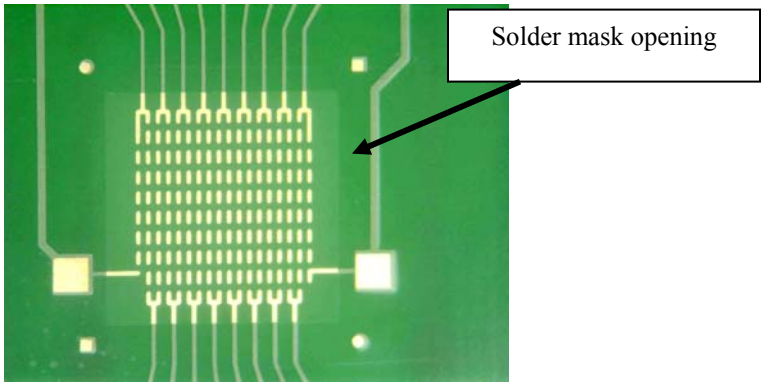
Figure 3.2 FA10 test die

3.2.2 Test Board

A FA10 test board designed by Auburn University was used, as shown in Figure 3.3. This board was made from a high Tg, FR-4 laminate, 0.67 mm thick with ten die sites. The board pads were 2.5 μm of electroplated nickel and 0.2 μm of immersion gold finish. This board had a large solder mask square opening at the die site.



(a) Test board



(b) Individual die site

Figure 3.3 Auburn FA10 test board

3.3 Wafer Coating Process

The underfill materials and the wafer coating process described in this section were developed and performed by the joint venture partner Loctite Electronic Materials. As illustrated in Figure 3.4, the wafer coating process started with the dicing of the wafer, after which the bulk material was coated on the wafer and B-staged to become tack free. The following is a step-by-step description of the requirements and coating processes used.

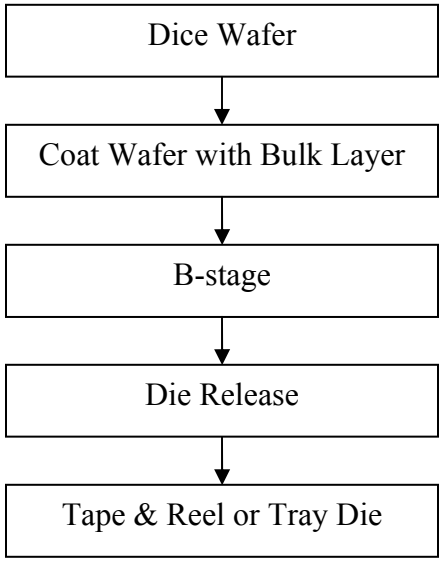


Figure 3.4 Wafer coating process flow

3.3.1 Wafer Dicing

Wafer dicing can be performed either before or after wafer coating. Some researchers [36, 48] have investigated the effect of wafer dicing after wafer coating. Since water is used in the cooling system for the saw blade, the compatibility of the

coated underfill with water is a concern. In addition, the presence of a coating in the saw street may cause saw blade failure [65].

In this work wafer dicing was performed prior to wafer coating. This process protected the coating materials from exposure to water. The tape for wafer mounting was not cut through during the cutting process. The individual dies were held together by the wafer saw tape for the following wafer coating step.

3.3.2 Bulk Material Coating

The bulk material provides the overall properties for the cured underfill. Good adhesion to the die and board is required for the bulk layer for high reliability [43]. The bulk layer should also be non-sensitive to reflow profile variations and cured after solder joint formation. If the material starts to gel too early, the bulk layer may prevent the solder bumps from wetting the pads. A Wafer-Applied Bulk Underfill (WABU) was used in this study. The properties of the bulk material are given in Table 3.1.

The filled bulk layer was coated using a modified stencil printing process on to the pre-sawn wafer. The saw streets were kept clean and the solder balls did not have any bulk layer over the top during this process. This is important in order to form the solder joints as filler particles on the top of the solder ball would impede solder joint formation, resulting in low assembly yield [43].

Table 3.1 Properties of Bulk Materials

		WABU Bulk Material
Physical properties, Before B-Staging	Appearance	Black, viscous fluid
	Filler content	60%
	Viscosity@25 ºC	42000 cps
	Shelf life @ RT	>6 month
Physical Properties, B-Staged Materials	Viscosity@ 90 ºC Viscosity@ 120 ºC	223.0 Poise 37.0 Poise
Physical Properties, Cured Materials	Tg, ºC by TMA	137.2
	Flexual Modulus, GPa	12.1
	Flexual Strength, MPa	152.4
Handling	Gel time @ 121 ºC	>30 minutes
Recommended Curing Schedule	165 ºC 180 ºC	2 hours 1 hour

3.3.3 B-staging

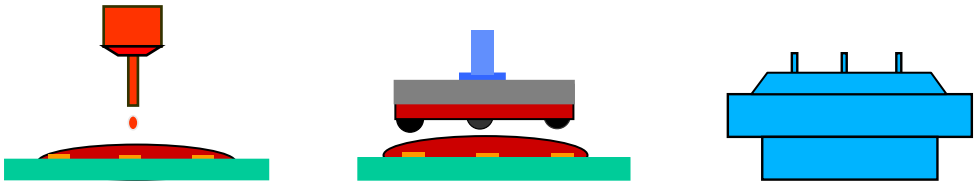
The bulk coated dies should be as easy to handle as other SMT components. Therefore, the bulk layer should be essentially tack free at room temperature. The coated wafer was placed in an oven for B-staging to create a solid and tack free surface. The B-staging conditions, such as temperature and time, should be carefully controlled so that the partially cured bulk layer can flow during the solder reflow stage.

3.3.4 Die Release and Loading

After B-staging, the dies were manually released from the wafer saw tape and loaded in a tape & reel or die tray. The dies were shipped and storage in metallized dry bags to protect them from moisture.

3.4 Overview of the Assembly Process

The assembly process at Auburn University began by baking the board to drive out moisture. After the dehydration bake, a controlled volume of fluxing underfill was dispensed over the pads on the boards. The coated die was automatically placed on the board with a Siemens F5 pick and place system. Following the coated die placement, the assembly was passed through the Heller 1800 reflow oven to form the solder joints and cure the underfill. A post cure was needed although this was targeted for elimination in future material development. After reflow, the assemblies were inspected by X-ray to ensure that the solder balls achieved good wetting in the pads. C-SAM was then performed to analyze for voids in the assemblies. Electrical continuity measurements were performed using a multimeter and a two-point measurement technique. The electrical continuity yield was defined as the percentage of the die that was fully connected. Figure 3.5 illustrates the assembly process flow.



Fluxing underfill Dispense Coated Die Placement Solder Reflow & Underfill Cure

Figure 3.5 Assembly process flow

3.5 Dehydration of the Test Board

It is well known that organic PCB boards absorb and retain moisture from the ambient air. The moisture will form vapor during the reflow process. This vapor is trapped in the gelling underfill layer and causes underfill voids. Baking the PCB board prior to assembly is an effect way to drive out the moisture. All of the boards tested in this experiment were baked thoroughly for over 6 hours at 125 °C.

3.6 Fluxing Underfill Dispensing Volume

Insufficient fluxing underfill dispensing might cause partial solder wetting, a small fillet or voiding. Excess fluxing underfill dispense can result in the die shifting before reflow due to buoyancy and the fillet force produced by the liquid fluxing underfill [66].

To determine the optimum fluxing underfill amount, the weight of fluxing underfill (264245) dispensed was measured using a microbalance. An 18 gage needle was used for dispensing, and the underfill volume was expressed in terms of the dispensed weight. This test was performed on test boards, where the openings of the solder mask on

the die site could retain the fluxing underfill and avoid fluxing underfill spread during the reflow process.

Table 3.2 summarizes the results of the fluxing underfill dispensing weight (volume) studies. The bulk coating layer thickness on the dies in this test was 3.4 mils thick. A fluxing underfill volume less than 1.4 mg was not enough for solder wetting, while a flux volume greater than 4.5 mg led to die shifting. The results indicate good dispense volume process tolerance.

Table 3.2 Effect of fluxing underfill dispensing weight

Underfill Volume	<1.4mg	2.6mg	4.5mg	6.5mg	>8.6mg
Solder wetting	Partial wetting	Good	Good	Some die shift	Die shift

3.7 Reflow Profile Development

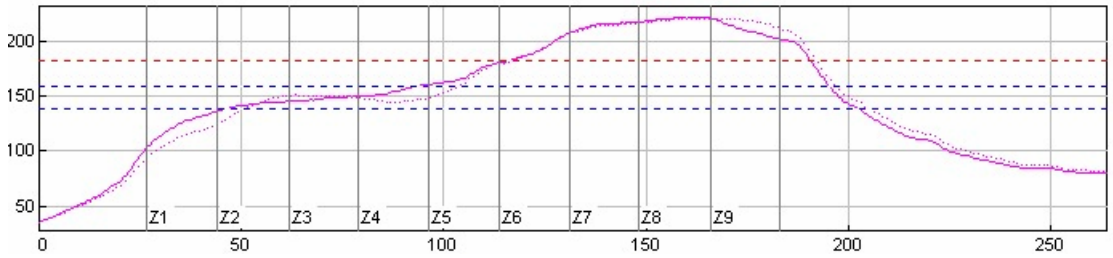
Reflow is a complex procedure to optimize for the wafer-applied bulk coated assembly process. Solder wetting and the underfill curing take place simultaneously, and their requirements often conflict. For instance, the bulk underfill must liquify during reflow so it will not prevent the solder balls from collapsing and forming joints. At the same time, it is desirable for the underfill to be cured when the board comes out of the reflow oven.

The two reflow profiles shown in Figure 3.6 were evaluated using fluxing underfill CNB946-17A in an air atmosphere. These profiles are compatible with the

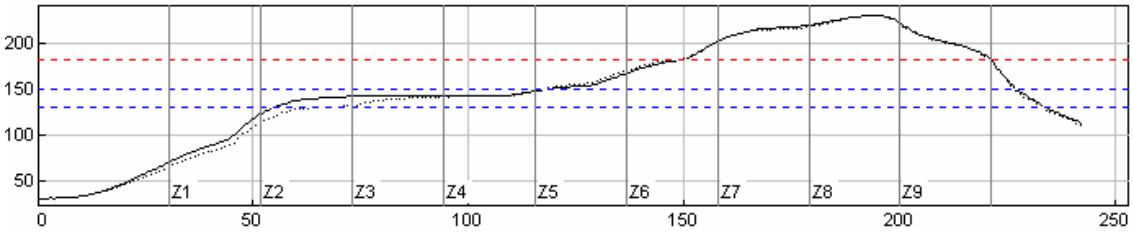
traditional SMT profile, and their parameters are listed in Table 3.3. Table 3.4 summarizes the assembly results for each profile.

Table 3.3 Reflow parameters for profiles A and B

	Soak temperature	Soak time	Peak temperature	Reflow time (above 183 °C)
Profile A	140-160 °C	45 sec	223 °C	74 sec
Profile B	130-150 °C	63 sec	231 °C	71 sec



(a) Profile A



(b) Profile B

Figure 3.6 Reflow profiles

Table 3.4 Results of assembly for two profiles

	Profile A	Profile B
Solder wetting	Poor (0% yield)	Good (100% yield)
Underfill voiding	Voids	Void free

The results show that profile B produced much better solder wetting than profile A. Profile B had a lower soak temperature and longer soak duration. This low soak temperature prevented the underfill from prematurely gelling, and the longer duration allowed the flux to completely act on the oxide of the solder, both of which are important for solder wetting.

Profile B was adopted as the reflow profile for the assembly process. Figure 3.7 displays a cross-section picture that shows good solder wetting. Some solder wet the connecting trace, resulting in less solder volume in the joint. However, good stand-off was retained.

Although the underfill fillet solidified after reflow, DSC tests showed that the underfill was incompletely cured. This would later affect reliability because an insufficiently cured underfill suffers from reduced strength. All of the assemblies required a certain amount of post cure, typically 60 minutes at 165 °C. New flux material could be formulated to achieve cure during reflow.

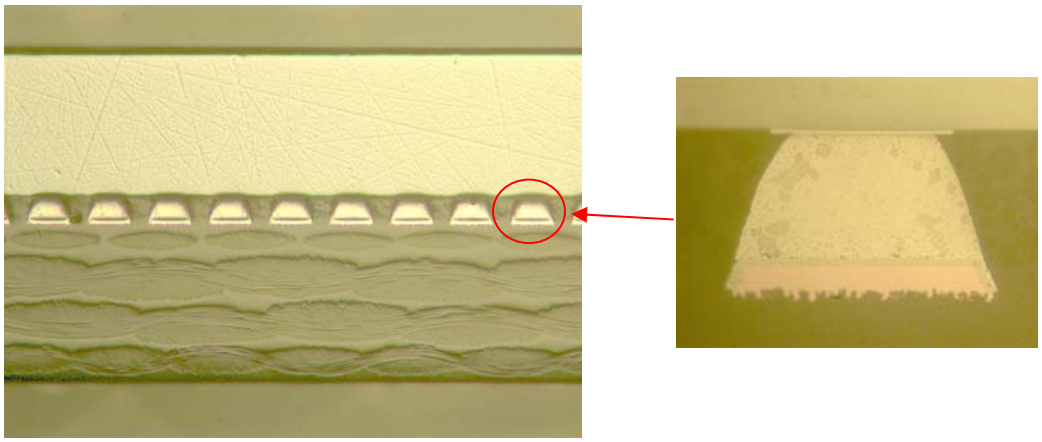


Figure 3.7 Cross-section shows good solder wetting

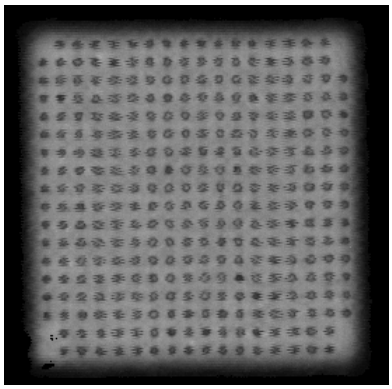
3.8 Placement Speed and Force

The placement parameters were based on previous work done by colleagues at Auburn University. The placement speed (acceleration rate) is an important factor that affects underfill voiding. The dispensing pattern used here was a center drop. The coated die first touched the center of the fluxing underfill on the board during the placement process. As the die continued moving down, the coated die squeezed and pushed the fluxing underfill outward. As the fluxing underfill moved, it passed around obstacles, such as solder bumps and copper traces. Air bubbles may become trapped in or behind these obstacles. Another important parameter was the placement force that brings the bumps into contact with the pads. Sufficient placement force was essential in order to cause squeeze flow of the fluxing underfill and ensure the bumps touch the pads, which is necessary for solder wetting.

Zhao [67] used a DOE to optimized placement parameters for fluxing underfill flip chip assembly. The minimum placement acceleration (0.1g) and maximum placement

force (10N) were selected. The assemblies with optimized parameters had a 100% yield and void free underfill. A similar study was conducted by Yan [68]. The coated FA10 test dies were placed in a fluxing underfill on the PCB board. The optimized placement force was 9N and resulted in good solder wetting and low underfill voiding.

In this study, a placement acceleration of 0.1g and placement force of 9 N were used for die placement. Figure 3.8 shows a C-SAM image of a flip chip die assembly with WABU bulk underfill and CNB 946-04 fluxing underfill.



CNB 946-04, void free

Figure 3.8 C-SAM picture of assembly with CNB 946-04 fluxing underfill and WABU bulk underfill

3.9 Reliability Tests

Assemblies with WABU bulk underfill and an optimized fluxing underfill (264292-1) were subjected to liquid-to-liquid thermal shock test (LLTS) after post curing at 165 °C for 70 minutes. All assemblies had excellent solder wetting onto the substrate pads and were nearly void free. LLTS was implemented under the following conditions:

- Extreme temperatures: -40 °C and +125 °C
- Dwell time at the extremes: 5 minutes
- Transition time: 1 minute

The resistance of the daisy chain was monitored in-situ to accurately determine the cycles-to-failure. The tests were conducted in a Blue-M thermal shock chamber. The failure of an assembled die was defined as its resistance increased by 10% over its initial resistance. The test was terminated at 1465 cycles. 9 dies were tested, and the results are listed in Table 3.5. The Weibull plot is shown in Figure 3.9. The characteristic life was 1122 cycles, and the slope of line was 4.24.

Table 3.5 Reliability test results

Number of Failed Dies	Cumulative Number of Failed Dies	Cycles to Failure
1	1	601
1	2	801
1	3	874
1	4	911
1	5	918
1	6	1323
1	7	1338
1	8	1378
0	8	1465 (test stopped

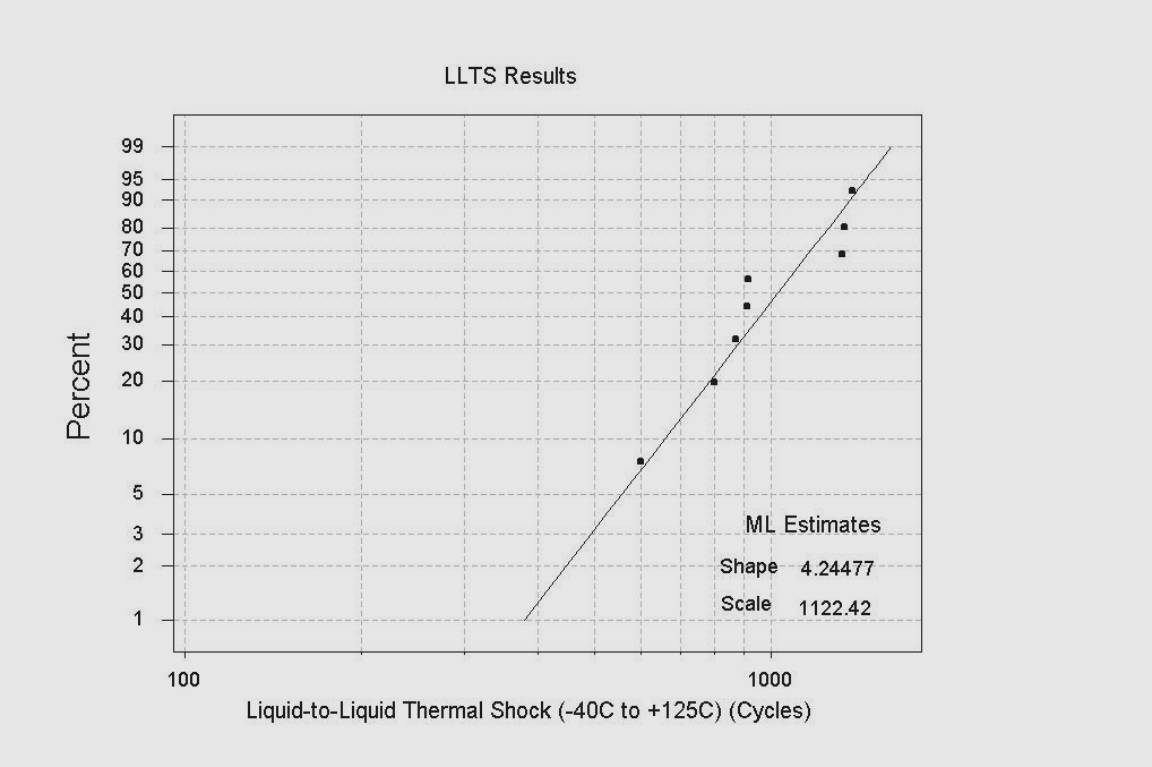


Figure 3.9 Weibull plot of cycles to failure

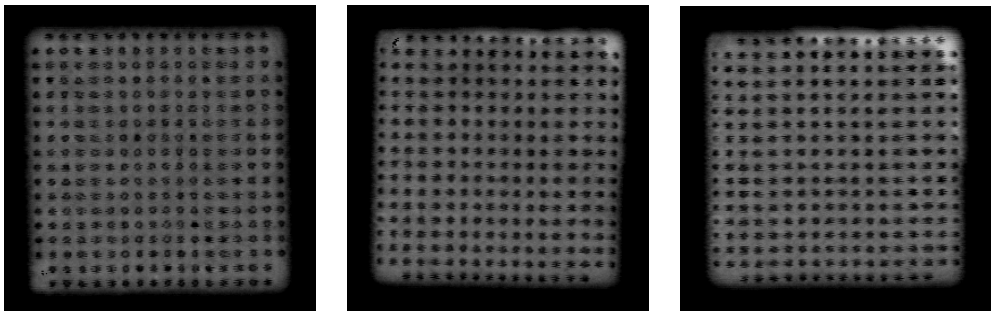
3.10 Failure Analysis

A series of examinations were performed to investigate the failure mode, including visual inspection of the underfill fillet for fillet cracks, C-SAM for underfill delamination, and cross-sectioning for solder fatigue cracking.

The test board was removed for C-SAM inspection after being subjected to 1000 cycles and after the test had been stopped. Figure 3.10 shows a typical C-SAM image of a part at 0, 1000 and 1465 cycles. The pictures show that the delamination was initially near the edges of die and developed with increasing cycles. Electrical openings in the daisy chains were found in the delaminated area.

A number of underfill fillet cracks that initiated after 1000 cycles were observed. Figure 3.11 shows an example of underfill fillet cracking.

Solder failures were inspected optically after cross-sectioning the assemblies. The cross-sectioning image verified the failure as open, as shown in Figure 3.12. The cracks were found to be in the solder joints near the UBM.



(a) 0 cycle (b) 1000 cycles (c) 1465 cycles

Figure 3.10 Delamination progression with LLTS

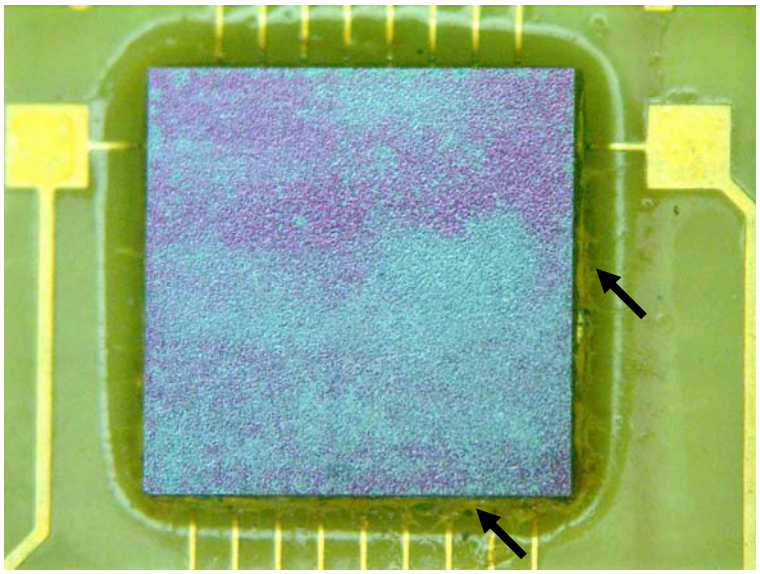


Figure 3.11 An example of underfill fillet cracking

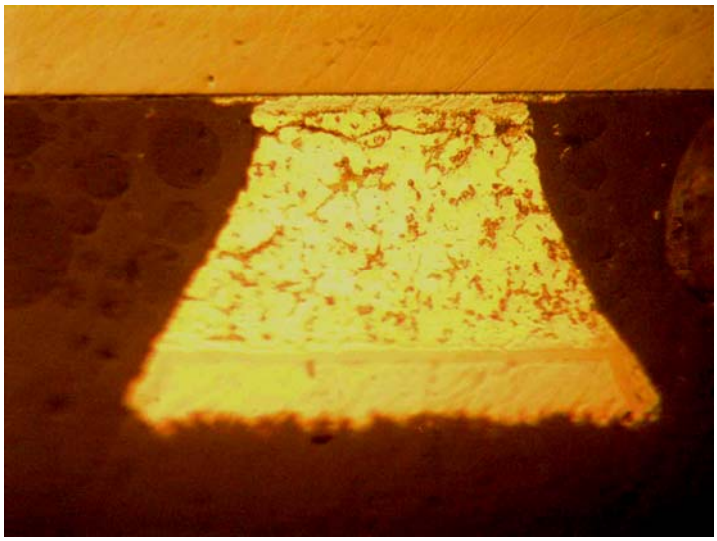


Figure 3.12 A solder crack, which occurred near the UBM

3.11 Summary

The wafer-applied bulk coated die with dispensed fluxing underfill assembly process was successful demonstrated. Fluxing underfill dispensing volume was optimized. Reflow profile and placement parameters were also discussed. Assemblies consistently resulted in a nearly void free underfill with good electrical performance. The reliability of assemblies in liquid-to-liquid thermal shock tests showed that the parts passed 600 cycles with no failures. A cross sectional analysis of the failed parts indicated that failures were located at the interface between the solder ball and UBM, and the failure mode was solder fatigue cracking.

CHAPTER 4

LID ATTACHMENT

4.1 Introduction

Increased microprocessor speeds, power dissipation and device size reduction require integrated thermal management solutions for current and future generations of microprocessors especially those using flip chip packaging. These solutions are usually provided in the form of a lid that is integrated into the package [69]. In these devices, the lid is attached on the back of the die using a thermally conductive adhesive or solder. Solder is widely used in high thermal conductive connections.

Tin-lead solder can be used in lid attach systems. However, environmental and health concerns are driving a shift to the use of lead-free solder. Lead-free solders usually have a high melting temperature and need flux to achieve good wetting. Unfortunately, the flux may induce solder voids and its residue needs to be removed by cleaning, so it would be preferable to use a fluxless soldering process for lid attachment.

In this experiment, indium was selected as the fluxless solder. It has a low melting point, extreme softness, high ductility, and excellent wetting characteristics. Pure indium has a melting point of 156.6 °C, and a Young's modulus of 11 GPa [70]. In comparison, the Young's modulus of the SnPb eutectic is 33 GPa, and SnAgCu eutectic is 46 GPa [63]. Due to its good ductile properties, indium can absorb a severe CTE mismatch between the lid and the die by stress absorption in the bonding layer via plastic

deformation. This chapter presents an overall lid assembly methodology, along with a report on the reliability testing of assembled parts.

4.2 Test Vehicle

The test dies were cut from a silicon test wafer that was deposited with thin film metalization layers using an E-beam evaporation system. The metalization layer stack, from the Si outward, was Ti (500 Å), Ni (2700 Å) and Au (1500 Å). The dies were 22 mm × 22 mm × 0.6 mm thick.

The Cu lids were electroplated with a few micrometers of nickel. After the surface was cleaned with acetone, a gold layer (2000 Å) was deposited on the surface of the lids using an E-beam in the laboratory at Auburn University. The size of the Cu lids was 22 mm × 22 mm in × 1.0 mm thick.

Indium preforms (99.9% wt% indium) were purchased from Williams Advanced Materials. The size of the preforms was 22 mm × 22 mm and either 2 mils, 4 mils or 6 mils thick.

4.3 Overview of the Assembly Process

The assembly process began by cleaning the lids and dies. The lids and dies were cleaned in an Ar plasma at 0.3 kW and 0.6 torr for 5 minutes. An indium preform was manually placed over the backside of the die, and then the lid was placed on top of the preform. After the lid placement, the assembly was passed through the Heller 1800 reflow oven or placed into the SST vacuum furnace. As an alternative, an HP thermocompression bonder was also used to place the lid and then heat the assembly.

During the soldering process, a weight was added on the top of the lid. After soldering, the assemblies were inspected by X-ray or C-SAM to analyze for voids in the assemblies. Figure 4.1 illustrates the schematic of the assembly process.

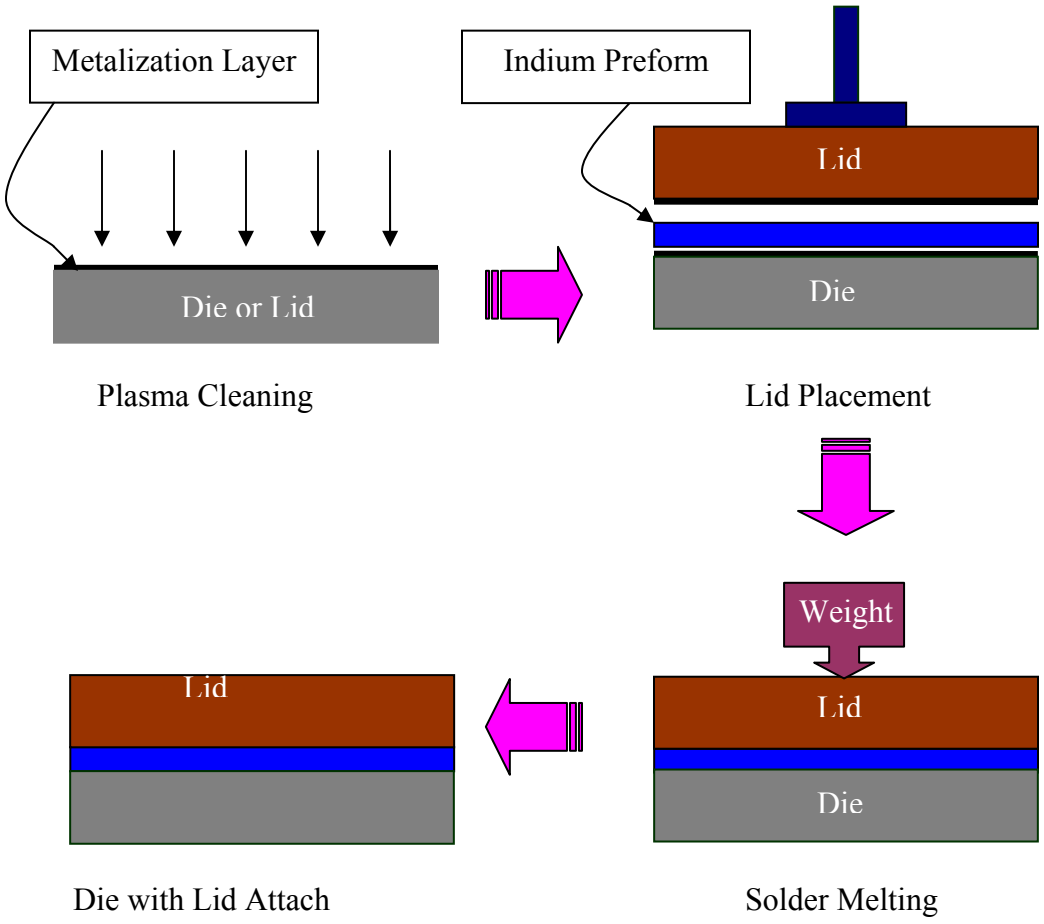


Figure 4.1 Schematic of lid attach process

4.4 Lid Shear Testing

To test the bonding strength, assemblies were cut into small pieces (5 mm × 5 mm) and sheared using a Dage shear machine, as illustrated in Figure 4.2. A desired shear failure mode is when the fracture is through the solder layer leaving the solder on both the lid surface and the die backside. This is termed cohesive failure. An undesired die shear failure mode is when the fracture occurs at either the lid/solder interface or the solder/die interface. This is referred to as adhesive failure. Two failure modes were shown in Figure 4.3.

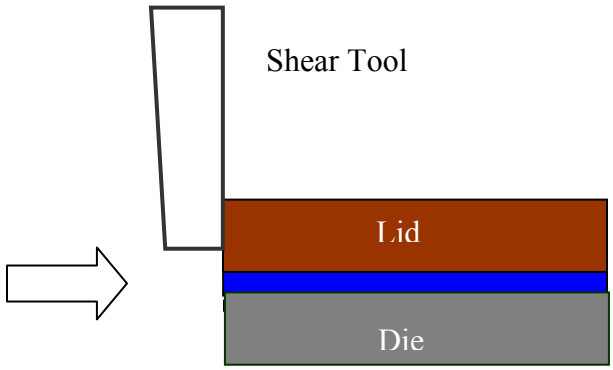
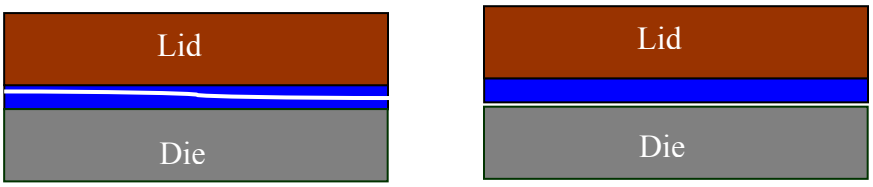


Figure 4.2 Shear test



(a) Cohesive failure (b) Adhesive failure

Figure 4.3 Shear test failure mode

4.5 Assembly Equipment Selection

In the first stage, two silicon dies were attached together. This sandwich structure (Si-In-Si) was used to fine tune and verify the integrity of the assembly process before assembling any real lids (Cu) to the silicon dies.

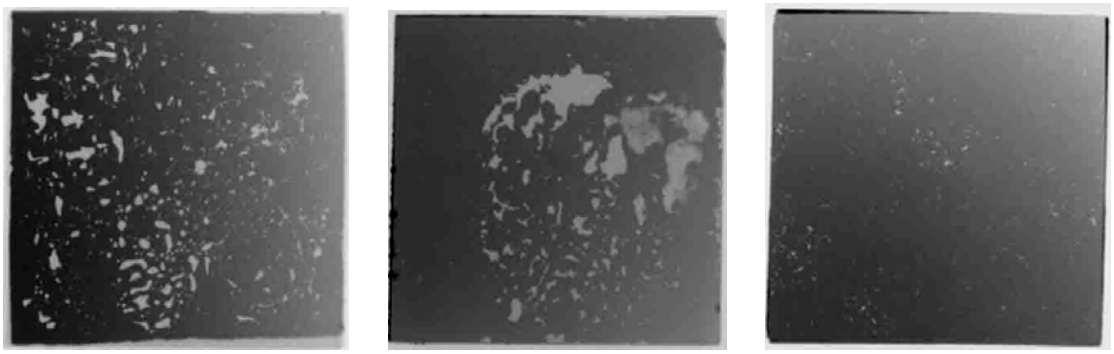
The initial attach experiments were performed in a Heller 1800 reflow oven. This assembly method is preferred by industry due to its high volume capability and low cost. The unbonded die-indium-die structure was manually placed in a fixture specifically designed to center and hold it in place during the reflow process, and a weight was placed on top of the die. The assembly was then passed through the reflow oven under a nitrogen atmosphere. The reflow profile was set at 180 ºC for 200 seconds. Various weights were tried. Many voids in the solder bond were observed when examined by X-ray imaging, as shown in Figure 4.4 (a).

The second trial was conducted using an HP thermocompression bonder with various bonding temperatures and forces. The bonding temperatures were 165, 180 and

200 ºC, and the bonding forces were 50g, 100g, 200g and 400g. The X-ray image in Figure 4.4 (b) is typical of the results obtained, revealing that once again all the parts had solder voids.

The assemblies described above were both conducted at atmospheric pressure, and many voids appeared in the solder bond. Obviously, this is not desirable from the viewpoint of reliability and thermal conductivity.

In an attempt to reduce the voids, an SST 3150 high vacuum furnace, was used to assemble parts at a low pressure (~ 10^{-5} torr). Parts with various assembly conditions were built, and the X-ray images showed the parts had a much lower voiding level, as shown in Figure 4.4(c). Clearly, this low pressure environment benefited the quality of the assembled parts, producing far fewer voids.

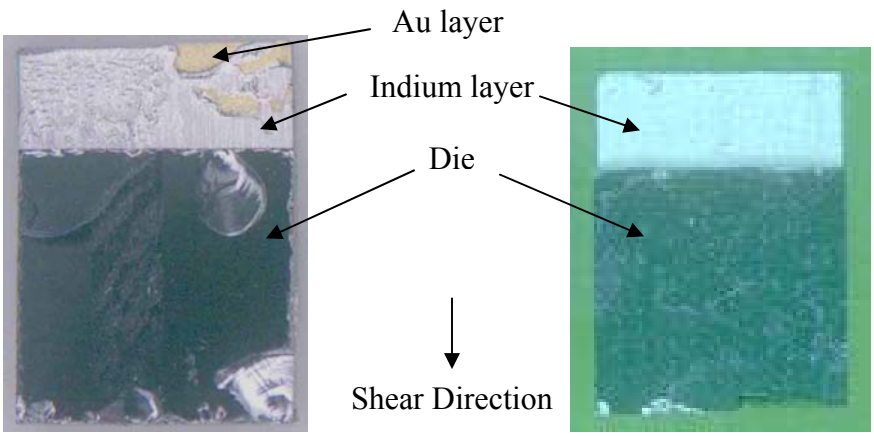


(a) Reflow oven (b) Thermocompression bonder (c) High vacuum furnace

Figure 4.4 Examples of bonding voids visible in X-ray images

The sample shown in Figure 4.5 (a) was assembled in the reflow oven. The failure mode is partial adhesive failure. The sample in Figure 4.5 (b) shows a cohesive failure mode. Both samples were only partial sheared, and the die was still on the substrate. The

sample with the cohesive failure was assembled in the SST vacuum furnace. Based on the results of this experiment, the SST high vacuum furnace was selected as the primary assembly tool.



(a) Partial adhesive failure
(Partial fracture at In/Au interface)

(b) Cohesive failure
(Fracture at In layer)

Figure 4.5 Fracture surface after shear test

4.6 SST Thermal Profile Optimization

The SST profile optimization was realized using Taguchi's parameter design. Here, the primary goal was to find factor levels that minimized variation while adjusting the process on target. Once the most effective factor levels have been determined, the optimal factor level is selected and applied to the process to achieve the best results.

Parts with Si-In-Si structure were assembled in the SST high vacuum furnace. Prior to assembly, all of the dies were Ar plasma cleaned at 0.3 kV, 0.6 torr for 5 minutes. The thickness of the indium preform was 4 mils. A 20g force was applied on top of the stack. The preheat ramp time was set for 2 minutes (from room temperature to soak

temperature). In this experiment, four controllable factors, ramp time, soak time, peak temperature and dwell time, were studied using Taguchi's design of $L_9(3^4)$. These factors are illustrated in Figure 4.6.

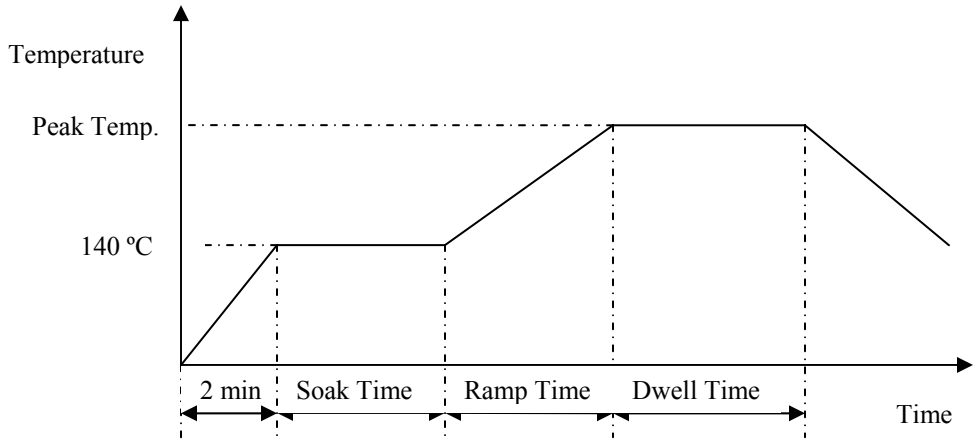


Figure 4.6 Heating profile

All factors had three levels, as shown in Table 4.1. The response variable was bond voids. The design layout and experimental results are shown in Table 4.2.

Table 4.1 Controllable factors

Controllable Factor	Level 1	Level 2	Level 3
A: Ramp Time	1 min	2 min	3 min
B: Soak Time	1 min	2 min	3 min
C: Peak Temperature	180 °C	200 °C	220 °C
D: Dwell Time	1 min	3 min	5 min

Table 4.2 The design layout and experimental results

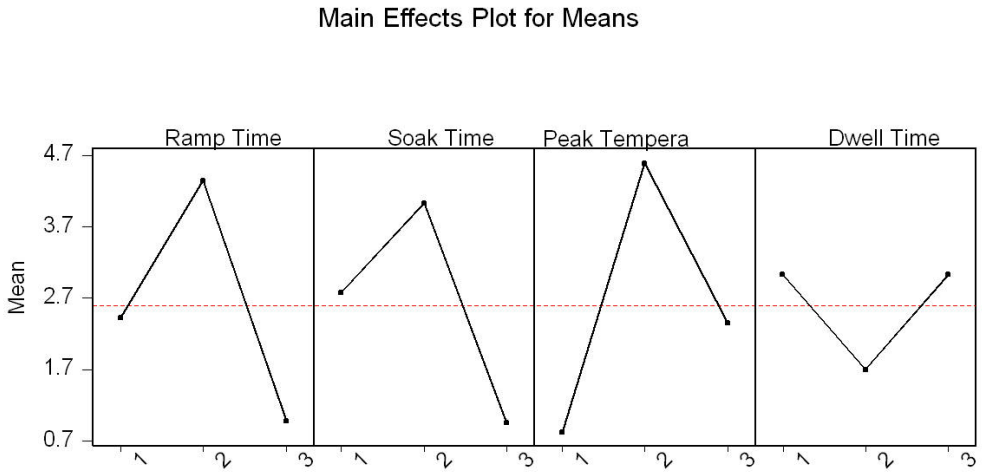
Exp. No.	Ramp Time (minutes)	Soak time (minutes)	Peak Temp. (°C)	Dwell Time (minutes)	Void (%)	
					Sample 1	Sample 2
1	1	1	180	1	1.0	1.6
2	1	2	200	3	4.0	6.0
3	1	3	220	5	1.1	0.9
4	2	1	200	5	8.0	6.0
5	2	2	220	1	5.5	6.5
6	2	3	180	3	0.10	0.01
7	3	1	220	3	0.11	0.09
8	3	2	180	5	1.0	1.2
9	3	3	200	1	1.9	1.7

To examine the voids in the solder bond, X-ray images were analyzed using the WB Analysis software developed by Robert Dean, and the void percentage was calculated. Lower bonding void levels are desired, so, the design type is smaller-the-better (STB).

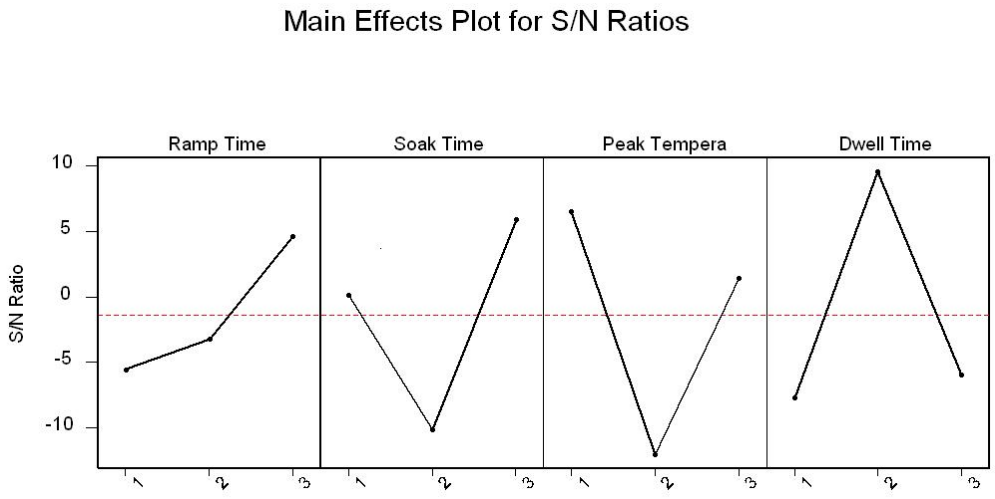
Minitab statistical analysis software was employed to analyze the data from Table 4.2. The response table for mean is given in Table 4.3. Ranks in this table are assigned based on Delta values which are the highest value minus the lowest value for each factor. Figure 4.7 shows the mean bonding voids and S/N ratio.

Table 4.3 Response table for mean

Level	Ramp Time	Soak Time	Peak Temp.	Dwell Time
1	2.43333	2.80000	0.81833	3.03333
2	4.35167	4.03333	4.60000	1.71833
3	1.00000	0.95167	2.36667	3.03333
Delta	3.35167	3.08167	3.78167	1.31500
Rank	2	3	1	4



(a) Mean effects plot for means



(b) Mean effects plot for S/N ratio

Figure 4.7 The prediction profile for mean underfill voids and S/N ratio

Based on these results, the peak temperature was the most important factor and had a maximum influence on the void formation followed by the ramp time, soak time and dwell time. The main effects and S/N ratios plots also show non-linearity, which indicate that two-factor interactions were present. Figure 4.8 shows the interaction effect of the four factors. Four response curves in plots (row 2, column 3), (row 1, column 4), (row 2, column 4) and (row 3, column 4) crossed each other, indicating the strong interaction between peak temperature and soak time, and dwell time and the other three factors. There existed a weak interaction between ramp time and soak time, and ramp time and peak temperature since the curves in plots (row 1, column 2) and (row 1, column 3) slightly crossed.

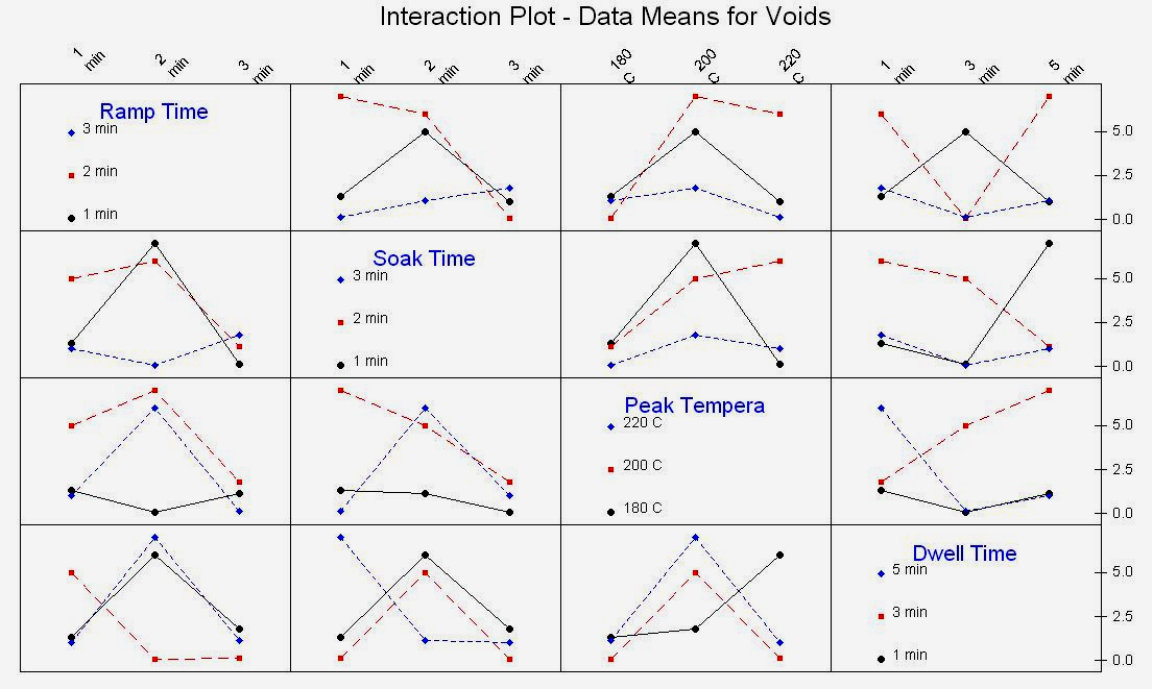


Figure 4.8 2-factor interaction plots

The means and S/N ratios plots suggest the factor level that will minimize void formation is $A_3B_3C_1D_2$. In other words, the optimal combination is ramp time at level 3 (3 minutes), soak time at level 3 (3 minutes), peak temperature at level 1 (180 °C), and dwell time at level 2 (3 minutes). The optimum profile is described as follows:

- Preheat time (to 140 °C): 2 minutes
- Soak time (140 °C): 3 minutes
- Ramp time (140~180 °C): 3 minutes
- Peak temperature: 180 °C
- Dwell time (180 °C): 3 minutes

Once these optimal process factors had been determined, confirmatory runs were carried out to verify the results of the statistical analysis. Figure 4.9 shows that an assembly with only tiny voids was achieved using these optimized parameters.

Figure 4.9 Assembly with optimized placement parameters, X-ray image showing only tiny voids

4.7 Copper Lid Assembly

Parts with copper lids on Si dies were built in this experiment. However, poor wetting was observed. This is thought to be because the temperature difference between the heating station and the bond interface became significant when copper lids were used instead of the Si used in the process optimization. Since copper has a high thermal mass, it may cause the indium preform temperature to increase slowly, and preventing it from reaching its melting temperature during the dwell period.

Based on the profile described in the previous section, three profiles were modified and evaluated. Their ramp time (3 minutes), soak time (3 minutes) and dwell time (3 minutes) were kept the same as the optimum profile in previous section. The

variations were the soak and peak temperatures. To examine the assembly for voiding and wetting, both C-SAM images and cross-sections were examined. Since the tiny voids might be on the rough surface of the Cu lid, C-SAM provided a better method for identifying voids. The results in Table 4.3 show that good wetting was achieved when the profile C was used. An example of assemblies with good wetting and void free is shown in Figure 4.10.

Table 4.4 Reflow profile measurement

	Description of Set Point Temperature	Wetting Status
Profile A	Soak Temp. 140 °C, Peak Temp. 180 °C	No wetting
Profile B	Soak Temp. 150 °C, Peak Temp. 200 °C	Partial wetting
Profile C	Soak Temp. 150 °C, Peak Temp. 230 °C	Wetting

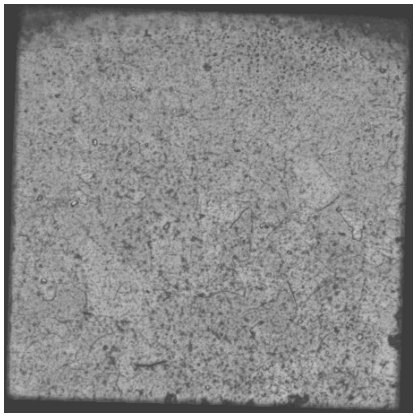


Figure 4.10 An example of C-SAM image showing good wetting and void free

4.8 Reliability Test: Multiple Reflows

Many packages such as BGAs need to pass through multiple reflows during assembly onto printed circuit boards. At high temperature, the growth of intermetallic compounds (IMC) at the joint interface is of particular concern. Excessively thick IMC layers may significantly degrade the physical and mechanical properties of the bonding joints. Therefore, it is essential to study the solder bond after multiple reflow operations.

Parts with a Si-In-Si sandwich structure were built for this test. All assemblies exhibited good wetting and minimal voids. This test focused on changes in the bond adhesion after multiple reflows.

4.8.1 Test Profile

The lead-free reflow profile shown in Figure 4.11 was used as the test profile. The parameters of the profile were as follows:

- Peak temperature: 245 °C
- Time above 225 °C: 63s
- Time between 150 to 170 °C: 72s

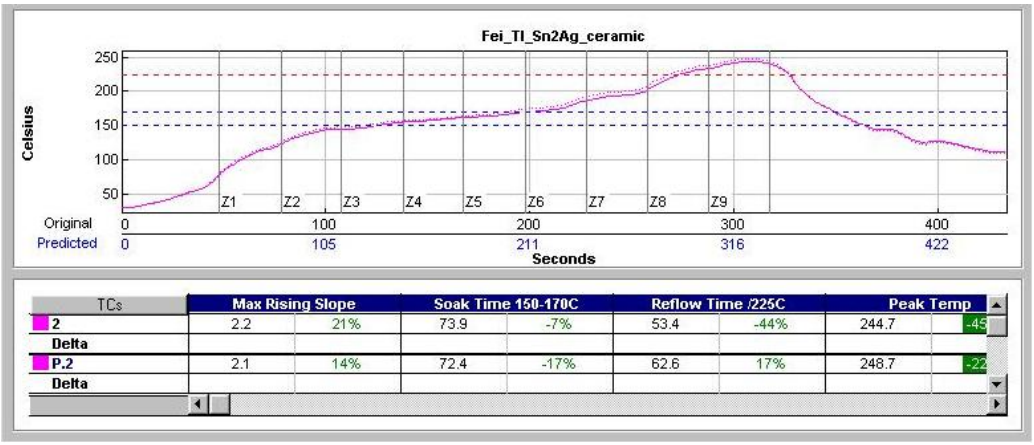


Figure 4.11 Reflow profile for multiple reflow test

4.8.2 Shear Test Results

Parts passed through the reflow oven 1, 3 or 5 times, and were then cut into small pieces (5 mm × 5 mm) for testing. These samples were sheared using the Dage die shear machine. The shear strength results are plotted in Figure 4.12. No significantly change in the shear strength was observed after 5 reflows, and all shear failure modes were cohesive. Therefore, the solder bond was deemed to have good reliability even after multiple reflow operation.

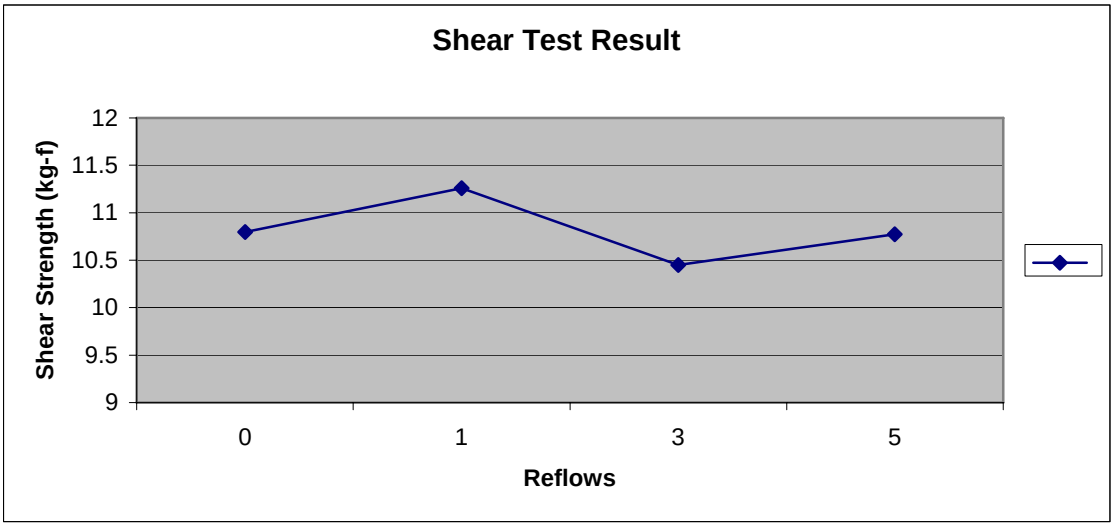


Figure 4.12 Shear test results for multiple reflows

4.8.3 IMC Analysis

Some samples were mounted in epoxy, cross-sectioned, ground, and polished. The die-solder interface was then analyzed using a SEM. The formation of IMC in the interface between the indium solder and the silicon die backside metallization was observed as shown in Figure 4.13. The thickness of IMC increased with increasing number of reflows. The dark area under the IMCs was SiO_2 layer. It was also found that, during polishing, some silicon was separated from the die and became embedded in the indium matrix due to the soft nature of indium solder. These particles were confirmed as silicon by Energy Dispersive Spectroscopy (EDS).

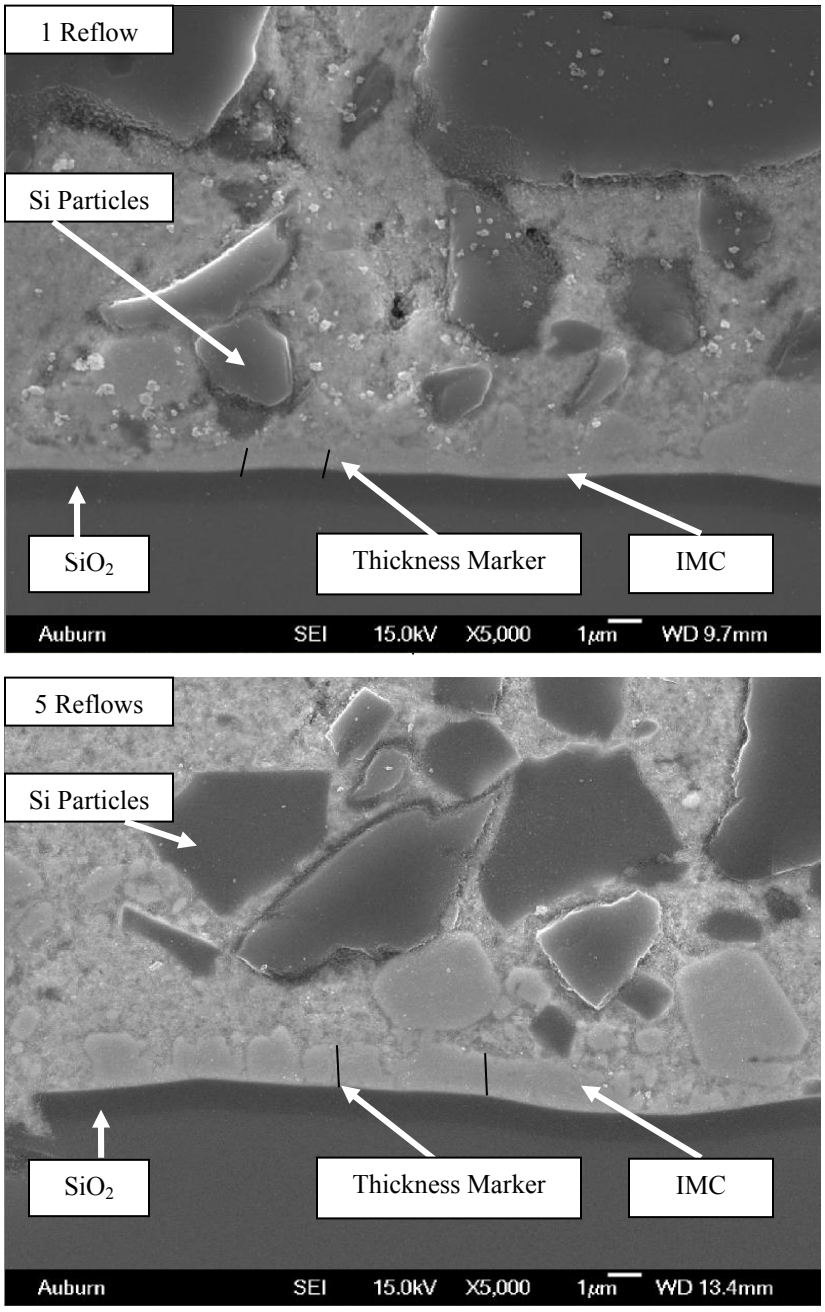


Figure 4.13 SEM images showing the IMC growing after reflow

From the In-Au phase diagram [71], there are a total of fourteen equilibrium phase, two of them are identified as intermetallic compounds InAu (36.79 wt. % of indium) and In_2Au (53.8 wt. % of indium). Chu et al [72] found that the In_2Au formed when indium bumps bonded on a thin film (Au/Ni/Ti) on a fused silica in the bonding temperature range between 100 °C and 250 °C. So et al also reported that the thin gold film can quickly diffuse into the bulk indium and forms In_2Au [73]. According to the In-Ni phase diagram [74], several intermetallic phases such as $InNi_3$, $InNi_2$, In_9Ni_{13}, InNi, In_3Ni_2, and $In_{72}Ni_{28}$ could be formed. Kim and Jung reported that only one IMC, $In_{27}Ni_{10}$, was found at the In/Ni interface when a piece of 100In solder melted on the electroplated Ni (4 to 5 μm) on the Cu substrate. Based on above analysis, the IMCs in this sample could be In_2Au and combined with some In-Ni IMC such as $In_{27}Ni_{10}$.

4.9 Reliability Test: High Temperature Storage

High temperature storage testing was performed to assess the impact of time and temperature on package reliability. Parts with a Si-In-Si sandwich structure were built for this test, and stored in a furnace at either 80, 100 or 125 °C. Test points were set at 0, 48, 100, 250, 500, 1000, 1500 and 2000 hours.

4.9.1 Shear Test Results

At each sampling time, one part was removed from the furnace and cut into 10 pieces, each 5 mm square. These samples were sheared, and the results are shown in Figure 4.14. No significant change in the shear strength was observed as aging time

increased. The standard deviation was less than 1 kg-f. This indicates that high temperature storage had no significant impact on bond strength.

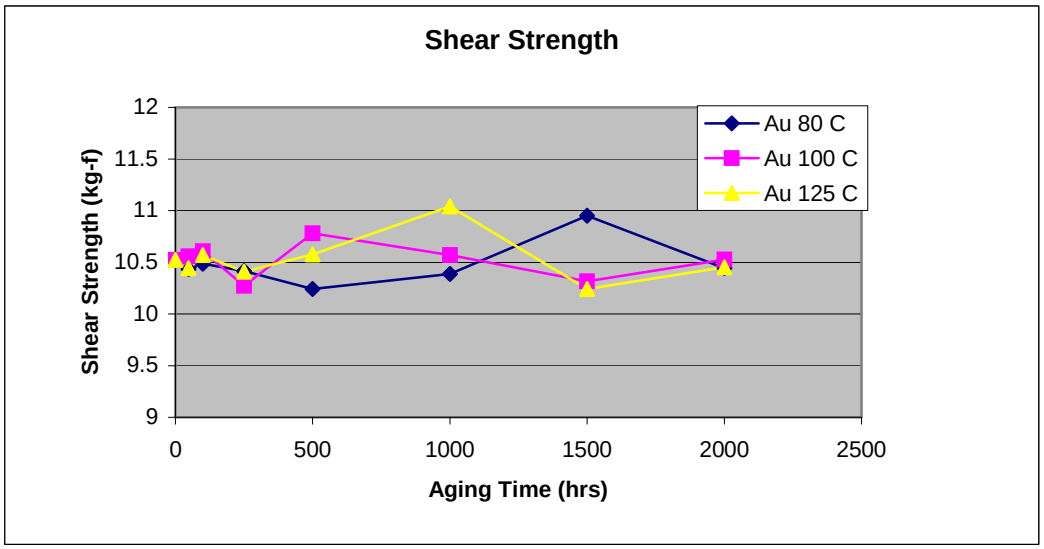


Figure 4.14 Shear test results

4.9.2 Growth Kinetics of the IMC

At each sampling time, samples were also cross-sectioned and analyzed using a SEM. The growth kinetics of the IMC layer formed between the 100In and the Au/Ni/Ti/Si substrate were examined. A quantitative analysis of the IMC layer thickness as a function of aging time and temperature was conducted.

Generally, the solid-state growth of the IMC can follow linear or parabolic growth kinetics. The linear growth is the growth rate limited by the reaction rate at the growth site. In contrast, the parabolic growth is the growth limited by volume diffusion [75]. Therefore, the growth rate of an IMC during an interdiffusion of metals will follow a parabolic law as follows [75, 76]:

$$X = kt^n \qquad (4.1)$$

Where X is the thickness of the IMC at aging time t, and k is the growth rate constant dependent on the interdiffusion coefficients, n is the time exponent.

The n takes the value of 0.5 when the interdiffusion is controlled by volume diffusion. The growth of IMC thickness is proportional to the square root of aging time. The equation is as:

$$X = kt^{1/2} \qquad (4.2)$$

Figure 4.15 shows that the growth of IMCs followed the equation 4.2, implying that the growth of the intermetallic layer was diffusion controlled. The value of the growth constant k, at a particular temperature, can be calculated by the slope of the linear fitting lines of X versus $kt^{1/2}$.

As shown in Figure 4.15, the IMC thickness growth had a linear relationship with $t^{1/2}$. Table I lists the growth rate constants of IMC at different aging temperatures. Most of the linear correlation coefficient values (R^2) for these plots were greater than 0.96. This confirms that the growth of the IMC layers is diffusion controlled over the temperature range studied. Therefore, the IMC growth will keep continue as long as the diffusion process existence and reactants are available. The IMC phase may change over time. It has been observed by Chu et al [72] that the IMCs thickness could be much thicker than the original thin films layers on the device. They found that the IMCs could be formed up to 3 μm during indium solder bonded on a thin film Au(0.3 μm)/Ni(0.15 μm)/Ti(0.1 μm) on a silica at 250 °C.

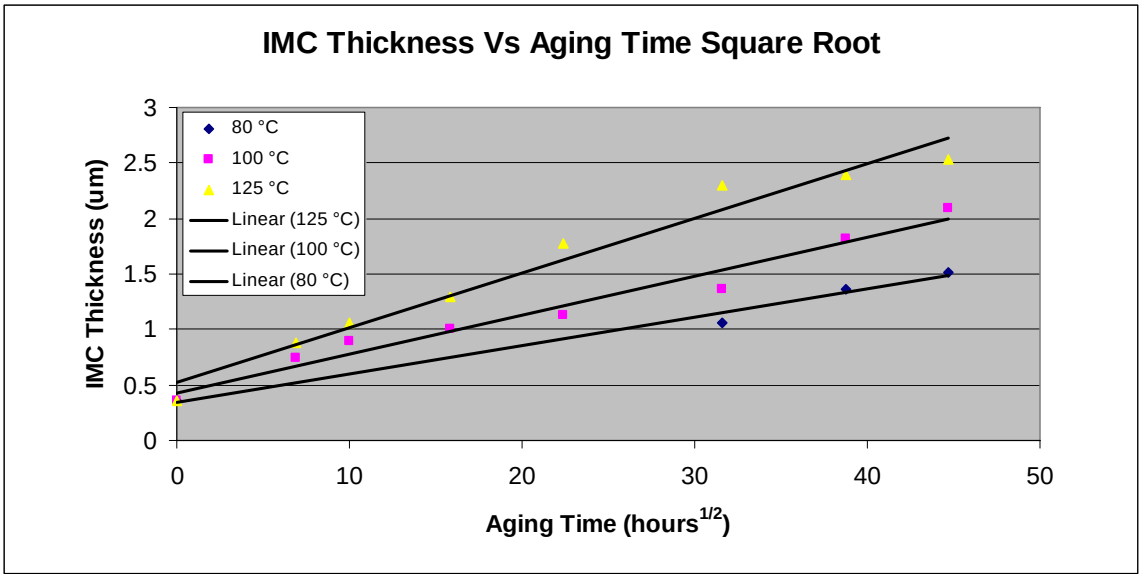


Figure 4.15 The IMC layer thickness increase during high temperature storage

Table 4.5 Growth constants and linear correlation coefficients

Aging Temperature	k (μm/hour$^{1/2}$)	R^2
80 °C	0.0255	0.9869
100 °C	0.0350	0.9694
125 °C	0.0493	0.9691

A simple Arrhenius equation was used to determine the activation energy of IMCs growth [88]:

$$K^2 = k_0^2 A \exp(-Q/RT) \qquad (4.3)$$

Where A is a prefactor, T is the absolute temperature, R is the gas constant (8.314J/mol-K), and Q is the activation energy. An Arrhenius plot, as shown in Figure

4.16, was obtained for the growth of the IMC. The value of Q was calculated from the slope of this plot using a linear regression analysis. The activation energy of the IMC was estimated to be 34.4 kJ/mol.

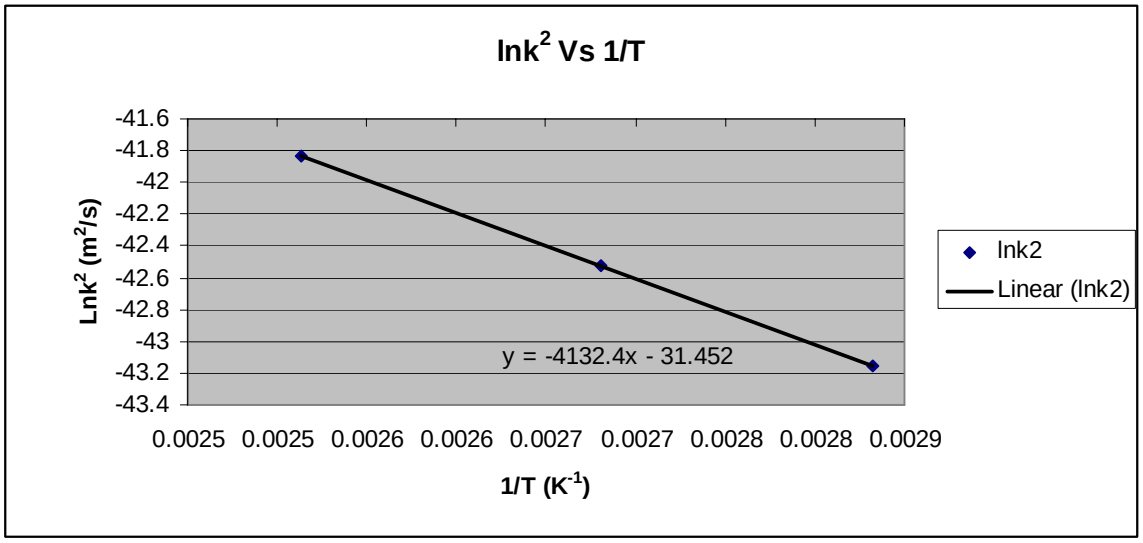


Figure 4.16 Arrhenius plot for the IMC growth

4.10 Reliability Test: Thermal Shock

Assemblies with a Cu-In-Si structure were subjected to an air-to-air thermal shock test (AATS). Three preform thicknesses as 2mils, 4 mils and 6 mils were used. A sample size of 10 was tested for each preform thickness. Some assemblies had small voids due to the Cu lid surface defects such as scratches. The cycle was from -55 °C to +80 °C, with 10 minutes at each temperature extreme and a 1-minute transition time. Parts were removed from the chamber and checked under C-SAM every 250 cycles. The test was terminated at 2000 cycles.

4.10.1 Shear Test Results

Assemblies were cut into small pieces (5 mm × 5 mm) for shear testing after 2000 cycles. For comparison purposes, assemblies without AATS were also tested. Figure 4.17 shows the shear strength results. No significantly change in the shear strength was observed after 2000 cycles, and all shear failure modes were cohesive. This indicated that the assemblies had good reliability in AATS testing.

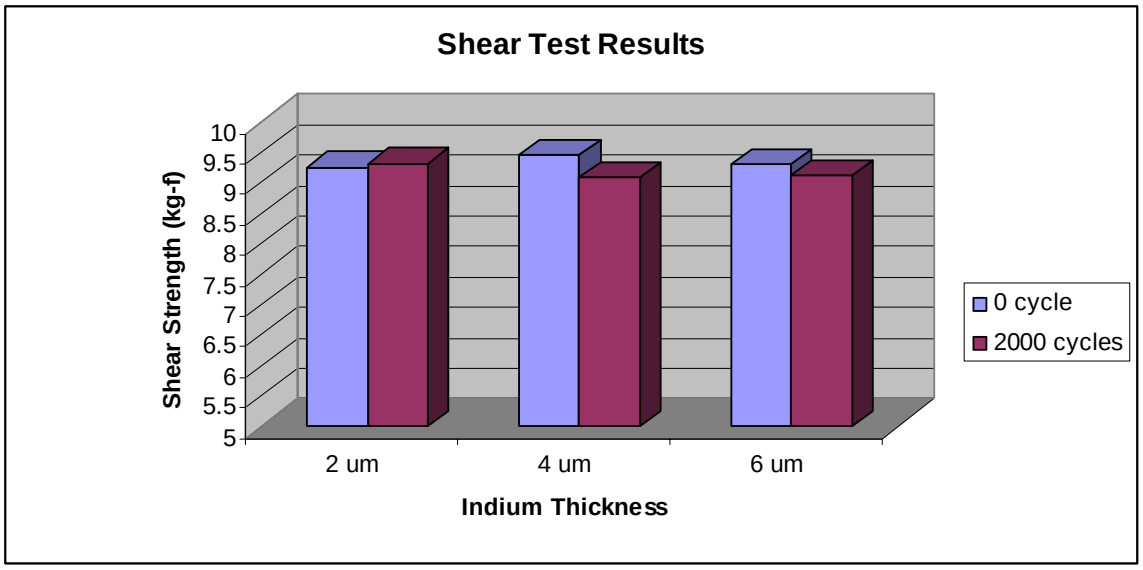
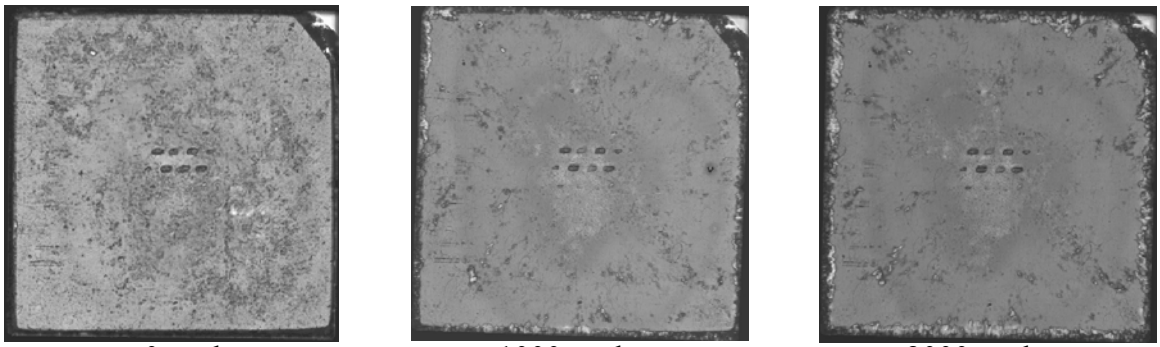


Figure 4.17 Shear test results for AATS

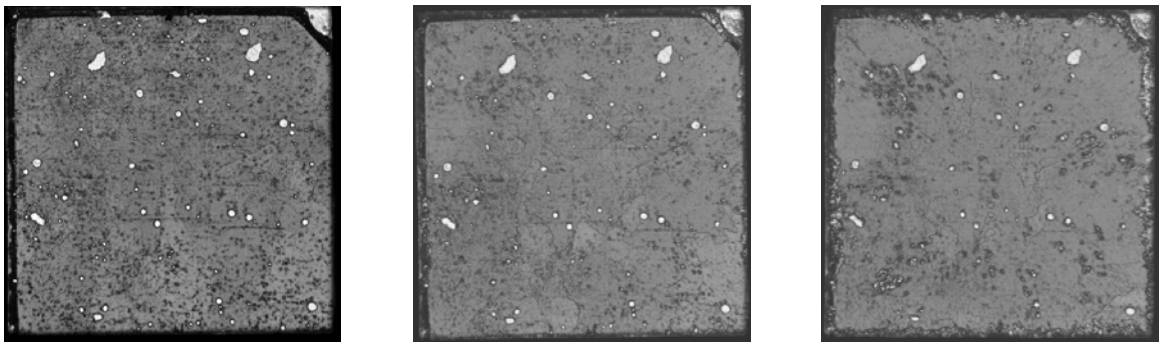
4.10.2 Test Analysis

Figure 4.18 shows the examples of C-SAM pictures. A few white areas were observed along the edge of assemblies at 1000 cycles, and slightly increased as the number of cycles increased. The overall white areas were still minimal after 2000 cycles.



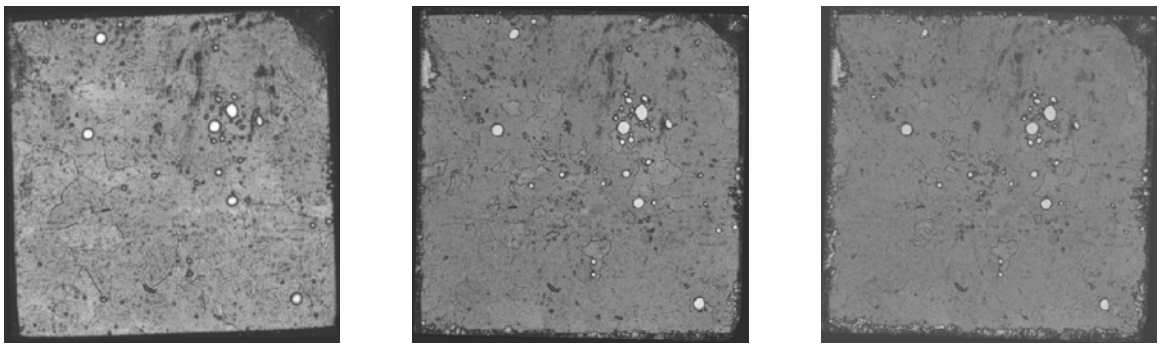
0 cycle 1000 cycles 2000 cycles

(a) Assemblies with 2 mils indium



0 cycle 1000 cycles 2000 cycles

(b) Assemblies with 4 mils indium



0 cycle 1000 cycles 2000 cycles

(c) Assemblies with 6 mils indium

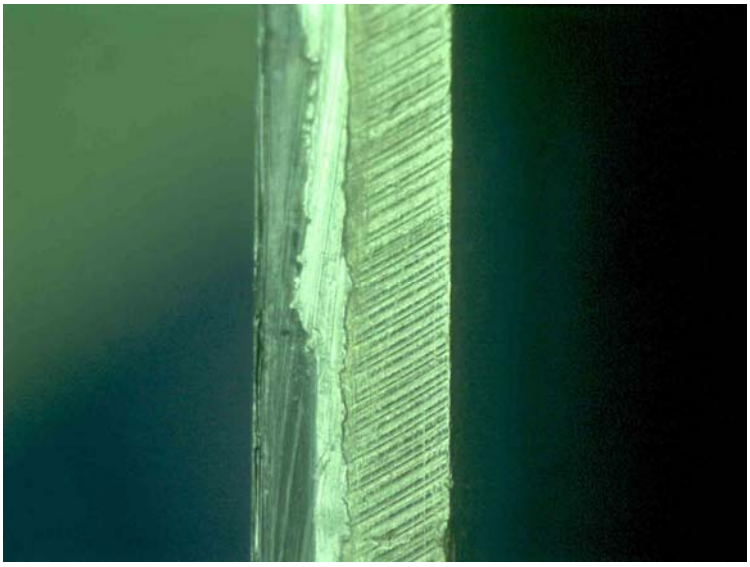
Figure 4.18 C-SAM images during AATC

It is well known that the high standoff of solder joints in a package can increase thermal fatigue life [77, 78]. In this case, the assemblies with thicker indium solder

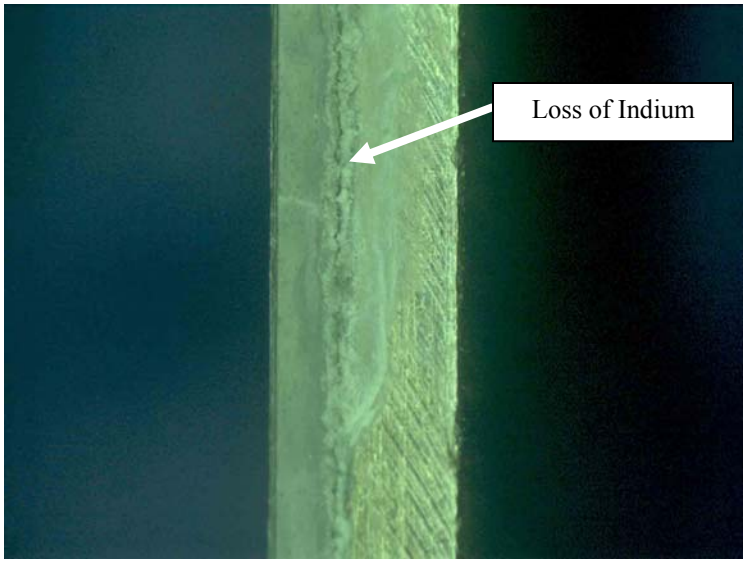
should have better reliability. In another words, the level of failure such as cracking or delamination should decrease as the indium thickness increased. However, no significant difference in white area was observed as the indium thickness increased during AATS. Therefore, it is unlikely that these white areas were indium delamination.

Further study indicated these white areas were potentially caused by loss of indium at the perimeter of the Si die. Side view image (Figure 4.19 (b)) shows loss of indium at the part edge after 2000 cycles. Figure 4.19 (a) is an example of part without the AATS. The proposed phenomenon is similar to the pump-out effect in packages using the thermal grease as the thermal interface material (TIM) between the die and the heatsink [79, 80]. It is observed that all of the typical greases are subject to pump-out under cyclical stresses encountered during temperature cycling [81]. Since there is a thermal stress exerted at the grease or indium solder due to the CTE mismatch between the heatsink or Cu lid and the Si die (or Si die and In layers), the thermal cycle test can be considered as a dynamic mechanical test. Mahajan et al [82] studied the pump-out effect by simulating the squeezing action on the grease caused by die warpage change during the thermal cycle. They proposed a design rule for the formulation of TIMs to reduce the pump-out by keeping the ratio of G'' and G' less than or equal to 1. The G" and G' are the loss modulus and storage modulus which are indicators for viscous and elastic properties, respectively. A low value of G''/G' indicates a more solid-like material [83]. On the other hand, TIMs with more liquid-like or lower viscosities are typical less resistant to pump-out effects [84]. The value of G"/G' of pure indium is 1.00045 [85]. Based on the above analysis, the pump-out phenomenon is related to the flow ability of TIMs. Therefore, it is reasonable to postulate that the indium solder tended to flow and

to be pumped out during the thermal cycle test. Ductile indium exhibited good resistant to delamination but suffered slightly due to the pump-out problem during AATS.



(a) Part without AATC



(b) Parts after 2000 cycles

Figure 4.19 Side views of parts showing indium loss after 2000 cycles

4.11 Summary

Indium solder offers excellent performance for lid attachment applications. Successful assembly requires a high vacuum environment and the development of an optimized profile in order to minimize solder voids and enhance solder wetting. Reliability testing showed indium solder retained good adhesion to the lid and die even after multiple reflows operation and high temperature storage. The growth kinetics of IMC for the interface between indium and Au/Ni/Ti coated die was also examined. In thermal cycle testing, indium was potentially found to be pumped-out slightly along the perimeter of the parts. This phenomenon requires further study to verify and to establish the reliability implications.

CHAPTER 5

CONCLUSIONS

5.1 Large Size, Fine Pitch Lead-Free Flip Chip Assembly

Large size, fine pitch lead-free flip chips are highly desirable for many industrial applications. However, the application presents some issues in the assembly process. In this research, assembly processes for a 20.5 millimeters square die with pitches down to 6 mils have been successfully developed. The research focused on solder wetting enhancement and underfill voiding elimination.

In this study, two fluxes were evaluated, and flux TF 38 was found to offer good flux activity for solder wetting. A reflow profile for 97.5Sn2.5Ag solder was established and resulted in good solder wetting. A fishbone diagram was used to illustrate the void formation factors. The critical factors, including dispensing process, flux residue and die condition, were discussed and optimized. Optimum dispensing parameters were found to be edge dot dispense pattern and 50 mg dispensing volume. Assemblies cleaned after reflow were studied, and no significant improvement on the underfill voiding was observed when using this process because of suspected insufficient cleaning under the large die. Die cleaning prior to assembly was found to result in void free assemblies because the cleaning process decreased the die-to-underfill wetting angle and benefited the underfill flow.

After process optimization, excellent solder wetting and void free underfill assembly were ultimately achieved. In the air-to-air thermal cycling test, the characteristic life of the assembly was 2610 cycles.

The significance of this experiment was a large size, fine pitch lead-free flip chip assembly process was demonstrated and verified as a feasible way to build high yield and reliability flip chip packages. The contribution of the research described in this study is to suggest a die cleaning process prior to assembly for the large size, fine pitch lead-free flip chip packaging. This cleaning process could help improve existing flip chip assembles and aid development of future flip chip packages.

5.2 Wafer-Applied Bulk Coated Flip Chip Assembly

The work demonstrated the optimized assembly process for wafer-applied bulk coated flip chip. Some key factors were discussed, and guideline for high yield and reliability assembly were provided. Dispensing volume was optimized, and the volume between 2.6 mg and 4.5mg was found to be necessary for good solder wetting. The reflow profile proved to be a significant factor affecting the assembly yield. Two reflow profiles were examined. Profile B with low soak temperature resulted in nearly void free underfill with good electrical performance. The placement parameters were also discussed, and the placement acceleration (speed) of 0.1g and force of 9N was used.

Assemblies with nearly void free underfill and good electrical performance were subjected to liquid-to-liquid thermal shock reliability tests. A characteristic life of 1122 cycles was achieved. The results show the promising future of the wafer-applied bulk coated flip chip process.

This dissertation presented, for the first time, the process of wafer-applied bulk coated flip chip assembly integrated with fluxing underfill. This flip chip assembly technology combined the advantages of both wafer-applied underfill and fluxing underfill. The specific contributions of this study are given as followings.

(1) Some assembly process parameters were discussed and optimized for high yield and reliability flip chip assembly.

(2) The results of this investigation are also important for proving the concept of integrating the wafer-applied underfill and fluxing underfill in the flip chip assembly.

5.3 Lid Attachment

Lid attachment technology has been driven by the need for superior heat dissipation in electronics packaging. A lid attachment methodology using pure indium has been developed in this study.

Three attachment techniques were evaluated in an attempt to reduce the solder voids. The SST high vacuum furnace was found to yield the best results. This study demonstrates the use of the DOE methods to effectively and efficiently determine what the most important factors and optimize the SST thermal profile. The optimum combination was found to be a ramp time of 3 minutes, a soak time of 3 minutes, a peak temperature of 180 °C, and a dwell time of 3 minutes. This thermal profile was modified when the Cu lids were used. With optimization of the attachment tools and profiles, good solder wetting and minimal voiding level were achieved.

Multiple reflows, high temperature storage and AATS tests were conducted on assemblies. All of the assemblies showed good solder bond stability after these tests. Additionally, the growth rate of these IMCs was found to increase with the aging temperature and time. A linear relationship was found between the growth of the IMC thickness and the square root of the aging time. The activation energy for IMC growth was found to be 34.4 kJ/mol. The activation energy corresponds to temperature sensitivity of IMC growth. The IMC growth is less depend on temperature when the activation energy is low. In thermal cycle testing, indium was found to be slightly pumped-out from interface layer. The significant of this experiment is that all of the assemblies had high reliability, passing 5 reflows and survived up to 2000 hours at 125 °C. The proposed indium pump-out phenomenon has not previously been reported in the packaging industry.

The assembly process for the lid attachment with pure indium has been developed. The successful implementation of this fluxless assembly process will promote more applications of pure indium.

5.4 Recommendation for Future Work

Chemical analysis of the die surface before and after cleaning should be conducted to study the change in wetting angle of the underfill on large size, fine pitch lead-free die. In the wafer-applied bulk coated flip chip assembly, development of more suitable fluxing underfill materials is needed. Increasing the toughness of the fluxing underfill is required to postpone fillet cracking during the thermal cycling test. The future

work on lid attachment should include studies of the indium pumped-out behavior and how to avoid it.

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