Electronic characterization of technologically relevant interfaces on $\beta-\mathbf{Ga_2O_3}$ and $4\mathbf{H}-$SiC wide bandgap semiconductors

by

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Abstract

Conventional silicon power device technologies are rapidly approaching their performance limits in power devices. Therefore, exploration of novel materials for next-generation power electronics is necessary. In this regard, wide bandgap (WBG) semiconductors are an ideal solution. The excellent material properties as well as availability of the single crystal material attracts more attention towards 4H-SiC and β-Ga_2O_3. Specially, for power electronics, WBG Schottky diodes and metal oxide field effect transistors (MOSFETs) are attractive for high voltage applications due to lower power/energy loses. In such devices, metal-semiconductor interfaces (Schottky diodes) and dielectric-semiconductor interface (MOSFETs) play a critical role in the physics of device operation.

However, various non-idealities and defects that are present at such interfaces as well as defects present in the bulk of the semiconductors affect power device performance and reliability. Bulk defects in the semiconductor cause recombination current under reverse bias, increase substrate resistivity and affect in degradation of voltage blocking capability of the power device. On the other hand, interface defects such as high density of interface traps (D_{it}) in oxide-semiconductor interface known to be the reason for very low channel mobility in MOSFETs. Furthermore, surface roughness at the interface, surface contamination at the interface and as well as a reaction at the interface can also affect the power device performance. Therefore, electronic characterization of interfaces on 4H-SiC and β-Ga_2O_3 is a fundamental step in the development of power devices based on these materials. Furthermore, power device fabrication requires several processing steps such as metallization, dielectric formation, and reactive ion etching. These unit steps introduce new or altered metal-semiconductor interfaces or oxide-semiconductor interfaces as well as semiconductor surface. Therefore, it is essential to fully understand the nature of the various defects introduced by these unit steps. In this thesis, electronic characterization of metal-semiconductor, dielectric-semiconductor interface as well as

bulk defect investigation has been carried out to identify the defect structures as well as their behavior as follows.

Metal/WBG interface

• β-Ga_2O_3 is fairly new material for power device technology. Therefore, first, metal-semiconductor interfaces fabricated by metallization of Al, Mo, Au and Ni on β-Ga_2O_3 has been investigated. Al-β-Ga_2O_3 interface demonstrate a Ohmic contact behavior. On the other hand, Mo, Au and Ni-β-Ga_2O_3 interfaces demonstrate rectifying behavior. Furthermore, electronic properties of Ni/($\bar{2}$01) β-Ga_2O_3 Schottky barrier diodes in low temperature range has been investigated. Temperature-dependent electrical measurements reveal that, below 273 K, current-voltage characteristics of Ni/β-Ga_2O_3 SBDs demonstrate a strong temperature dependence on the extracted barrier height and ideality factor due to Schottky barrier spatial inhomogeneity. In this study, investigation of bulk traps in β-Ga_2O_3 was carried out by using electronic defect spectroscopy on Ni/β-Ga_2O_3 Schottky barrier diodes. An electronic deep level trap or defect energetically located 0.77 eV below the conduction band of β-Ga_2O_3 and a concentration of 2.6×10^{16} cm^{-3} (10 % doping concentration) was detected.

Dielectric/WBG interface

• 4H-SiC is a more mature material compared to β-Ga_2O_3 and MOSFETs based on this material has been already commercialized. However, the performance of these devices are far from theoretically expected, due to high near-interface state density at the SiO_2/4H-SiC interface. In this regard, electronic properties of SiO_2-4H-SiC interface based on phosphorus (P) incorporated SiO_2 has been investigated. In this study, constant capacitance deep level transient spectroscopy (CCDLTS) measurements determine the main interface defects reduced by P incorporation at the SiO_2-4H-SiC interface. These measurements confirm that optimum amount of P incorporation in SiO_2 results in a reduction of the energetically shallow near-interface trap density to an order of magnitude lower than standard nitrided thermal oxides. The study reveals that two near-interface oxide traps, named O1 (carbon dimer C_O=C_O) and O2 (interstitial Si (Si_i)), that are typically observed in thermal oxides on 4H-SiC are also present in PSG devices with much lower concentration.

• 4H-SiC based trench MOSFETs fabrication requires unit process steps such as dielectric formation, and reactive ion etching (RIE). However, these process advent additional interface issues due to the anisotropy thermal oxidation on different crystal faces of 4H-SiC which results in different oxide thickness in sidewall and trench bottom. In this regard, alternative oxidation method with plasma oxidation and electronic properties of resultant SiO_2/4H-SiC has been investigated. Oxidation growth rates of Si-face and a-faces of 4H-SiC were investigated by carrying out oxidation in the 850 °C - 950 °C temperature range in a plasma afterglow furnace for application to trench MOSFET. At 900 °C, plasma oxidation results in almost equal oxide thickness on Si-face and a-face. Electronic characterization results indicate that after nitric oxide(NO) annealing, the electronic properties of the plasma oxidized SiO_2/SiC interface is comparable to gate oxides formed by standard dry oxidation based process. Furthermore, RIE is known to be introduce defects to oxide-semiconductor interface as well as to the semiconductor substrate. In this regard, effect of reactive ion etching (RIE) of 4H-SiC surfaces prior to gate oxidation was investigated. Results indicate that optimized RIE process does not create additional interface or bulk traps, if RIE produces a smooth surface and if any RIE damaged layer formed on the SiC surface is removed via growing and etching a thin sacrificial oxide prior to the gate oxidation. In addition, preliminary trench MOSFETs based on optimized RIE process and plasma oxidation process has been fabricated and characterized in this work.

• Electronic characterization of oxide-side wall interface of trench structures indicates higher interface traps compared to planar oxide-4H-SiC interface. Furthermore, trench structures shows that formation of V-shaped trench structures due to developed RIE process.

• Development of β-Ga_2O_3 based MOSFETs requires good quality dielectric-β-Ga_2O_3 interface. In this regard, electrotonic properties of dielectric-Ga_2O_3 interfaces and the impact of post-deposition annealing have been investigated in thin film formed by low-pressure chemical deposition (LPCVD SiO_2) and atomic layer deposition (ALD Al_2O_3) on $(\bar{2}01)$ oriented n-type β-Ga_2O_3 single crystals. It was observed that the SiO_2-β-Ga_2O_3 has higher interface and near-interface trap density than the Al_2O_3-β-Ga_2O_3 interface. Among the different dielectrics studied, LPCVD SiO_2 was found to have the lowest dielectric leakage and highest breakdown field.

These results are essential for processing of high performance 4H-SiC and β-Ga_2O_3 devices, as these factors will critically impact device performance such as channel transport, threshold voltage stability and device reliability.

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Chapter 1

Introduction

1.1 Motivation for wide bandgap (WBG) semiconductors

Over the past few decades, continuous technological advances for the development of semiconductor electronic devices has resulted in wide use of consumer electronic devices, advanced automobiles and increase in data communication transmission speed. Electric power conversion such as AC to DC rectifiers, DC to AC inverters, DC to DC and AC to AC converters circuits are core components in modern electronic systems. These involve regulation and conversion of electric power by different semiconductor electronic device components such as diodes and transistors, before it is supplied to the loads. Figure 1.1 shows current and future major applications of power devices which include power supplies, motor control, telecommunications, heating, robotics, electric/hybrid vehicles, traction, lighting ballasts, and electric power transmission [1].

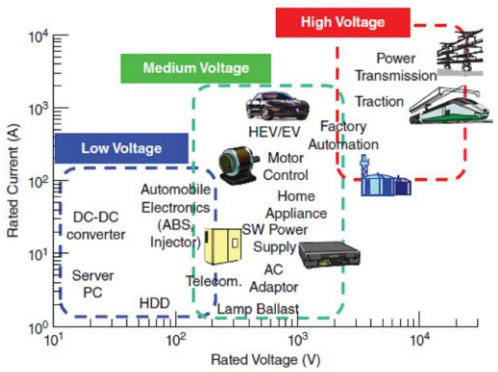

Figure 1.1: Major application areas of power devices plotted as a function of rated voltage.[1]

The most important characteristic of a high voltage power device is the capability to withstand high voltage in its "Blocking state". Thus, vertical power device is highly desirable for high voltage applications due to its n-drift region which has been designed to support the blocking voltage. Amongst vertical devices, two-terminal devices such as bipolar pin (*p*-type/intrinsic/*n*-type) and unipolar Schottky diodes are the simplest and cheapest to fabricate. Among three-terminal devices, popular power devices are Si-based insulated gate bipolar transistor (IGBT) and unipolar power MOSFETs such as Double-Diffused MOSFET (DMOSFETs) and trench MOSFETs [2]. Bipolar device operates with an injection of minority carriers during its on-state, and it requires minority carrier removal during its off-state. This process introduces significant power loss and degrades the power efficiency[2]. In this regard, unipolar power devices such as SBDs and MOSFETs are more favorable than IGBTs for high voltage (above 1 kV) power device applications.

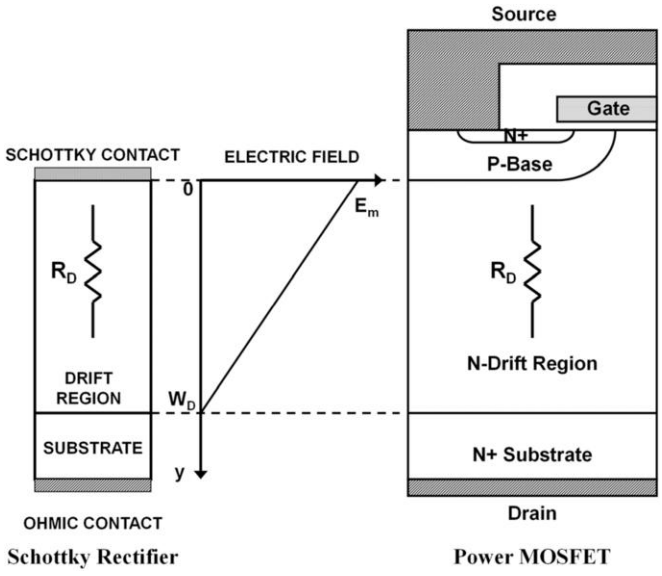

Figure 1.2: One-dimensional electric field distribution within vertical power devices and the typical structures for the vertical Schottky power rectifier and the vertical power D-MOSFET.[3]

Figure 1.2 shows typical structures for the unipolar Schottky power diode and the unipolar vertical power MOSFET (DMOSFET) device[3]. Schottky barrier diodes (SBD) produce current rectification. Both devices contain a drift region, which is designed to support the blocking voltage. The doping concentration and thickness this region are chosen to achieve the desired

"blocking" voltage. The resistance of the drift region can be related to the fundamental properties of the semiconductor material[2]. The one dimensional solution of the Poisson's equation for drift region with uniform doping leads to a triangular electric field distribution as shown in figure 1.2. The maximum blocking voltage that can be supported by the drift region is the determined by the maximum electric field (E_m) at the surface of the semiconductor reaching the critical electric field (E_c) as this represent the breakdown of the semiconductor. The specific-on-resistance (per unit area) of the ideal drift region with uniform doping concentration (N_D) is given by[2]

$$R_{on,sp} = \left[\frac{W_D}{q\mu_n N_D}\right] \tag{1.1}$$

For a desired breakdown voltage (*BV*) , the depletion width (W_D) is given by[2]

$$W_D = \frac{2BV}{E_c} \tag{1.2}$$

The required doping concentration in the drift region to obtain desired *BV* is given by[2]

$$N_D = \frac{\epsilon_s E_c^2}{2qBV} \tag{1.3}$$

Substituting equations 1.2 and 1.3 in equation 1.1, the specific-on-resistance of the ideal drift region can be estimated by[2]

$$R_{on,sp} = \left[\frac{4BV^2}{\epsilon_s \mu_n E_c^3}\right] \tag{1.4}$$

where ϵ_s is the semiconductor's dielectric constant, μ_n is the carrier mobility, and E_c is the critical electric field at the onset of breakdown. The specific on-resistance $R_{on,sp}$ is used to estimate theoretical resistive energy loss in the ideal material and does not take into account of any other sources of resistance. The low specific-on-resistance of the ideal drift region can be obtained by having higher electron mobility (μ_n). However, high critical electric field for breakdown (E_c), has much stronger impact due to its cubic dependence of on specific-on-resistance. The denominator of equation 1.4 ($\epsilon_s \mu_n E_c^3$) refers to the well-known *Baliga's figure of merit for power devices*(BFOM)[2], which is commonly used to compare ideal conduction

losses in different semiconductors, compared to conventional silicon for power applications as shown in table 1.1.

Figure 1.2 shows power MOSFET structure, which contains "gate", p-base region, n+ source, n-drain region and n-drift region. The "ON/OFF" state of the MOSFET device is defined by the applied gate voltage. When a positive gate voltage is applied, the current will flow between the source and drain through channel region by applying drain voltage. Moreover, MOSFET device is capable of supporting high voltage when the drain bias is positive, and the gate electrode is shorted with source electrode by the external gate bias circuit. In this blocking mode, most of the applied voltage is supported across the n-drift region, similar to the SBD.

Materials parameters	Si	GaAs	4H-SiC	GaN	β-Ga_2O_3	Diamond
Bandgap,E_g (eV)	1.1	1.43	3.25	3.4	4.3-4.9	5.5
Dielectric constant,ϵ	11.8	12.9	9.7	9	10	5.5
Breakdown field, E_c (MV/cm)	0.3	0.4	2.5	3.3	8 (*est.*[4])	10
Electron mobility, μ_n (cm^2/V·s)	1480	8400	1000	1250	300 (*est.*[5])	2000
Thermal conductivity λ (W/cm·K)	1.5	0.5	4.9	2.3	0.1-0.3	20
Figures of merit relative to Si						
Baliga's FOM[2] $= \epsilon \cdot \mu \cdot E_c^3$	1	14.7	317	846	3214	24660

Table 1.1: Material properties of some semiconductors and normalized unipolar power-device *Baliga's figures of merit*(BFOM)[6, 7]

The efficiency of power conversion using currently available power semiconductor device technology is not high enough for future applications. Approximately 10% of the electric power is lost as heat driving. Even in conventional AC to DC and DC to AC convertors, the efficiency is still as low as about 0.8 [1]. Therefore, higher power efficiency devices as well as "miniaturization" of power converters are attractive. In this regard, exploration of novel materials for next-generation power electronics is necessary. Mainly, wide bandgap (WBG) semiconductors are receiving considerable attention due to their attractive properties which results in more compact and energy efficient power devices (Table 1.1). Furthermore, wide bandgap semiconductors are more favorable for high temperature applications due to their inherent temperature limits compared to narrow bandgap semiconductors.

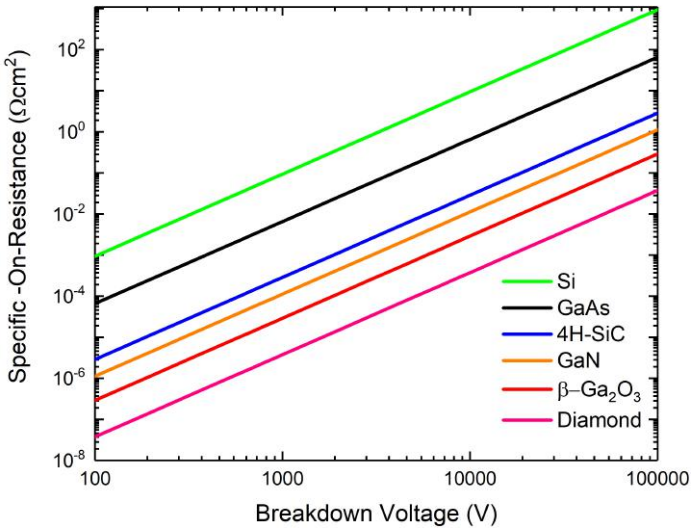

Figure 1.3: Specific on-resistance as a function of breakdown voltage under ideal punch-through conditions for semiconductor materials

Figure 1.3 shows the ideal-specific on-resistance of various semiconductors as a function of device breakdown voltage based on equation 1.4. Due to the excellent material properties and the availability of high quality epitaxial wafers, 4H-SiC is currently the most technologically advanced WBG semiconcutor. Furthermore, one of the great advantages in 4H-SiC is thermal oxide grows on SiC surface similarly to silicon. While 4H-SiC MOSFETs have been successfully commercialized in the power electronics market[1, 2, 8], the performance of these devices is limited by a low device mobility and high density of near-interface states at the SiO_2/4H-SiC interface. Therefore, systematic investigations to identify the origin of the interface states and the nature of interfacial defect passivation mechanisms was one aspect of this thesis (chapter 4 and chapter 5).

The significantly lower ideal $R_{on,sp}$ for β-Ga_2O_3 is very attractive for high voltage electronics beyond SiC and GaN. However, β-Ga_2O_3 is new wide bandgap material and faces more challenges compared to matured semiconductor technologies[6, 7]. In this regard, electronic characterization of metal-β-Ga_2O_3 junctions (chapter 2) and oxide-β-Ga_2O_3 interfaces (chapter 6) are essential studies which are required for laying the foundations of power electronics technology based on this material.

For the rest of this dissertation, our discussion will be based on electronic properties of metal-β-Ga_2O_3 interfaces, oxide-4H-SiC interfaces and oxide-β-Ga_2O_3 interfaces.

1.2 Physical properties of 4H-SiC

As a result of rapid progress in SiC growth and device technologies in last decade, 4H-SiC power devices such as DMOSFET, trench MOSFETs are now commercially available[1, 9]. The major benefits of 4H-SiC devices include lower power dissipation, smaller size, and simplified cooling units of power converters[1, 2, 9]. Due to semiconductor maturity, number of research studies on device physics, device processing technologies of 4H-SiC have been already carried out in this area[1, 2, 9]. Herein, we briefly discuss its fundamental properties of 4H-SiC.

1.2.1 Crystal structure of 4H-SiC

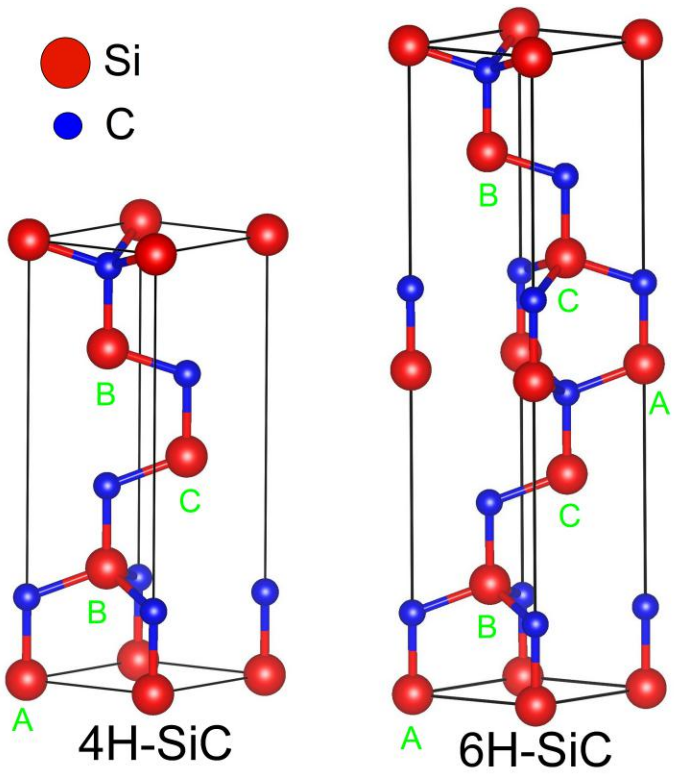

Figure 1.4: Crystal structures of 4H-SiC and 6H-SiC. Occupation sites label as A, B, and C for repeating sequence. Drawing was produced by using the VESTA software[12]

Silicon carbide (SiC) is a IV-IV compound material with a rigid stoichiometry of 50% silicon (Si) and 50% carbon (C). Both Si ($3s^2 3p^2$) and C($2s^2 2p^2$) atoms have four valence electrons

in their outermost shells. Therefore, Si and C atoms are tetrahedrally bonded by covalent bonds to form a SiC crystal. The chemical bonding between Si and C atoms has a very high bond energy of 4.6 eV. This strong chemical bonding gives SiC material, very high hardness, chemical inertness, and high thermal conductivity [1, 10]. From a crystallographic point of view, SiC can adopt different crystal structures by varying only in stacking sequence, without changing its chemical composition[1, 11]. Polytypes of SiC are represented by the number of Si-C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal and R for rhombohedral). Each of these structures exhibit unique electrical, optical, thermal, and mechanical properties. Among these polytypes, 3C-SiC, 4H-SiC and 6H-SiC polytypes are very popular and have been extensively investigated to date. The unit cells of 4H-SiC and 6H-SiC are shown in figure 1.4. Here, A, B, and C are the potentially occupied sites in a hexagonal close-packed structure. Thus, 4H-SiC is designated by repeating sequence of ABCB and 6H-SiC is designated by repeating sequence of ABCACB.

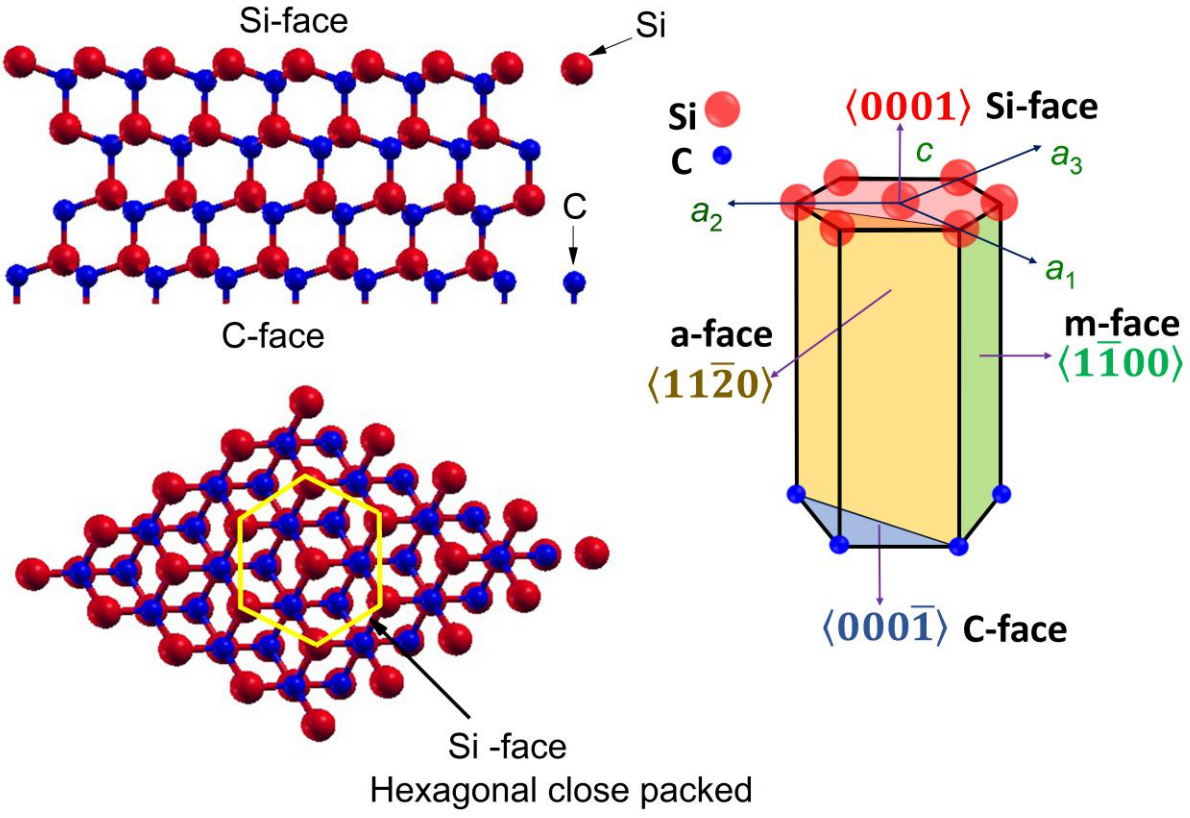

Figure 1.5: Schematic illustrations of bond configurations in a hexagonal SiC polytype and definition of several major planes in a hexagonal SiC polytype. Bond configuration drawing was produced by using the XCrySDen software [13].

Figure 1.5 shows a schematic illustration of bond configurations in a hexagonal polytype of SiC and definition of several major crystal planes. Here, the (0001) face, where Si atoms are directed along <0001> (*c-axis*) is referred as the "Si-face", while the (0001) face, where C atoms are directed along $<000\bar{1}>$ is referred as the "C-face". Other than Si and C faces, $(11\bar{2}0)$ face is referred as "a-face", and $(1\bar{1}00)$ face is referred as "m-face". While a-face and m-face are mixture of Si and C atoms, Si-face and C-face are polar planes. The surface energy, chemical reactivity and electronic properties are significantly dependent on these crystal faces[1]. Table 1.2 summarizes the major physical properties of 3C-SiC, 4H-SiC and 6H-SiC polytypes.

Property	3C-SiC	4H-SiC	6H-SiC
Band gap, E_g (eV)	2.36	3.26	3.02
Breakdown field, E_c (MV/cm)			
$E_c \perp$ to c-axis <0001>	1.4	2.2	1.7
$E_c \parallel$ to c-axis <0001>	1.4	2.8	3.0
Electron mobility, μ_n (cm^2/V·s)			
$\mu_n \perp$ to c-axis <0001>	1000	1020	450
$\mu_n \parallel$ to c-axis <0001>	1000	1200	100
Hole mobility (cm^2/V·s)	100	120	100
Dielectric constant			
$\epsilon_s \perp$ to c-axis <0001>	9.72	9.76	9.66
$\epsilon_s \parallel$ to c-axis <0001>	9.72	10.32	10.03
BFOM (n-type, $\parallel$ to c-axis <0001>)	61	626	63
BFOM (p-type, $\parallel$ to c-axis <0001>)	2	25	19

Table 1.2: Major physical properties of common SiC polytypes at room temperature, including the Baliga's figure-of-merit (BFOM) $\epsilon_s \mu_n E_c^3$ normalized with respect to the value for Si [1].

4H-SiC exhibits significantly higher BFOM than other SiC polytypes due to high critical field strength and high electron mobility. Therefore, 4H-SiC has been almost exclusively employed for power device applications. In fact, the characteristics of commercial 4H-SiC power devices (Schottky barrier diodes and field effect transistors) have already outperformed the theoretical limits of 3C-SiC and 6H-SiC unipolar devices[1]. Furthermore, the availability of 4H-SiC Si-face wafers with relatively large diameters and reasonable quality has fast-paced the fabrication of 4H-SiC-based electronic devices[1].

1.2.2 Band structure of 4H-SiC

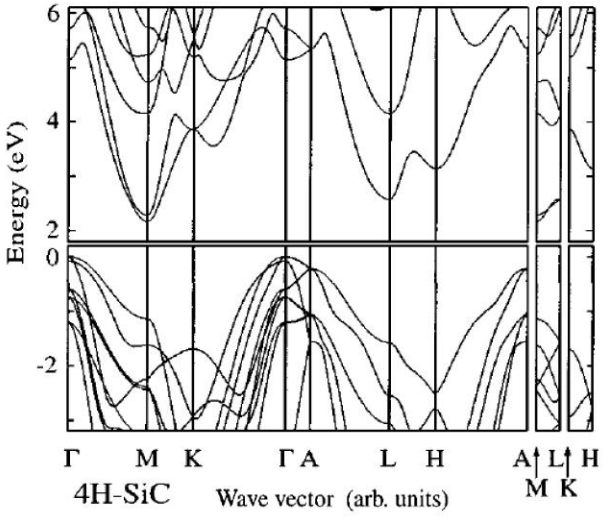

Figure 1.6: Band structure for 4H-SiC [14]

Figure 1.6 shows the energy band structure of 4H-SiC as obtained from Density Functional Theory. 4H-SiC has an indirect bandgap, as is also the case for all the other SiC polytypes[1]. The top of the 4H-SiC valence band is located at the Γ point and the conduction band minima appear at M point[1]. The number of conduction band minima in the first Brillouin zone (Mc) is 3 for 4H-SiC. However, due to the calculation limitation, calculated energy band gap is under estimated about 40% in this band diagram[14]. In this study, 1s wave function of the carbon atom and 1s, 2s, and 2p of the silicon atom were considered to be core states[14]. Furthermore, the valance band of 4H-SiC consider to be due to the all the higher states. However, clear configuration of wave function for the conductance band is not reported. Theoretically calculated (first principle calculations) and experimentally reported effective mass of electron and hole for 4H-SiC are shown in table 1.3.

1.2.3 Melt growth and epitaxy of 4H-SiC

The standard technique for 4H-SiC bulk growth is the seeded sublimation (or modified Lely) method [1]. Figure 1.7 shows the schematic illustration of seeded sublimation growth reactor and typical grown boule. Sublimation (phase transition) growth of SiC is consists with three

		Experiment	Theory
Electron effective mass	$m_{ML\parallel}$	0.33	0.31
	$m_{M\Gamma}$	0.58	0.57
	m_{MK}	0.31	0.28
	$m_{\perp}$	0.42	0.40
Hole effective mass	$m_{\parallel}$	1.75	1.62
	$m_{\perp}$	0.66	0.61

Table 1.3: Effective masses of electrons and holes in 4H-SiC [1].

steps[1]: (i) Sublimation of the SiC source: The crucible contain with source material (SiC powder) is heated by radio frequency (rf) induction up to the process temperature of about 2300$\sim$ 2500 °C[1] where source sublimates. (ii) Mass transport of sublimated species: In this process mass transport from the source to the seed is enhanced by low pressure conditions[1]. (iii) Surface reaction and crystallization: The seed temperature is fixed at about 100 °C lower than the source temperature, so that sublimated SiC species condense and crystallize on the seed[1]. This growth method is also referred as "physical vapor transport (PVT)" growth.

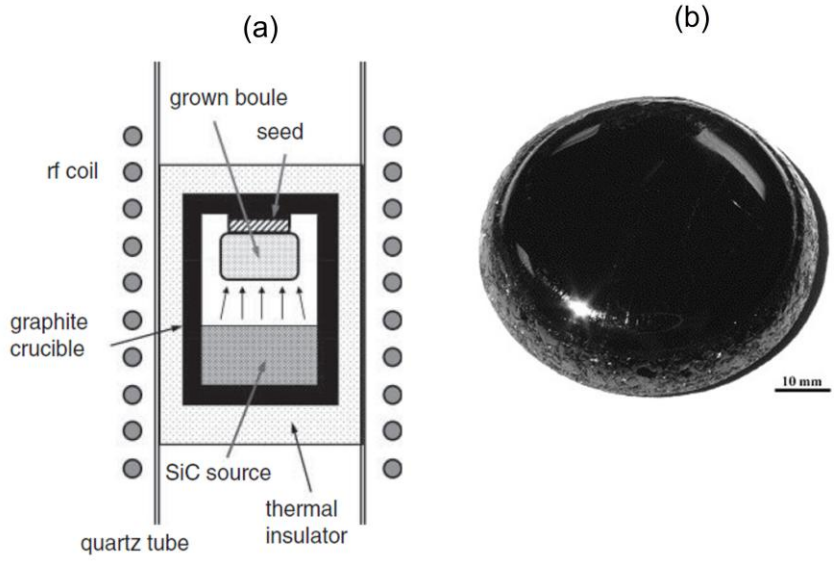

Figure 1.7: (a)Schematic illustration of a seeded sublimation growth of SiC[1] (b) Typical grown SiC boule[15].

In SiC technology, epitaxial growth is mainly performed by chemical vapor deposition[1]. Several reactors with unique designs are documented in reference [1]. All these reactors require very high temperature (1500-1700°C) chemical vapor deposition for SiC epitaxial growth.

1.2.4 Doping and impurity

The *n*-type doping of SiC generally achieved by introducing group V impurities, such as N, P to the semiconductor. In SiC technology, *n*-type conductivity is usually obtained by introducing nitrogen gas into the growth ambient[1]. The *p*-type conductivity of SiC generally achieved by introducing Al impurity during the SiC growth process,by adding an aluminum-containing compound such as trimethylaluminum (TMA: $Al(CH_3)_3$) to the SiC source[1].

1.3 Physical properties of β-Ga_2O_3

Gallium oxide (Ga_2O_3) in various forms (polycrystalline powders, thin films, nano-crystals) has a long history of several applications like catalysis[16, 17], gas sensors[7, 17, 18, 19] , transparent conducting substrates (TCO) [20, 21] and solar-blind photodetectors [7, 22]. Furthermore, Ga_2O_3 can form several different polymorphs phases, designated as α (corundum), β (monoclinic), γ (defective spinel) , and ε , δ (orthorhombic)[23]. Among these different phases of Ga_2O_3, β-Ga_2O_3 (monoclinic) structure is known to be the only stable polymorph through the whole temperature range up to its melting point 1800 °C [7, 17, 23, 24]. Furthermore, thermal stability of β-Ga_2O_3 enables bulk single crystal growth and subsequent epitaxial films via high temperature processes such as crystallization from a melt or vapor phase growth.[17]

1.3.1 Crystal structure of β-Ga_2O_3

The unit cell of β-Ga_2O_3 is shown in figure 1.8. Crystal structure of β-Ga_2O_3 is base-centered monoclinic with space group 12 (C2/m) and contains two types of gallium ions: tetrahedral geometry Ga(1) and octahedral geometry Ga(2) and three types of oxygen ions : O(1), O(2), and O(3)[25]. Crystals or wafers with different orientations of β-Ga_2O_3 are being used in research and development, including $(\bar{2}01)$, (010), and (001) planes. However, availability of commercial wafers is currently limited to (010) and $(\bar{2}01)$ orientations. Crystal planes of β-Ga_2O_3 are

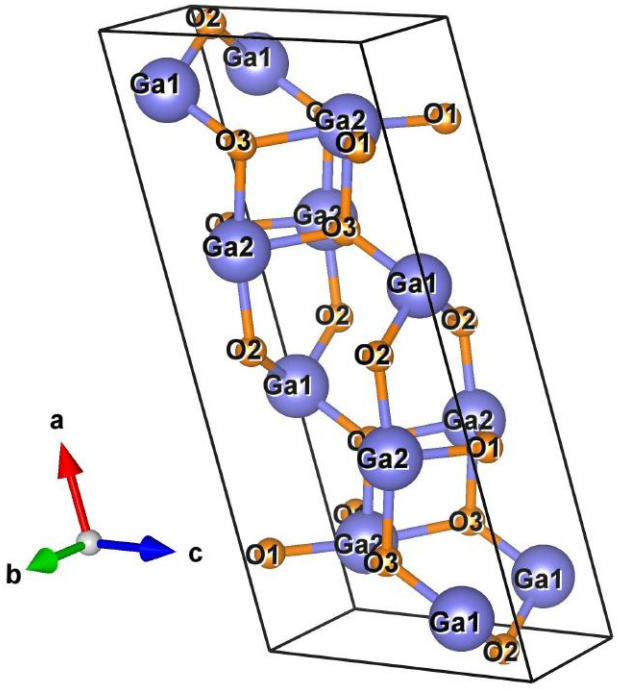

Figure 1.8: Unit cell of β-Ga_2O_3. It possesses two inequivalent Ga sites: Ga(1), Ga(2) and three inequivalent O sites: O(1), O(2), and O(3). Drawing was produced by using the VESTA software[12]

believed to be non-polar surfaces[26]. However, two types of gallium ions and three types of oxygen ions can lead to a different type of non-polar terminations on crystal faces. Therefore, crystal surfaces (planes) with different atomic arrangement lead to a different physical, optical, and electrical properties [7, 26, 27, 28].

1.3.2 Physical properties of β-Ga_2O_3

Table 1.4 summarizes some major physical properties of β-Ga_2O_3. The reported room-temperature band gap of β-Ga_2O_3 varies from 4.6-4.9 eV [29, 30, 31, 32] and it is associated with large estimated critical electric field strength of 8 MV/cm [4]. Compared to other wide bandgap semiconductors, β-Ga_2O_3 has more advantages due to its ultra wide energy band gap. However, β-Ga_2O_3 have a thermal conductivity is about twenty times smaller than that of 4H-SiC and ten times smaller than that of GaN. Furthermore, the thermal conductivity in β-Ga_2O_3 shows a strong anisotropy [7, 17, 33, 34]. Therefore proper thermal management require for a future β-Ga_2O_3 devices.

Property	β-Ga_2O_3	4H-SiC
Crystal structure	Monoclinic	Hexagonal
Group of symmetry	C2/m	C_{6v}^4
Lattice parameters		
	a = 12.214 Å	a = 3.0798 Å
	b = 3.037 Å	c = 10.0820 Å
	c = 5.798 Å	
	$\alpha = \gamma = 90°$, $\beta = 103.8°$	$\alpha = \beta = 90°$, $\gamma = 120°$
Band gap, E_g	4.6-4.9 eV	3.26 eV
Density	5.95 g/cm^3	3.21 g/cm^3
Dielectric constant	10.2	9.76-10.32
Melting point	1800 °C	2830 °C
Specific heat	0.56 Jg^{-1}K^{-1}	0.69 Jg^{-1}K^{-1}
Thermal conductivity,λ		
	0.13 W/cm·K (100)	3.3-4.9 W/cm·K
	0.13 W/cm·K ($\bar{2}$01)	
	0.14 W/cm·K (001)	
	0.27 W/cm·K (110)	
	0.23 W/cm·K (010)	
Saturation velocity, v_s		
	1.8×10^7 cm/s (001)	2 cm/s
	2×10^7 cm/s (010)	

Table 1.4: Major physical properties of β-Ga_2O_3 and 4H-SiC .[1, 7, 17]

1.3.3 Band structure of β-Ga_2O_3

In the literature, first-principles calculations based on Density Functional Theory (DFT) have reported the electronic band structure of β-Ga_2O_3.[31, 32, 35, 36, 37, 38, 39] All the DFT calculations agree with the fairly flat valence band in β-Ga_2O_3 and the location of the conduction-band minimum at the zone center Γ point (Figure 1.9 (a))[37]. The conduction-band states are known to be resulting from Ga 4s orbitals. Theoretical calculations show that electron effective mass (DOS based) (m_e^*) is within 0.28 m_0 [37] and 0.34 m_0[31]. On the other hand, the valence-band states, are derived mainly from O 2p orbitals and are characterized by small dispersion, and large hole effective mass [37]. According to calculations, the hole effective mass (DOS based) (m_h^*) is 40 m_0 [37].

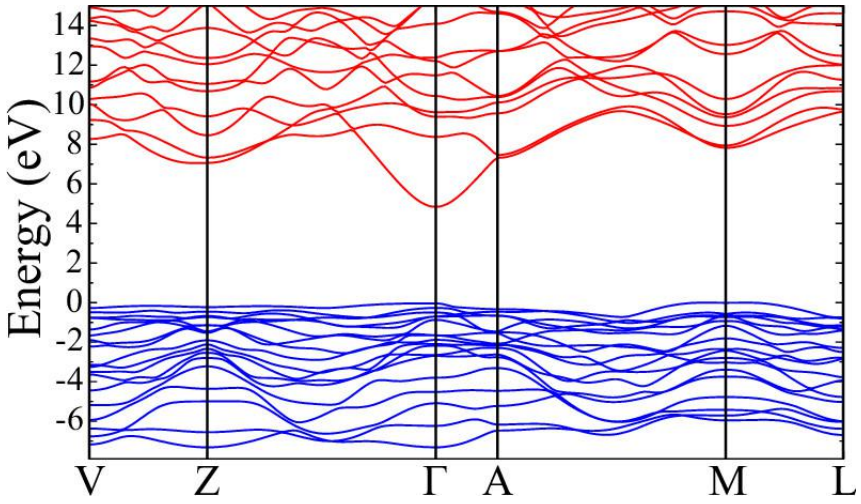

Figure 1.9: Band structure for β-Ga_2O_3 [37]

1.3.4 Melt growth and epitaxy of β-Ga_2O_3

It has been established that β-Ga_2O_3 can be grown from liquid-phase by common techniques, such as Czochralski (CZ) method[33, 40], floating-zone (FZ)[41, 42], Bridgman (horizontal or vertical) method[43] and an edge defined film-fed (EFG) method[44, 45]. Among them, EFG method is the leading and most established melt growth method used by current commercial wafer suppliers of β-Ga_2O_3 single crystals[46]. Furthermore, large diameters (2 in. and 4 in.) of $(\bar{2}01)$ β-Ga_2O_3 wafers have been demonstrated by EFG approach[45]. A schematic drawing of the EFG process is shown in figure 1.10 (a) [45]. In this method, 5N(99.999%) Ga_2O_3 powder is used as the source material, which is liquified when heated to melting point 1800 °C. Typically, radio-frequency (RF) induction coil is used as the heat source. Once the capillary action has begun, the melt moves up through a slit in the die. Crystal growth is then initiated on a β-Ga_2O_3 seed crystal, which is placed on top surface of the die. Here, shape of the grown crystal is determined by the top surface of the die [45]. Figure 1.10 (b) shows state-of-the-art bulk β-Ga_2O_3 crystals grown by EFG method [45]. Figure 1.10 (c) shows photographs of the β-Ga_2O_3 single crystal substrates made from the bulk crystal. The (010) or (001) oriented substrates are commercially available only as 10 mm$\times$ 15 mm rectangular shapes and $(\bar{2}01)$ oriented substrates are available as 10 mm$\times$ 15 mm rectangular or, 2 and 4 inches diameter substrates.

The single crystal substrates provide wafers needed for epitaxy as well as for preliminary test device fabrication, such as vertical Schottky barrier diodes and metal oxide capacitors

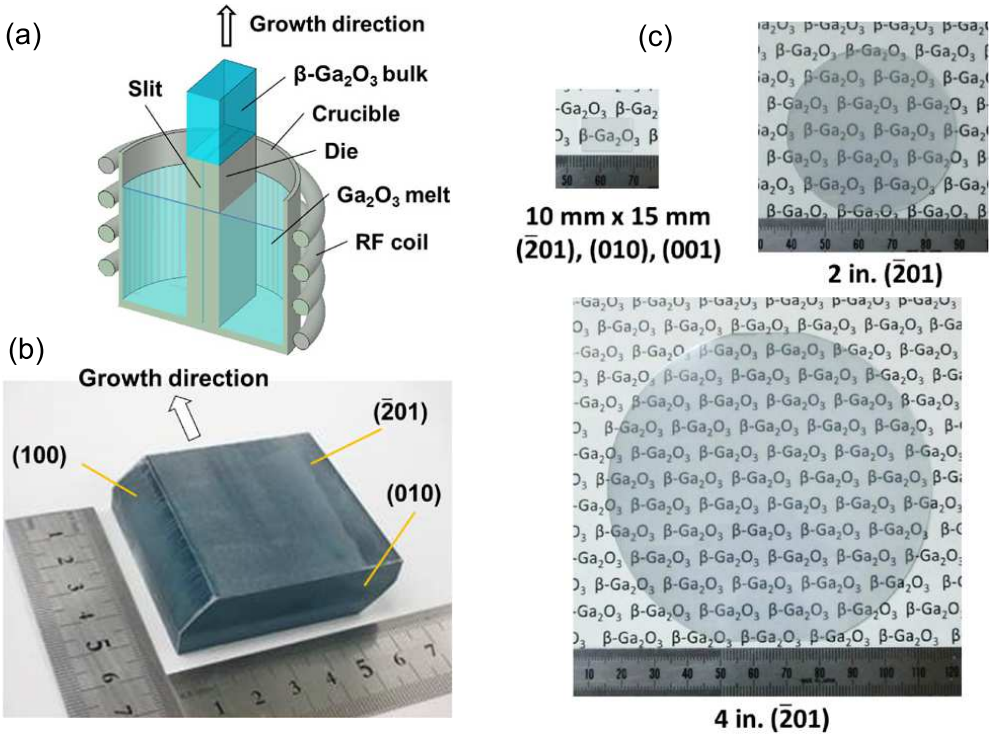

Figure 1.10: (a) Illustration of EFG process (b) EFG-grown β-Ga_2O_3 bulk crystal (c) Commercially available β-Ga_2O_3 substrates [45].

for initial electrical characterization. However, it is essential to have high-quality epitaxial growth layers to enable more complex power devices. In this regard, common epitaxial growth process such as Molecular beam epitaxy (MBE)[47, 48, 49, 50, 51], plasma-assisted molecular beam epitaxy (PAMBE)[54], Metal Organic Chemical Vapor Deposition (MOCVD)[52, 53] and hydride vapor phase epitaxy (HVPE)[55, 56, 57] have been demonstrated effective growing of high-quality epitaxial layers.

1.3.5 Doping and impurity

Pure stoichiometric β-Ga_2O_3 is known to be insulating. However, it also exhibits excellent *n*-type conductivity when it is synthesized in reduced oxygen growth conditions. In early research work, the *n*-type semiconductivity was commonly attributed to oxygen vacancies[33, 58, 45, 59, 60, 61]. However, the relation between oxygen vacancies and unintentional *n*-type semiconductivity of β-Ga_2O_3 is still not fully understood and remains questionable[37].

Commercially available unintentionally doped (UID) bulk single crystals (EFG) exhibit *n*-type semiconductivity up to $\sim 10^{17}$ cm^{-3} dopant concentration. The origin of the unintentional doping (UID) has been attributed to presence of higher amount of Si impurity in the source powder. Furthermore, analysis of impurities in EFG bulk β-Ga_2O_3 also shows significant amount of Fe, and Ir in the crystal. The *n*-type conductivity of β-Ga_2O_3 can be controlled from 10^{16} cm^{-3} to 10^{19} cm^{-3} carrier concentrations by intentionally doping with group IV elements such as Si, Sn or Ge [45, 48, 50, 54]. In addition, ion implantation of silicon has been used to increase *n*-type conductivity as well [62].

The possibility of *p*-type conductivity in β-Ga_2O_3 remains controversial. So far there is no evidence of hole conduction in *p*-type Ga_2O_3. But, it has been demonstrated that *n*-type conductivity can be compensated by addition of deep acceptors such as Mg and Fe [53, 63, 64]. As mentioned earlier, large effective mass for holes in the valence band[37] present an obstacle for *p*-type conductivity in this class of materials.

1.4 Motivation for electronic characterization of metal-semiconductor and oxide-semiconductor interfaces on β-Ga_2O_3 and 4H-SiC wide bandgap semiconductors

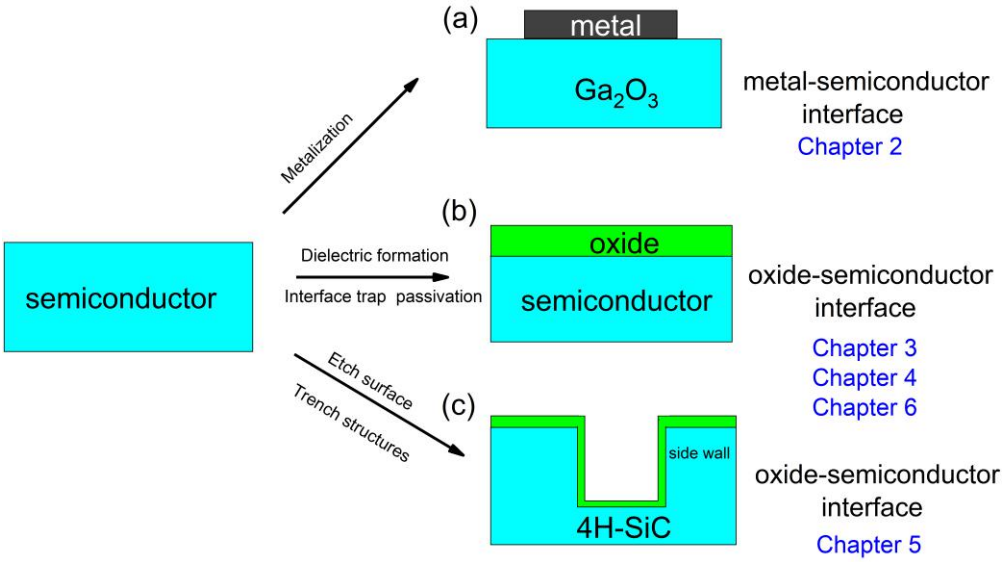

Figure 1.11: Metal-semiconductor and oxide-semiconductor interfaces on β-Ga_2O_3 and 4H-SiC wide bandgap semiconductors.

As we disused in section 1.1, WBG semicondcutor Schottky diodes (SBDs) and MOSFETs power devices are promising for rectification and conversion of high voltages in electronic systems. However, to fabricate these devices, it requires to form metal-semiconductor interface and dielectric-semiconductor interfaces. In this regard, processing steps such as metallization (figure 1.11 (a)) and dielectric formation (figure 1.11 (b)) need be performed on semiconductor material. In addition, development of the advanced MOSFET geometries such as trench MOSFETs required reactive ion etching step (figure 1.11 (c)). As a result of these processing steps it creates new or altered interfaces. Furthermore, it is known that poor quality interfaces as well as inherent bulk defects in semiconductor can affect the power device performances. Therefore, it is required to perform electronic characterization on interfaces after these fabrication steps as well as bulk defect investigation on new semiconductor materials to understand the effect of these defects on device performances.

β-Ga_2O_3 is an exciting emerging WBG semiconductor and has the potential to revolutionize the future high voltage power electronics. Demonstrations of Ga_2O_3 power rectifiers, MESFETs and MOSFETs have shown rapid progress towards a practical technology based on this material. β-Ga_2O_3 power rectifiers (SBDs) can easily fabricated by metallization of Ga_2O_3 as shown in figure 1.11 (b). However, Schottky barrier heights and ideality factors extracted form characterization of metal-Ga_2O_3 interface, are important physical quantities that need to be studied in detail. Furthermore, investigation of inherent bulk defects in fairly new Ga_2O_3 substrates needed to be carried out to evaluate the quality of the semiconductor. These invitations are essential for development of power electronic devices based on this material (Chapter 2).

Although 4H-SiC MOSFETs have been successfully commercialized in power electronics market, MOSFET channel mobility is around 5% ($\mu_{channel}/\mu_{bulk}$)of that theoretically expected, due to high density of interface traps (D_{it}) in SiO_2-4H-SiC interface. Interface traps known to be originated from dangling bonds, C dimers, Si interstitials, O vacancies which are formed at the SiO_2-4H-SiC interface during the dielectric formation (figure 1.11 (b)). In this regard, incorporation of phosphorus atoms via conversion of SiO_2 to phospho-silicate glass (PSG) has been shown to improve the MOS channel mobility up to 10% ($\mu_{channel}/\mu_{bulk}$). However, detailed

understanding of the effect of P on defects at SiO_2-4H-SiC interface is lacking. Therefore, systematic investigations to identify the origin of the traps and nature of the trap passivation mechanism by P is required (Chapter 4).

4H-SiC trench MOSFET is a fascinating device design, as it offers low specific on resistance and higher current densities, which can potentially reduce device cost. However, trench power MOSFET devices required different geometry compared to other MOSFETs. MOS devices on 4H-SiC trench geometry advents an additional issue due to anisotropic thermal oxidation on different crystal faces which results in different oxide thicknesses on the trench bottom and the sidewalls. Therefore, studies about alternative oxidation process for anisotropy oxidation and characterization of electronic properties of the resultant SiO_2/4H-SiC interface on different crystal faces are required (Chapter 4). Furthermore, to have trench structure in 4H-SiC, it requires etching with RIE step(figure 1.11 (c)). This RIE step known to result in surface roughness, surface contamination and introduce of bulk defect to the epitaxial layer. Therefore, it is essential to understand the nature of residual damage caused by RIE as well as the damage recovery process (Chapter 5).

Furthermore, development of MOS devices based on β-Ga_2O_3 material requires a gate oxide formation via deposited gate dielectric (figure 1.11 (b)). In this regard, systematic comparison of electronic properties of different gate dielectric-Ga_2O_3 interfaces are important as these factors impact critical MOSFET parameters such as sub-threshold swing, threshold voltage, channel mobility and device stability (Chapter 6).

1.4.1 Thesis outline

The layout of this thesis as follows.

The chapter 2, includes a broad introduction of the fundamentals of metal-semiconductor interfaces and fundamentals of semiconductor traps. This is followed by original results in electronic characterization of β-Ga_2O_3 Schottky barrier diodes.

The chapter 3, gives the basic fundamentals of MOS devices and the several characterization methods to estimate interface traps. This chapter serves as the technical background for subsequent chapters.

The chapter 4, includes a rigorous investigation of near interface traps on P-doped SiO_2/4H-SiC interface by constant capacitance deep level transient spectroscopy (CCDLTS) measurements. Furthermore, electronic characterization of oxide grown by plasma oxidation is also presented.

The chapter 5, discuses the detail investigation of RIE induced effects and electronic characterization of oxide grown on RIE etched 4H-SiC surface. Furthermore, electronic characterization of 4H-SiC trench side walls and 4H-SiC trench MOSFETs are also presented.

The chapter 6, is a systematic investigation of interface trapping in $(\bar{2}01)$ β-Ga_2O_3 MOS capacitors with deposited dielectrics.

The chapter 7, is the conclusion and some suggestions for future work regarding the topics addressed in this thesis.

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Chapter 2

Electronic properties of β-Ga_2O_3 metal− semiconductor interfaces and bulk defect spectroscopy

In the literature, physics of metal-semiconductor contacts has been studied widely due to their importance in rectifying behavior as well as a tool for analysis of different fundamental properties of the semiconductor[1, 2]. In this chapter, first we discuss the basic physics of metal-semiconductor contacts, and electrical properties of β-Ga_2O_3 SBDs. Next, we discuss physics of bulk traps, Deep Level Transient Spectroscopy (DLTS) technique and investigation of bulk traps using β-Ga_2O_3 Schottky barrier diodes. Part of this chapter has already been published by the author in Semiconductor Science and Technology journal(Analysis of temperature dependent forward characteristics of Ni/$(\bar{2}01)\beta$-Ga_2O_3 Schottky diode)[46].

2.1 Introduction to Metal− Semiconductor Contacts

When a metal forms a contact with a semiconductor at thermal equilibrium, Fermi levels of the metal and semiconductor coincide with each other. Illustration of the band alignment between the metal and *n*− type semiconductor is shown in Figure 2.1. The energy difference between the vacuum level and Fermi level is called *work function*. For the metal, *work function* is denoted by $q\phi_m$ (*metal work function*) which is a constant. The energy difference between the vacuum level and the conduction band edge of the semiconductor also a constant and called by *electron affinity* ($q\chi_s$). Due to the energy band alignment, two type of barriers will be formed as shown in figure 2.1. These are (*a*) The Schottky barrier ($q\phi_{bn}$) *energy barrier between metal Fermi level to conduction band edge of the semiconductor at the interface* and (*b*) Built in potential

barrier (qV_{bi}) *barrier between the conduction band edge of the semiconductor to conduction band edge of the metal-semiconductor interface*.

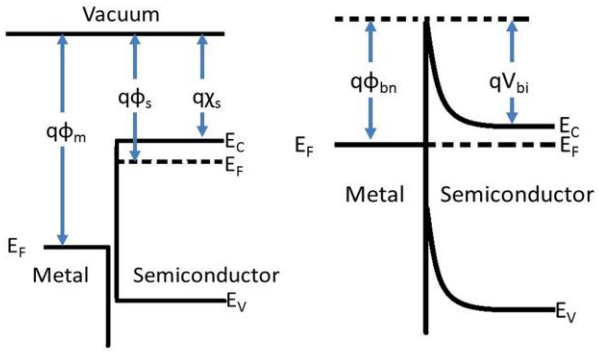

Figure 2.1: Energy-band diagram of metal-n type semiconductor contacts under thermal equilibrium

Under the thermal equilibrium (without any bias), the ideal value for the Schottky barrier height($q\phi_{bn}$) is given by Schottky$-$ Mott rule [2],

$$q\phi_{bn} = q(\phi_m - \chi_s) \tag{2.1}$$

2.1.1 Space charge region of Schottky diode

Solving the Poission's equation, under the depletion approximation and using the boundary conditions for the one-side abrupt junction, equation for the depletion width (space charge region) can be obtain as follows[2].

$$-\nabla^2\Phi = \frac{\rho}{\epsilon_s} \tag{2.2}$$

$$\vec{E} = -\vec{\nabla}\Phi \tag{2.3}$$

$$\nabla.\vec{E} = -\nabla^2\Phi = \frac{\rho}{\epsilon_s} \tag{2.4}$$

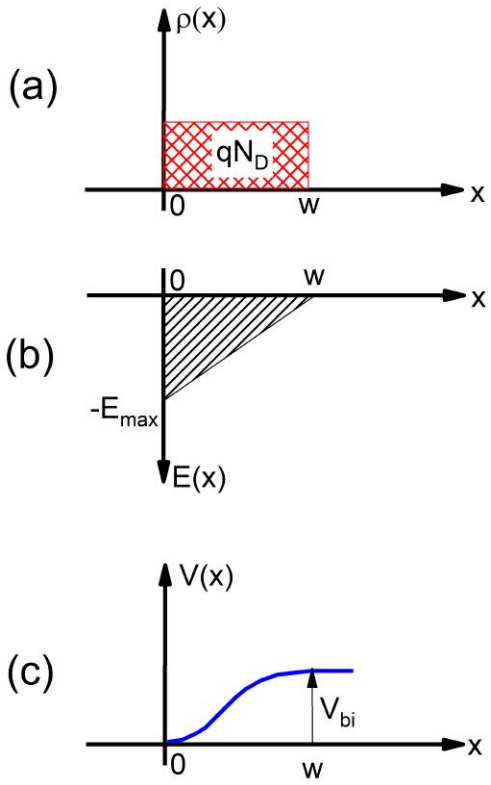

Figure 2.2: (a) Space-charge distribution in one-side abrupt junction in thermal equilibrium. (b) Electric field distribution (c) Potential variation with x where V_{bi} is the built-in potential.

For the one dimension case, equation 2.4 can be further reduced to

$$-\frac{\partial E}{\partial x} \equiv -\frac{\partial^2 V}{\partial x^2} = \frac{\rho(x)}{\epsilon_s} \tag{2.5}$$

Furthermore, with the approximation of $\rho(x) \simeq qN_D$ for $x < W$ (figure 2.2(a)) and $\rho(x) \simeq 0$, and $dV/dx \simeq 0$ for $x > W$ (W is the depletion width), Electric field $E(x)$ and Potential $V(x)$ can be obtained by integrating equation 2.5 as follows

$$E(x) = \frac{qN_D}{\epsilon_s}(x - W) \quad \text{for} \quad 0 < x \leq W \tag{2.6}$$

and

$$E(x) = -E_{max} + \frac{qN_D}{\epsilon_s}x \tag{2.7}$$

where E_{max} is the maximum field at $x = 0$ (figure 2.2(b)) and can be obtained by

$$|E_{max}| = \frac{qN_D}{\epsilon_s}W \tag{2.8}$$

and

$$V(x) = E_{max}(x - \frac{x^2}{2W}) \tag{2.9}$$

Furthermore, when $x = W$, built-in potential V_{bi} (figure 2.2(c)) can be found by,

$$V_{bi} = \frac{1}{2}E_{max}W \tag{2.10}$$

Eliminating E_{max} from equations 2.8, 2.10 and solving the equation for W, expression for depletion width (W) can be written as follows.

$$W = \sqrt{\frac{2\epsilon_s V_{bi}}{qN_D}} \quad \text{cm} \tag{2.11}$$

2.1.2 Effect of Applied Bias

In the case of applied bias, $q\phi_{bn}$ is independent of the bias voltage, since there is no voltage drop across the metal. The total voltage drop will be only sustained across the space charge region of the semiconductor. Then, curvature of the bands change and qV_{bi} gets modified (Figure 2.3). Furthermore, the barrier $q\phi_{bn}$ limits the flow of the electrons from the metal into the semiconductor and qV_{bi} limit the electron flow from the semiconductor into the metal, respectively. Since forward bias acts like effectively reducing in qV_{bi}, electrons can flow from the semiconductor to the metal (figure 2.3). Under reverse bias, qV_{bi} increases and block the electron flow (figure 2.3). Therefore, the SBD shows rectifying behavior, that current increases sharply in the condition of forward bias, whereas little or no current flows in the reverse bias.

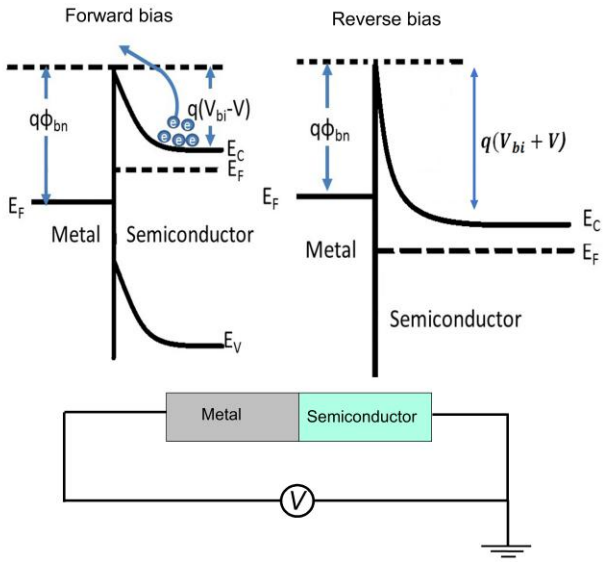

Figure 2.3: Energy-band diagram of metal-n type semiconductor under different biasing conditions.

2.1.3 Current transport mechanism under forward bias in Schottky diode

The current transport process in Schottky barrier diode is mainly due to the majority carriers and can be categorize as (1) electron transport from the semiconductor to the metal over the potential barrier (figure 2.4 [1]), (2) tunneling of electrons through the barrier (figure 2.4 [2]) and (3) edge leakage current due to the high electrical field or interface current due to traps (figure 2.4 [3]).

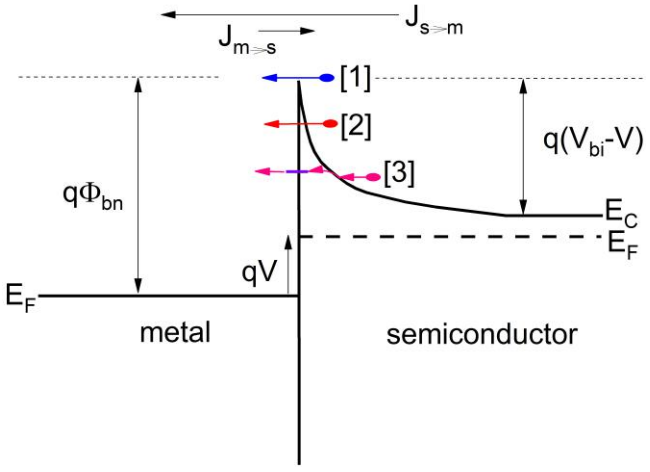

Figure 2.4: Basic transport process under forward bias [2].

In this work, we studied electron transport over the barrier by considering the thermionic emission theory. Thermionic emission theory is derived based on three assumptions where (1)

Schottky barrier height is much larger than kT; (2) shape of the barrier is immaterial and (3) current flow depend solely on the barrier height. Therefore, current density from the semiconductor to the metal, $J_{s\to m}$, can be derived by considering the traveling electrons with sufficient energy to overcome the barrier[2].

$$J_{s\to m} = \int_{E_F+q\Phi_{bn}}^{\infty} qv_x dn \tag{2.12}$$

where $E_F + \Phi_{bn}$ is the minimum required energy for the electron emission in to the metal, v_x is the electron velocity in the direction of the transport. The electron density in an incremental energy range (dn) is given by,

$$dn = D(E)f(E)dE \tag{2.13}$$

where D(E) is the parabolic density of state function for free electron which is given by,

$$D(E) = \frac{4\pi(2m^*)^{3/2}}{h^3}\sqrt{E - E_C} \tag{2.14}$$

$f(E)$ is the distribution function,

$$f(E) = \frac{1}{\exp(\frac{E-E_F}{kT}) + 1} \tag{2.15}$$

By considering Boltzmann approximation, $E_C - E_F \gg kT$, $f(E)$ can be rewritten as follows

$$f(E) = \exp\frac{-(E - E_F)}{kT} = \exp\frac{-(E + E_C - E_C - E_F)}{kT} \tag{2.16}$$

Accordingly, equation 2.14 can be simplified as follows

$$dn = \frac{4\pi(2m^*)^{3/2}}{h^3}\Big(\sqrt{E - E_C}\Big)\exp\Big[(E - E_C + (E_C - E_F))/kT\Big]dE \tag{2.17}$$

Furthermore, considering the kinetic energy of the electrons in the conduction band, energy of the electron can be written as

$$E = \frac{1}{2}m^*v^2 + E_C \tag{2.18}$$

Therefore,the quantities dE and $\sqrt{E - E_C}$ can be extracted from the above equation as follows.

$$dE = m^*vdv \tag{2.19}$$

and

$$\sqrt{E - E_C} = v\sqrt{m^*/2} \tag{2.20}$$

Substituting equation 2.19 and 2.20 into the equation 2.17 gives

$$dn = 2\Big(\frac{m^*}{h}\Big)^3 \exp\Big(\frac{-qV_n}{kT}\Big) \exp\Big(\frac{-m^*v^2}{2kT}\Big)\Big(4\pi v^2 dv\Big) \tag{2.21}$$

In addition, considering $v^2 = v_x^2 + v_y^2 + v_z^2$, $4\pi v^2 dv = dv_x dv_y dv_z$ and equation 2.21, $J_{s\to m}$ can be written as follows

$$J_{s\to m} = \Big(\frac{4\pi q m^* k^2}{h^3}\Big)T^2 \exp\Big(-qV_n/kT\Big) \exp\Big(\frac{-m^*v_{ox}^2}{2kT}\Big) \tag{2.22}$$

where v_{ox} is the minimum velocity required to surmount the barrier, which can be calculated by considering the energy conservation as follows.

$$\frac{1}{2}m^*v_{ox}^2 = q(V_{bi} - V) \tag{2.23}$$

where V_{bi} is the built in potential (see figure 2.4). Accordingly, current density of semiconductor to metal can be simplified as follows.

$$J_{s\to m} = \Big(\frac{4\pi q m^* k^2}{h^3}\Big)T^2 \exp\Big(-(E_c - E_F + qV_{bi})/kT\Big) \exp\Big(\frac{qV}{2kT}\Big) \tag{2.24}$$

$$J_{s\to m} = A^{**}T^2 \exp\Big(-q\Phi_{bn}/kT\Big) \exp\Big(\frac{qV}{kT}\Big) \tag{2.25}$$

where $q\Phi_{bn}$ is the Schottky barrier hight which equals to the $E_c - E_F + qV_{bi}$ (see figure 2.4) and $A^{**} = \frac{4\pi q m^* k^2}{h^3}$ is the effective Richardson constant.

The barrier height remains the same for electrons moving from metal into semiconductor, (in other words current flowing is unaffected by the applied voltage) and current density for metal to semiconductor $J_{m\to s}$ can be obtained by setting $V = 0$ in equation 2.25 as follows

$$J_{m\to s} = -A^{**}T^2 \exp(-q\Phi_{bn}/kT) \tag{2.26}$$

Then, total current density is given by

$$J_n = J_{s\to m} + J_{m\to s} = A^{**}T^2 \exp(-q\Phi_{bn}/kT)\Big[\exp(\frac{qV}{kT}) - 1\Big] \tag{2.27}$$

$$J_n = J_{st}\Big[\exp(\frac{qV}{kT}) - 1\Big] \tag{2.28}$$

where

$$J_{st} = A^{**}T^2 \exp(-q\Phi_{bn}/kT) \tag{2.29}$$

2.1.4 Depletion capacitance with applied bias

Considering the applied bias, depletion width (W) (equation 2.11) can be written in the form

$$W = \sqrt{\frac{2\epsilon_s(V_{bi} - V - \frac{kT}{q})}{qN_D}} \tag{2.30}$$

Accordingly, expressions for the space charge per unit area of the semiconductor (Q_{sc}) and depletion layer capacitance C per unit area can be written as follows,

$$Q_{sc} = qN_D W = \sqrt{2qN_D(V_{bi} - V - \frac{kT}{q})} \tag{2.31}$$

$$C \equiv \frac{|\partial Q_{sc}|}{\partial V} = \sqrt{\frac{q\epsilon_s N_D}{2(V_{bi} - V - \frac{kT}{q})}} = \frac{\epsilon_s}{W} \tag{2.32}$$

2.2 Electronic characterization of metal-β-Ga_2O_3 interface

Herein, we report current-voltage and capacitance-voltage measurements based device characterization of the metal(Al, Mo, Au, Ni)-β-Ga_2O_3 contacts. The sample used in this work was diced from a 2 inch diameter, 680 μm thick, $(\bar{2}01)$ oriented *n*-type (UID Si-doped, 2.8×10^{17} cm^{-3}) single crystal $\beta-Ga_2O_3$ wafer grown by the edge-defined film-fed growth (EFG) method[4].

Initial investigation of edge-defined film-fed grown(EFG) $\beta-Ga_2O_3$ crystals

Prior to SBDs fabrication surface roughness, elemental composition and crystal quality was investigated on EFG grown $\beta-Ga_2O_3$ single crystal sample. Figure 2.5 shows atomic force microscopy (AFM) image, X-ray photoelectron spectroscopy (XPS) spectra, transmission spectra and secondary-ion mass spectrometry (SIMS) analysis on $\beta-Ga_2O_3$ crystal substrate. AFM scan shows an almost atomically smooth surface with RMS roughness of $\sim$ 0.3 nm. XPS spectra on substrate surface shows Ga: 32.9 at% and O: 50.1 at% elemental composition. Accordingly, calculated Ga:O stoichiometry is 2:3, which is consistent with the material composition. Transmission spectra shows the weakest absorption point around 260 eV (E(eV)=1240/λ(nm), $\sim$ 4.76 eV), which is consistent with reported bandgap of $\beta-Ga_2O_3$ 4.3 eV-4.9 eV. SIMS analysis result shows that $\sim 10^{18}$ cm^{-3} Si impurity in these samples, as expected.

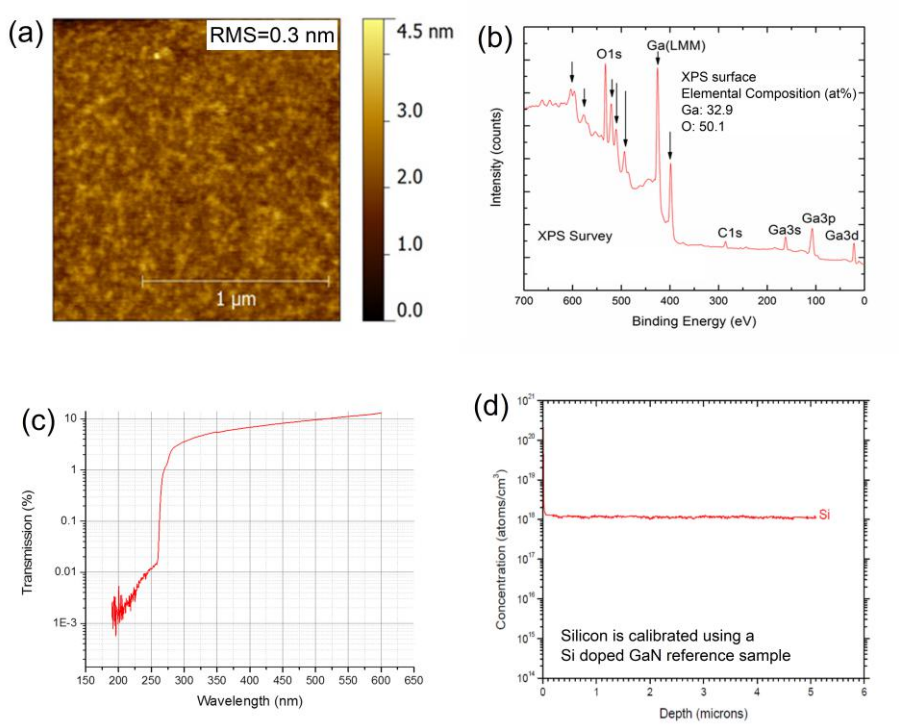

Figure 2.5: (a) AFM image of $(\bar{2}01)\beta$-Ga_2O_3 surface (b) XPS spectra of $(\bar{2}01)\beta$-Ga_2O_3 surface. XPS analysis was performed by Dr. M. Bozack from Physics Department. (c) Transmission spectra of $(\bar{2}01)\beta$-Ga_2O_3 substrate. Transmission spectroscopy analysis was performed by Dr. A. M. Armstrong at Sandia National lab. (d) SIMS analysis of β-Ga_2O_3 substrate. The Si was calibrated using a Si doped GaN reference sample. SIMS analysis was performed by Dr.V. Chia at Balazs^{TM} NanoAnalysis.

Experimental methods

The square pieces (5 mm$\times$5 mm) were first cleaned and circular patterns of 300 μm diameter thin film of metal (Al, Mo, Au, Ni) with average thickness of $\sim$ 100 nm was deposited as metal contact by following the mask alignment, photolithography, DC sputtering and lift off process. Detailed process steps are given in Appendix B. Large area ohmic contact was formed by depositing about $\sim$100 nm of Titanium (Ti) on the backside. Here Ti was chosen as the back Ohmic contact due to the small work function (4.33 eV) and reported work in the literature [5]. The sample was then attached to a gold plated ceramic plate by using conducting silver paint to measure the electrical properties. The current-voltage (I-V) and the capacitance-voltage

(*C*-*V*) characteristics of the diodes were measured at room temperature using a Keithley 6517 electrometer/high resistance system and using a Keithley 590 CV analyzer, respectively. Furthermore, temperature dependant characterization of Ni SBDs was performed by carrying out *I*-*V* measurements from room temperature to 373 K using a Keithley 6517 electrometer/high resistance system and low temperature (85-300 K) *I*-*V* and *C*-*V* measurements under vacuum (2.0×10^{-4} Torr) using cryogenic probe station using a Keithley 4200 parameter analyzer.

Room temperature electronic characterization of metal-($\bar{2}01$)β-Ga_2O_3 interfaces

Figure 2.6 (a) shows cross-sectional schematic of the Schottky diode with its equivalent circuit. The room temperature current density-voltage (*J*-*V*) characteristics of metal-β-Ga_2O_3 contacts fabricated with Al, Mo, Ni, Au are shown in figure 2.6 (b).

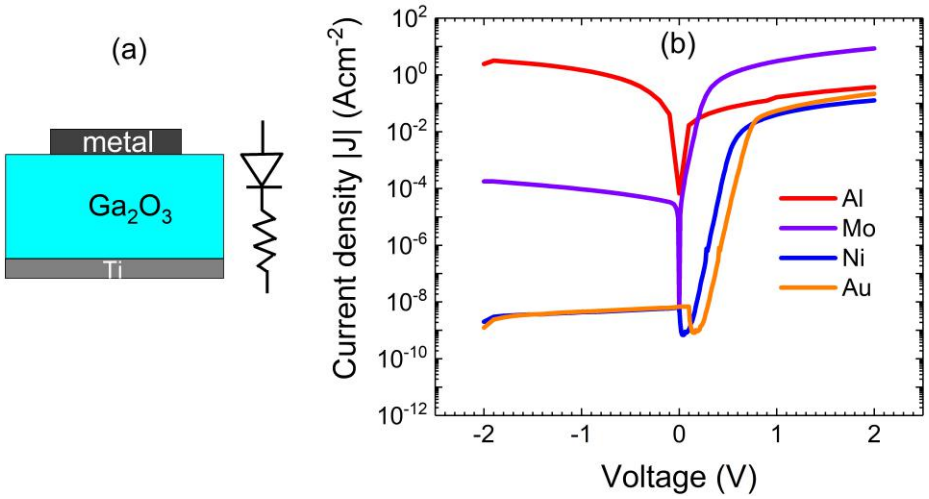

Figure 2.6: (a) Cross-sectional schematic illustration of metal-β-Ga_2O_3 contact and equivalent circuit for electrical characterization. (b) Typical |*J*|-*V* characteristics of Al, Mo, Ni and Au SBDs at room temperature.

It was found that Al-β-Ga_2O_3 contact shows Ohmic (non-rectifying) behavior and while the other metal contacts show rectifying behavior. Therefore, SBDs analysis was carried out only for Mo, Ni, and Au contacts. The analysis as follows: Assuming that thermionic emission is the dominant current transport mechanism in the device[2], and taking into account the effect of series resistance $R_s(cm^2)$, for $V \gg$3kT/q, the diode equations 2.28 can be rewritten as follows[8]

$$J = J_s \exp\{q(V - JR_s)/nkT\} \tag{2.33}$$

$$J_s = A^{**}T^2 \exp\{-q\Phi_{bn}^J/kT\} \tag{2.34}$$

The effective Richardson constant A^{**} was calculated to be 41.04 $\text{Acm}^{-2}\text{K}^{-2}$ at room temperature, using electron effective mass $m = 0.342m_o$ [9], and free electron Richardson constant A^* = 120 $\text{Acm}^{-2}\text{K}^{-2}$ [2]. Fitting thermionic emission model to the linear range of the semi-log plot of J versus V, values for barrier height ($q\phi_{bn}^J$) and ideality factor (n) of the Schottky barrier diode (SBD) was determined according to equations 2.35 and 2.36 [2].

$$q\Phi_{bn}^J = kT \ln(A^{**}T^2/J_s) \tag{2.35}$$

$$n = (q/kT)\frac{dV}{d(\ln J)} \tag{2.36}$$

Furthermore, the series resistance $R_s(\Omega cm^2)$ was obtained by using the slope of plot of $dV/d(\ln J)$ vs. *J* according to the equation 2.37.

$$\frac{dV}{d(\ln J)} = R_s J + n\frac{kT}{q} \tag{2.37}$$

The parameters extracted from the room temperature current-voltage measurements are shown in table 2.1.

In addition, room temperature *C-V* measurements were also used to obtain the barrier height ($q\phi_{bn}^C$) as shown in figure 2.7. Using the capacitance per unit area (C) in the reverse bias voltage *V* (see inset of figure 2.7), Schottky barrier height ($q\phi_{bn}^C$) and dopant concentration (N_D) were extracted from capacitance voltage measurements according to[2]

$$\frac{1}{C^2} = \frac{2}{q\epsilon_s N_D}\left(q\phi_{bn}^C - V - (E_C - E_F) - \frac{kT}{q}\right) \tag{2.38}$$

where ϵ_s, E_C and E_F are the semiconductor permittivity, energy of conduction band minima and Fermi energy at thermal equilibrium respectively. The value used for the dielectric constant of β-Ga_2O_3 was 10.2 [10]. The Fermi level was calculated from the following equations[2].

$$E_C - E_F = kT \ln \frac{N_C}{n_e} \tag{2.39}$$

$$N_C = 2\left(\frac{2\pi m^* kT}{h^2}\right)^{3/2} \tag{2.40}$$

where n_e, N_C, and h are extrinsic carrier density of semiconductor, effective density of sates of the conduction band, and Plank's constant respectively. The extrinsic carrier density of semiconductor (n_e) was assumed to be equal to donor impurity density N_D which was extracted from *C*-*V* measurements.

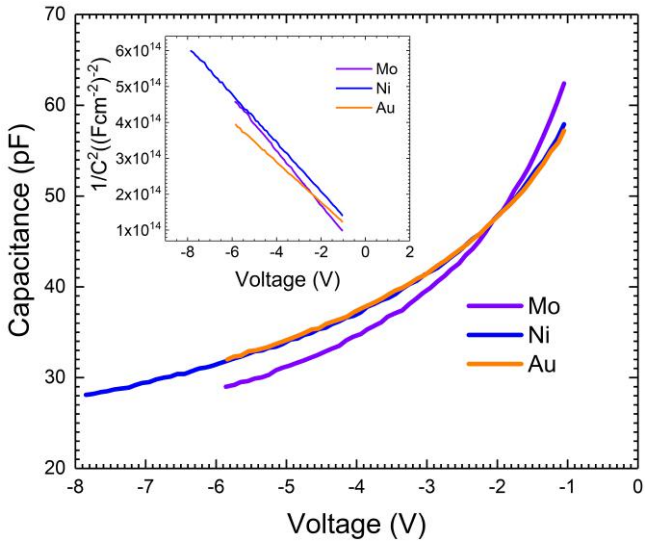

Figure 2.7: *C*-*V* characteristics of Mo, Ni and Au SBDs at room temperature. The inset shows $1/C^2$-*V* plot of SBDs at room temperature.

The *C*-*V* obtained results for ϕ_{bn}^C and N_D are shown in table 2.1. It was observed that at room temperature the experimental barrier heights closely agreed with theoretical values calculated by the Schottky-Mott rule (equation 2.1) using an electron affinity of 4.0 eV [6] for β-Ga_2O_3.

meatal	$q\Phi_m$	Ideal		*J-V*			*C-V*
		$q\Phi_{bn}^{id}$	n	$q\Phi_{bn}^{J}$	R_s	$q\Phi_{bn}^{C}$	N_D
	(eV)	(eV)		(eV)	(Ωcm^2)	(eV)	cm^{-3}
Al	4.06∼4.26	∼0.16	-	-	-	-	-
Mo	4.36∼4.95	∼0.65	1.04	0.66	0.23	0.38	1.97×10^{17}
Ni	5.04∼5.36	∼1.2	1.08	1.02	10.5	1.12	1.97×10^{17}
Au	5.1∼5.47	∼1.28	1.15	1.14	6.15	1.22	2.3×10^{17}

Table 2.1: Metal work function $q\Phi_m$, Ideal Schottky barrier height $q\Phi_{bn}^{id}$, Ideality factor *n*, *J-V* extracted Schottky barrier height $q\Phi_{bn}^{J}$, series resistance R_s ,*C-V* extracted Schottky barrier height $q\Phi_{bn}^{C}$ and extracted donor impurity density N_D for SBDs with different metal contacts at room temperature.

2.3 Temperature dependent electronic characteristics of Ni/β-Ga_2O_3 Schottky diode

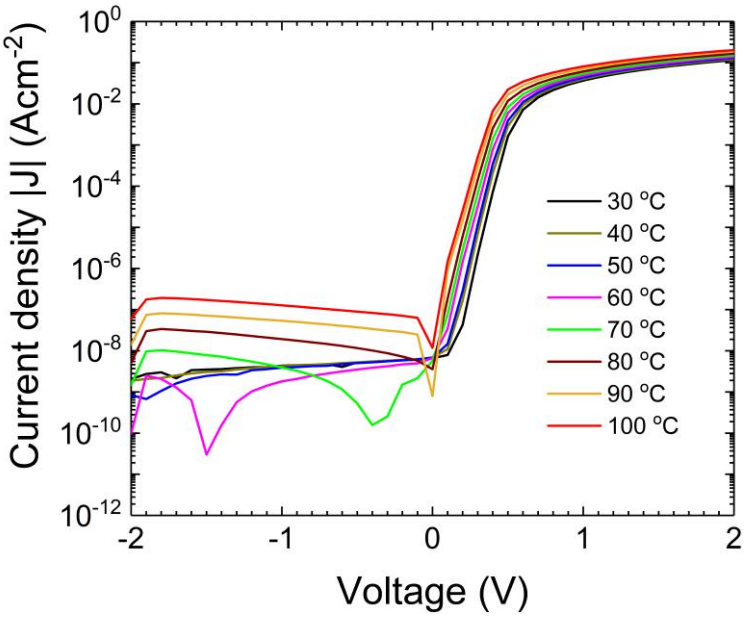

Figure 2.8: *I-V* measurements of Ni/$\beta-Ga_2O_3$ Schottky diodes in the temperature range from 30 °C to 100 °C.

Figure 2.8 shows temperature dependent *I-V* measurements of Ni/$\beta-Ga_2O_3$ Schottky diodes in the temperature range from 30 °C to 100 °C. Assuming that the effective Richardson constant (A^{**}) and the barrier height to be temperature-independent for a limited range of temperature, the slope and y axis intercept of the Richardson plot (Figure2.9) yields the Schottky barrier

height and the effective Richardson constant respectively[2, 3]. Accordingly, $q\phi_{bn}$ was determined to be 1.02 eV and extracted effective Richardson constant (A^{**}) to be 42.96 Acm^{-2}K^{-2}, in close agreement with the values extracted from room temperature *J*-*V* and *C*-*V* measurements.

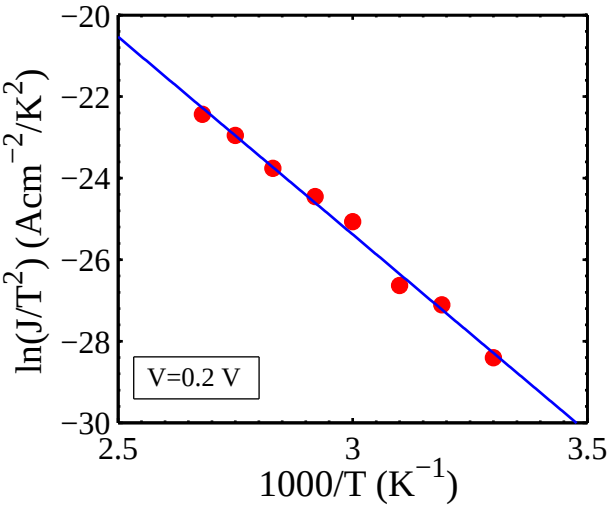

Figure 2.9: Richardson plot for the Ni/β-Ga_2O_3 Schottky barrier diode. Data extracted at V= 0.2 V in the 300 K to 373 K temperature range.

Analysis of low temperature (85 K to 292 K) *C*-*V* and *I*-*V* measurements of Ni/$\beta-Ga_2O_3$ Schottky diodes was also performed. The *C*-*V* characteristics were found to be essentially temperature independent as shown in the figure 2.10 (a). Temperature dependent *J*-*V* characteristics of the same device was shown in Figure 2.10 (b). As shown in figure 2.10 (c) strong temperature dependence of the extracted $q\phi_{bn}$ and n from the *J*-*V* curves and a large deviation from the barrier height extracted from *C*-*V* ($q\phi_{bn}^{C}$) was observed below 300 K. Furthermore, deviation of the Richardson plot from its straight line ideal behavior was also observed. Both these effects are signatures of energy barrier inhomogeneities [11] and the rest of this section presents an analysis to explain these low temperature non-idealities.

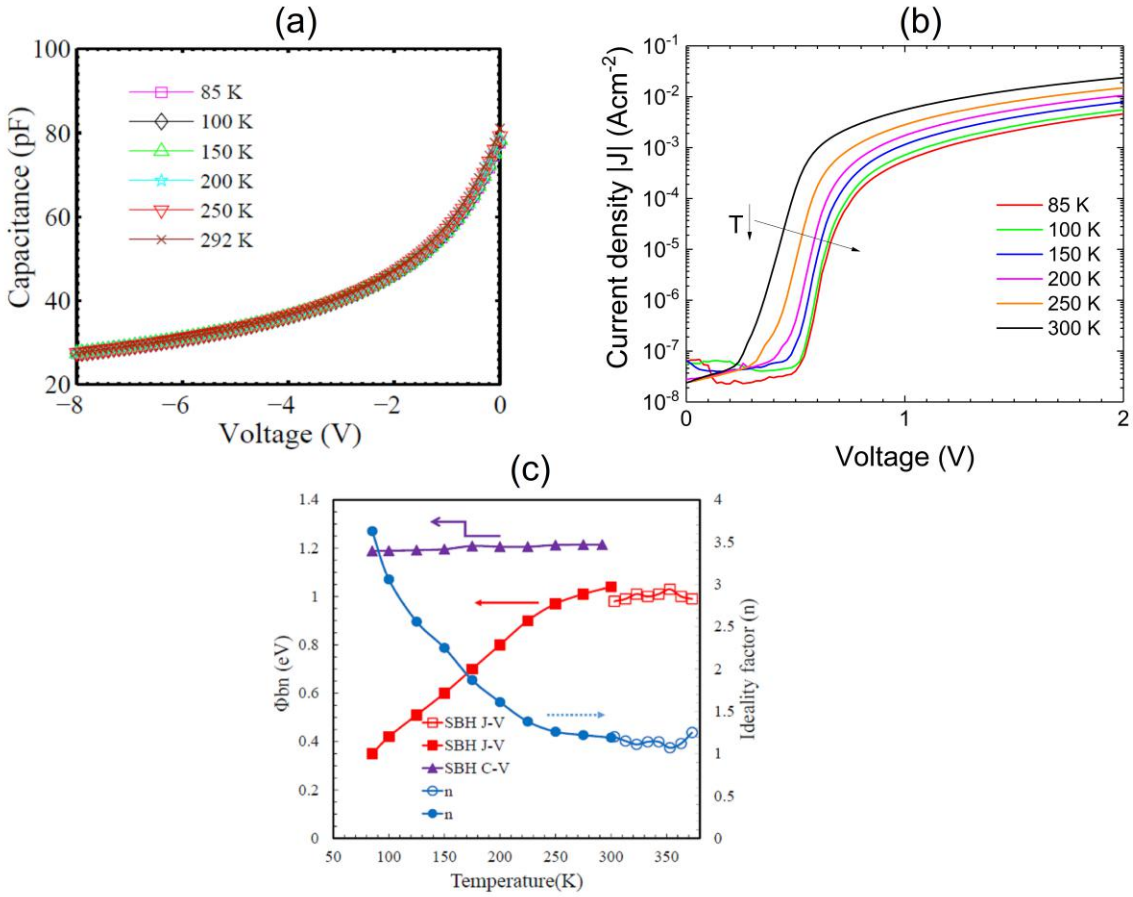

Figure 2.10: (a)C-V characteristics (b)Forward $J-V$ characteristics of Ni/β-Ga_2O_3 SBD in the temperature range of 85 K to 300 K. (c) Barrier heights and ideality factors from $J-V$ data plotted along with and barrier height from $C-V$ data for Ni/β-Ga_2O_3 SBD.

Effect of other current transport mechanisms in forward bias

In addition to thermionic emission, other main current transport mechanisms that may occur at Schottky barriers are field emission (tunneling) and thermionic-field emission. In order to establish whether the observed temperature dependence is associated with either of these mechanisms, the following analysis was carried out. The effect of thermionic-field emission can be expressed as a temperature independent effective tunneling barrier lowering which can be estimated by[1]

$$\Delta q\Phi_{tun} \approx (\frac{3}{2}qE_{00})^{2/3}(qV_d)^{1/3} \tag{2.41}$$

where E_{00} is characteristic tunneling energy which was calculated by[12]

$$qE_{00} = \frac{\hbar}{2}\sqrt{\frac{N_D}{m^*\epsilon_s}} \tag{2.42}$$

Therefore, if the low temperature non-ideality was due to tunneling, the observed barrier lowering would be of the order of $\Delta q\Phi_{tun}$. In the temperature range 85 to 220 K, $\Delta q\Phi_{tun}$ was estimated to be 0.02 eV, for V_d = 0.6 V. However, observed amount of barrier lowering (figure 2.10 (c)) is much higher, thereby invalidating thermionic field emission as the cause.

Carrier freeze-out at low temperature

In order to measure the change in free electron concentration as a function of temperature, *C-V* measurements were analyzed in the temperature range of 85 K to 300 K. As shown in figure 2.10 (c), *C-V* measurements (and therefore the extracted dopant concentrations $\sim$1.97$\times$10^{17} cm^{-3}) were insensitive to temperature which implies that effects of carrier freeze-out were negligible. It should be noted that this result is contrary to temperature dependent conductivity and Hall effect measurements [13, 14], where a temperature dependence of the electron concentration was reported.

Effect of bulk traps on forward bias current

Room temperature *C-V* measurements as a function of frequency between 10 kHz and 5 MHz for Ni/β-Ga_2O_3 SBDs (figure 2.11) indicated that no measurable amount of trap levels exists in the space charge region, which suggest the negligible influence of minority carriers on forward current transport. However, Deep level transient spectroscopy (DLTS) performed on similar devices detected a dominant deep level at $E_C-0.79$ eV with trap concentration of 2.6$\times$10^{16} cm^{-3} (see section 2.3.3), [13, 15]. Additionally, lighted capacitance-voltage (LCV) measurements on similar Schottky diodes (section 2.3.4) [7] also indicate trap concentration of 4 $\times$10^{16} cm^{-3}. While these bulk defects can cause recombination current under reverse bias and increase substrate resistivity, for forward-biases about or greater than the built-in voltage, the recombination

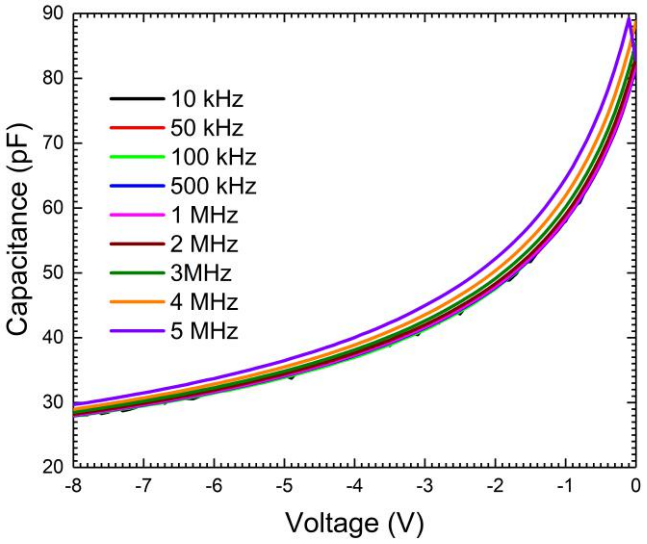

Figure 2.11: Room temperature *C-V* measurements as a function of frequency for Ni/β-Ga_2O_3 SBD.

current in the space charge layer is typically negligible compared to the diffusion current associated with the injected carriers[16].

2.3.1 Barrier inhomogeneities at Schottky metal/semiconductor interface

The increase of the ideality factors and the lowering of $q\phi_{bn}^{J}$ with decreasing temperature have been observed in other semiconductors and is typically attributed to barrier inhomogeneities at Schottky metal/semiconductor interfaces[11][17] – [31].Origin of the barrier inhomogeneity is attributed to thin interfacial layers between the metal and the semiconductor, interface defects and roughness associated with dislocations, grain boundaries and atomic steps in the metal. Different models have been used in the literature on other semiconductors [1, 2, 29, 33] to analyze the reverse current. In the forward bias regime, this behavior has been mainly described using two different models, which are: (i) the interfacial layer model[1, 2, 24, 25] where the barrier inhomogeneity is a result of interface states and their detailed energy distribution can be determined by a non-equilibrium approach model [26, 27, 28, 29, 30] and (ii) a general surface potential fluctuation model where the fluctuations are described by a Gaussian barrier distribution[11, 17, 18, 19, 20, 21, 22, 23, 31].

Interfacial layer model

Relationship of interface state densities with the ideality factor (*n*) is given by following equation [1, 2, 24]

$$n = 1 + \frac{\delta}{\epsilon_i}\Big(\frac{\epsilon_s}{W} + qD_{it}(m/s)\Big) \tag{2.43}$$

where δ, ϵ_i, ϵ_s, W and $D_{it}(m/s)$ are interfacial layer thickness, permittivity of interfacial layer, permittivity of semiconductor, zero-bias depletion width in the semiconductor and densities of interface states at the semiconductor/interfacial layer, respectively. Herein *W* was extracted from *C-V* measurements and the thickness of the interfacial layer was assumed to be δ = 2 nm. Additionally, permittivity of interfacial layer was assumed to be equal to permittivity of semiconductor (β-Ga_2O_3). From the experimental ideality factors, the average density of active interface states as a function of temperature was extracted using equation 2.43, as shown in figure 2.12. The results indicate that $D_{it}(m/s)$ increases strongly with decreasing temperature. Therefore, it is possible that the barrier inhomogeneity is a result of interface states and their detailed energy distribution. However, validity of the interfacial layer model depends on values of parameters such as thickness of the interfacial layer and dielectric constant of the interfacial layer which need to be known experimentally. Due to the unknown nature of these parameters for metal$-Ga_2O_3$ interfaces, general surface potential fluctuation model has been used to explain the low temperature characteristics.

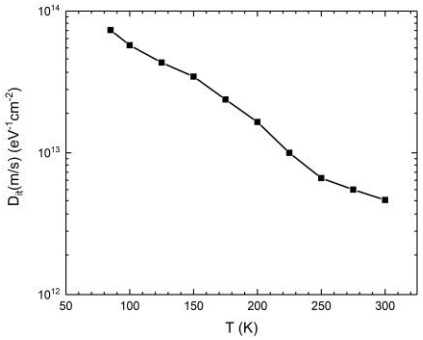

Figure 2.12: The variation of the interface state density at the semiconductor/interfacial layer ($D_{it}(m/s)$) as a function of temperature

General surface potential fluctuation model

The potential fluctuations at the interface are described by a Gaussian barrier distribution $P(\phi_{bn})$ with a standard deviation of barrier fluctuation σ_s around a mean barrier height $\overline{\phi_{bn}}$, as given below[11].

$$P(\phi_{bn}) = \frac{1}{\sigma_s\sqrt{2\pi}} e^{-(\overline{\phi_{bn}}-\phi_{bn})^2/(2\sigma_s^2)} \tag{2.44}$$

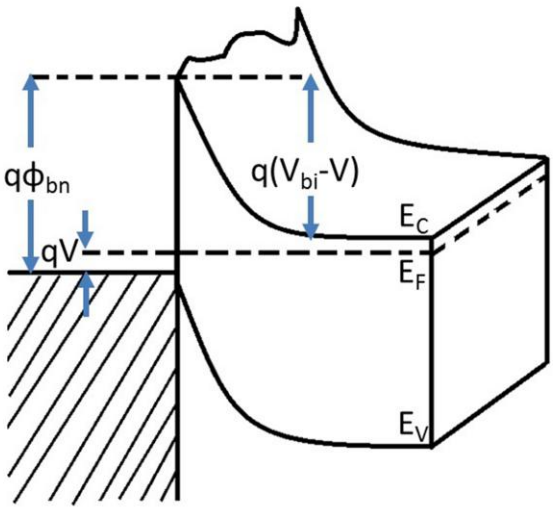

Figure 2.13: Band diagram of an inhomogeneous Schottky contact. Spatial variation of Schottky barrier and built-in potential result in different heights ϕ_{bn}^J

The schematic of potential fluctuations of the Schottky barrier is shown in figure 2.13. Based on Gaussian barrier distribution, quantitative expressions for the barrier height (ϕ_{bn}^J) and a voltage independent ideality factor (n) as a function of temperature can be written as:[11]

$$\phi_{bn}^J(V) = \overline{\phi_{bn}}(V) - \frac{q\sigma_s^2(V)}{2kT} \tag{2.45}$$

$$\frac{1}{n(T)} - 1 = -\rho_2 + \frac{q\rho_3}{2kT} \tag{2.46}$$

where $\overline{\phi_{bn}}$ is the mean barrier height as a function of bias voltage. Measure of the barrier height homogeneity is the voltage dependent standard deviation σ_s (low value of σ_s indicates a homogenous barrier height at the interface). The temperature independent voltage coefficient ρ_2

measures the sensitivity of mean barrier height $\overline{\phi_{bn}}$, and ρ_3 measures the sensitivity of standard deviation σ_s to the variation of the bias voltage. Based on equations 2.45 and 2.46, plots of $q\phi_{bn}^J$ vs $1/2kT$ and n^{-1}-1 vs $1/2kT$ should yield straight lines with slopes of σ_s^2 and ρ_3, and axis intercepts of $\overline{\phi_{bn}}$ and ρ_2, respectively. Accordingly, the surface potential fluctuation model was applied to analyze the low temperature *J-V* data as shown in figure 2.14(a) and 2.14(b). The slight deviation from the linear fit could be due to any inherent temperature dependence of the standard deviation σ_s[11]. Within the fitting error, extracted $\overline{\phi_{bn}}$, σ_s, ρ_2 and ρ_3 values for the Ni/β-Ga_2O_3 diode are shown in Table 2.2 and compared with other metal - semiconductor Schottky diodes reported in literature. The larger value of σ_s compared to the mean barrier height indicates a significantly large barrier inhomogeneity at the Ni/β-Ga_2O_3 interface.

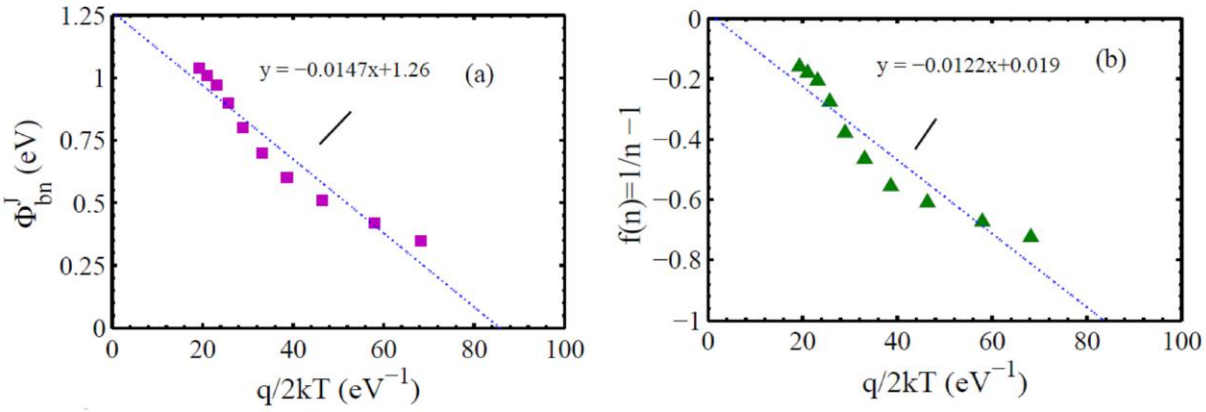

Figure 2.14: (a)Temperature dependence of the barrier height and (b) ideality factor function $f(n)$ extracted from the *J-V* curves according to equations 2.45 and 2.46 in the text.

Similar behavior of inhomogeneous barrier distribution in Pt/(100)β-Ga_2O_3 Schottky diodes has also been reported recently[32]. The barrier inhomogeneity strongly affects the low temperature current transport as the effective barrier height ($q\phi_{bn}^J$) decreases with decreasing temperature. While further experimental verification is necessary, the inhomogeneity possibly arises from defects at the metal/β-Ga_2O_3 interface.

Contact	Temperature range	$\overline{\phi_{bn}}(eV)$	$\sigma_s(meV)$	ρ_2	$\rho_3(mV)$
Ni-$(2\bar{0}1)\beta$-Ga_2O_3	85−300 K	1.26	121	-0.019	-12.2
Cu-β-Ga_2O_3[31]	50−320 K	1.32	126	0.15	-13
Pt-$(100)\beta$-Ga_2O_3[32]	125−300 K	1.27	130	-0.107	-16
PtSi/n-Si[11]	76−344 K	0.92	70	-0.11	-5.3
Sn/p-Si[18]	150−400 K	1.05	114	-0.14	-17
Ni/4H-SiC[19]	77−400 K	1.04	92	0.002	-10.6
Ni/6H-SiC[20]	77−600 K	1.86	121	0.021	-7.75
Au/Pd/n-GaN[23]	90−410 K	1.03	118	0.447	4.5

Table 2.2: Extracted mean barrier height $\overline{\phi_{bn}}$, standard deviation σ_s and voltage coefficients ρ_2, ρ_3 for Ni-$\beta-Ga_2O_3$ according to Gaussian distribution and reported values for other metal-semiconductor interfaces in the literature.

2.4 Investigation of bulk traps in the EFG growth $\beta-Ga_2O_3$ substrate by using Ni/$\beta-Ga_2O_3$ Schottky

All semiconductors contain defects. These may be crystal defects, point defects, foreign atoms (impurities) or extended defects (stacking fault, edge dislocation) [3]. These defects can affect the reliability of the devices, and increase the resistivity of the material. We investigated deep level traps in the Ga_2O_3 by using the Ni/β-Ga_2O_3 Schottky diodes with DLTS and lighted capacitance-voltage (LCV) measurements. LCV measurements and I-V curves in the dark, under 5.80 eV illumination and the responsivity (R) measurements were performed by Dr. Andrew M. Armstrong at Sandia National Laboratories, Albuquerque, New Mexico[7].

2.4.1 Capture and Emission Rates of point defect: A Mathematical description

To understand the capture and emission processes from a defect/*trap level*, we first consider a *Generation-Recombination* center ($G-R$), where an electron from conduction band is captured by the center (Figure 2.15 process a), a process which is characterized by a capture coefficient (c_n). Two possibilities for the captured electron arises : (1) electron emission (which is characterized by the emission coefficient e_n) back to the conduction band (Figure 2.15 process b) or (2) it can capture a hole from valence band (Figure 2.15 process c). Then two possibilities for hole arises (i) hole emission back to the valence band (Figure 2.15 process d) or (ii) capture an

electron from conduction band (Figure 2.15 process a). The *Trapping* event can be defined as the event, where only one of two bands and the center participate in capturing and emission[3].

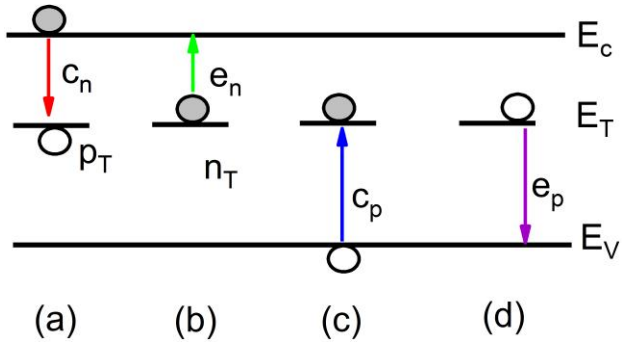

Figure 2.15: Energy band diagram for a semiconductor with generation and recombination center. (a)electron from conduction band captured by a center (b)electron emission back to the conduction band (c)capture a hole from valence band (d)emits the hole back to the valence band

The electron emission rate due to the trapping mechanism can obtain by reviewing the variation of the electron density in the conduction band [3, 34]. First, we consider an n-type semiconductor with electron trap level located ΔE_T below the bottom of the conduction band. Let N_T, n_T and n be the number of total traps, the number of occupied traps (number of electrons in the trap level E_T) and the number of electrons in the conduction band, per unit volume respectively. Change in electron density in the conduction band can expressed in terms of reduction due to the electron capture by the traps and increase due to electron emission,

$$\frac{dn}{dt} = \text{electron emission} - \text{electron capture} = e_n n_T - c_n n(N_T - n_T) \tag{2.47}$$

Electron emission depends on the density of the occupied traps n_T and the emission coefficient, e_n (s^{-1}). However, the capture process depends on a number of electrons in the conduction band (n), number of unoccupied traps ($N_T - n_T$) and the capture coefficient, c_n, (s^{-1}). Number of electrons in the conduction band, n, can be obtained by the equation below.

$$n = N_C \exp\left(\frac{-(E_C - E_F)}{kT}\right) \tag{2.48}$$

where N_c is the effective density of states in the conduction band which is given by equation 2.40. Furthermore, relationship between n_T and N_T can be obtained by considering the free energy F of the electrons on the trap level relative to conduction band by [35]

$$F = -n_T \Delta E_T - kT \ln \left\{ \frac{N_T!}{n_T!(N_T - n_T)!} \right\} \tag{2.49}$$

Equation 2.49 can further simplified by using $logx! \sim xlogx - x$,

$$F = -n_T \Delta E_T - kT \Big\{ - n_T \ln \frac{n_T}{N_T} - (N_T - n_T) \ln \frac{N_T - n_T}{N_T} \Big\} \tag{2.50}$$

Accordingly, the chemical potential $\mu \equiv E_F$ of the electrons can be derived as

$$\mu = \frac{\partial F}{\partial n_T} = -\Delta E_T - kT \Big\{ - \ln \frac{N_T}{N_T - n_T} \Big\} \tag{2.51}$$

Therefore, expression for number of occupied traps, n_T, can be obtained by using equation 2.51 as follows.

$$n_T = \frac{N_T}{1 + \exp\left(\frac{-(\Delta E_T + \mu)}{kT}\right)} = \frac{N_T}{1 + \exp\left(\frac{-(-E_T + E_F)}{kT}\right)} = \frac{N_T}{1 + \exp\left(\frac{(E_T - E_F)}{kT}\right)} \tag{2.52}$$

Considering the *Principle of Detailed Balance*, which states that "*under equilibrium conditions each fundamental process and its inverse process must self-balance independent of any other process that may be occurring inside the material*" and with the assumption of *the emission and capture coefficients remains equal to their equilibrium values under non-equilibrium conditions*, equation 2.47 can written as

$$\frac{dn}{dt} = 0 = e_n n_T - c_n n(N_T - n_T) \tag{2.53}$$

Furthermore, combining the equations 2.48 and 2.52 gives

$$\begin{aligned} e_n n_T = c_n n(N_T - n_T) &= c_n n\left(n_T + n_T \exp\left(\frac{E_T - E_F}{kT}\right) - n_T\right) \\ &= c_n N_C \exp\left(\frac{E_T - E_F}{kT}\right) \exp\left(\frac{-(E_C - E_F)}{kT}\right) \\ &= c_n N_C \exp\left(\frac{-(E_C - E_T)}{kT}\right) \end{aligned} \tag{2.54}$$

With $e_n = 1/\tau_n$ and $c_n = \sigma_n \upsilon_{th}$, the trap emission time constant, τ_n, is

$$\tau_n = \frac{\exp\Big((E_C - E_T)/kT\Big)}{\sigma_n \upsilon_{th} N_C} \tag{2.55}$$

and the trap emission coefficient(emission rate) is

$$e_n = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-(E_C - E_T)}{kT}\right) \tag{2.56}$$

where σ_n and υ_{th} are the *electron capture cross sections* and the *electron thermal velocity* ($\upsilon_{th} = \sqrt{3kT/m_e^*}$), respectively. A similar expression for hole emission can be analogously derived as

$$\tau_p = \frac{\exp\Big((E_T - E_V)/kT\Big)}{\sigma_p \upsilon_{th} N_V} \tag{2.57}$$

where σ_p and N_V are the *hole capture cross section* and *density of states in the valence band*. Equation 2.56 is the fundamental equation for analysis of DLTS measurements in this thesis, as discussed below.

2.4.2 Introduction to Deep-Level Transient Spectroscopy (DLTS)

Deep-Level Transient Spectroscopy (DLTS) is a very important technique which can be used to detect the traps in semiconductors by using capacitance transients.[36] The important feature of the DLTS is the capability to set an emission rate window such that the spectrometer only responds when it sees a transient with a rate within this rate window. The emission rates of the traps are thermally activated as shown in equation 2.56. The fundamental idea is that thermal

emission from traps having a single energy level decays exponentially in time, and therefore the corresponding transient decays exponentially. Thus, if the emission rate of the trap varied by changing the sample temperature, the spectrometer shows a response peak at the temperature where the trap emission rate within the rate window of the spectrometer.

Time-varying exponential capacitance transient $C(t)$ can be written as [3].

$$C(t) = C_0\Big[1 - \Big(\frac{n_T(0)}{2N_D}\Big)\exp\Big(-\frac{t}{\tau_n}\Big)\Big] \tag{2.58}$$

Here the temperature dependence of τ_n is given by equation 2.55, C_0 is the capacitance of the device with no deep-level traps and $n_T(0)$ is the initial steady-state density given by equation 2.52. Therefore, DLTS signal (capacitance transient measured at two different time) can be written as follows (see Appendix C for detail derivation)

$$S(T) = C(t_1) - C(t_2) = C_0\frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{t_2}{\tau_n}\Big) - \exp\Big(-\frac{t_1}{\tau_n}\Big)\Big] \tag{2.59}$$

When DLTS spectra shows a peak (maximum or minimum) at temperature *T*, emission rates (e_n) of the traps will be equal to rate window of the spectrometer(τ_{max}^{-1}). Set values of t_1 and t_2 in spectrometer determine the rate window of the spectrometer. Therefore, relationship between τ_{max} and t_1 and t_2 is derived by finding the maximum (or minimum) for $S(T)$ (differentiating $S(T)$ with respect to τ_n and setting the result equal to zero).

$$\begin{gathered}
\tfrac{dS(T)}{d\tau_n} = 0 \\
C_0\tfrac{n_T(0)}{2N_D}\Big[-t_2(-1)\exp\Big(-\tfrac{t_2}{\tau_{max}}\Big) - -t_1(-1)\exp\Big(-\tfrac{t_1}{\tau_{max}}\Big)\Big] = 0 \\
t_1\exp\Big(-\tfrac{t_1}{\tau_{max}}\Big) = t_2\exp\Big(-\tfrac{t_2}{\tau_{max}}\Big) \\
\exp\Big(\tfrac{(t_2-t_1)}{\tau_{max}}\Big) = \tfrac{t_2}{t_1} \\
\tfrac{(t_2-t_1)}{\tau_{max}} = \ln\Big(\tfrac{t_2}{t_1}\Big) \\
\tau_{max} = \tfrac{t_2-t_1}{\ln(t_2/t_1)}
\end{gathered} \tag{2.60}$$

Thus, the emission rate corresponding to the maximum of a trap peak observed in a DLTS spectra is a precisely defined quantity. An schematic of capacitance transient monitored as a function of temperature is shown in figure 2.16.

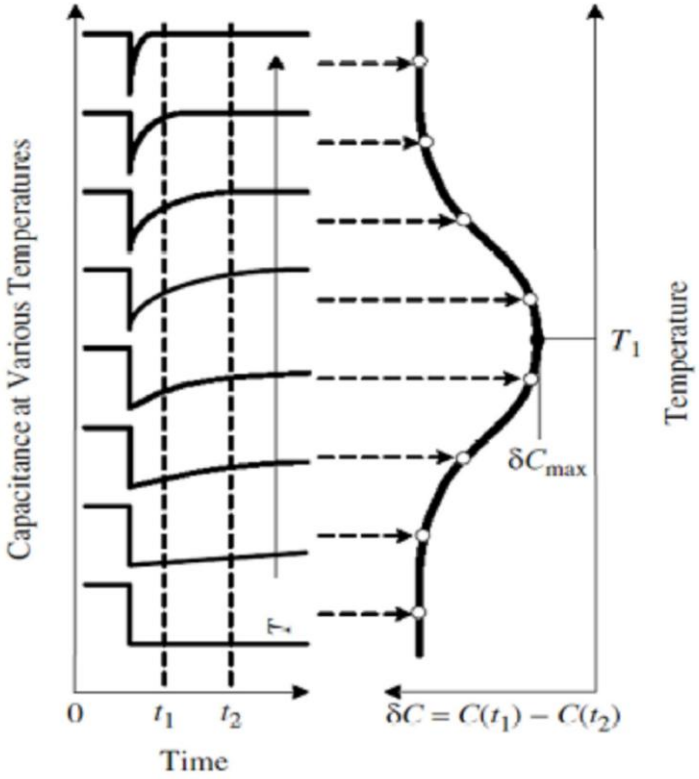

Figure 2.16: The left-hand side shows capacitance transients at various temperatures, while the right-hand side shows the corresponding DLTS signal resulting from the difference between the capacitance at time t_1 and the capacitance at time t_2 as a function of temperature.[3].

2.4.3 DLTS measurements of Ni/$\beta-Ga_2O_3$ Schottky diode

For the DLTS measurements made here, reverse voltage was applied to the SBD diode to hold the device in depletion mode. A 25 ms trap filling voltage pulse (V_P) was periodically applied to charge and discharge the traps. Throughout the charging pulse, traps will be filled with electrons and followed by thermally emitting to the conduction band (figure 2.17). This trapping and de-trapping due to the applied pulse causes a change of depletion layer width and the time variation of capacitance. Herein, the capacitance transient after the filling pulse was monitored as a function of temperature and measured at two different times t_1 and t_2, with $t_2 = 2.5t_1$, which determined the spectrometer rate window (τ_{max}^{-1}). The resulting DLTS signal, $\Delta C = C(t_1) - C(t_2)$, is a maximum when the emission rate of the traps, e_n, is equal to the spectrometer rate window (τ_{max}^{-1}) as it explained in the section 2.3.2.

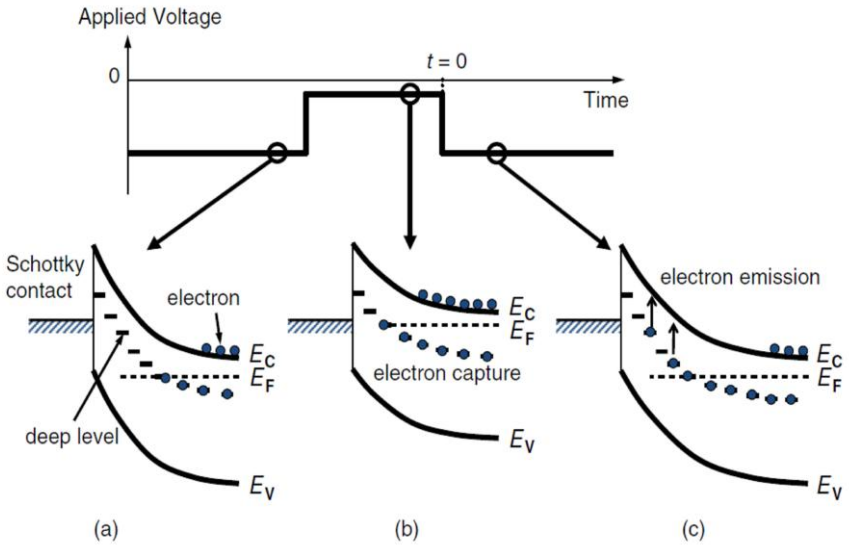

Figure 2.17: Typical bias voltage sequence that is applied during DLTS measurements of an *n*-type semiconductor (Schottky structure), along with the energy band diagrams, which correspond to (a) the steady state under a reverse bias voltage, (b) during application of a pulse voltage, and (c) after application of the pulse voltage, respectively.[39]

DLTS spectra of a Ni/$\beta-Ga_2O_3$ Schottky diode for temperature range from 200 K to 500 K are shown in figure 2.18 (a). The spectra show one major peak, which arises from a dominant deep level electron trap. The activation energy ($E_C - E_T$) and the capture cross section (σ_n) of this trap level were determined from the slope and intercept of the Arrhenius plot of $\ln(\tau_n T_2)$ vs. 1000/T (Figure 2.18 (b)), respectively, where T is the temperature of the DLTS peak[3, 37, 38]. Results were $E_C - E_T$ =0.77 eV and $\sigma_n = 2.8\times10^{-15}$cm^2.

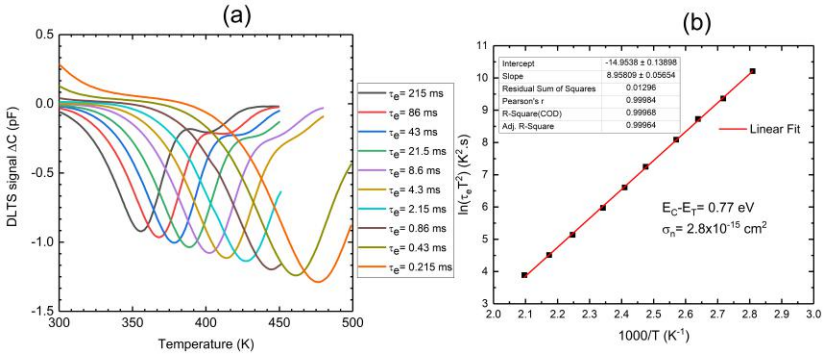

Figure 2.18: (a)DLTS spectra of Ni/$\beta-Ga_2O_3$ Schottky diode for temperature range from 200 K to 500 K with constant voltage(V_R)=-5 V and filling pulse(V_P)=0 V.(b)Arrhenius plot for the DLTS peak seen in (a).

The trap concentration, N_T ,was calculated from the corresponding DLTS peak amplitude (ΔC). The N_T value can be found by using the equation(see Appendix C for detail derivation)[3, 37],

$$N_T = \frac{3 \cdot 2 \cdot N_D \cdot \Delta C}{C_o(V_R)} \left(\frac{W_R^2}{\Big(W_R - \lambda(E_T)\Big)^2 - \Big(W_P - \lambda(E_T)\Big)^2} \right) \tag{2.61}$$

where the factor of 3 arises from the sampling times, t_1 and t_2 of the capacitance transient in the DLTS spectrometer with $t_2 = 2.5t_1$ (see Appendix C for detail derivation). $C_o(V_R)$ is corresponding capacitance for constant voltage V_R. W_P is the depletion layer width during the filling pulse and W_R is the depletion layer width for constant voltage. $\lambda(E_T)$ is the width of the transition region at the edge of the depletion region, where traps at E_T are filled with electrons, which is given by[38]

$$\lambda(E_T) = \sqrt{\frac{2 \cdot \epsilon_{rs}\epsilon_o\Big(E_T - E_F)\Big)}{qN_D}} \tag{2.62}$$

where q is the elementary charge, ϵ_{rs} is relative dielectric constant, ϵ_o is the vacuum permittivity 8.8×10^{14} Fcm^{-1}, E_F is the position of the Fermi level from bottom of the conduction band at the temperature of the DLTS peak and E_T is the trap energy level from the bottom of the conduction band edge. Calculated trap concentration (N_T) for the $E_C - E_T$ =0.77 eV trap in the $(\bar{2}01)\beta-Ga_2O_3$ is 2.6$\times$10^{16} cm^{-3}. These results are consistent with the recent studies of DLTS on both (010) and ($\bar{2}$01) oriented EFG grown β-Ga_2O_3 materials [13, 15, 40, 41] where these defect has been identified as an extrinsic defect attributed to the Fe impurities in the bulk crystals[41]. In this work [41] it was shown that upper bandgap of MBE and HVPE grown epitaxial films are free from the Fe related E_2 deep level trap. While improvement of defect free crystal growth is an absolute necessity for the further development of this technology, relatively clean upper bandgap in the epitaxy layers are encouraging for β-Ga_2O_3 future device applications.

2.4.4 Lighted Capacitance-Voltage(LCV)measurements and Solar-blind Photoconductivity gain of Ni/β-Ga_2O_3 Schottky diodes

We have used DLTS measurements for bulk trap investigation in the upper half of the band gap (0.15 eV to $\sim$ 1.0 eV) of the EFG grown β-Ga_2O_3. Investigating the energetically deeper traps (below 1.0 eV) requires UV assisted measurements such as lighted capacitance-voltage measurements (LCV) or deep level optical spectroscopy DLOS measurements. In this regard, LCV measurements and photo responsivity measurements were performed by Dr. Andrew M. Armstrong at Sandia National Laboratories, Albuquerque, New Mexico[7] on SBDs fabricated on this work.

Herein, N_t was calculated by comparing the *C-V* characteristics in the dark and under photo illumination. First, *C-V* characteristics were performed in the dark and then LCV sweeps were taken under sub-band gap illumination (4.5 eV) (Figure 2.19(a)). The difference between N_D extracted from two *C-V* has been use to extract N_t value by using the following equation.

$$[N_D - N_t]W = -\frac{C^3}{q\epsilon_s(dC/dV)} \tag{2.63}$$

where N_D is the ionized donor density, *C* is the capacitance per unit area, *q* is the Coulomb charge, ϵ_s is the semiconductor permittivity, *V* is the applied voltage and *W* is the depletion width given as in equation 2.32. The difference between the space-charge profiles in Figure 2.19(b) indicates a net N_t of 4.0×10^{16} cm $^{-3}$. LCV and DLTS measured N_t values shows same order of magnitude. Therefore, it can be assumed that major trap in the EFG grown β-Ga_2O_3 is arising from the Fe impurities in these bulk substrates.

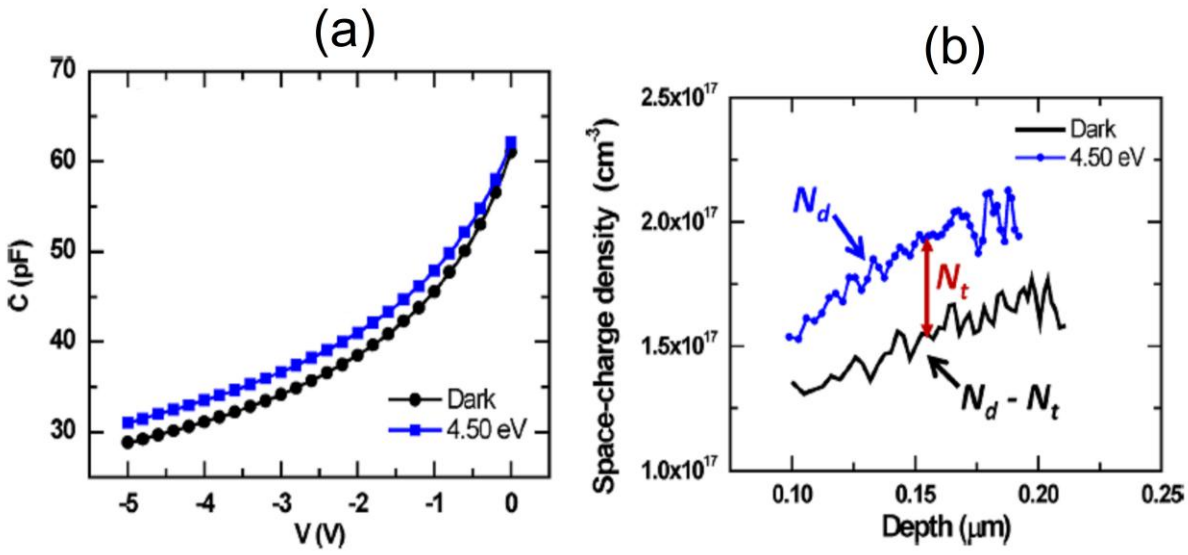

Figure 2.19: (a) Dark and lighted capacitance-voltage data measured for the Schottky diode.(b)Net doping density calculated from the capacitance-voltage and lighted capacitance-voltage data from Figure 2.19. The net defect density is the difference between the space-charge density in the dark and under 4.50 eV illumination[7]. Measurements were performed by Dr. Andrew M. Armstrong at Sandia National Laboratories, Albuquerque, New Mexico

Photoconductive gain was determined from the responsivity (R) of the diodes, where responsivity was measured as the electrical output per optical input. Responsivity was calculated as

$$R = \frac{\Delta I}{q\phi A h\nu} \tag{2.64}$$

where ΔI is the steady-state increase in the current under illumination, ν is th frequency of the optical signal, A is the device area, h is the Plank's constant and ϕ is the photon flux. Figure 2.20 (a) shows the reverse bias I-V curves of the Schottky diode taken in the dark and under 5.80 eV illumination. Figure 2.20 (b) shows the calculated photo responsivity (R) of a Schottky diode biased at -20 V and illuminated with light ranging from the IR to UV-C wavelengths [7]. As shown in figure 2.20 (a), these devices showed excellent rectification and low reverse leakage current in dark condition. However, large photoresponse was found when

illuminated at 5.80 eV . This illumination procedure has been carried out with forward bias also and no significant photocurrent was found at forward bias $I - V$.

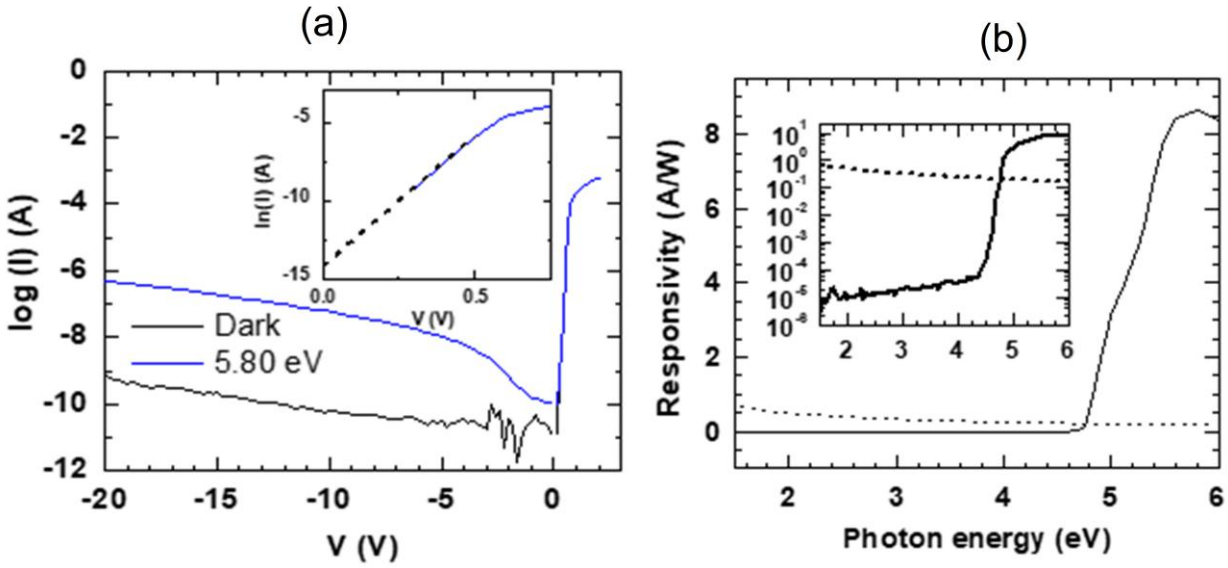

Figure 2.20: (a) Schottky diode $I-V$ measurements in the dark and under 5.80 eV illumination conditions. Large photoresponsivity is observed only for reverse bias. The inset shows the semi-log plots of forward $I - V$ characteristics for both illumination conditions,which are unaffected by illumination. (b) Responsivity of the Schottky diode at -20 V. The diode shows excellent solar rejection ratio $> 10^5$ for $h\nu < 4.4$ eV ($\lambda >$280 nm) relative to $h\nu > 5.63$ eV ($\lambda <$220 nm). The inset shows the same data re-plotted on a logarithmic scale for the y-axis to better show the magnitude of solar rejection. Photoconductive gain is observed for $h >$ 4.70 eV[7]. Measurements were performed by Dr. Andrew M. Armstrong at Sandia National Laboratories, Albuquerque, New Mexico

The observed photoresponse in reverse bias and strong photoconductive gain for illumination above the band gap of the β-Ga_2O_3 have been attributed to the self-trapping of holes (STH) in the valence band. STHs formation of this class of material can be explained as follows. When the lattice has a strong electron-phonon coupling, local distortion of the lattice ion positions can be initiated by holes in the valence band. This distortion in lattice produces an electrostatic potential which spatially localizes the hole[7, 42, 43]. Therefore, when Photo illumination above-bandgap of β-Ga_2O_3 creates electron-hole pairs in the depletion region near the

metal-β-Ga_2O_3 interface, holes become self-trapped. These self trapped holes remain in the space-charge region near the interface and produce an excess positive space-charge sheet. This positive charge sheet causes barrier height lowering. Therefore, electron can easily flow from metal to semiconductor and results in the high leakage current (strong photoconductive gain for $h\nu > 4.7$ eV).

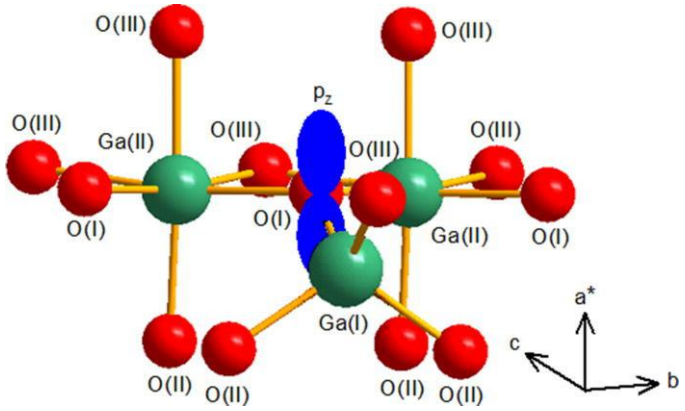

Figure 2.21: Model of the STH in β-Ga_2O_3. The unpaired spin (the hole) is localized in a O 2p orbital on a threefold oxygen ion O(I).[43]

Theoretical calculations have shown that the hole can be localized in a O 2p orbital on one oxygen ion and form a self-trapped hole (STH)[42, 43]. Figure 2.21 shows the proposed model for the STH in β-Ga_2O_3 [43]. Kananen et al.[43] proposed that small shifts in the position of the neighboring Ga(I) ion by moving away from the O(I) ion causes a lattice distortion and form the STH.

Accordingly, if accepter impurities are introduced to create holes, they are also likely to be trapped as these UV light generated holes. Therefore, the flat valance band structure with the large effective hole mass and the tendency to form localized polarons (self-trapped holes) due to the orbital composition of the valence band [42, 43, 44, 45] will be an insurmountable obstacle to the achievement of *p*-type conductivity in β-Ga_2O_3.

2.5 Summary

To summarize, fundamentals of forward bias current transport mechanism and depletion capacitance of Schottky diode has been discussed and electrical characteristics of Schottky barrier diodes with metal contacts on $(\bar{2}01)$ $\beta-Ga_2O_3$ have been investigated. Temperature dependent

electrical measurements was carried out with Ni SBD, which revealed strong temperature dependence of the extracted barrier height and ideality factor below 273K. These observations have been explained by considering the effect of barrier inhomogeneity on low temperature current transport. Using a Gaussian potential fluctuation model, a large standard deviation of barrier fluctuation compared to the mean barrier height was observed which indicates the presence of large barrier inhomogeneity at Ni/$\beta-Ga_2O_3$ interface. Furthermore, Ni/$\beta-Ga_2O_3$ SBDs were used to investigate the bulk traps in $\beta-Ga_2O_3$ semiconductor. DLTS measurements on Ni/$\beta-Ga_2O_3$ SBDs revealed a majority carrier deep level trap $E_C - E_T$ =0.77 eV with concentration of 2.6×10^{16} cm^{-3}, possibly associated with Fe impurities in the crystal. In addition, strong photoconductive gain was observed for these Schottky diodes and was attributed to the self-trapping of holes (STH) in the valence band.

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Chapter 3

Fundamental of metal-oxide-semiconductor (MOS) based electronic characterization

The MOS capacitor is an important diagnostic tool to study electronic properties of dielectric-semiconductor interfaces. This device structure is key to understanding the properties metal oxide semiconductor field effect transistor (MOSFET). The most straightforward MOS structure was first proposed in 1959 as a voltage-variable capacitor by Moll[1]. Silicon-SiO_2 based MOS capacitors were first employed by Terman[2], Lehovec and Slobodskoy[3]. Furthermore, Si-SiO_2 based field effect transistors were first demonstrated by D.Kahng, and M. M. Atalla[4] in 1960.

In this chapter, we will comprehensively discuss MOS capacitor fundamentals, specific bias regions, interface traps, interface trap investigation techniques and lateral MOSFETs fundamentals.

3.1 MOS capacitor fundamentals

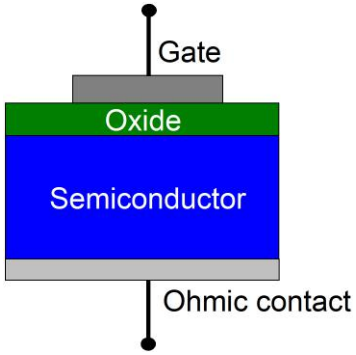

Figure 3.1: The metal-oxide-semiconductor capacitor

The MOS capacitor consists of a sufficiently thick metallic layer called *gate* , a thin insulating film(*oxide*), *semiconductor* and back *ohmic* contact. Such a structure is shown in Figure 3.1.

3.1.1 Energy-band diagram at thermal equilibrium

Figure 3.2 (a) shows the energy band diagrams for the individual components of the MOS structure. At thermal equilibrium, Fermi level is constant throughout all three-components (the metal, the oxide, and the semiconductor in figure 3.2(b)). However, work function difference between metal and semiconductor causes band bending inside the semiconductor (figure 3.2 (b)). Furthermore, work function difference ($q\phi_m > q\phi_s$) causes negative charges to move from the metal into the direction of the semiconductor[5, 6, 7]. However, there will be no carrier transport through the oxide. Therefore, negative charge will be gathered as a thin sheet of negative charge at the surface of the metal[5, 6, 7]. According to the Gauss's law, the charges within the structure must sum to zero. Charge balance of the system will occur by the positive charge ionized donors of the semiconductor, which extends into the semiconductor from its surface[5, 6, 7].

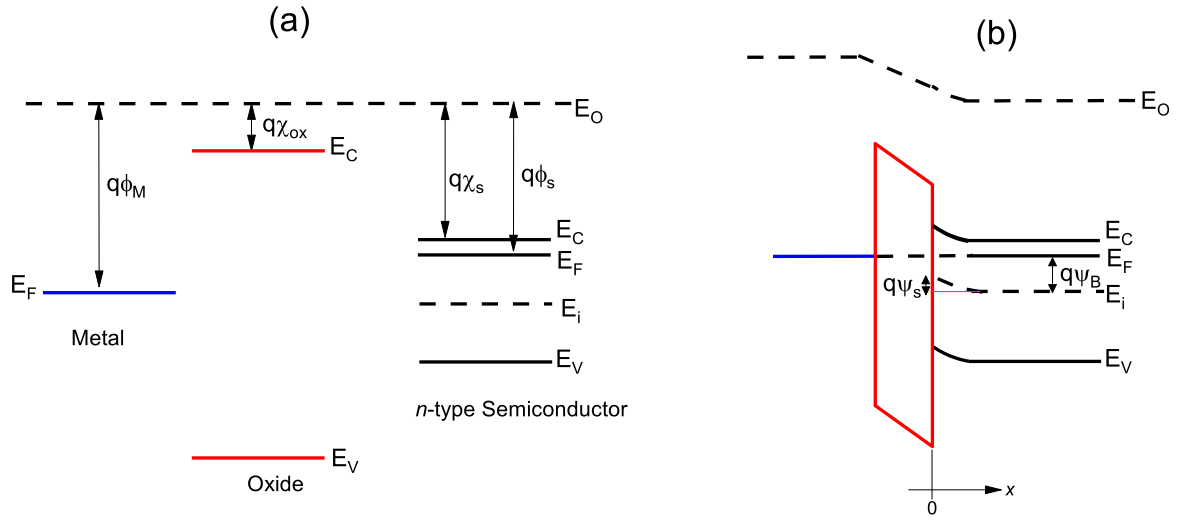

Figure 3.2: (a)Energy levels in three components which form an MOS system (b)Energy-band diagram of real MOS structre

3.1.2 Surface space-charge region electrostatics

In this section, we establish analytical relationships between the surface potential, space charge, and electrical field. First, we define the potential $\psi(x)$ by the equation[5]

$$\psi(x) = \frac{1}{q}\Big(E_i(x = bulk) - E_i(x)\Big) \tag{3.1}$$

where $\psi(x)$ is measured with respect to the intrinsic Fermi level E_i and *x* is the depth into the semiconductor as measured from the oxide/semiconductor interface (figure 3.2 (b)). $\psi(x = \infty)$ is defined as zero in the bulk of the semiconductor and $\psi(x = 0)$ is called the *surface potential* (ψ_S) at the semiconductor surface, which is given by[5]

$$\psi_S = \frac{1}{q}\Big(E_i(x = bulk) - E_i(x = 0)\Big) \tag{3.2}$$

The carrier densities as a function of $\psi(x)$ are given by following equations:

$$\begin{aligned} n &= n_0 \exp\Big(\beta\psi(x)\Big) \\ p &= p_0 \exp\Big(-\beta\psi(x)\Big) \end{aligned} \tag{3.3}$$

where $\psi(x) > 0$ when the band is bent downward and $\psi(x) < 0$ when the band is bent upward. n_0 and p_0 are the densities of electrons and holes. β is q/kT. At the surface, carrier densities are given by[5]

$$\begin{aligned} n_s &= n_0 \exp\Big(\beta\psi_S\Big) \\ p_s &= p_0 \exp\Big(-\beta\psi_S\Big) \end{aligned} \tag{3.4}$$

bulk potential (ψ_B) is given by

$$\psi_B = \frac{1}{q}\Big(E_i(x = bulk) - E_F\Big) \tag{3.5}$$

The relationship between bulk carrier densities and ψ_B are given by the equation 3.6. According to the equation, ψ_B is related to the semiconductor doping concentration[5].

$$\begin{aligned} n_0 &= n_i \exp\Big(-\beta\psi_B \Big) \approx N_D \quad \text{if } N_D \gg N_A \text{ for } \textit{n}\text{-type semiconductor} \\ p_0 &= n_i \exp\Big(\beta\psi_B\Big) \approx N_A \quad \text{if } N_A \gg N_D \text{ for } \textit{p}\text{-type semiconductor} \end{aligned} \tag{3.6}$$

The electric field at the surface (ξ_s), space charge per unit area (Q_s) and differential capacitance of the semiconductor space charge region (C_s) can be obtained by solving the one-dimensional Poisson's equation as follows[5]:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\epsilon_s} \tag{3.7}$$

where, ϵ_s is the permittivity of the semiconductor and $\rho(x)$ is the total space-charge density, which is given by,

$$\rho(x) = q(N_D^+ - N_A^- + p - n) \tag{3.8}$$

Considering the charge neutrality at the bulk ($\rho(x) = 0$) and $\psi(x) = 0$, the Poisson's equation (equation 3.7) can be re-written as follows.

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\epsilon_s}\Big[p_0\Big(\exp(-\beta\psi) - 1\Big) - n_0\Big(\exp(\beta\psi) - 1\Big)\Big] \tag{3.9}$$

The relation between the electric field ($\xi = -d\psi/dx$) and the potential (ψ) can be obtained by integrating equation 3.9, which then can be simplified to equation 3.10[5].

$$\xi^2 = \Big(\tfrac{2qn_0}{\epsilon_s\beta}\Big)\Big[\Big(\exp(\beta\psi) - \beta\psi - 1\Big) + \tfrac{p_0}{n_0}\Big(\exp(-\beta\psi) + \beta\psi - 1\Big)\Big] \tag{3.10}$$

The extrinsic Debye length (L_D) for electrons is a measure of the distance in a semiconductor where it retains the charge balance by majority carriers under thermal equilibrium[5, 8]. This is given by

$$L_D = \sqrt{\frac{\epsilon_s}{qn_0\beta}} \tag{3.11}$$

and

$$F\Big(\beta\psi, \frac{p_0}{n_0}\Big) = \Big[(\exp(\beta\psi) - \beta\psi - 1\Big) + \frac{p_0}{n_0}\Big(\exp(-\beta\psi) + \beta\psi - 1\Big)\Big]^{1/2} \tag{3.12}$$

Electric field can be written as

$$\xi = -\frac{\partial\psi}{\partial x} = \pm\frac{2}{\beta L_D}F\Big(\beta\psi, \frac{p_0}{n_0}\Big) \tag{3.13}$$

where the positive sign is for $\psi > 0$ and a negative sign is for $\psi < 0$. Accordingly, electric field at the surface can be obtained by setting $\psi = \psi_S$:

$$\xi_s = \pm\frac{\sqrt{2}}{\beta L_D}F\Big(\beta\psi_S, \frac{p_0}{n_0}\Big) \tag{3.14}$$

Furthermore, space charge per unit area (Q_s) can be found by applying the Gauss's law as follows.

$$Q_s = -\epsilon_s\xi_s = \mp\frac{\sqrt{2}\epsilon_s}{\beta L_D}F\Big(\beta\psi_S, \frac{p_0}{n_0}\Big) \tag{3.15}$$

The differential capacitance of the space charge region (C_s) can be obtained by

$$C_s = \frac{\partial Q_s}{\partial\psi_S} = \frac{\epsilon_s}{\sqrt{2}L_D}\frac{\Big[\exp(\beta\psi_S) - 1 + \Big(p_0/n_0\Big)\Big(1 - \exp(-\beta\psi_S)\Big)\Big]}{F\Big(\beta\psi_S, \frac{p_0}{n_0}\Big)} \quad \text{F/cm}^2 \tag{3.16}$$

Considering, $n_0 \approx N_D$, $p_0 \approx \frac{n_i^2}{N_D}$ and equation 3.6 for *n*-type semiconductors, extrinsic Debye length for electrons (equation 3.11) and C_s (equation 3.16) can be further simplified as follows.

$$L_{Dn} = \sqrt{\frac{\epsilon_s}{qN_D\beta}} \tag{3.17}$$

$$C_s = \frac{\epsilon_s}{\sqrt{2}L_{Dn}} \frac{\Big[\exp(\beta\psi_S) - 1 + \Big(\exp(2\psi_B\beta)\Big)\Big(1 - \exp(-\beta\psi_S)\Big)\Big]}{\Big[\exp(\beta\psi_S) - \beta\psi_S - 1 + \Big(\exp(2\psi_B\beta)\Big)\Big(\exp(-\beta\psi_S) + \beta\psi_S - 1\Big)\Big]^{1/2}} \quad \text{F/cm}^2 \tag{3.18}$$

Similarly, we can derive equations for *p*-type semiconductors by considering $p_0 \approx N_A$, $n_0 \approx \frac{n_i^2}{N_A}$ and equation 3.6 for *p*-type semiconductors. Accordingly, extrinsic Debye length for holes and C_s for *p*-type semiconductors are given by following equations:

$$L_{Dp} = \sqrt{\frac{\epsilon_s}{qN_A\beta}} \tag{3.19}$$

$$C_s = \frac{\epsilon_s}{\sqrt{2}L_{Dp}} \frac{\Big[1 - \exp(-\beta\psi_S) + \Big(\exp(-2\psi_B\beta)\Big)\Big(\exp(\beta\psi_S) - 1\Big)\Big]}{\Big[\exp(-\beta\psi_S) + \beta\psi_S - 1 + \Big(\exp(-2\psi_B\beta)\Big)\Big(\exp(\beta\psi_S) - \beta\psi_S - 1\Big)\Big]^{1/2}} \quad \text{F/cm}^2 \tag{3.20}$$

Figure 3.3 shows a variation of the space-charge density in a *p*-type semiconductor as a function of the surface potential.

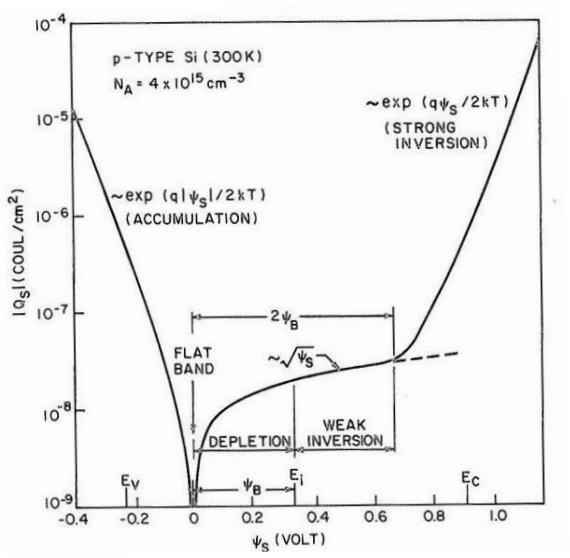

Figure 3.3: Plot of variation of space-charge density as a function of the surface potential for *p*-type silicon with $N_A = 4 \times 10^{15} cm^{-3}$ at room temperature.[5, 9]

3.1.3 Capacitance of the MOS system for specific biasing regions

Under the normal operating conditions, the back side of the MOS capacitor is grounded, and dc bias V_G is applied to the gate metal. Applied voltage divides across the oxide and semiconductor according to the following equation.

$$V_G = V_{ox} + \psi_S + \psi_{MS} \tag{3.21}$$

where V_{ox} and ψ_S are potential across the oxide and surface potential, respectively. ψ_{MS} is the work-function difference which is given by $\psi_{MS} = \frac{1}{q}\Phi_M - \Phi_S$.

The overall capacitance *C* of the MOS system is the series connection of the oxide capacitance C_{ox} (fixed) and the semiconductor space charge region capacitance C_s (variable). The equivalent circuit is shown in figure 3.4, and total capacitance is given by equation 3.22

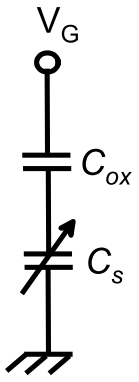

Figure 3.4: The equivalent circuit for the total capacitance of MOS system.

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_s} \quad \text{which simplifies to} \quad C = \frac{C_{ox}C_s}{C_{ox} + C_s} \quad \text{F/cm}^2 \tag{3.22}$$

With the applied bias, $V_G \neq 0$, Fermi energies of the metal and the semiconductor separates by an amount of qV_G; which is given by [6]

$$E_F(metal) - E_F(semiconductor) = -qV_G \tag{3.23}$$

Application of dc bias doe not change the semiconductor Fermi energy, but Fermi level of the metal will go up-and-down with applied bias. If $V_G > 0$, Fermi level of the metal will move downward and if $V_G < 0$ Fermi level of the metal will move upward. Since work function quantities are fixed values, movement of metal Fermi level leads to a band bending in other features of the band diagram. Then as the bias voltage change, the surface potential ψ_S changes and MOS capacitor experiences different operation modes. The following study, we discuss the flat band, accumulation, depletion, inversion regions for *n*-type MOS capacitor. Corresponding block charge diagrams are plotted by assuming a perfect gate oxide and charge neutrality of the system.

Flat-Band condition

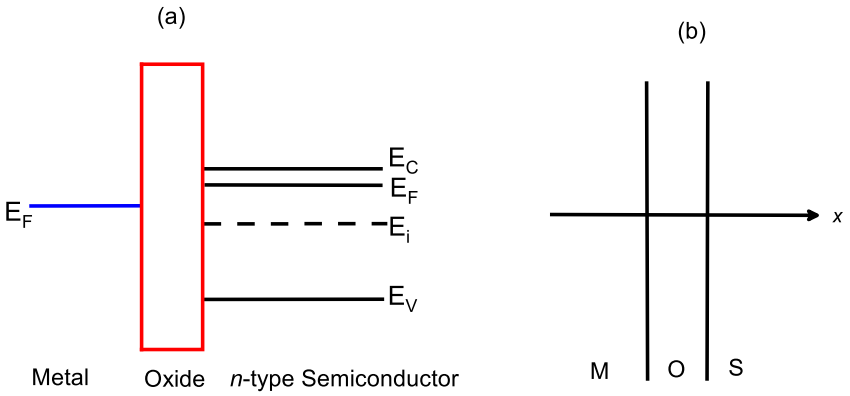

Figure 3.5: (a)Energy band diagram and (b)block charge diagram of MOS system at flat-band condition.

As the applied voltage is set to a value which exactly compensates the work function difference, energy bands in the MOS system will level (see Figure 3.5 (a)). Then, $\psi_S = 0$ and stored charge in the MOS capacitor will reduce to zero (see Figure 3.5 (b)). Then, at the flat-band condition C_s can be obtained by expanding the exponential terms in equation 3.18 and substituting $\psi_S = 0$.

$$C_s(flat-band) = \frac{\epsilon_s}{L_{Dn}} \quad \text{F/cm}^2 \tag{3.24}$$

Furthermore, by substituting C_s(flat-band) (equation 3.24) and $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ to equation 3.22, total capacitance at flat-band condition (Flat-band capacitance) can be simplified to,

$$C_{FB} = \frac{\epsilon_{ox}}{t_{ox} + (\epsilon_{ox}/\epsilon_s)L_{Dn}} \quad \text{F/cm}^2 \tag{3.25}$$

where ϵ_{ox}, ϵ_s and t_{ox} are permittivity of the oxide, permittivity of the semiconductor and oxide thickness. The calculated C_{FB} value can be used to find the corresponding flat-band voltage(V_{FB}).

Accumulation

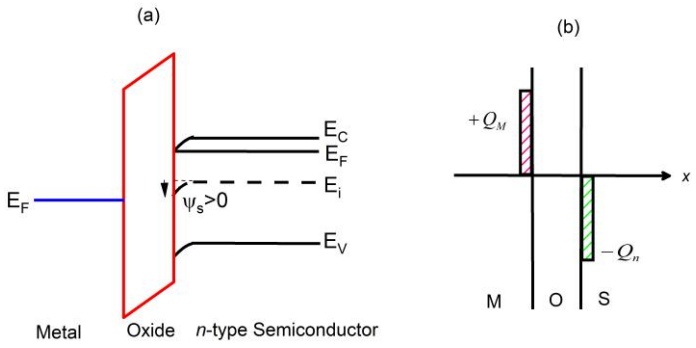

Figure 3.6: (a)Energy band diagram and (b)block charge diagram of MOS system at accumulation condition.

The application of positive bias higher than the flat-band voltage ($V_G > V_{FB}$) of an *n*-type MOS capacitor causes a band bending in both the oxide and semiconductor ($\psi_S > 0$) as shown in figure 3.6 (a). When $V_G > 0$ places positive charge on gate surface, negatively charged electrons move toward the semiconductor/oxide interface to maintain charge neutrality. Block charge diagram at accumulation condition is shown in Figure 3.6 (b). Charge configuration is shown in Figure 3.6 (b)is similar to an ordinary parallel-plate capacitor and therefore provides an experimental way to determine t_{ox} by

$$C(accu) \simeq C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} \quad \text{F/cm}^2 \tag{3.26}$$

Depletion

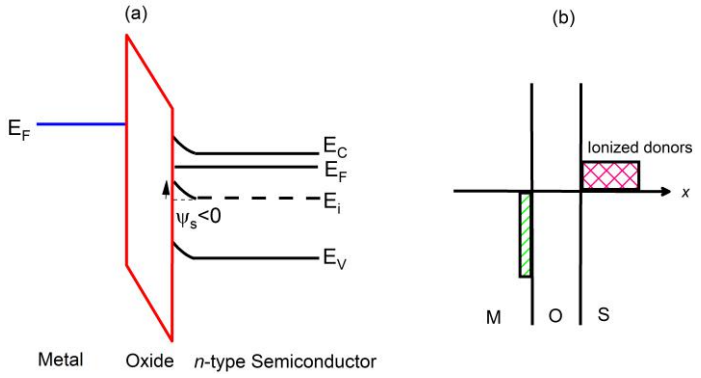

Figure 3.7: (a)Energy band diagram and (b)block charge diagram of MOS system at depletion condition.

As the condition $V_G < V_{FB}$ is applied to *n*-type semiconductor, slope of the band bending and surface potential will be negative ($\psi_S < 0$) (see Figure 3.7 (a)). The approximate charge distribution is shown in figure 3.7 (b). In depletion biasing, hole concentration at the oxide-semiconductor interface is much less than the background doping concentration (N_D). Therefore, depletion width in the semiconductor(W_D) can be obtained as follows.

$$W_D = \sqrt{\frac{2\epsilon_s|\psi_S|}{qN_D}} \tag{3.27}$$

where ψ_S is surface potential at the semiconductor surface.

In depletion biasing, semiconductor capacitance can be expressed by

$$C_s = \frac{\epsilon_s}{W_D} \quad \text{F/cm}^2 \tag{3.28}$$

Accordingly, if the negative gate charge increases more, depletion layer widens almost instantaneously and reduces the total capacitance. In the deep depletion mode, the *C*-*V* measurements provide an experimental way to determine the semiconductor doping concentration by using the following formula.

$$\frac{d(1/C^2)}{dV} = \frac{2}{q\epsilon_s N_D} \tag{3.29}$$

Inversion

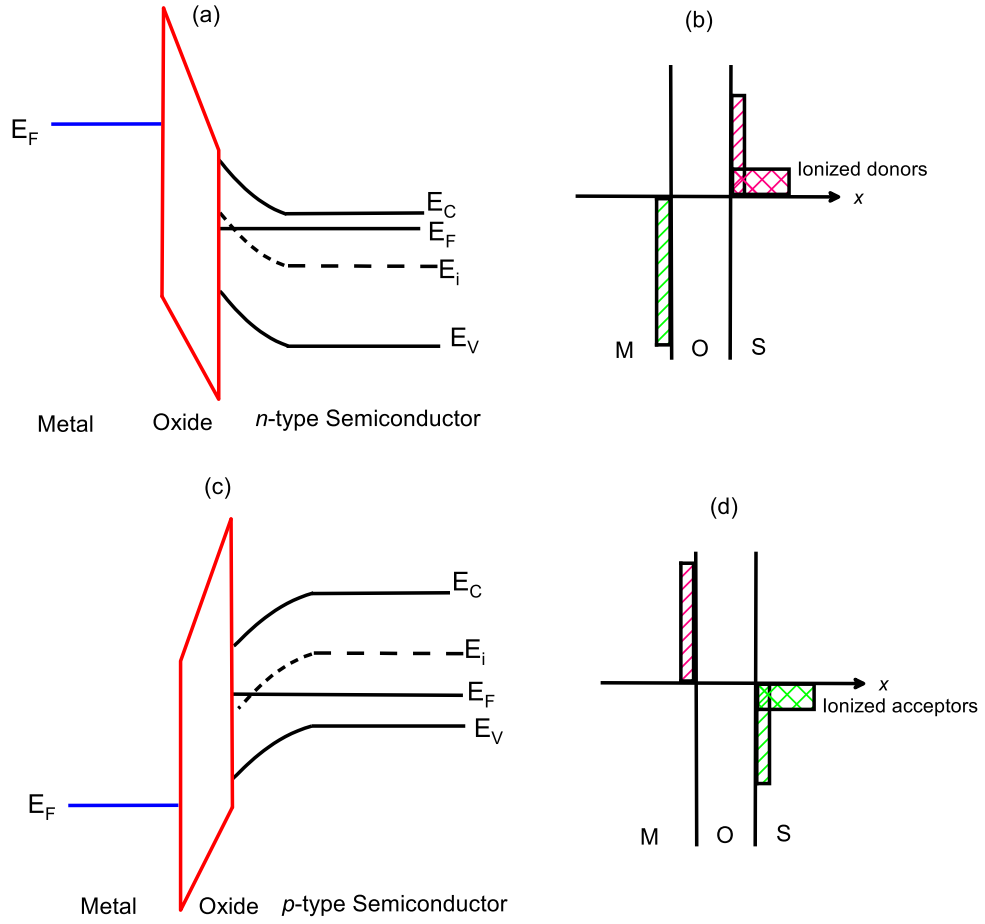

Figure 3.8: (a)Energy band diagram and (b)block charge diagram of MOS systems at inversion condition.

With the application of sufficiently high negative voltage, *n*-type semiconductor bands bend even more upward. Consequently, intrinsic Fermi level E_i at the semiconductor surface will

cross over the Fermi level E_F as shown in figure 3.8 (a). Therefore, surface will contain more holes (minority carriers) than electrons (majority carriers). The corresponding bias region is called *Inversion*. If E_i is slightly above the E_F at the surface, hole density is low (order n_i) in the inversion layer and the MOS system is said to be biased in *weak inversion*. However, if the applied negative voltage is increased more, $\psi_S = 2\psi_B$ condition will occur and *strong inversion* begins. At *strong inversion*, number of holes in the inversion layer is equal to the number of ionized donors ($p_s = N_D$) and semiconductor depletion-layer width reaches its maximum W_{Dmax} (bands are bent far enough).

$$W_{Dmax} = \sqrt{\frac{4\epsilon_s \psi_B}{qN_D}} \tag{3.30}$$

Table 3.1 shows the summary of different surface charge conditions for *n*-type semiconductor.

$\psi_S > 0$	Accumulation of electrons (band bend downward)
$\psi_S = 0$	Flat-band
$\psi_B < \psi_S < 0$	Depletion of electrons (band bend upward)
$\psi_S = \psi_B$	Intrinsic condition (midgap with $n_s = p_s = n_i$)
$\psi_S = 2\psi_B$	Onset of strong inversion ($p_s = N_D$)
$\psi_S < 2\psi_B$	Strong inversion ($p_s > N_D$)

Table 3.1: Surface-Charge conditions for *n*-type MOS system.

From the discussions above and considering the polarity change, a summary of different regions distinguished by surface potential and surface charge conditions for a *p*-type semiconductor can be tabulated as follows.[5, 7] An example of energy band diagram for *inversion* in *p*-type semiconductor is shown in figure 3.8 (c).

$\psi_S < 0$	Accumulation of holes (band bend upward)
$\psi_S = 0$	Flat-band
$\psi_B > \psi_S > 0$	Depletion of holes (band bend downward)
$\psi_S = \psi_B$	Intrinsic condition (midgap with $n_s = p_s = n_i$)
$\psi_S = 2\psi_B$	Onset of strong inversion ($n_s = N_A$)
$\psi_S > 2\psi_B$	Strong inversion ($n_s > N_A$)

Table 3.2: Surface-Charge conditions for *p*-type MOS system .

Under normal gate bias, narrow bandgap semiconductor MOS systems demonstrate all the bias regions (accumulation, flat-band, depletion and inversion). However, in wide bandgap semiconductors, it is impossible to form inversion layer under normal gate bias due to the low minority carrier generation. Therefore, with the increase of negative gate bias, wide bandgap semiconductor MOS system forms deep depletion.

3.2 Dielectric-semiconductor interface traps and oxide charges

In the previous discussion, consideration of traps within the oxide and at the interface was neglected. Figure 3.9 shows a schematic of different types of charges at the oxide-semiconductor interface[5].

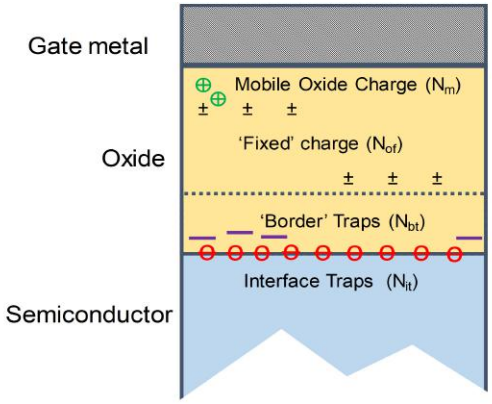

Figure 3.9: Charge traps and their location for oxide-semiconductor interface.

Interface trapped charges are also known as *interface states, fast states or surface states*. These are defects that introduce energy levels in forbidden band gap at the oxide-semiconductor interface and distributed with density D_{it} (traps $cm^{-2}eV^{-1}$) throughout forbidden band gap energy region. Interface trap level is considered as an *Acceptor* level if it become negatively charge by accepting an electron (electrically neutral when empty). If interface trap level become positively charge by giving an electron(electrically neutral when occupied by an electron), then interface trap level is considered as a *Donor* level. Interface traps in upper half of the bandgap are believed to be acceptor levels while trap energy levels which are located in lower half of the bandgap are treated as donor like[5, 8]. These interface trap levels always remain fixed in energy relative to the conduction band and valence band of the semiconductor at the surface.[6]

Border traps or *near-interface oxide traps* are states in the near-interface oxide, that typically interact with the semiconductor by tunneling to and from states in the conduction band, resulting in longer capture and emission time constants, depending on their energy level as well as their proximity from the interface[10, 11].

Also certain MOS interfaces may contain ***fixed oxide charges*** which are usually related to the poor control of oxide process. In addition, ***mobile oxide charges*** caused by ionic contamination such as Na^+, Li^+, may contain in the oxide [8]. Usually, *interface traps* and *border traps(near-interface oxide traps)* are the only two types of trap states that may change charge occupancy as the surface Fermi level changes. *Fixed* and *mobile* oxide charges do not change charge state when the surface Fermi level changes.

It is widely believed that shallow interface traps with energy levels just below the conduction band of the 4H-SiC are responsible for the degradation of *n*-channel 4H-SiC MOSFETs characteristics[12, 13, 14]. Thus, characterization of interface traps near to the conduction band of *n*-type MOS capacitors is more relevant. Throughout this study, we consider traps near the conduction band edge of *n*-type semiconductors as electron traps. To a first order approximation, all electron traps below the Fermi level are treated as filled and, all electron traps above the Fermi level are treated as empty (remains electrically neutral). Figure 3.10 shows filling of interface trap levels under depletion and accumulation biasing in the *n*-type MOS device.

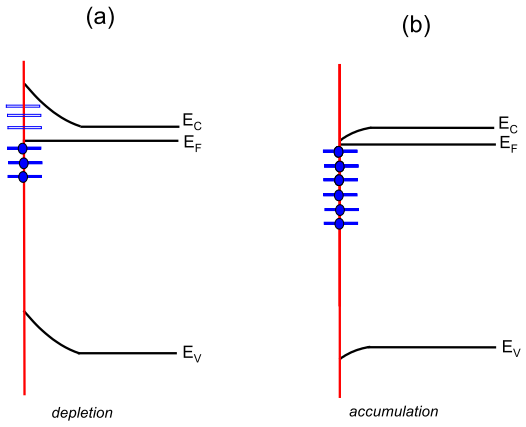

Figure 3.10: Band diagrams illustrating the filling of the interface traps under (a) depletion and (b) accumulation biasing in *n*-type MOS device. Filled interface traps are indicated by the *bold lines and balls* and unoccupied traps by the *hollow lines*

Occupancy of these electron traps can change by a change in the gate bias or Fermi level, external light illumination or due to thermal emission caused by heating/cooling of the system. Accordingly, several methods have been used in this thesis to investigate traps in 4H-SiC and Ga_2O_3 *n*-type MOS capacitors, (i) simultaneous high-low frequency capacitance-voltage (*C-V*) measurements, (ii) Gray-Brown technique, (iii) photo-assisted *C-V* measurements and (iv) Constant Capacitance Deep Level Transient Spectroscopy (CCDLTS) method. Following is a brief discerption of these methods.

3.2.1 Simultaneous high-low frequency capacitance-voltage (C-V) measurements

As we discussed earlier, semiconductor bands at the surface bend (surface potential ψ_S changes) as a function of the gate bias. Interface trap occupancy also varies with the gate bias since interface trap levels always remain fixed in energy relative to the conduction band of the semiconductor. Therefore, interface traps can be investigated by a small perturbation in semiconductor band bending, relative to the Fermi level, which is accomplished by an infinitesimal change in the gate bias. In this regard, if high frequency (100 kHz or 1 MHz) small ac signal(15 mV RMS) on top of a dc voltage is applied as a test signal to the MOS capacitor, interface traps does not respond to the ac probe frequency (perturbations of the surface potential caused by the ac components of the gate bias) due to the large emission time of interfaces traps[8, 15]. Therefore, interface traps do not contribute to the total device capacitance in depletion. Accordingly, total capacitance, C_{HF} at high frequencies is given by (considering $C_{it}(\omega) = 0$ in figure 3.11)[8, 15]

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_s} \tag{3.31}$$

Note that at high frequency, interface traps still respond to the dc bias, resulting in a distortion of the voltage scale of the high frequency *C-V* known as *C-V stretch out*. In contrast, for the low frequency (quasi-static) measurements (C_{LF}), interface states respond, and total capacitance ideally includes capacitance component due to all traps. Accordingly, formula for total capacitance(low frequency equivalent circuit is shown in figure 3.11) can be written as [8, 15]

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_s + C_{it}} \tag{3.32}$$

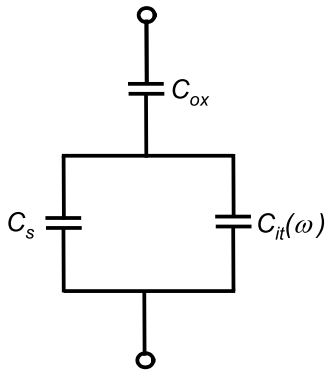

Figure 3.11: Equivalent circuit of overall capacitance when interface traps present.

Using equations 3.31 and 3.32, expression for C_{it} can be obtained by the following equation[15]

$$C_{it} = \Big(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\Big)^{-1} - \Big(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\Big)^{-1} \tag{3.33}$$

C_{it} is also related to the interface state density D_{it} by $D_{it} = C_{it}/q^2$.[8] Therefore, comparison of the C_{HF} and C_{LF}, *C-V* curves can be used to extract D_{it} by the following equation[8]

$$D_{it} = \frac{C_{ox}}{q^2}\Big(\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}}\Big) \tag{3.34}$$

This method can be used to extract the interface state density D_{it} as function of gate voltage. D_{it} over the energy range profile can be obtained by finding the relation between extracted trap energy level and gate bias. In this regard, relation between surface potential and the energy level of the interface state can be obtained by finding the energy position opposite to the Fermi level at the surface, which is given by [15]

$$E_C - E_T = \frac{E_g}{2} + \psi_S - \psi_B \tag{3.35}$$

The surface potential, as function of gate bias can experimentally obtain by the following equation.[15]

$$\psi_S(V_G) - \psi_S(V_{FB}) = \int_{V_G}^{V_{FB}} \left[1 - \frac{C_{LF}}{C_{ox}}\right] dV \tag{3.36}$$

where V_{FB} is determined by finding the gate voltage corresponding to the C_{FB} (3.25) value. Integrating equation 3.36 gives the experimental ψ_S versus V_G curve (figure 3.12 (b)) which can be used with equation 3.35 to determine the relation between gate voltage and energy level of the extracted interface state.

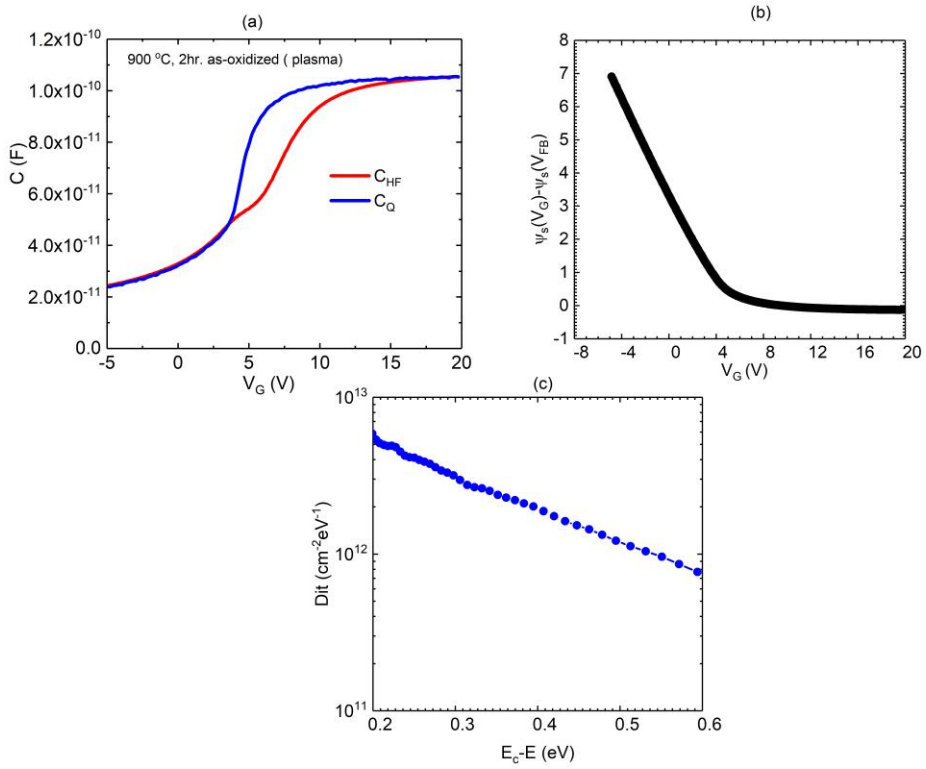

Figure 3.12: (a)Measured high frequency 100 kHz C_{HF}-V, quasi-static C_Q-V (b)ψ_S versus gate voltage (V_G) profile (c) D_{it} versus $E_C - E_T$ profile by simultaneous hi-low C-V measurement at room temperature for *n*-type 4H-SiC MOS capacitors with a plasma grown unpassivated SiO_2.

The energy limit of high and low frequency for estimation of D_{it} can be found by considering the emission time constant τ_e of electrons from interface states, which is given by following equation[16]

$$\tau_e = \frac{\exp\Big((E_C - E_T)/kT\Big)}{\sigma_n \upsilon_{th} N_C} \tag{3.37}$$

where σ_n and υ_{th} are the *electron capture cross sections* and the *electron thermal velocity* ($\upsilon_{th} = \sqrt{3kT/m_e^*}$), respectively.

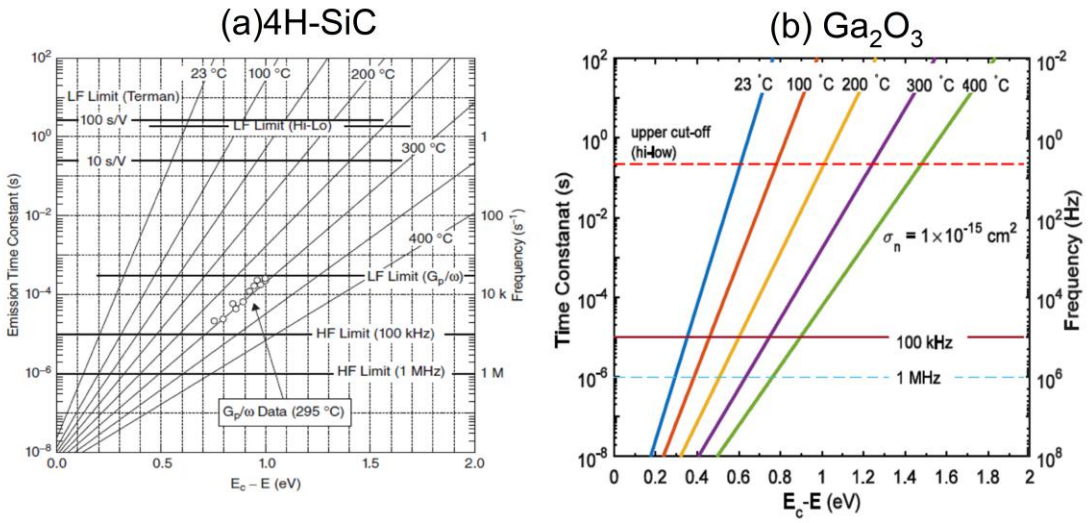

Figure 3.13: Time constants for electron emission from an interface state to conduction band in (a) 4H-SiC [16, 17] (b)Ga_2O_3 and estimated cut-off limits for simultaneous hi-low method.

Figure 3.13 shows the emission time constant from the interface states as a function of the energy level, estimated based on typical interface trap cross-section of $1\times10^{-15}cm^2$. In this thesis, reported interface trap profiles from simultaneous high-low frequency measurements at room temperature are accurate only in a limited energy range, ranging from about 0.2 (flat-band) eV to 0.6 eV below the conduction band edge [16]. Figure 3.12 (a) shows an example of simultaneous high-low frequency *C-V* characteristics at room temperature and Figure 3.12 (c) shows extracted D_{it} profile based on simultaneous high-low frequency *C-V* method for *n*-type 4H-SiC MOS capacitors with a plasma grown un-passivated SiO_2 which will be discussed in chapter 4.

3.2.2 Gray-Brown technique

In the Gray-Brown technique, interface traps are extracted by measuring high frequency capacitance at various temperature.[18] Reduction of temperature causes the bulk Fermi level to shift closer to the conduction band edge and changes the occupancy of interface states at the flat-band. Therefore, the 'freeze out' of shallow near-interface traps results in additional fixed negative charge at lower temperatures and leads to a shift in the flat-band voltage. Accordingly,

when small signal *C-V* measurements are carried out using a 1 MHz (or 100 kHz) frequency at 77 K and 298 K, *C-V* shows a flat-band voltage shift. Using the flat-band voltage shift, an effective density of near-interface states (N_{it}) near to the conduction band (between E_F at 80 K to E_F at 278 K below the conduction band-edge (E_C)) of the semiconductor can be estimated by[19]

$$N_{it} = \frac{C_{ox}\Delta V_{FB}}{Aq} \tag{3.38}$$

where C_{ox}, A, and q are the oxide capacitance, gate area and electron charge respectively. ΔV_{FB} is the difference between the flat-band voltages at 77 K and 298 K. Figure 3.14 shows typical 1 MHz frequency *C-V* characteristics of *n*-type 4H-SiC MOS capacitor with a nitrided SiO_2, at room temperature and 77 K.

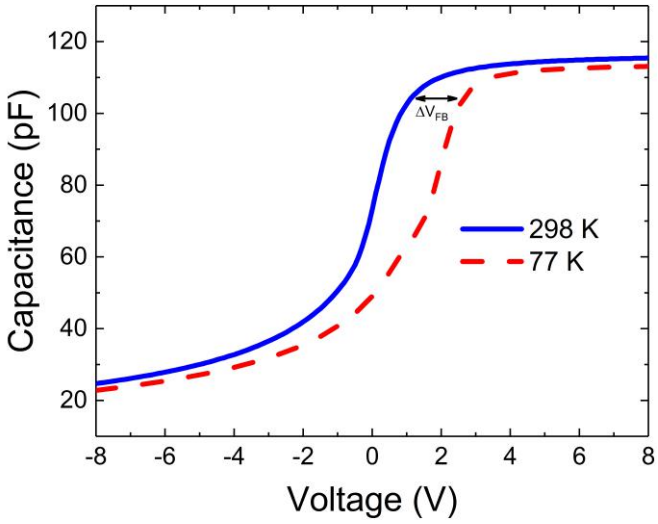

Figure 3.14: Temperature dependent 1 MHz *C-V* curves showing the flat band voltage shift with temperature for for with post-oxidation annealed in nitric oxide (passivated) *n*-type 4H-SiC MOS capacitor.

3.2.3 Photo-assisted *C-V* measurements

Photo-assisted *C-V* measurements can be used to measure energetically deeper interface traps and border traps[16, 20, 21]. In this technique first, the gate voltage is swept from accumulation to depletion in the dark. Next, UV light is illuminated with sample biased in the deep depletion.

The generated holes move towards the oxide/semiconductor interface due to the built-in electric field (negative gate bias) and empty electron traps (interface traps, oxide traps) through recombination by the capture of holes. Upon turning off the UV the device is swept from depletion to accumulation in the dark, causing electron traps to be refilled. Change in deep trap occupancy due to the UV exposure causes an interface trap ledge in high frequency *C-V* curves. Furthermore, flat-band voltage shift (ΔV_{FB}) can be linked with trapping and de-trapping of the 'border' traps, since these slow traps influence the capacitance when they are close to the flat-band voltage (near accumulation)[16, 20, 21].

Comparison of the high frequency dark *C-V* and the *C-V* after UV exposure can be used to estimate the total number of deep interface trap density (N_{it}^{deep}) and 'border' traps (N_{bt}) density by following equations.

$$N_{it}^{deep} = \frac{C_{ox}\Delta V}{Aq} \tag{3.39}$$

$$N_{bt} = \frac{C_{ox}\Delta V_{FB}}{Aq} \tag{3.40}$$

where C_{ox}, A, q, ΔV, ΔV_{FB} are oxide capacitance, gate area, electron charge, voltage shift at a given capacitance and flat-band voltage shift respectively. An example of the photo-assisted *C-V* measurement data on ALD Al_2O_3 $\beta-Ga_2O_3$ MOS capacitor is shown in figure 3.15.

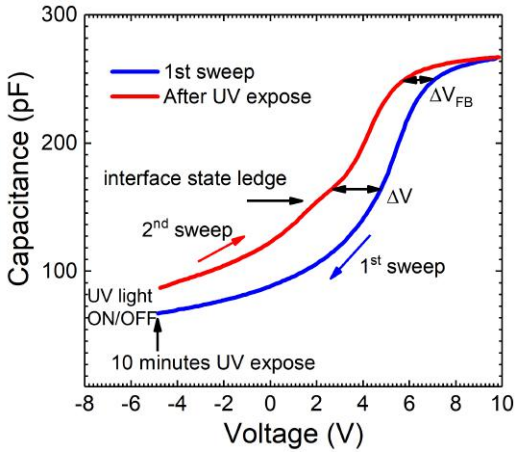

Figure 3.15: Photo assisted high frequency (100 kHz) C-V measurement data on $\beta-Ga_2O_3$ MOS capacitor with on Al_2O_3 dielectric.

3.2.4 Constant Capacitance Deep Level Transient Spectroscopy (CCDLTS) measurements

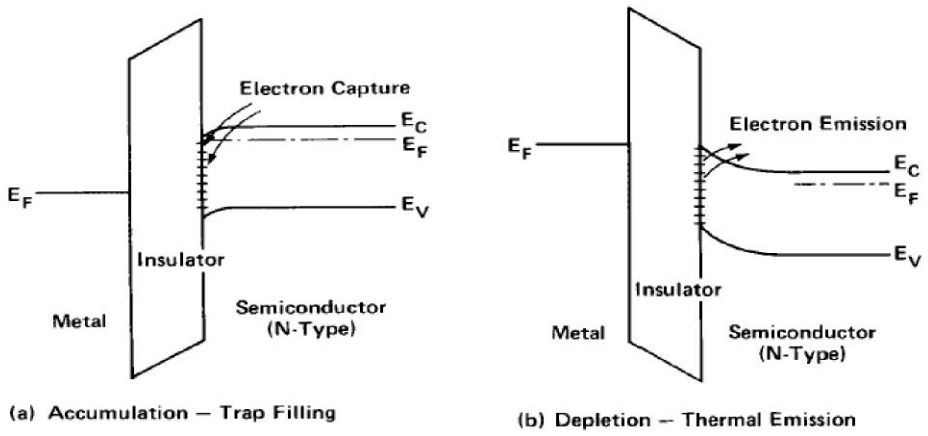

Figure 3.16: Qualitative schematic of CCDLTS measurements indicating interface trap filling and discharge.[23]

Constant capacitance deep level transient spectroscopy (CCDLTS) technique is an appropriate technique to measure thermal emission rates of electron traps in MOS systems [11, 23]. The emission rates of the traps are thermally activated as discussed in section 2.4.2. Thermal emission from traps having a single energy level decays exponentially in time, and therefore the corresponding transient decays exponentially. Consequently, if the emission rate of the trap varied by varying the sample temperature, the transient will show a response peak when the trap emission rate is within the window[22] (see chapter 2 section 2.4.2). Thus, if the emission rate of the trap varied by varying the sample temperature, the spectrometer shows a response peak at the temperature where the trap emission rate within the rate window. The emission rate (e_n) of trapped electrons is given by

$$e_n = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-(E_C - E_T)}{kT}\right) \tag{3.41}$$

where $E_C - E_T$ is the emission activation energy of the trap level, σ_n is the electron capture cross section, $\upsilon_{th} = \sqrt{3kT/m_e^*}$ is the electron thermal velocity, $N_C = 2(2\pi m^* kT/h^2)^{3/2}$ is

the effective density of states in the conduction band for electrons, and m^* is the effective mass of the semiconductor.

In CCDLTS, a feedback circuit adjusts the voltage applied to the MOS capacitor to hold the capacitance at a constant value with the sample biased in deep depletion. A 25ms trap filling voltage pulse (V_P) is periodically applied to charge and discharge the traps (figure 3.16). Then the voltage transient after the filling pulse is monitored as a function of temperature and measured at two different times t_1 and t_2, with $t_2 = 2.5t_1$, that determines the spectrometer rate window (τ_{max}^{-1})(see chapter 2.4.2). The resulting CCDLTS signal, $\Delta V = V(t_1) - V(t_2)$, is a maximum when the emission rate of the trap, e_n, is equal to the spectrometer rate window. Then $E_C - E_T$ and σ_n can be determined from the slope and intercept of the Arrhenius plot of $ln(T^2 e_n)$ versus 1000T, respectively, where T is the temperature of the CCDLTS peak and e_n is the instrument rate window.

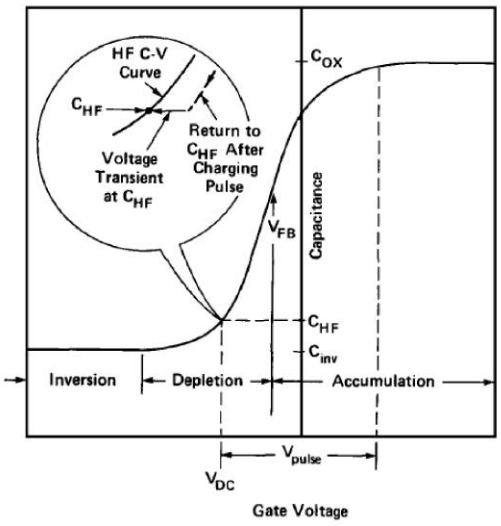

Figure 3.17: High frequency C-V characteristics for an n-type MOS capacitor. The insert schematically illustrates the relaxation of the gate voltage toward the depletion bias V_{dc} after a voltage pulse V_{pulse} into accumulation during the CCDLTS measurements[23].

The pulse voltage response is illustrated in figure 3.17 with high frequency *C-V* characteristics for *n*-type MOS capacitor. In CCDLTS method,reverse voltage is applied to the MOS capacitor to hold the device in depletion mode. Therefore, the CCDLTS signal only depends on the difference in net charge (Q_{is}) at the interface which is caused by electron emission of

the interface traps. Accordingly, dependence of the CCDLTS signal on electron emission from continuous distribution of interface is given by,[23, 11] (see appendix D for more detail)

$$\Delta V = \Big(Aq/C_{ox}\Big) N_{it}(E) \int \Big[\exp(-e_n t_1) - \exp(-e_n t_2)\Big] dE \tag{3.42}$$

where C_{ox}, A, and q are the oxide capacitance, gate area and electron charge respectively.

CCDLTS: Near-interface oxide trap analysis

In the case of MOS capacitor, increasing the applied voltage up to the accumulation moves the Fermi level at the oxide/semiconductor interface closer to the E_C. Therefore, as the filling voltage (V_P) in CCDLTS measurement pulse is increased above the flat-band voltage ($V_P > V_{FB}$), near-interface trap levels at energies closer to the conduction band are occupied (figure 3.18 (a)). When pulse amplitude is '0' before the next duty cycle, MOS capacitor goes to its initial depletion point due to the constant capacitance set point. Therefore, occupied traps are de-trapped by the Fermi level change (figure 3.18 (b)). Accordingly, near interface oxide traps on MOS capacitor can be investigated by taking CCDLTS spectra by pulsing the capacitor from depletion to the accumulation [11].

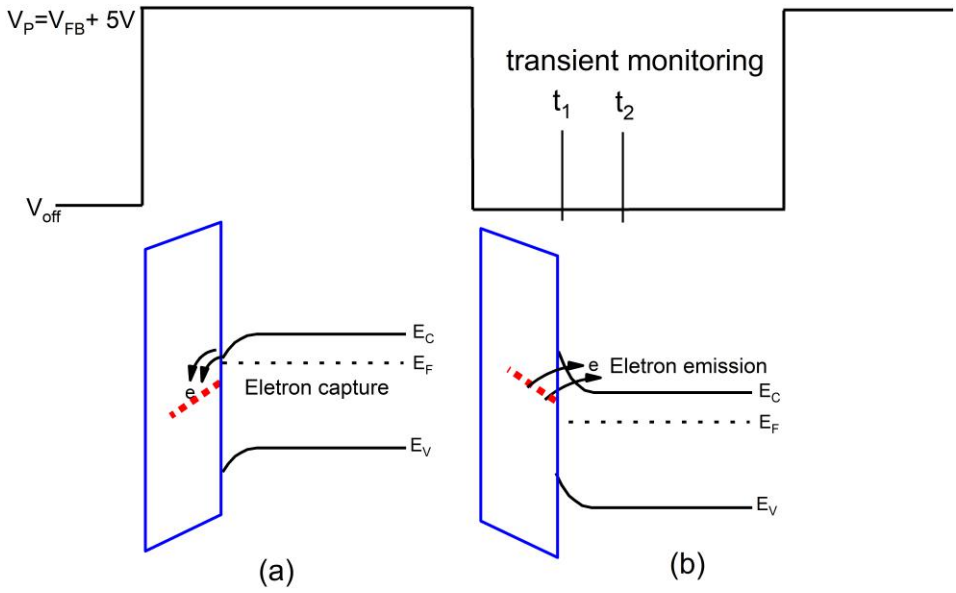

Figure 3.18: Energy band diagrams for a MOS capacitor at (a) at a filling voltage $V_P > V_{FB}$ near-interface oxide trap filling (b) near-interface oxide trap emission before next duty cycle.

In 4H-SiC, the energetically shallow traps also spatially extend into the oxide and communicate with 4H-SiC via electron tunneling. As a result, saturation of the CCDLTS signal is not observed as trap filling voltage is increased with higher filling pulse. Therefore, in this work, to compare different oxide/4H-SiC interfaces, the spectra were compared at the same V_P-V_{FB}. The amplitude of the CCDLTS signal is directly proportional to the trap density N_{it}. The areal density of the near-interface traps can be calculated by [11, 24]

$$N_{it} = \frac{3 \times (C_{ox}/A)\Delta V(T_o)\Delta W}{q} \tag{3.43}$$

where the factor of 3 arises from the sampling times t_1 and t_2 (see Appendix C) of the voltage transient in the DLTS spectrometer, $\Delta V(T_o)$ is the maximum CCDLTS signal at the peak temperature T_o and ΔW is the broadening factor, which is calculated by taking the ratio of the integral of the experimental CCDLTS signal (ΔV) over the measured temperature range to the integral of the intensity of a theoretical CCDLTS peak for a trap having a single energy level[11].

CCDLTS : Semiconductor bulk trap analysis using MOS capacitors

While MOS capacitor is pulsed from depletion to accumulation, semiconductor depletion width also reduces. Therefore, depth profile of point defects in the semiconductor epi-layer can also be investigated by the CCDLTS measurements. However, to avoid any detection of the oxide traps, MOS capacitor is pulsed from depletion to the flat-band voltage (figure 3.19 (a)). Similar to the oxide traps, bulk traps are also filled during the filling pulse and de-trapped before the next duty cycle of the pulse (figure 3.19 (b)). This method is analogy to the bulk trap investigation in SBDs by DLTS where we used capacitance transient in analysis (section 2.4.3). However, N_T calculation is different due to the voltage transient used in the CCDLTS method. For the bulk traps on the semiconductor side, the CCDLTS signal is expected to increase with increasing filling voltage and saturate at $V_P \simeq V_{FB}$, as the semiconductor depletion width approaches zero and all the bulk traps are occupied[11, 24].

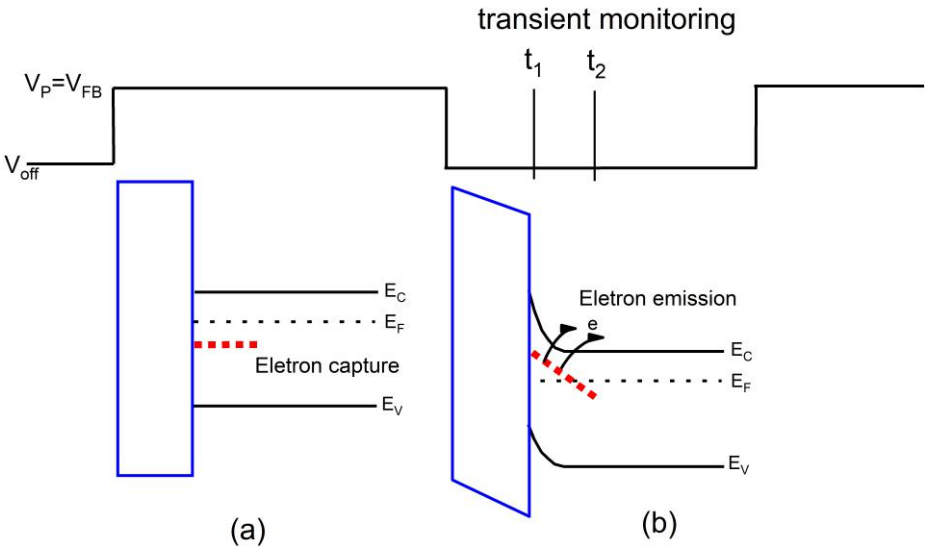

Figure 3.19: Energy band diagrams for a MOS capacitor at (a) at a filling voltage $V_P \simeq V_{FB}$ bulk trap filling (b) trap emission before next duty cycle

The trap concentration in the semiconductor is calculated from the corresponding CCDLTS peak amplitude (ΔV). Considering the values of depletion width during the filling pulse (W_P) and at constant capacitance when carriers are emitted (W_R), N_T values can be found by using the following equation [24],

$$N_T = \frac{3 \cdot 2 \cdot \epsilon}{q} \frac{\Delta V}{\left[(W_R - \lambda(E_T))^2 - (W_P - \lambda(E_T))^2\right]} \tag{3.44}$$

where q is the elementary charge, ϵ is the semiconductor permittivity, $\lambda(E_T)$ is the width of the transition region at the edge of the depletion region, where the space charge is due to ionized donors N_D and the traps at E_T are filled with electrons, and is given by[24]

$$\lambda(E_T) = \sqrt{\frac{2 \cdot \epsilon(E_F - E_T)}{qN_D}} \tag{3.45}$$

where E_F is the position of the Fermi level at the temperature of the CCDLTS peak and E_T is the trap level energy[24].

3.3 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

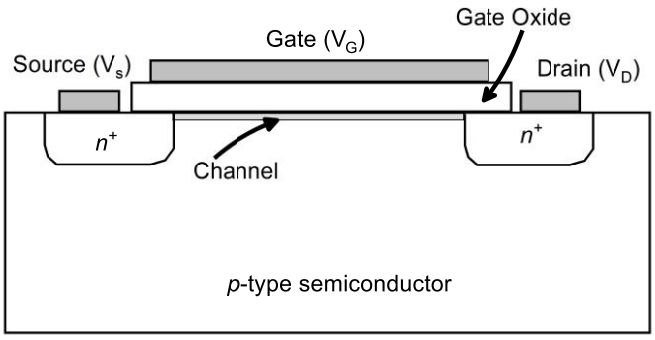

Figure 3.20: Schematic diagram of an *n*-channel MOSFET.

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a three-terminal switch, which is an important device for microprocessors and semiconductor memories. Vertical MOSFETs such as Double-implanted MOSFETs (DMOSFETs) and Trench MOSFETs are used as power devices. Here, we briefly discuss the basic principle of lateral MOSFET operation. The basic structure of an *n*-channel *lateral* MOSFET is shown in figure 3.20. It consists with MOS system on *p*-type semiconductor and highly doped *n*-type junctions, called *Source* and *Drain*. These junctions are electrically disconnected from each other. However, when the necessary gate voltage is applied to the MOS system to invert the semiconductor surface, *n*-type inversion layer at the surface provides a conducting channel between them. The necessary applied gate voltage is known as the *threshold voltage* V_T, which can be express as [7]

$$V_T = V_{FB} + 2|\psi_B| + \frac{1}{C_{ox}}\sqrt{2\epsilon_s q N_A (2|\psi_B|)} \tag{3.46}$$

As the applied *gate* voltage satisfies the condition $V_G > V_T$, electrons enter from the *source* and leave at the *drain*(small voltage is applied between junctions). Here gate voltage must apply to form a *channel* (connection). Therefore, type of the MOSFETs are labelled as *normally off* (enhancement-mode) devices. Note that, due to the wide energy bandgap, minority carrier generation in wide bandgap semiconductors are limited and not enough to form the inversion layer under normal gate bias conditions. However, diffused electrons are supplied from the source and drain regions help to form the inversion layer.

3.3.1 Carrier Mobility

In the presence of an electric field, free carriers in the semiconductor are accelerated and transported along the direction of the electric field. Carrier motion due to an electric field can be characterized by the *mobility* (μ), which is defined as the proportionality constant relating the carrier velocity to the electric field. In the case of *n*-channel MOSFET, on-state current flow is induced by the formation of an inversion layer on the *p*-base region by the application of a gate voltage to create a strong electric field normal (E_N) to the semiconductor (figure 3.21 (a)). At the same time, carrier transport through the channel layer is achieved by the application of a tangential electric field (E_T) (figure 3.21)(a). Furthermore, free carriers in the channel moving under influence of E_T are confined to a thin layer located close to the surface ($\sim 5nm- \sim 10nm$ near the oxide/semiconductor interface) by E_N. Therefore, both electric field components influence the velocity of the moving carriers.

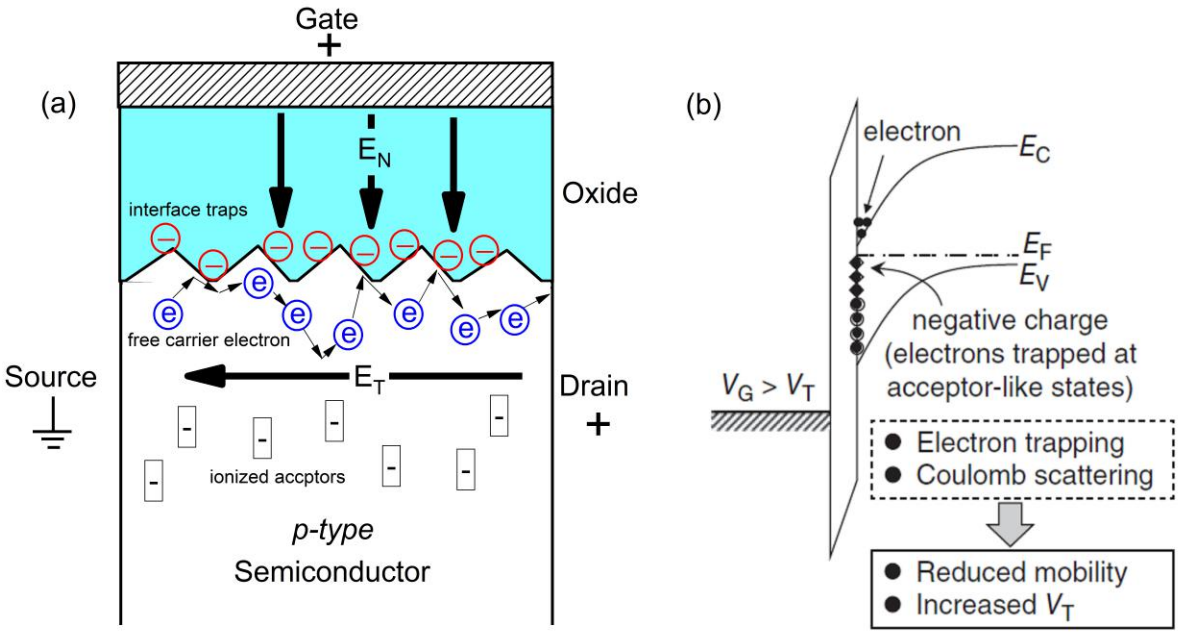

Figure 3.21: (a) A pictorial representation of current transport at the interface in a *n*-channel MOSFET. (b) Major limiting factors of channel mobility in *n*-channel MOSFETs[17]

As the carrier electrons in the inversion layer (*channel*) are transported along the direction of the tangential electric field (E_T), their velocity increases until they undergo several surface scattering process such as (a) surface phonon scattering due to the lattice vibrations,

(b) Columbic scattering due to the interface state charge and (c) surface roughness scattering due to the deviation of the surface [25, 17]. Consequently, the carrier mobility depends on these scattering processes. A schematic of the *n*-channel MOSFET, oxide-semiconductor interface with electric field components, interface traps, fixed oxide charge, ionized donors and the rough interface between the layers are shown in figure 3.21 (a).

High interface state (trap) density near to the conduction band edge results in electron trapping and Columbic scattering in 4H-SiC MOSFETs. This is considered as the major cause for the degradation in the *n*-channel mobility, and device characteristics (figure 3.21 (b)). When high normal electric field is applied , it increases the velocity of the carriers towards the surface and brings the inversion layer charge distribution further closer to the surface. Therefore, surface roughness scattering may be prominent when the device is operated at high gate bias.

Since both tangential electric filed (E_T) and electric field normal (E_N) to the semiconductor influence the velocity of the moving carriers, their effect has to be characterized separately.

Effective mobility (μ_{eff})

Effective mobility (μ_{eff})) of electrons in the inversion layer is defined as[25]

$$\mu_{eff} = \frac{\int_0^{x_i} \mu(x) n(x) dx}{\int_0^{x_i} n(x) dx} \tag{3.47}$$

where $\mu(x)$ and *n(x)* are the local mobility and free carrier concentration in the inversion layer at depth *x* from the oxide-semiconductor interface and x_i is the thickness of the inversion layer. Effective mobility is a measure of the conductance of the inversion layer and can be used to determine the channel resistance. Determination of the effective mobility is usually performed by using lateral MOSFETs with gate length *L* and width *W*. The drain current (I_D) versus drain voltage (V_{DS}) taken as $V_{DS} \rightarrow 0$ can be used to determine the drain conductance (g_d) and thereby, the effective channel mobility (μ_{eff}) can be extracted as follows.

$$g_d = \left.\frac{\partial I_D}{\partial V_D}\right|_{V_{DS}\rightarrow 0} = \mu_{eff} C_{ox} \frac{W}{L} (V_G - V_T) \tag{3.48}$$

$$\mu_{eff} = \frac{L}{WC_{ox}(V_G - V_T)} \frac{dI_D}{dV_D}\bigg|_{V_{DSsmall}} \tag{3.49}$$

Field-effect mobility (μ_{FE})

The application of a MOSFET is mostly characterized by its transconductance (g_m). The drain current (I_D) versus gate voltage (V_G) can be used to determine the transconductance (g_m) and thereby, the field effect channel mobility (μ_{FE}) can be extracted as follows.

$$g_m = \frac{\partial I_D}{\partial V_G} = \mu_{FE} C_{ox} \frac{W}{L}(V_D) \tag{3.50}$$

$$\mu_{FE} = \frac{L}{WC_{ox}V_D} \frac{dI_D}{dV_G} \tag{3.51}$$

Field-effect mobility is extracted by considering output (drain) current dependence on gate voltage (electric field normal (E_N) to the semiconductor). It is a very useful parameter to characterize the mobility limiting mechanisms, which occurs near to the semiconductor surface (surface phonon scattering, Columbic scattering due to interface traps and surface roughness scattering).

3.4 Summary

In summary, the fundamentals of MOS capacitors and properties of different bias regions has been discussed. Several interface trap characterization techniques for MOS capacitors have been introduced, including simultaneous high-low frequency capacitance-voltage (C-V) measurements, Gray-Brown technique, photo-assisted C-V measurements and Constant Capacitance Deep Level Transient Spectroscopy (CCDLTS) method. These methods have been extensively used in original research presented in the subsequent chapters.

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Chapter 4

Electronic properties of SiO_2/4H-SiC interface PART I
(i) P doped SiO_2 (ii) Plasma oxides

As we have discussed in the chapter 1, 4H-SiC is attracting lot of attention as a single crystal material for power electronic devices which can operate at high voltages, high temperatures, and high frequencies [1, 2, 3]. Although 4H-SiC MOSFETs have excellent features, the performance of these devices are far from theoretically expected, due to high near-interface state density (D_{it}) at the SiO_2/4H-SiC interface and low inversion layer mobility. The low channel mobility in 4H-SiC MOSFETs has been correlated with the high D_{it} energetically located close to the 4H-SiC conduction band-edge, and spatially located in the near-interfacial oxide region[4, 5, 6, 7]. Herein, we first provide background about thermal oxidation oxidation of 4H-SiC and reduction of interface trap by NO annealing. Next, we discuss about P doping of SiO_2 to form PSG gate dielectric and deep level transient spectroscopy measurements to determine the nature of the trap passivation in PSG gate dielectric. Following this, we examine the oxidation growth rates of the Si-face and a-faces of 4H-SiC by carrying out oxidation, in a plasma afterglow furnace.

4.1 Thermal oxidation of 4H-SiC

A unique advantage of SiC is that it is the only compound semiconductor that can be thermally oxidized to give high-quality SiO_2 [1]. Therefore, thermal oxides of SiC are utilized as a gate dielectric in metal-oxide-semiconductor (MOS) devices as well as to passivate the SiC surface. In general terms, the oxidation of SiC is more or less same as the oxidation of Si. However, the major difference from Si oxidation process is, the presence of carbon atoms, which is one

of the unit element in SiC crystal. Therefore, thermal oxidation of SiC is considerably more complicated than oxidation of Si. The oxidation of SiC is about one order of magnitude slower than that of Si for same growth conditions. Thermal oxidation of SiC can be expressed by the following simple equation:

$$SiC + \frac{3}{2}O_2 \rightarrow SiO_2 + CO \tag{4.1}$$

Based on the Deal Grove model[8] for oxidation of Si, Y. Song, et al.[9] proposed a modified Deal-Grove model to explain the thermal oxidation of SiC with the five-step process (i) transport of molecular oxygen gas to the oxide surface; (ii) in-diffusion of oxygen through the oxide film (iii) reaction with SiC at the oxide/SiC interface; (iv) out-diffusion of product gases through the oxide film; and (v) removal of product gases away from the oxide surface.

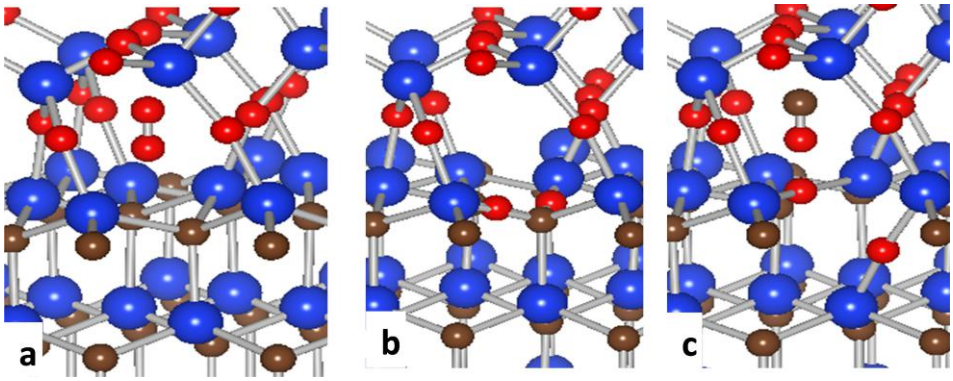

Figure 4.1: The oxidation of SiC is illustrated with ball-and-stick models. Blue balls are silicon atoms, brown balls are carbon atoms, and red balls are oxygen. (a)O_2 molecule approaching the SiC-Oxide interface. (b)O_2 breaking apart at interface to form stronger SiO and CO bonds.(c)the structure after a CO molecule is emitted leaving behind a V_CO_2 complex in SiC.[3]

Reconstructions at SiC-oxide interface during the oxidation can be explained by the three-step process as shown in figure 4.1 [3]. At an abrupt SiC-oxide interface, oxidation of a new layer of SiC starts with (a) O_2 molecule approaching the interface through the growing oxide, following (b) O-O bonds break apart to form the stronger Si-O-C bonds at the interface, and (c) carbon monoxide (CO) molecule leaving behind oxygen passivated carbon vacancy (V_CO_2) with only Si-O-Si bonds[3]. Most of the carbon atoms in SiC are expected to be removed by out diffuse as CO molecules. However, a small portion of carbon atoms are expected to be diffused into the SiC bulk region and leading to reduction of carbon-vacancy-related defects. It

is believed that carbon atoms still have high possibility to remain near the oxide/SiC interface and cause several types of defects near the oxide/SiC interface, such as carbon cluster, and carbon interstitials[3, 10, 11, 12].

4.1.1 Properties of the SiO_2/4H-SiC interface

High near-interface state density at gate dielectric SiO_2/4H-SiC interface known to be one of the major channel mobility limiting factors in 4H-SiC MOSFETs. While quantification of interface traps in SiO_2/4H-SiC system using different techniques has been reported in the literature, the exact origins of high interface state density for 4H-SiC is not very well understood. Theoretical considerations indicate that interface traps are: (i) carbon or Si-related defects (clusters, dangling bonds, vacancies) at the SiC/SiO_2 interface [13, 14, 10, 15, 16, 11, 17], (ii) defects formed in the bulk of SiO_2 [12, 18, 19, 20, 21], and (iii) physical stress in SiO_2/SiC stacks[22, 23].

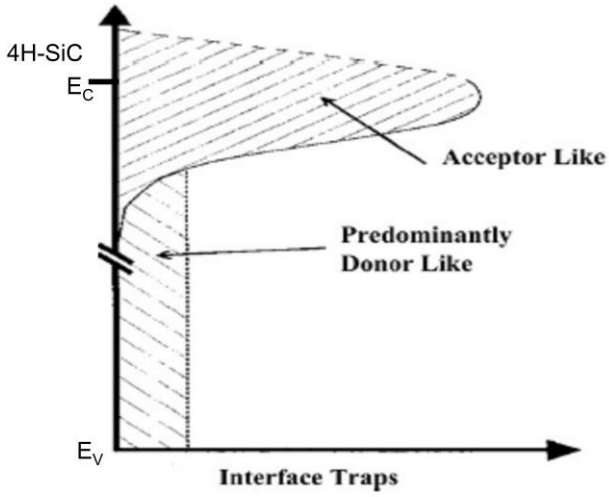

Figure 4.2: Qualitative representation of the interface trap distribution at the 4H-SiC-SiO_2 interface [7].

Interface trap measurements by different techniques have reported an exponential increase of interface state density near to the conduction band edge of 4H-SiC(0001). Although, the exact origins of these defects are still not very well understood, experimental investigations lead to a interface state distribution as shown in figure 4.2. When interface state density is very high, electrons are trapped in inversion layer and act as Coulomb scattering centers and cause very low channel mobility ($\sim$5-8cm^2/V$\cdot$s) in 4H-SiC *n*-channel MOSFETs (without any post

oxidation treatments) [1, 4, 24, 25]. In general, the low channel mobility in 4H-SiC MOSFETs has been correlated with high D_{it} energetically located close to the 4H-SiC conduction band-edge, and spatially located in the near-interfacial oxide region.

4.1.2 Interface nitridation

Reduction in interface traps is needed for developing high performance 4H-SiC MOSFETs. In this regard, post-oxidation annealing (POA) is one of the key methods to passivate the interface traps. In Si technology, well-established POA method is hydrogen passivation which is known to be very effective in reduction of D_{it} due to the passivation of Si dangling bonds at the SiO_2/Si interface. However, in the case of 4H-SiC, the oxide-semiconductor interface is entirely different and effect of similar hydrogen annealing process on interface states are not as dramatic[1]. The most established approach for trap passivation of SiO_2/4H-SiC interfaces involve the nitridation of SiO_2. Post-oxidation annealing in nitric oxide (NO) [26, 27, 31], nitrous oxide (N_2O)[28, 29] ambient or plasma of N [30] result in a reduction in D_{it} by incorporation nitrogen atoms into the interface region. Figure 4.3 shows D_{it} evaluated by conventional high (1 MHz)-low method on 4H-SiC MOS structures. As shown in figure 4.3, it is evident that nitridation achieves reduction in the interface state density over the entire range of energies within the bandgap.

4.2 Phosphosilicate glass (PSG) gate dielectric

Okamoto et al.[32, 33] first demonstrated that conversion of SiO_2 into a phospho-silicate glass (PSG) via annealing in phosphoryl chloride ($POCl_3$) results in $\sim$3 times higher channel mobility ($\sim$90cm^2/V$\cdot$s) compared to a standard nitrided interface[32, 33]. Conversion of SiO_2 into phosphosilicate glass (PSG) causes an almost uniform distribution of phosphorus in the gate oxide. The correlation of interface trap density and P coverage at the interface has been reported recently[34]. The results indicate that the P incorporation both at the PSG/SiC interface and in the bulk decreases as increases in annealing temperature.

In addition, P inclusion into the gate oxide layer is also causes SiC surface doping[35, 36], which also known as counter doping. This effect is linked to the group V elements, i.e. they act

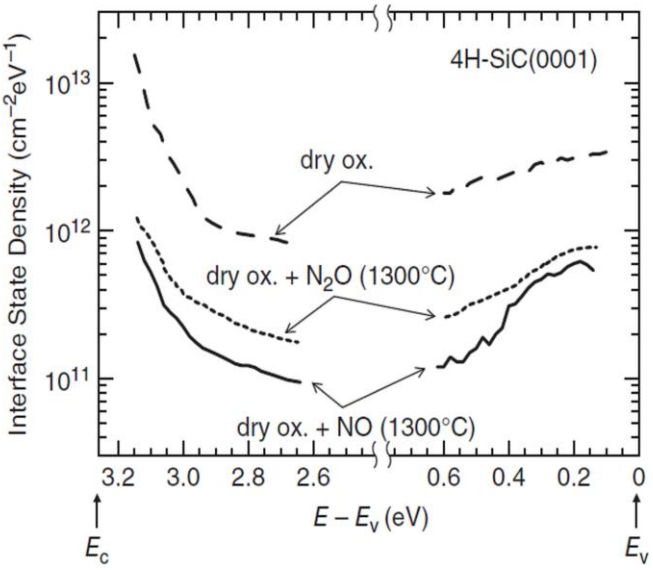

Figure 4.3: Distribution of interface state density near the conduction and valence band edges obtained from *n*- and *p*-type 4H-SiC(0001) MOS capacitors, respectively [1].

as donors when they accumulate at the SiO_2 /SiC interface and convert the doping type (from *p* to *n*) in a very thin layer ($\sim$10 nm) at the SiC surface. Therefore, the higher channel mobility in PSG/4H-SiC MOSFETs is attributed due to a combination of low D_{it} at PSG/4H-SiC interfaces and channel surface doping by phosphorus. However, the formation of a phospho-silicate glass (PSG) introduces polarization charges in the dielectric[37], which results in threshold-voltage instability and remains as an intrinsic problem for further practical application of this exciting gate dielectric[34, 38, 39]. While, quantification of electron traps in the PSG/4H-SiC system using different techniques has been reported in the literature[32, 33, 38, 34, 40, 41, 42], systematic investigation to identify the origin of the traps and the nature of the trap passivation mechanisms are sparse.

4.2.1 PSG formation and sample matrix

The samples used in this work were square pieces (5 mm$\times$ 5 mm) diced from Si-face *n*-type 4H-SiC wafers doped with nitrogen at $\sim 2\times10^{16}$ cm^3. Gate oxides were formed by dry oxidation at 1150 °C to grow oxide thickness of $\sim$60 nm. After oxidation, the samples were annealed at 1000 °C (PSG1000) and 1100 °C (PSG1100) for 15 min in a gas mixture of $POCl_3$, O_2, and N_2 to convert the SiO_2 into phospho-silicate glass (PSG). Figure 4.4 shows the schematic of

the phosphoryl chloride ($POCl_3$) annealing process for PSG formation. In this process, $POCl_3$ vapor is transferred from the bubbler into the furnace tube by flowing N_2 (flaw rate at 100 sccm) through the bubbler. Inside the furnace tube, $POCl_3$ vapor reacts with O_2 (flaw rate 133 sccm) and generate phosphorus pentoxide (P_2O_5). Meanwhile, P_2O_5 diffuses into the SiO_2 due to the additional N_2 flaw at 300 sccm (drive-in) and convert SiO_2 to PSG gate dielectric. PSG is composite with chemical formula $(P_2O_5)_x(SiO_2)_{1-x}$, where x is the mole fraction of P_2O_5. It has been reported that P doping of SiO_2 at 1000 °C results in higher phosphorus concentration in the PSG ($\sim$5%) compared to that doped at 1100 °C ($\sim$4%).

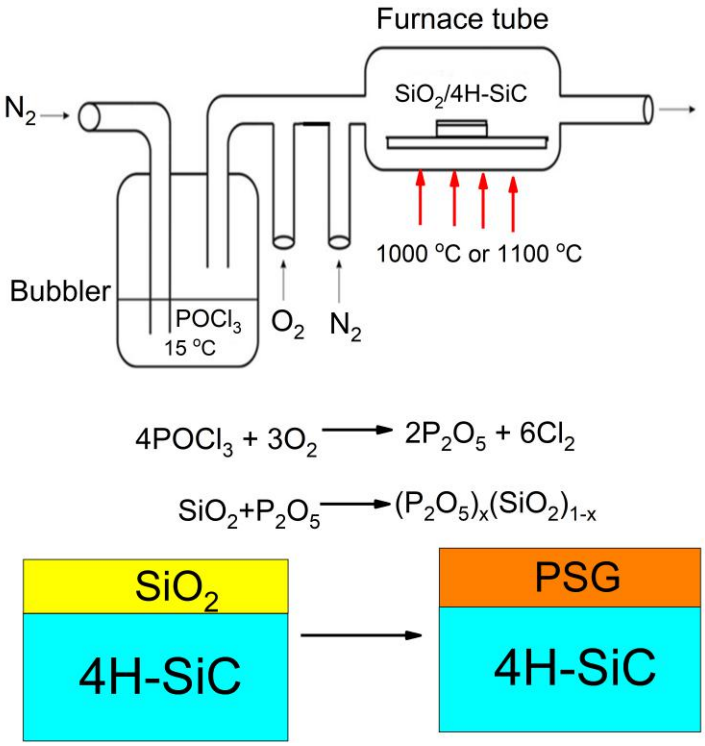

Figure 4.4: Schematic of PSG formation

For comparison, reference samples were also fabricated with gate oxides formed by dry oxidation followed by annealing in nitric oxide (NO) at 1175 °C for 2 hours (NO120). Following this, circular gate contacts with a diameter of 500 μm were formed by thermally evaporating Aluminum (Al) by using a shadow mask. The thermal evaporation was performed under a pressure of $\sim 7\times10^{-6}$ Torr using Al (99.999%) pellets and a tungsten basket heater. Subsequently, after removal of the oxide from the backside, samples were packaged on a copper substrate and wire-bonded for electrical characterization.

4.2.2 Low temperature *C-V* analysis

First, 'Gray-brown technique' was carried out by performing small signal *C-V* measurements using 1 MHz frequency at 77 K and 298 K on these MOS capacitors (see section 3.2.2 for technical details about the technique). Figure 4.5 shows typical *C-V* characteristics at room temperature and 77 K, for the NO120, PSG1100 and PSG1000 4H-SiC MOS capacitors. The NO120, *C-V* curves shift towards more positive voltages compared to PSG samples as the temperature is reduced.

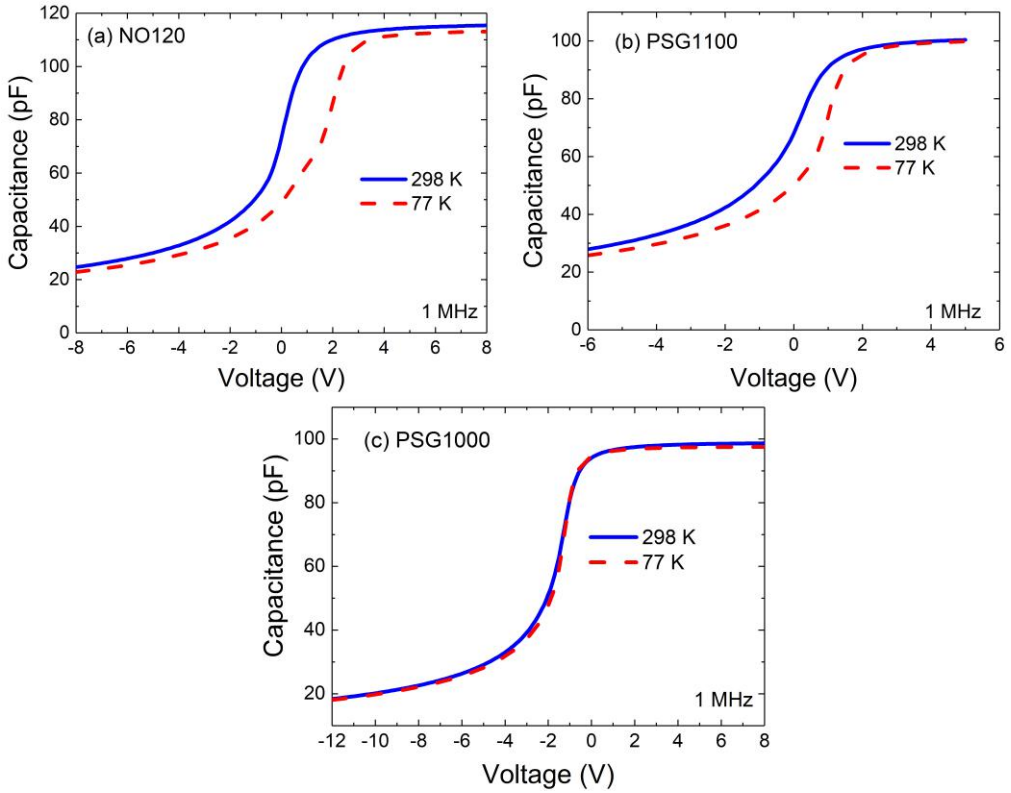

Figure 4.5: Temperature dependent 1 MHz *C-V* curves showing the flat band voltage shift with temperature for (a) NO120 (b) PSG1100 and (c) PSG1000 4H-SiC MOS capacitors. At each temperature, the voltage was scanned from accumulation to depletion.

As we discussed in section 3.2.2 , using the flat-band voltage shift and equation 3.38 , an effective density of near-interface states (N_{it}), energetically between ∼0.05 eV to ∼0.2 eV below the conduction band-edge (E_C) of 4H-SiC has been estimated [43, 44, 45]. The calculated N_{it} values are shown in Table 4.1. The flat-band voltage shift, ΔV_{FB}, for PSG1000 was below the detection limit of the measurements, demonstrating the significant reduction of N_{it} compared to NO120. The PSG1100 samples, with lower P concentration compared to PSG1000,

also shows a reduction in N_{it} compared to NO annealing, but the effect is smaller. This result confirms that P doping in SiO_2 results in a greater reduction of N_{it} compared to NO annealing.

Sample Info	Gray-Brown ~0.05-0.2 eV N_{it} ($\times 10^{11}$ cm^{-2})
NO120	6.65
PSG1100	3.68
PSG1000	Below detection limit

Table 4.1: N_{it} values from Gray-Brown technique on NO120 and PSG1100 MOS capacitors.

4.2.3 Constant Capacitance Deep Level Transient Spectroscopy (CCDLTS) measurements

The constant capacitance deep level transient spectroscopy (CCDLTS) technique is appropriate for measuring thermal emission rates of electron traps in 4H-SiC MOS systems[20, 46]. Here, CCDLTS measurements in the temperature range 77 K-298 K were performed to detect the dynamics of electron emission from near-interface traps in the oxide as described in chapter 3[20]. In this work, the upper limit of the temperature range was 298 K, to minimize effects of polarization charge in the PSG. Figure 4.6 shows the series of CCDLTS spectra taken with increasing trap filling pulse voltages (V_P) in the temperature range 77 K-298 K on the NO120, PSG1100 and PSG1000 4H-SiC MOS capacitors. The spectra for all three samples show two broad peaks with different magnitudes, but it is evident that the amplitudes of the peaks are significantly lower for the PSG1000 sample.

As we discussed in section 3.2.4, in CCDLTS, a feedback circuit adjusts the voltage applied to the MOS capacitor to hold the capacitance at a constant value with the sample biased in deep depletion. A 25ms trap filling voltage pulse (V_P) is periodically applied to charge and discharge the traps[20, 45, 46]. The thermal emission from traps having a single energy level decays exponentially in time, and therefore the corresponding voltage transient decays exponentially. The emission rate (e_n) of trapped electrons is given by (see chapter 2.4.1 for derivation)

$$e_n = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-(E_C - E_T)}{kT}\right) \tag{4.2}$$

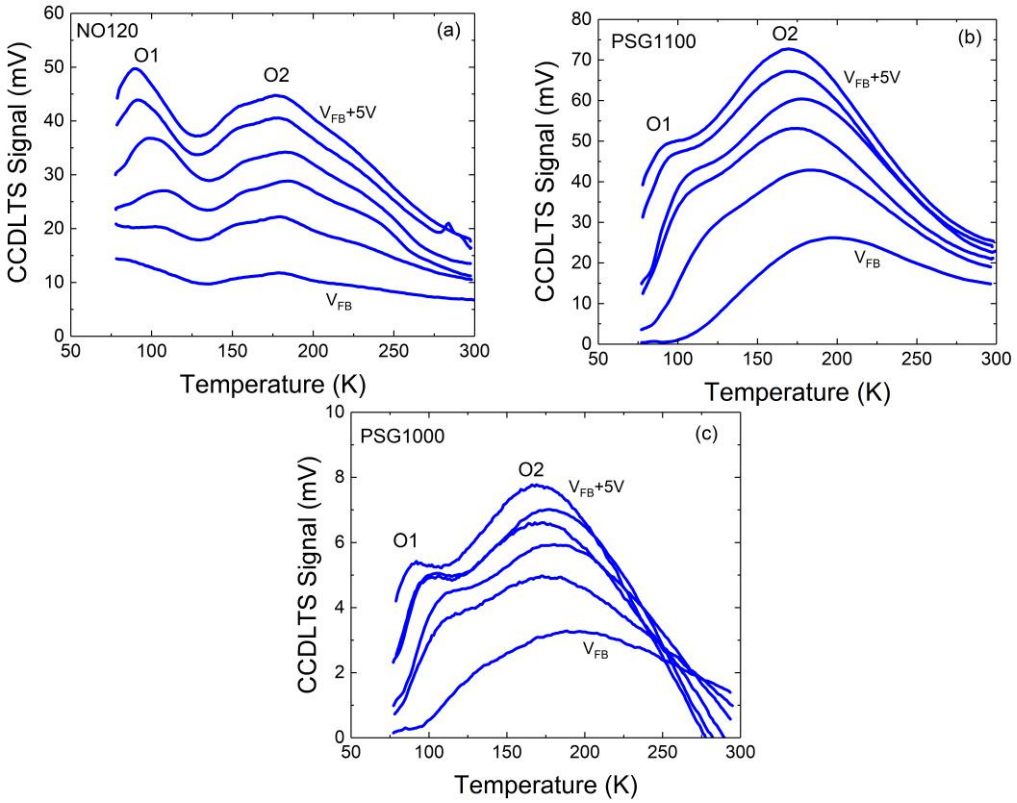

Figure 4.6: CCDLTS spectra with increasing filling pulse voltage for (a) NO annealed for 120 min (b) PSG 1100 °C and (c) PSG 1000 °C samples. The constant capacitance was 37 pF and the electron emission rate was 116.27 s^{-1}.

where $E_C - E_T$ is the emission activation energy of the trap level, σ_n is the electron capture cross section, $\upsilon_{th} = \sqrt{3kT/m_e^*}$ is the electron thermal velocity, $N_C = 2(2\pi m^* kT/h^2)^{3/2}$ is the effective density of states in the conduction band for electrons, and $m^* = 0.36m_o$ [47] is the effective mass for 4H-SiC. For the CCDLTS measurements reported here, the voltage transient after the filling pulse was monitored as a function of temperature and measured at two different times t_1 and t_2, with t_2=2.5t_1, that determines the spectrometer rate window (τ_{max}^{-1})[48]. The resulting CCDLTS signal, ΔV= V(t_1)-V(t_2), is a maximum when the emission rate of the traps, e_n, is equal to the spectrometer rate window (τ_{max}^{-1})[48]. The activation energy (E_C-E_T) and the capture cross section σ_n can then be determined from the slope and intercept of the Arrhenius plot of ln(T^2/e_n) versus 1000/T, respectively, where T is the temperature of the CCDLTS peak maximum and e_n is the instrument rate window.

Example of CCDLTS spectra for NO120 and PSG1100 samples using various rate windows with a filling voltage of V_P=V_{FB}+5V are shown in figure 4.7 (a), and figure 4.7 (c).

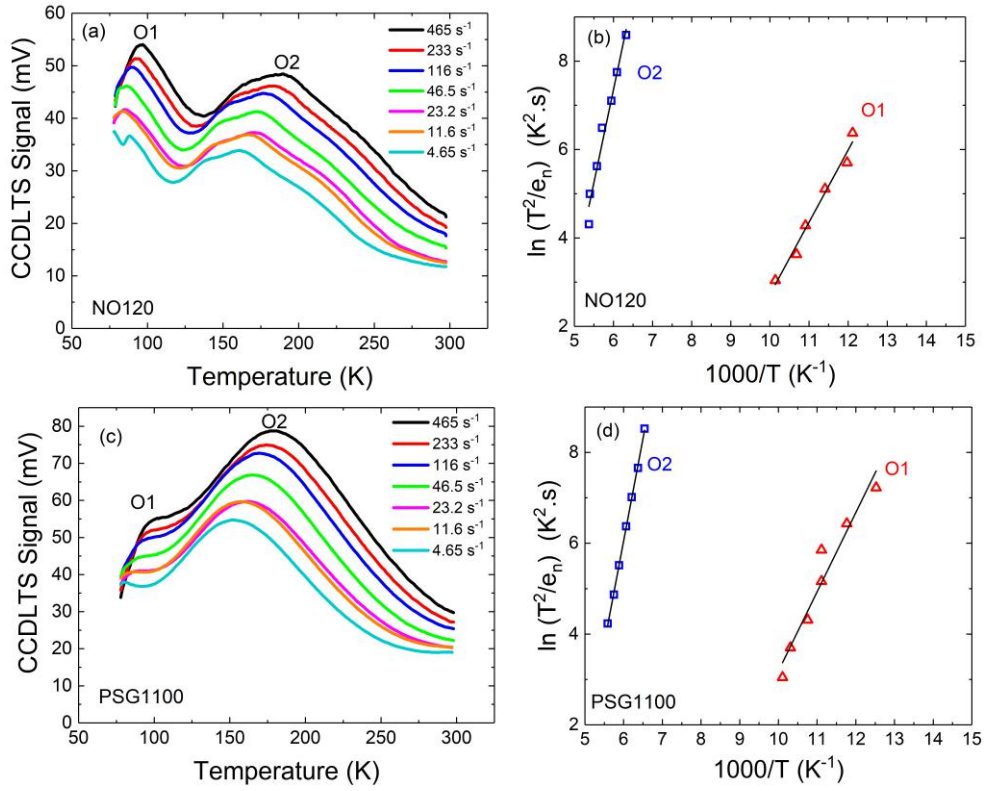

Figure 4.7: Example of CCDLTS spectra with various rate windows for (a) NO120 sample and (c) PSG1100 sample. (b) and (d) are Arrhenius plots of the two peaks shown in (a) and (c). The constant capacitance was 37 pF and the filling pulse voltage V_P=V_{FB}+5V.

Furthermore, Arrhenius plots for two peaks observed in the CCDLTS spectra are shown in figure 4.7 (b), and figure 4.7 (d). The analysis was carried out for three to five devices on each sample and extracted values of trap activation energy (E_C-E_T) and trap cross-section (σ_n) for the observed peaks in samples NO120, and PSG1100 are shown in Table 4.2. The spectra in figure 4.6 (c) for PSG1000 show shifting peak maxima at a constant rate window and therefore the thermal emission rate and capture cross section could not be accurately calculated for this sample. But the similarity of the activation energies and capture cross-sections between NO120 and PSG1100 strongly suggest that traps in these two samples have the same physical origin. These two broad peaks, named O1 and O2, [20] are typically observed in different thermal oxides on 4H-SiC[20, 45, 49, 50]. The physical origin of these defects has been attributed to carbon dimers substituted for O dimers (C_O=C_O) in SiO_2 and interstitial Si (Si_i) in SiO_2 [14, 12, 20].

In the case of a MOS capacitor, the resulting voltage transient (CDDLTS signal) is expected to increase with the increase of filling voltage above flat-band voltage ($V_P > V_{FB}$) since

the N_{it} density increases exponentially near the conduction band edge but it is expected to saturate at a certain filling voltage if all the traps were spatially located at the physical interface. However, in 4H-SiC, the shallow traps also spatially extend into the oxide and communicate with the 4H-SiC via electron tunneling. As a result, saturation of the CCDLTS signal is typically not observed as trap filling increases with higher electric field or higher filling pulse. Therefore, to compare different interfaces, the spectra are compared at the same V_P-V_{FB}. The amplitude of the CCDLTS signal is directly proportional to the trap density, and the areal density of the near-interface traps were calculated by equation 4.3[20].

$$N_{it} = \frac{3 \times (C_{ox}/A)\Delta \mathrm{V}(T_o)\Delta \mathrm{W}}{q} \tag{4.3}$$

where the factor of 3 (see Appendix C)arises from the sampling times t_1 and t_2 (t_2=2.5t_1) of the voltage transient in the DLTS spectrometer,[20] $\Delta \mathrm{V}(T_o)$ is the maximum CCDLTS signal when V_P=V_{FB}+5V at the peak temperature T_o and ΔW is a broadening factor, which is the ratio of the integral of the experimental CCDLTS signal ΔV over the measured temperature range to the integral of the intensity of a theoretical CCDLTS peak for a trap having a single energy level. The previously calculated broadening factors for O1 and O2 are 4 and 6 respectively[20]. The $\Delta \mathrm{V}(T_o)$ for the O1 trap was determined by extrapolation of the low temperature tail of the O2 peak down to the O1 peak temperature and then subtracting its contribution from the O1 peak signal. Example of $\Delta \mathrm{V}(T_o)$ measurement step for O1 and O2 peak in NO120 sample is shown in figure 4.8.

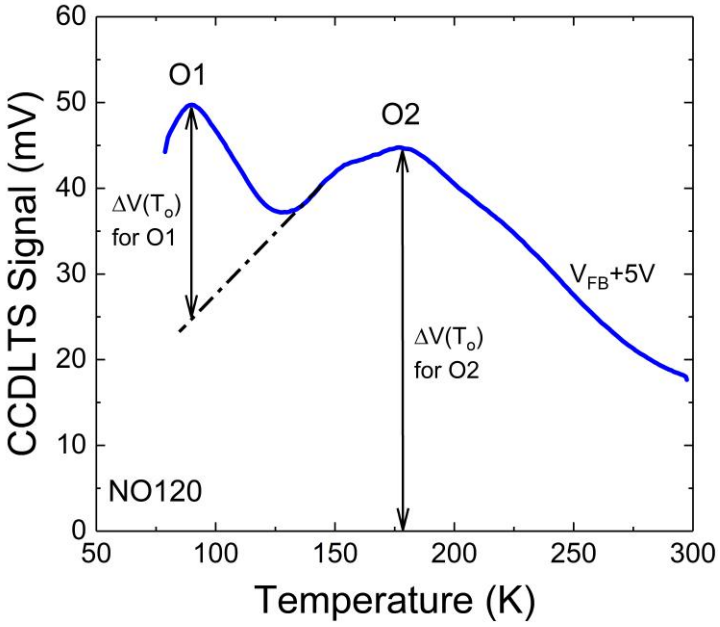

Figure 4.8: CCDLTS signal amplitude for O1 and O2 trap peak

Sample Info	O1			O2		
	E_C-E_T (eV)	σ_n (cm^2)	N_{it} (cm^{-2})	E_C-E_T (eV)	σ_n (cm^2)	N_{it} (cm^{-2})
NO120	0.15	1×10^{-15}	1.21×10^{11}	0.35	2×10^{-14}	2.97×10^{11}
PSG 1100	0.15	1×10^{-15}	3.12×10^{10}	0.38	7×10^{-13}	4.14×10^{11}
PSG 1000	-	-	4.84×10^{9}	-	-	4.76×10^{10}

Table 4.2: Emission activation energies (E_C-E_T) , electron capture cross section (σ_n) and density of the near-interface raps N_{it} extracted from the CCDLTS spectra. The values given are the average of measurements from three to five devices on each sample. The standard deviation (SD) of the N_{it} values is $<$18%. The SD of the E_C-E_T is $\pm$0.01 eV. The scatter in σ_n values was about an order of magnitude for NO120 but nearly two orders of magnitude for PSG 1100.

N_{it} values obtained from CCDLTS are shown in Table 4.2. These new results show that the concentration of the O1 trap is about two orders of magnitude ($\sim10^9$ cm^{-2}) and the O2 trap is about one order of magnitude ($\sim10^{10}$ cm^{-2}) lower in the PSG1000 compared to NO120 samples. On the other hand, PSG1100 samples, with lower P concentration, show a reduction for the shallower O1 trap only. This large reduction in O1 and O2 near-interfacial oxide traps in PSG/4H-SiC MOS system results in the high channel field-effect mobility (105 cm^{2}V^{-1}s^{-1}) in PSG/4H-SiC MOSFETs[34, 42].

4.2.4 O1 and O2 trap passivation mechanism by phosphorus

The DLTS results were correlated to the first-principles calculations to identify physical structure of defects in PSG gate dielectric. The First-principle calculations were performed by Dr. X. Shen, Dept. of Physics and Materials Science, University of Memphis. The density functional theory (DFT) calculations were carried out in a 114-atom unit cell of amorphous SiO_2 constructed by a Monte-Carlo bond-switching method with the use of PBE exchange-correlation functional, plane-wave basis, and PAW potentials implemented in the VASP code. The kinetic energy cutoff of the plane-wave basis is 212 eV. Brillouin zone sampling is done with single k-point at (1/4, 1/4, 1/4).

As we have mentioned earlier, the O1 and O2 traps are suggested to be the C_O=C_O defects and Si interstitials (Si_i) in the near-interfacial oxide, respectively. Figure 4.9 shows the geometry of C_O=C_O and Si_i in SiO_2[14, 12]. The C_O=C_O defect has a double bond and reported to be arise from the transformation of carbon pairs (C_i=C_i) formed at the interface during oxidation[12]. Silicon interstitials (Si_i) are known to be created in SiO_2 during the oxidation of SiC due to the interstitial silicon atom pushing an oxygen out of its place and making a Si-Si-Si bridge instead of a Si-O-Si bridge[12].

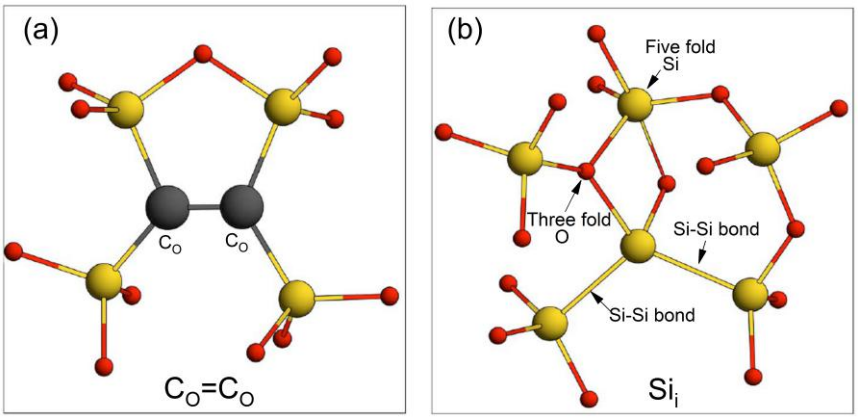

Figure 4.9: (a) Carbon dimers substituted for O dimers (C_O=C_O) in SiO_2 (b) Interstitial Si (Si_i) in SiO_2. Silicon: larger yellow; oxygen: smaller red; and carbon large black spheres[12].

So far, trap passivation mechanism by phosphorus is partially understood. It has been reported that, at the interface as well as in the bulk PSG layer, P is primarily bound to O atoms,

which are themselves bonded to Si or C atoms[51]. This suggests that the trap passivation mechanism due to P may be related to re-arranging the critical interfacial dielectric layer, relieving interface stress and possibly allowing better passivation of the dangling bonds[51]. Accordingly, the effect of phosphorus on near-interface traps can be summarized by the following theories reported in the literature: (1) the P atoms act as a network former and the result in reconstruction of the oxide network in SiO_2 (Si-Si bonds elimination)[33, 38, 51] (2) C related defects are removed by the P doping of SiO_2[38, 52, 53, 54] where threefold carbon atoms at the interface are replaced by P=O group[38]. In this regard, it has been reported recently that $POCl_3$ annealing can form a peculiar O_3PO structure which can act as a carbon absorber[38, 52, 53, 54]. While theory in (2) explains passivation of a single three-fold carbon defect, it cannot explain the elimination of C_O=C_O defects, as this defect is very compact and there is not enough space to accommodate P=O group that is much larger than a single carbon. Therefore, a different mechanism must be in play in reducing the C_O=C_O defects. Also, how the PSG annealing reduces Si interstitials needs to be elucidated.

As shown in figure 4.10 (a), C_O=C_O defect features a carbon double bond with large bonding energy, which makes the C_O=C_O defects very stable against annealing. Through first-principles calculations, it was found that P substitution of the Si atoms bonded to the C_O=C_O defect (figure 4.10 (b)-(e)) weakens the carbon double bond, as indicated by the increase of the bond length. Therefore, P doping at nearby Si sites reduces the stability of the C_O=C_O defects and makes them easier to anneal them out. The same mechanism is also at play in the additional oxidation SiC during PSG annealing, and suppresses the formation of C_O=C_O defects at the newly formed near-interface oxide layer.

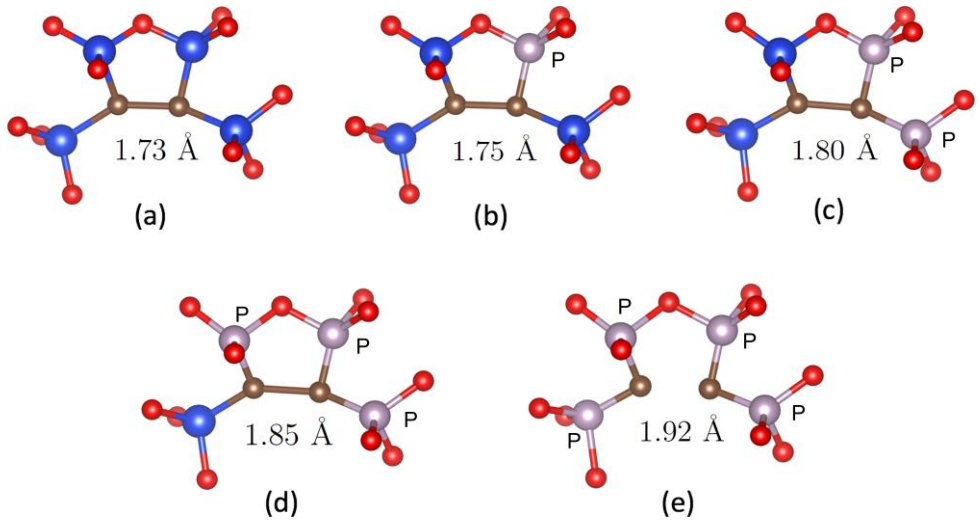

Figure 4.10: Atomic structures of the C_O=C_O defect. (b)-(e) Structures of C_O=C_O defect after P substituting 1-4 Si atom(s) bonded to the defect. All structures are relaxed. Si in blue, O in red, and P in purple. First-principle calculations were performed by Dr. X. Shen, Dept. of Physics and Materials Science, University of Memphis.

For the Si interstitial (Si_i), it should be noted that this defect has a complex structure consisting of several electrically active centers (figure 4.9 (b)): two Si-Si bonds, one three-fold oxygen, and one five-fold Si[12]. Upon P atom incorporation, the Si-Si bonds and three-fold oxygen can be eliminated through the network restructuring, while the five-fold Si atom can be substituted by a P atom and become electrically inert. In this way, the areal density of near-interface Si interstitial defects can be reduced. Comparing NO annealing (NO 120) to the best PSG annealing (PSG1000), it is clear that the best PSG outperforms NO annealing in reducing O1 and O2. We note that NO annealing does not lead to network restructuring as PSG does, and thus is less effective in reducing the Si interstitial (Si_i). Also, while P atoms replace Si atoms in SiO_2 during annealing, N atoms are likely to replace O or C atoms. Therefore, N atoms cannot weaken the carbon double bond in the C_O=C_O defect in the way P atoms do. As a result, NO anneal is less effective in reducing the O1 and O2 defects compared with PSG.

4.3 Motivation for plasma oxidation

4H-SiC power DMOSFETs [1, 2, 3] are regarded as one of the most promising power switching device for high voltage applications. However, in the power DMOSFETs, internal resistance in the current flow path limits the current handling capability and increase the power dissipation. Therefore, total device resistance ($R_{ON,SP}$) is a useful parameter to evaluate on-state power loss in vertical power MOSFET. Figure 4.11(a) shows the cross-section of a full DMOSFET cell including the important resistance components[1].

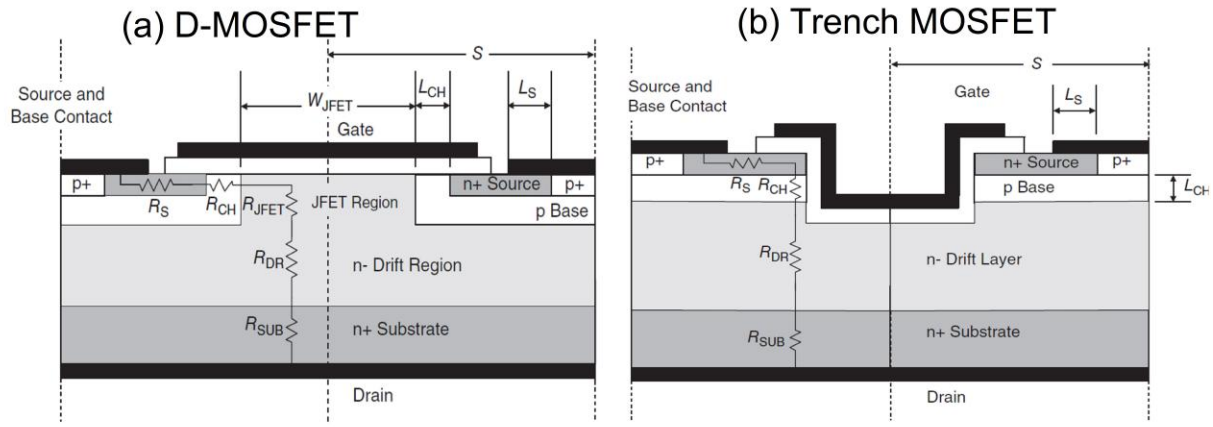

Figure 4.11: (a) Power D-MOSFET structure with its internal resistances (b) cross-section of a full trench MOSFET cell showing the important resistance components [1].

Trench MOSFET is an important device design for 4H-SiC power MOSFETs, as it offers low specific on resistance and higher current densities, which can potentially reduce device cost[1, 2, 3, 55, 56, 57, 58, 59]. More recently, high voltage range (1200V) 4H-SiC trench MOSFET has been introduced to the market by Infineon Inc. [60]. Figure 4.11 (b) shows the major resistances in the trench MOSFET device[1]. Trench device geometry effectively eliminates the JFET resistance present in the DMOSFET. Furthermore, trench MOSFET enables higher number of device per unit area and reduces the cell pitch. Therefore, $R_{DR,SP}$ will be reduced in these devices. 4H-SiC tench MOSFETs are typically fabricated using Si-face oriented wafers, where trench side walls may correspond to the a-face $(11\bar{2}0)$ or m-face $(1\bar{1}00)$. However, standard thermal oxidation process cannot be used for trench MOSFETs due to anisotropic thermal oxidation on different crystal faces which results in non-conformal oxide thicknesses on the trench bottom (Si-face) and the sidewalls (a-face or m-face).

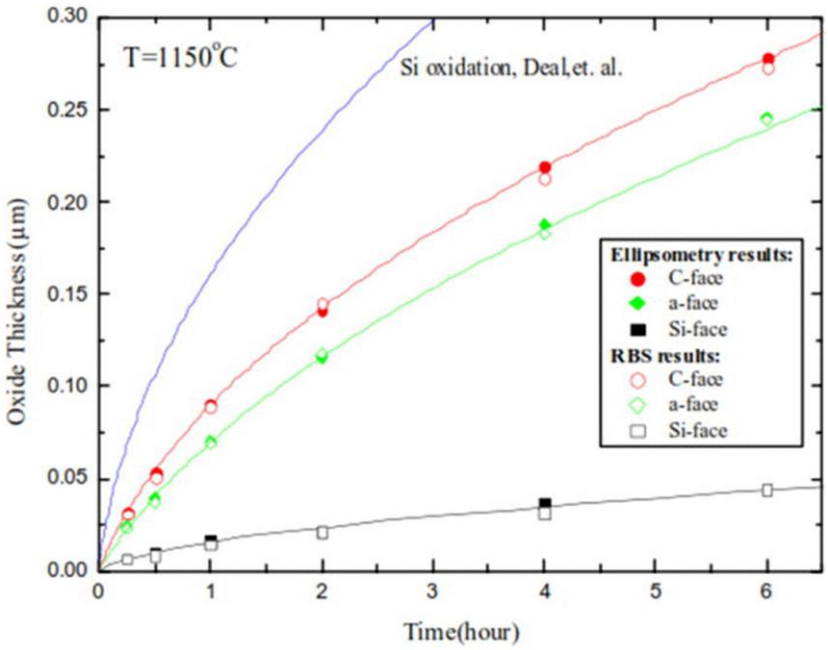

Figure 4.12: Oxide thickness as a function of time for dry thermal oxidation of the C-face, a-face, and Si-face of 4H-SiC at 1150 °C, the solid symbols are ellipsometer results, and the opened symbols are Rutherford backscattering spectrometry (RBS) results[3, 9]

.

Figure 4.12 shows oxide thickness versus the oxidation time for thermal oxidation of 4H-SiC at 1150 °C. It shows that C-face has the highest oxidation rate among three SiC faces and Si-face has the lowest rate, and it differs by a significant amount. Oxide growth in a-face also shows higher oxidation rate compared to Si-face. In 4H-SiC thermal oxidation, oxide thickness is almost proportional to oxidation time when the oxide is very thin (*surface-reaction-limited regime*). However, when the oxide becomes thick, oxidation gradually slowdown, and the oxide thickness becomes almost proportional to the square root of the oxidation time (*diffusion-limited regime*)[1, 9].

Interface state distributions of crystal faces of 4H-SiC are very different from each other. Figure 4.13 shows interface state density distributions for n-type 4H-SiC, Si-face (0001), C-face $(000\bar{1})$, a-face $(11\bar{2}0)$, m-face$(1\bar{1}00)$ MOS structures prepared by (a) as-oxidized and (b) as-oxidized with subsequent NO annealing [1]. It is apparent that NO annealing causes a drastic reduction in interface state density for all the crystal faces. On Si-face, interface states densities show a sharp peak near to the conduction band edge for both cases. However, interface state distributions show rather 'flat' behavior in non-standard faces (C-face, a-face, and m-face) of

4H-SiC. High channel mobilities on a-face 95∼115 $cm^2/V{\cdot}s$ and 45 $cm^2/V{\cdot}s$ on C- face have been also reported recently [1, 61]. The a-face results are promising for development of trench MOSFETs on Si-face 4H-SiC wafers, where the channel will be on a-face[62].

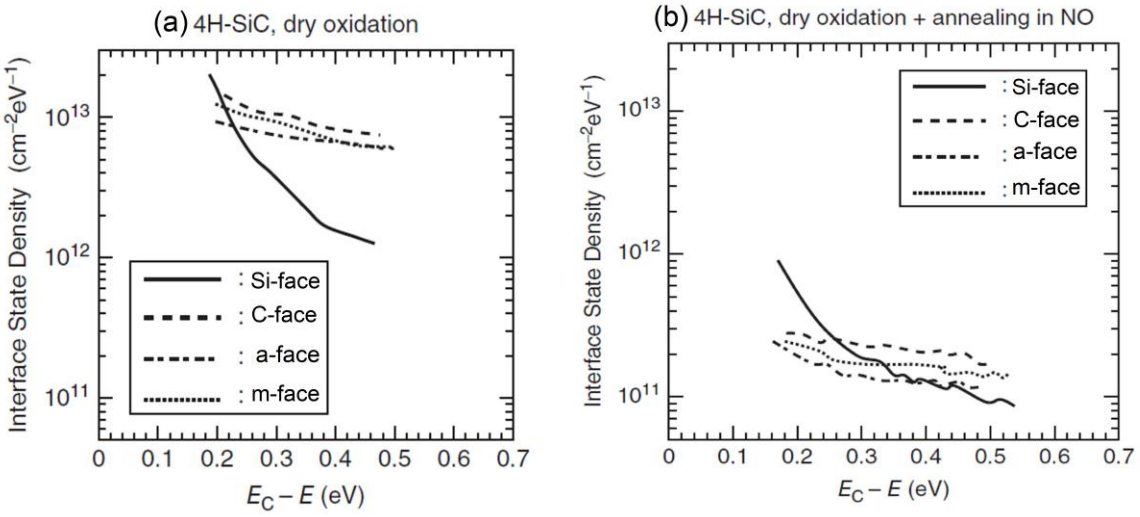

Figure 4.13: Interface state density distributions obtained from n-type 4H-SiC MOS structures on different crystal face prepared by (a) as-oxidized (b) oxidation followed by NO annealing [1].

4.4 Atomic oxidation of 4H-SiC by afterglow plasma oxidation

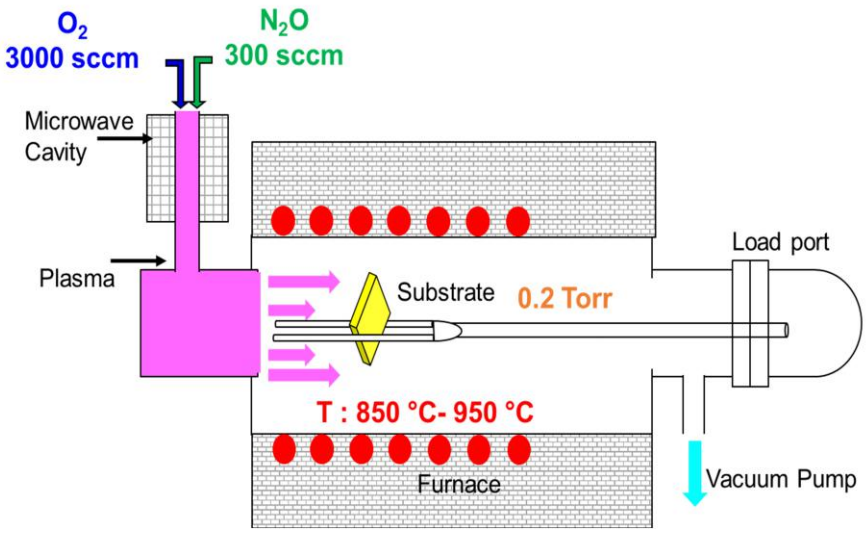

Figure 4.14: Schematic of afterglow thermal oxidation system

In afterglow plasma oxidation process, oxidation of the SiC occurs by the flow of the reactive atomic oxygen species generated by the exciting oxygen gas in a microwave discharge. A schematic of the microwave plasma furnace used in this work is shown in figure 4.14. The microwave excitation creates a plasma discharge and plasma afterglow species consisting of excited, unexcited neutral molecules and atoms enter the growth zone. In this process the RF source was set at 2 kW, 2.45 GHz, the chamber pressure was 0.2 Torr and gas flow rates were 3000 sccm O_2 and 300 sccm N_2O. Nitrous oxide (N_2O) was added as a radical agent to enhance the production of the atomic oxygen and serves no other known purpose [63]. The two principal oxidant species produced in plasma oxidation system are known to be ground state O and the singlet state (high-energy form of oxygen) of O_2, $O_2(a^1\Delta_g)$ also denoted as O_2^* [64]. Previous work has shown that about of $\sim 10^{15}$ cm^{-3} O atoms or O_2^* molecules flow in to the furnace for reaction with the semiconductor surface[64, 65].

In general, high oxidation rates at relatively low temperatures can be achieved by plasma oxidation process [64]. For example, to grow 70 nm oxide thickness on Si-face by thermal oxidation taken about 11 hour oxidation at 1150 $^\circ$C. However, plasma oxidation process take only 2 hour oxidation at 900 $^\circ$C to grow the same oxide thickness. The high oxidation rates by afterglow plasma oxidation at relatively low temperatures can be explained by considering following reasons.

(a) High concentration of reactants: In the thermal process alone, production of the necessary reactants for oxidation is controlled by the temperature of the process. However, in afterglow plasma oxidation, gaseous species can gain energy or be dissociated by the excited plasma discharge independent of the thermal environment[64, 65].

(b) Faster oxidation at the interface: X. Shen et al.[66] reported that SiC oxidation at the interface is dominated by an atomic oxygen mechanism. Therefore, growth rates are expected to be higher with the high concentration of atomic oxygen.

(c) Diffusion of the oxidant species in SiO_2: In thermal oxidation, molecular oxygen, O_2 need to diffuse through the passages between the void of the Si-O bond network. This results in *diffusion-limited oxide growth rate* when the oxide becomes thick. However, in the case of atomic oxygen, the situation is different. An atomic oxygen takes the form of Si-O-O-Si

peroxide linkage (bridge interstitial in a Si-O bond) and diffuses by hopping from one bond to another. Therefore dense oxide layer does not necessarily stop the atomic oxygen [66, 67].

4.4.1 Oxide growth rates on Si-face and a-face

To investigate the atomic oxidation and oxide growth rates, MOS capacitors were fabricated on Si-face (0001) and a-face ($11\bar{2}0$) *n*-type 4H-SiC epilayers. In the oxide growth process, plasma oxidation was carried out in the 850 °C - 950 °C temperature range for 2 hours. Following this, plasma oxidized samples were densified at 900 °C for 1 hour in N_2 500 sccm at atmospheric pressure. Subsequently, some samples were annealed in nitric oxide (NO) at 1175 °C for 2 hours (NO120) for trap pasivation. For comparison purpose, reference MOS capacitors with gate oxides formed by dry oxidation at 1150 °C (Si- face:10 hours and a-face:1 hour) followed by NO annealing (1175 °C for 2 hours) was also fabricated.

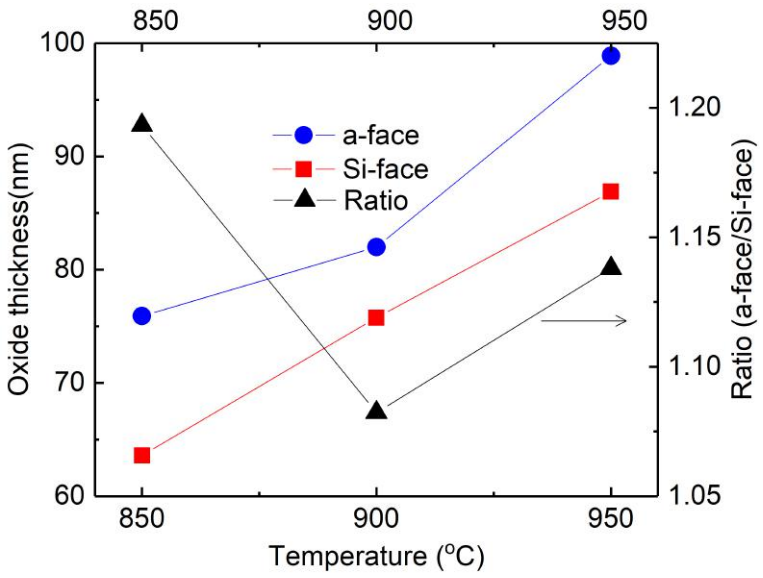

Figure 4.15: Oxide thicknesses after plasma oxidation at different oxidation temperatures for 2 hours and followed by 2 hour NO annealing

Shown in figure 4.15 are the oxide thicknesses extracted from *C-V* measurements on MOS capacitors, as a function of plasma oxidation temperature for Si-face and a-face samples. Oxide thickness (t_{ox}) is extracted by using following equation.

$$C_{ox} = \frac{A\epsilon_{ox}}{t_{ox}} \tag{4.4}$$

where C_{ox} is accumulation capacitance, A is device area and ϵ_{ox} is SiO_2 permittivity. The ratio of the oxide thickness grown on the two crystal faces suggests, 900 °C as the optimal temperature to obtain close to zero oxidation anisotropy by the plasma oxidation process. However, it is worthwhile to note that NO annealing at high temperature also causes re-oxidation of the interface and increases the oxide thickness. Figure 4.16 (a) shows the reported in the literature oxide thickness of the Si-face and a-face by thermal oxidation. We have included our plasma oxidation data for better comparison.

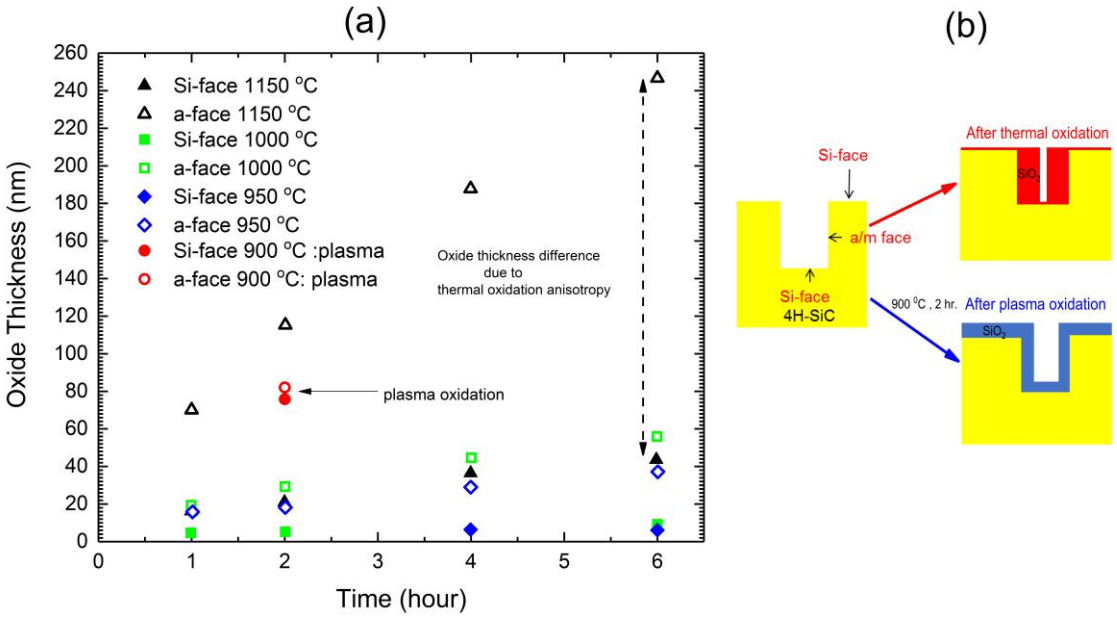

Figure 4.16: (a) Reported oxide thickness as a function of time and temperature for dry thermal oxidation of the Si-face and a-face by Y. Song et al.[3, 9]. We have included 900 °C 2 hr. plasma oxidation data for better comparison (b) Schematic illustration of expected oxide thickness in side wall and bottom of the trench due to oxidation processes

The minimal oxidation anisotropy by the plasma oxidation process is encouraging for the development of 4H-SiC tench MOSFETs. if plasma oxidation at 900 °C (optimal temperature) is used as the gate oxidation process,oxide thickness on the both side walls and the bottom are expected to be the same as shown in figure 4.16 (b).

4.4.2 Properties of plasma oxidized SiO_2/4H-SiC interfaces

As we have shown, 900 °C (optimal temperature) plasma oxidation process is a promising method for 4H-SiC power device development. However, it is crucial to obtain high-quality gate oxide and MOS interface by plasma oxidation method. In this regard, oxide quality comparison between the plasma oxide and well developed thermal oxide has been carried out.

Simultaneous high-low (hi-lo) frequency capacitance-voltage D_{it} profiles

To investigate SiO_2/4H-SiC interface properties, simultaneous high-low (hi-lo) frequency capacitance-voltage (*C-V*) characterization with high frequency of 100 kHz at room temperature was employed (see chapter 3, section 3.2.1 for detail description of the technique).

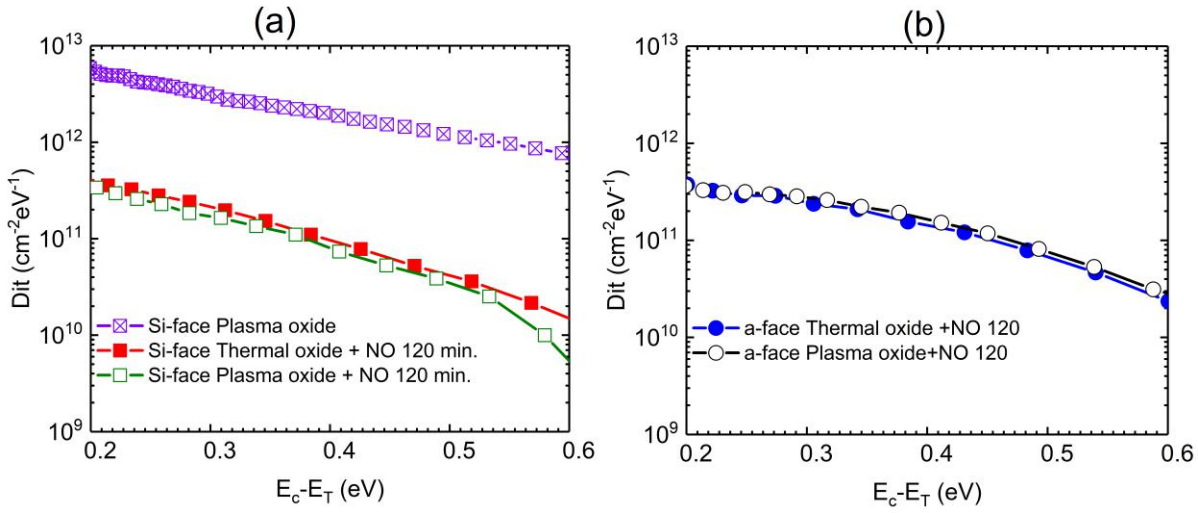

Figure 4.17: Hi-lo *C-V* extracted D_{it} comparison between Si-face and a-face capacitors with standard thermal and plasma oxidation

Figure 4.17 (a) shows the interface trap density (D_{it}) profiles for Si-face (0001) MOS capacitors with gate oxide grown by plasma oxidation (as-oxidized), followed by 1175 °C NO annealing and thermal oxidation (10 hour at 1150 °C) followed by annealing in NO. Figure 4.17(b) shows the D_{it} profiles for a-face ($11\bar{2}0$) MOS capacitors with gate oxide grown by plasma oxidation process followed by NO annealing (passivated) and thermal oxidation process(1 hour at 1150 °C) followed by NO annealing. As shown in figure 4.17 (a), as-oxidized interface by plasma oxidation suffer with higher interface trap densities near to conduction band

edge of the 4H-SiC . However, as it can be seen in figure 4.17 (a), greater reduction of these interface traps can be achieved by NO annealing process. Comparison of D_{it} profiles between the 900°C plasma oxidation process after 1175 °C NO annealing and reference thermal oxide annealed in NO under the same conditions shows similar profiles for both Si-face and a-face. This result suggests that SiO_2/4H-SiC interfacial electronic properties are dictated by the NO post-oxidation annealing step for both types of oxides.

Low temperature C-V measurements

Further interface trap investigation on plasma oxide was carried out by employing Gray-Brown technique as discussed in section 3.2.2. Calculated N_{it} values are shown in Table 4.3. The comparable values for N_{it} between two oxides confirms the observation of dictating property of NO post-oxidation annealing step.

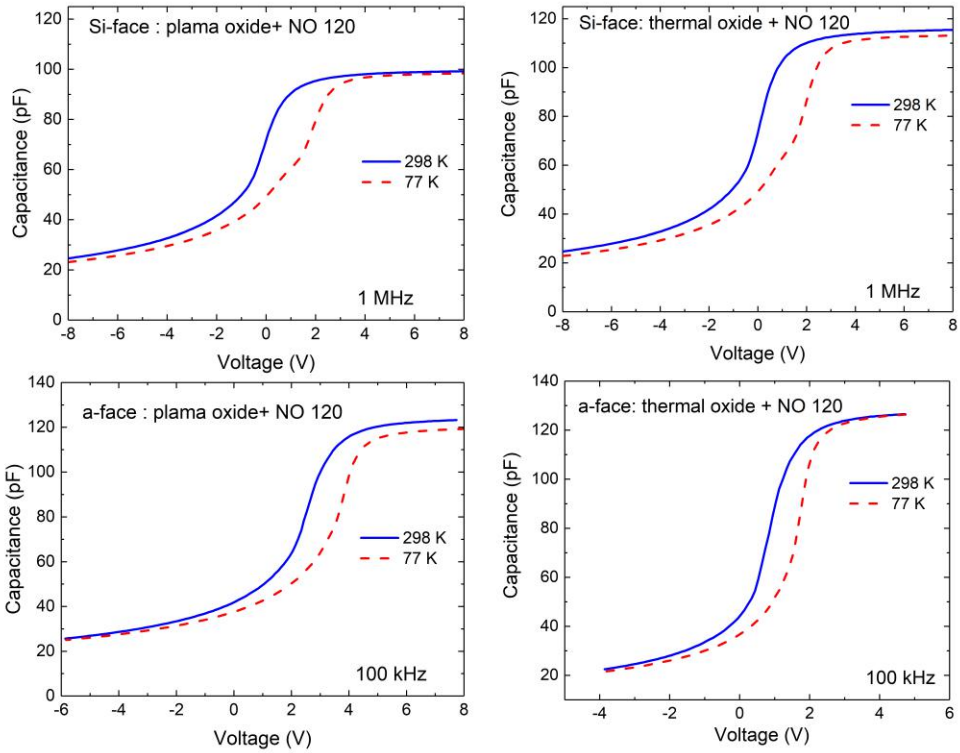

Figure 4.18: Temperature dependent high frequency *C-V* curves for Si-face and a-face MOS capacitors with standard thermal and plasma oxidation

Sample Info	Gray-Brown ∼0.05-0.2 eV $N_{it}(\times 10^{11}$ cm$^{-2})$
Si-face plasma oxide	5.0
Si-face thermal oxide	6.7
a-face plasma oxide	3.5
a-face thermal oxide	3.5

Table 4.3: N_{it} values from Gray-Brown technique .

Constant-Capacitance Deep Level Transient Spectroscopy (CCDLTS) measurements

After initial electrical testing, Si-face samples were repackaged and wire bonded to perform constant-capacitance deep level transient spectroscopy (CCDLTS) measurements. Figure 4.19 shows the series of CCDLTS spectra taken with increasing trap filling pulse voltages ($V_P > V_{FB}$) in the temperature range 77 K - 298 K on the Si face plasma oxidation MOS capacitor and compared with standard thermal oxidation sample. The two broad O_1 and O_2 peaks with activation energies of 0.13 eV and 0.33 eV and capture cross sections of 1×10^{-16} cm^2 and 1×10^{-15} cm^2 respectively, were observed in plasma oxide as well. In section 4.2.4 we have discussed about origin of the O_1 and O_2 trap and N_{it} value calculation has been already discussed in section 4.2.3. The N_{it} obtained from CCDLTS measurements are shown in the Table 4.4

Sample Info	O1 N_{it} $(\times 10^{11}$ cm$^{-2})$	O2 N_{it} $(\times 10^{11}$ cm$^{-2})$
Si-face plasma oxide	1.0	2.55
Si-face thermal oxide	1.21	2.97

Table 4.4: CCDLTS measurements extracted N_{it} values.

These results confirm that the nature of the near interfacial oxide traps of the plasma oxide is similar as thermal oxide. Furthermore, comparable N_{it} values by CCDLTS measurements shows the dominating behavior of NO annealing step.

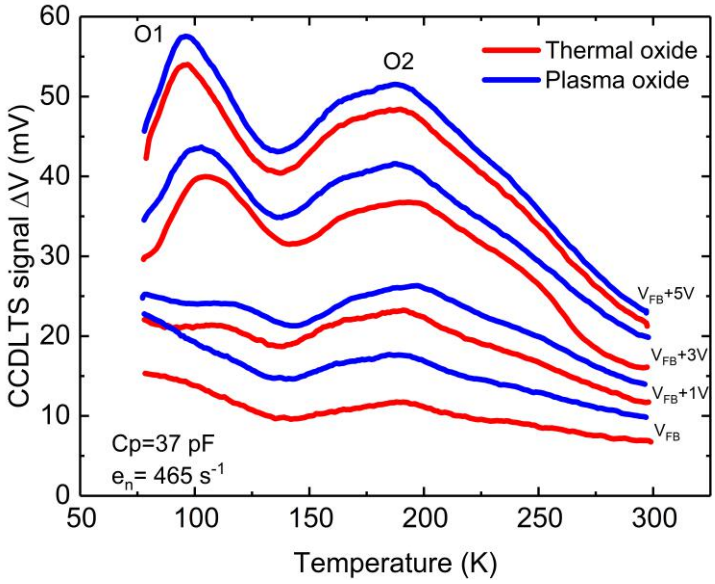

Figure 4.19: CCDLTS for detection of near interface traps in Si-face samples using different trap filling voltages in accumulation.

Oxide breakdown strength

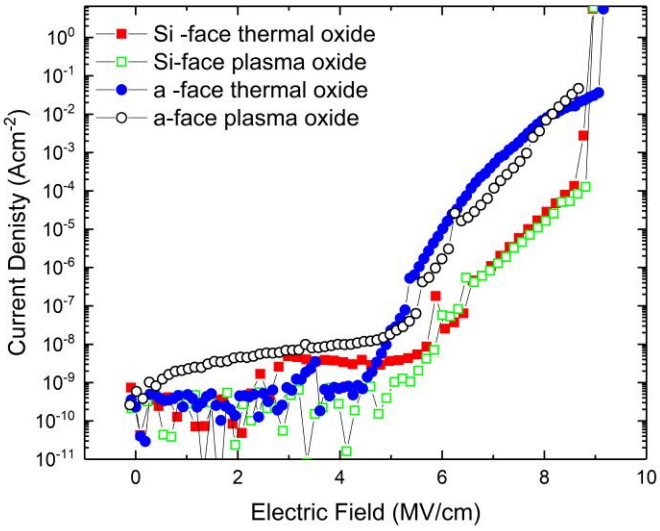

Figure 4.20: Current density- electric field characteristic of Si-face and a-face MOS capacitors in accumulation with plasma oxide and thermal oxide.

I-V measurements were carried out at room temperature in the dark using a Keithley 6517 electrometer/high resistance system to determine oxide breakdown strength. Figure 4.20 shows

the current density versus electric field characteristics acquired on these MOS devices. As can be seen in the figure 4.20, almost overlapped curves and comparable oxide breakdown fields indicate that the quality of the plasma oxide is similar to standard thermal oxide. Earlier breakdown of the a-face $(11\bar{2}0)$ MOS capacitors is likely due to lower quality of a-face wafer substrate used in this experiment.

4.5 Summary

• PSG/4H-SiC interfaces

Both 'Gray-Brown' technique and CCDLTS measurements results confirm that optimum P doping in SiO_2 results in a reduction of the energetically shallow near-interface trap density to an order of magnitude lower than standard nitrided thermal oxides. The CCDLTS measurements revealed that the two broad near-interface trap peaks, named O1 (E_C-0.15 eV) and O2 (E_C-0.4 eV) that are typically observed in thermal oxides on 4H-SiC, are also present in PSG devices. Theoretical models for the atomic-scale trap passivation mechanism also confirm that P doping is more effective than nitridation in near-interface trap passivation. This significant reduction of the near-interface traps, O1 and O2 detected by CCDLTS correlates with the higher channel mobility in PSG gated 4H-SiC MOSFETs.

• Characterization of atomic oxide growth SiO_2/4H-SiC interface

Plasma oxidation is a promising method to thermally grow conformal gate oxides for 4H-SiC trench MOSFETs. The results obtained here suggests that the SiO_2/4H-SiC interfacial electronic properties are dictated by the NO post-oxidation annealing step for both thermal and plasma oxides.

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Chapter 5

Electronic properties of SiO_2/4H-SiC interface PART II
(i) Interfaces on dry etched planar surface (ii) Interfaces on dry etched sidewalls

As we discussed in chapter 4, section 4.3, 4H-SiC trench MOSFET is a fascinating device design with greater advantages. However, processing of trench MOSFETs require reactive ion etching (RIE) in 4H-SiC. In this chapter we extend our discussion further and investigate interfaces on RIE etched 4H-SiC. Following, we implemented plasma oxidation and RIE process in the actual fabrication process of trench MOSFETs and investigated the properties of trench sidewall interfaces. In this regard, we have designed and fabricated trench MOS capacitors to obtain capacitance of side walls. Furthermore, we have fabricated the preliminary trench MOSFETs by implementing the optimized process conditions and characterized it.

5.1 Reactive Ion Etched (RIE) induced effects on 4H-SiC

Fabrication of trench MOSFETs on 4H-SiC advents another major challenge due its geometry as well as due to the unique physical and chemical properties of SiC. The processing of such devices requires the trench formation in mechanically hard and chemically inert 4H-SiC material. In this regard, Reactive ion etching (RIE) is widely employed to form trench structures in SiC. During the RIE process, both physical and chemical processes contribute to the removal of Si and C atoms from SiC, along with the bombardment and incorporation of energetic ions onto the surface[1]. RIE has been reported to introduce severe surface roughness, surface contamination, increase of interface states and deep level defects in the SiC epitaxial bulk layer through many microns in depth[2, 3, 4, 5, 6, 7]. These defects can cause the performance degradation in MOSFETs. Furthermore, RIE induced defects have been seen in other semiconductor

technologies as well (Si [8, 9, 10, 11, 12, 13], GaN[14, 15]). Therefore, it is very important to understand the nature of residual damage caused by RIE on 4H-SiC interface, as well as the interface recovery processes.

5.1.1 4H-SiC RIE etch induced effects investigation

Reactive ion etching (RIE) on SiC can employed by using different etch reactors such as Capacitively-Coupled Plasma CCP), Inductively-Coupled Plasma (ICP), and Electron Cyclotron Resonance (ECR) plasma reactors. The etch gas systems used in these reactors can be categorized as follows (i) fluorine-based (SF_6, CF_4, NF_3, BF_3, CHF_3), (ii) chlorine-based (Cl_2, $SiCl_4$, BCl_3), and (iii) bromine based (Br_2, IBr_2) gases [1, 1]. The etch rates and etch chemistry depends on etch reactors, etch gases and etch recipe.

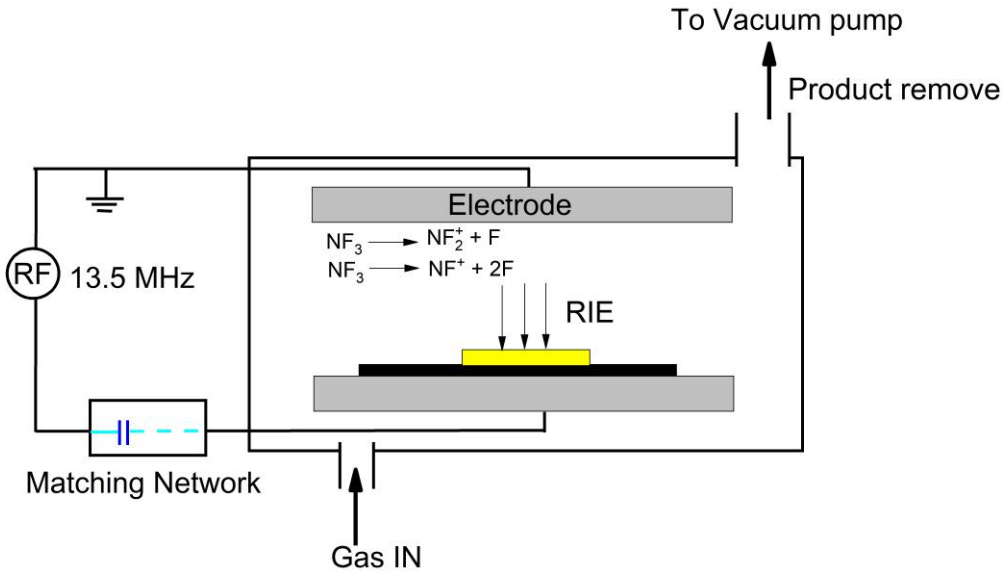

Figure 5.1: Schematic diagram of RIE process. Samples were mounted on graphite plate.

Here, we used Capacitively Coupled Plasma (CCP) RIE process to etch about 2 μm of Si-face and a-face SiC, using NF_3 as the etch gas with a flow rate of 18 sccm, maintaining a chamber pressure of 60 mTorr. The RF power was 40 W. Schematic diagram of RIE process is shown in figure 5.1. In RIE, active radicals (F) generated in a plasma induce chemical etching. Positive ions (NF_2^+, NF^+) are accelerated onto the surface and induce physical etching by ion bombardment[1, 1]. To assess the surface roughnesses, Atomic Force Microscopy (AFM) scans over several areas were measured. X-ray photoelectron spectroscopy (XPS) was used to

examine surface contamination on Si-face samples. After surface assessment was carried out, sacrificial oxide was formed by dry oxidation in pure O_2 at 1150 °C for 3 hours to consume the top surface of etched SiC, which was subsequently etched with BOE (Buffered oxide etch). To study the electrical properties of RIE effects, planar MOS capacitors were fabricated with thermal oxidation as well as with plasma oxidation. Electrical properties of etched surface MOS capacitors were compared with un-etched surface MOS capacitors, which we have discussed in section 4.4. Figure 5.2 shows major experiment procedure.

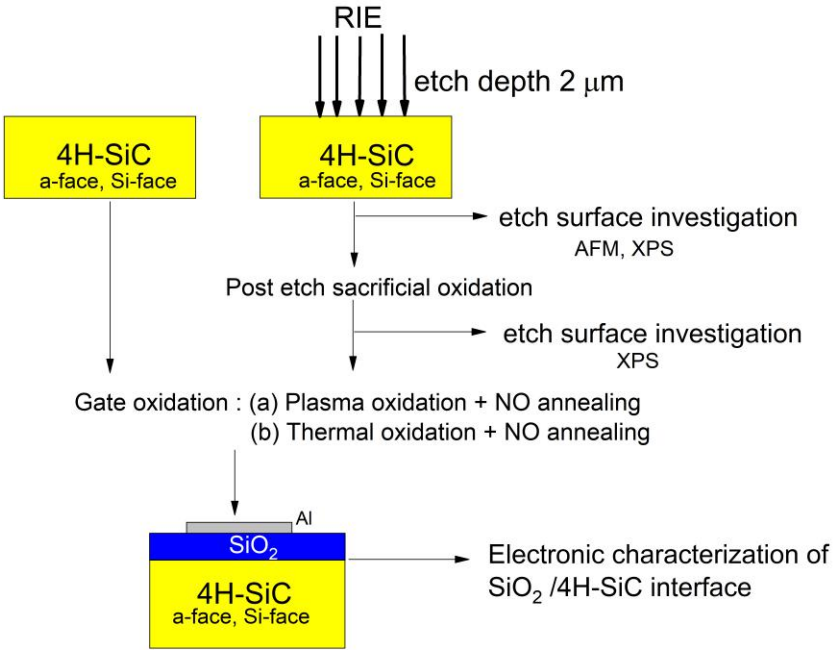

Figure 5.2: Experimental procedure to investigate electronic properties of SiO_2/(etched)4H-SiC interface.

5.1.2 Surface roughness and surface contamination on etched samples

AFM scans over several areas of each RIE sample shows that almost atomically flat surfaces (figure 5.3 RMS roughness ∼0.3 nm) were obtained after the RIE process. XPS spectra (figure 5.4) for the etched surface shows a F_{1s} peak which indicates surface contamination due to NF_3 gas used in the RIE. However, F_{1s} peak disappears from XPS spectra after the sacrificial oxidation, which indicates the removal of possible subsurface contamination layer.

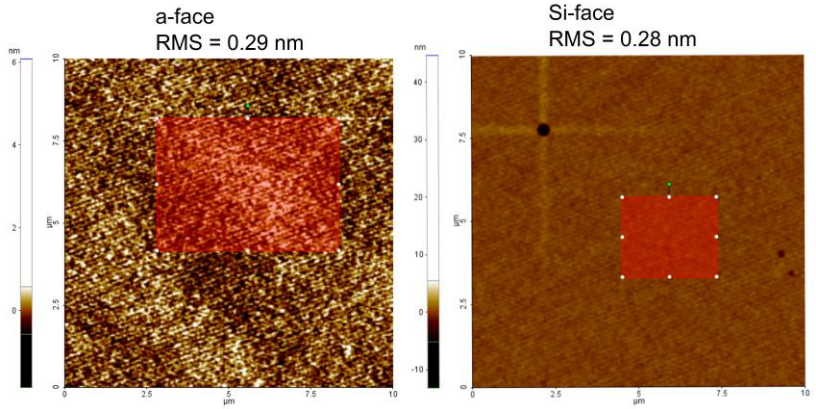

Figure 5.3: AFM scans on RIE samples. AFM scans were performed by Mr. B. Schoenek from Physics Department.

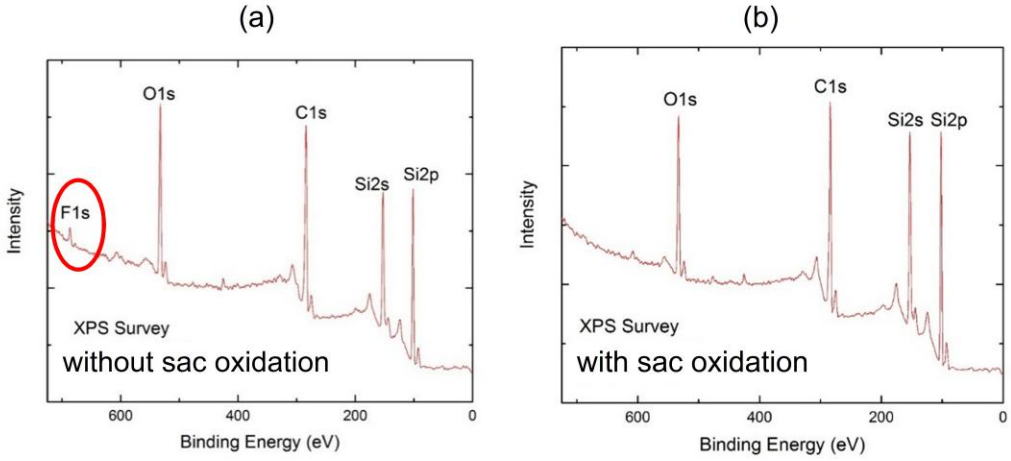

Figure 5.4: XPS spectra for with and without sacrificial oxidation. XPS analysis were performed by Dr. M. Bozack from Physics Department.

5.1.3 Electrical properties of MOS capacitors formed on etched surfaces

To investigate interface traps and oxide properties of the etched surfaces, simultaneous high-low frequency capacitance- voltage (*C-V*) characteristics of the MOS capacitors were measured using a Keithley 590 *C-V* analyzer at 100 kHz and KI 595 *C-V* meter at room temperature in the dark. The high frequency *C-V* curves at room temperature for MOS capacitors fabricated on Si-face (0001) and a- face ($11\bar{2}0$) 4H-SiC epitaxial layers, with and without RIE are shown in figure 5.5. Room temperature *C-V* measurements on capacitors formed on etched and un-etched surfaces do not reveal significant difference within experimental errors (figure 5.5).

Furthermore, as shown in figure 5.6, simultaneous hi-low frequency *C-V* extracted D_{it} profiles has no difference with or without RIE.

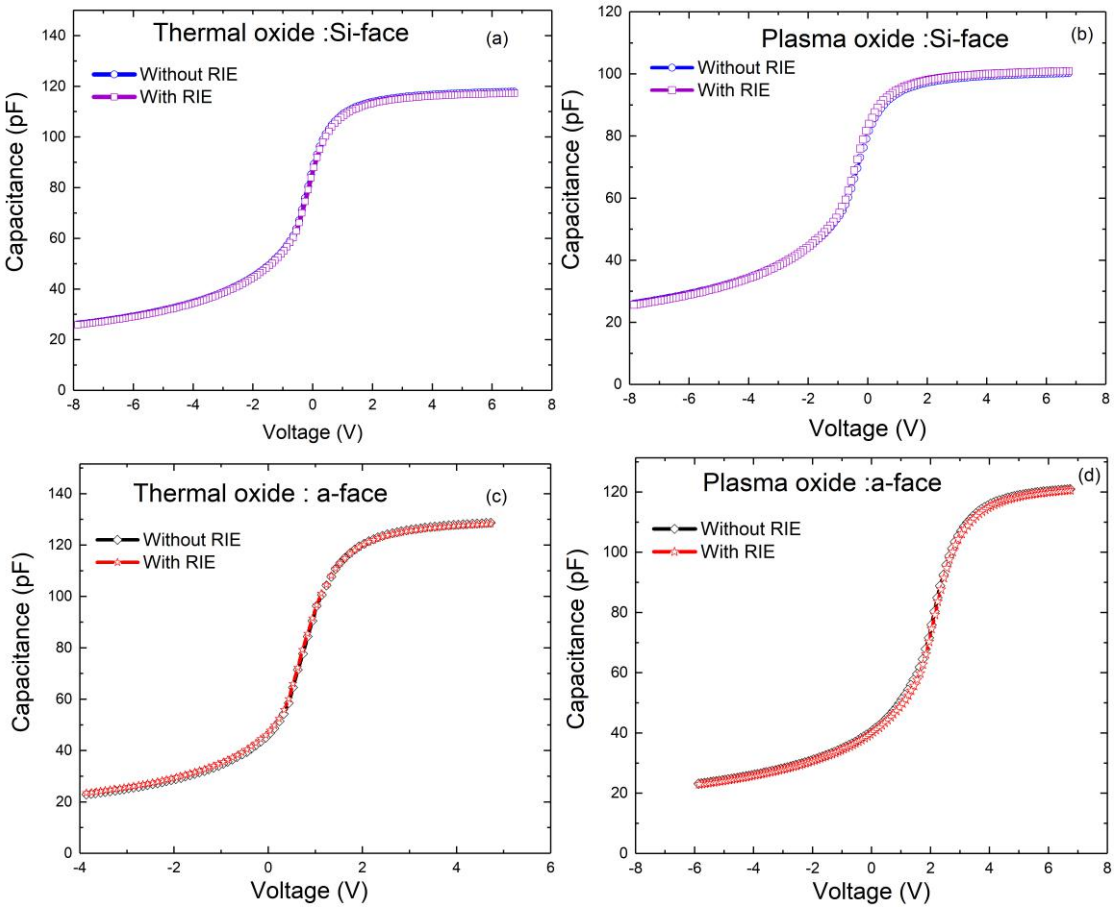

Figure 5.5: Room temperature measured high frequency 100 kHz *C-V* curves with and without RIE process (a) Si-face thermal oxide (b) Si-face plasma oxide (c) a-face thermal oxide (d) a-face plasma oxide.

For further interface trap investigation near the conduction band-edge, high frequency *C-V* measurements at 77 K and 298 K on etched samples were carried out. The average interface state per unit area (N_{it}) was estimated from the shift in the flat-band voltage ΔV_{FB} between room temperature and 77 K in accordance with the Gray-Brown method (see section 3.2.2). Extracted N_{it} values (Table 5.1) have comparable densities with un-etched surface MOS devices which were reported in chapter 4 Table 4.3.

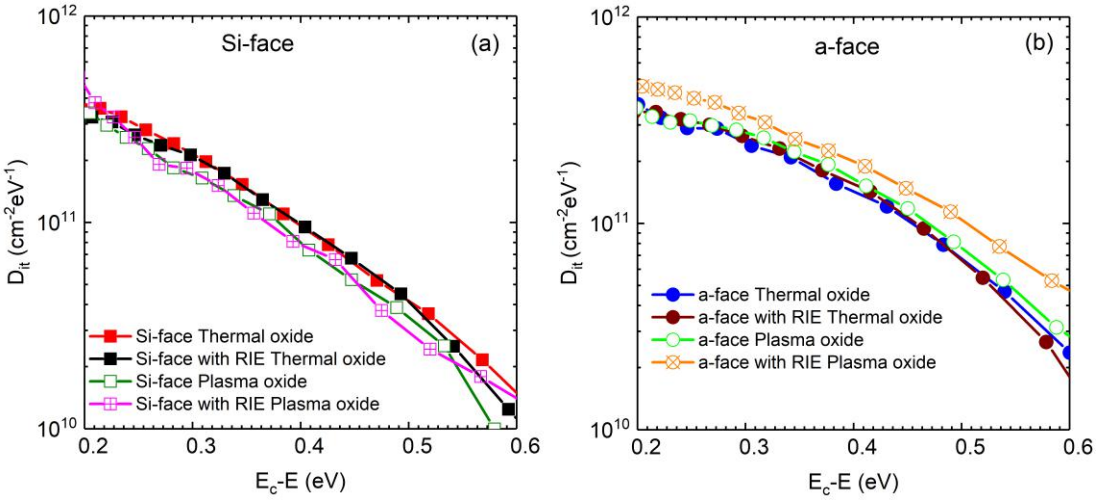

Figure 5.6: D_{it} comparison between (a)Si-face and (b)a-face capacitors with standard thermal, plasma oxidation and with/without RIE.

Sample Info	Gray-Brown ~0.05-0.2 eV N_{it} ($\times 10^{11}$ cm^{-2})
Si-face RIE plasma oxide	5.6
Si-face RIE thermal oxide	5.4
a-face RIE thermal oxide	3.5

Table 5.1: N_{it} values from Gray-Brown technique on RIE MOS capacitors.

CCDLTS measurements on MOS capacitors formed on etched surfaces

CCDLTS measurements were also performed to detect the dynamics of trapped electrons in both the oxide and the epitaxial layer in Si-face samples. For near interface oxide trap investigation, CCDLTS spectra is taken with pulsing the capacitor from depletion to the accumulation ($V_P > V_{FB}$) in the temperature range 77 K-298 K. For these measurements, constant capacitance set point was 37 pF which corresponds to the depletion width in 4H-SiC of 300 nm.

For the bulk defect investigation of 4H-SiC side of the interface, CCDLTS spectra was taken with increasing trap filling pulse voltages up to flat-band voltage ($V_P \simeq V_{FB}$) in the temperature range 77 K-500 K. For these measurements, constant capacitance set point was 25 pF which corresponds to the depletion width in 4H-SiC of 531 nm. Figure 5.7 shows high frequency *C-V* curve for RIE plasma oxide, with indicating corresponding constant capacitance

points and pulsed regions for both oxide and bulk defect investigation. In chapter 3, section 3.2.4 we have discussed this technique in more detail.

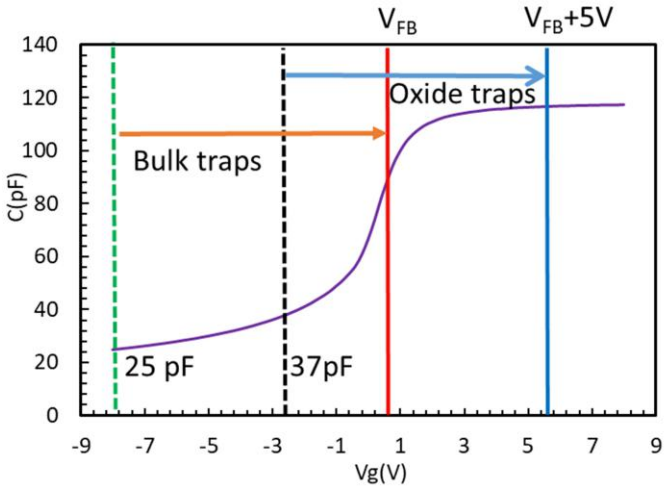

Figure 5.7: High frequency (1 MHz) *C-V* curve for RIE +plasma oxide MOS capacitor, corresponding constant capacitance points (C_p=37 pF for near interface trap investigation, C_p=25 pF for bulk trap investigation) and pulsed regions for both oxide and bulk defect investigation.

Near-interface oxide trap analysis

As shown in figure 5.8, CCDLTS for filling voltages greater than V_{FB} shows the same two broad near-interface peaks labeled O1 and O2 (Chapter 4 section) for RIE samples as well. The areal trap density of the near-interface oxide traps from CCDLTS are shown in Table 5.2. These oxide traps observed from CCDLTS measurements are consistent with un-etched MOS capacitors, which were discussed in chapter 4 and shows comparable N_{it} densities with Table 4.4 .

Sample Info	O1 N_{it} ($\times 10^{11}$ cm^{-2})	O2 N_{it} ($\times 10^{11}$ cm^{-2})
Si-face RIE+plasma oxide	1.12	2.46
Si-face RIE+thermal oxide	1.02	2.76

Table 5.2: CCDLTS measurements extracted N_{it} values on RIE samples.

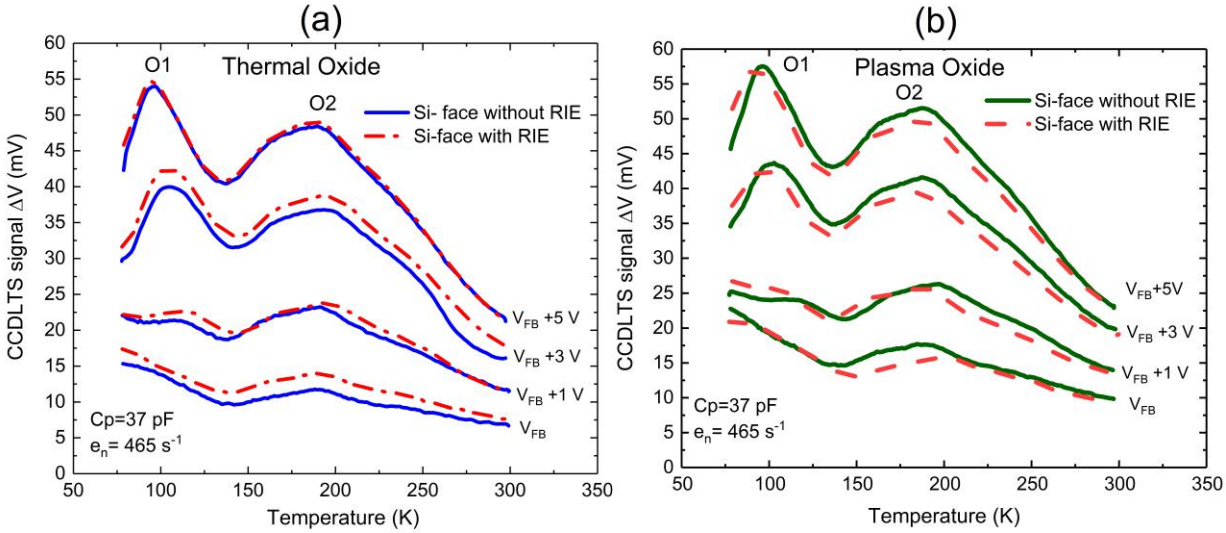

Figure 5.8: CCDLTS spectra on Si-face samples. The solid lines represent measurements on without RIE samples and dashed lines represent the measurements on etched surface with (a)thermal oxide and (b) plasma oxide MOS capacitors. The constant capacitance (C_P) was 37 pF and the electron emission rate was 465 s^{-1}.

CCDLTS measurements: SiC bulk defects investigation

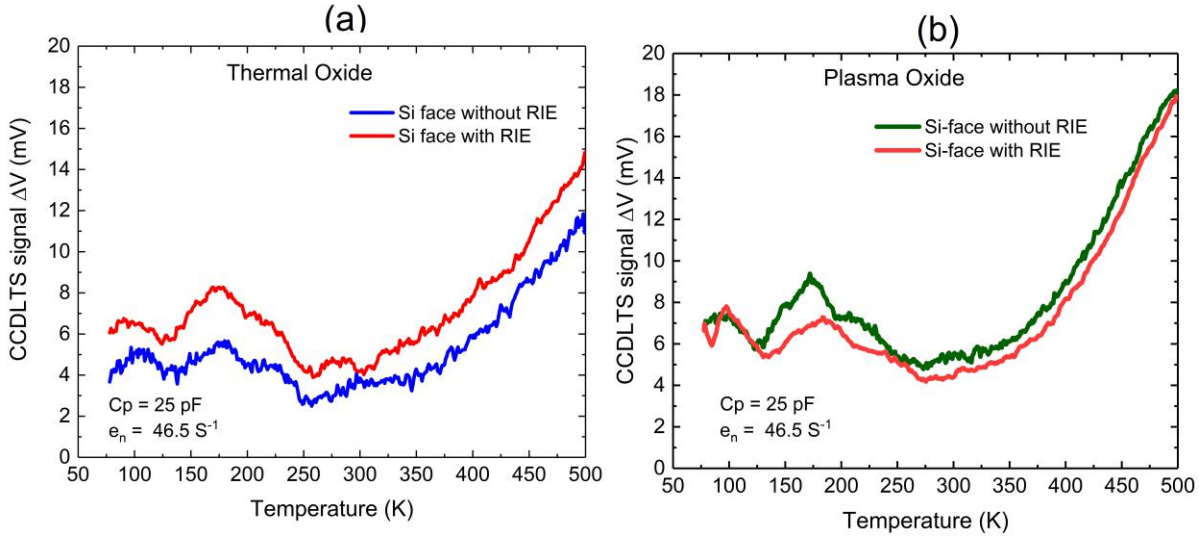

Figure 5.9: CCDLTS spectra for detection of bulk traps in RIE done sample with (a)thermal oxide and (b) plasma oxide. The constant capacitance (C_P) was 25 pF and the electron emission rate was 46.5 s^{-1}.

For traps located on 4H-SiC side of the interface, the CCDLTS signal is expected to increase with increasing filling voltage and saturate at $V_P \simeq V_{FB}$, as the semiconductor depletion width

approaches zero and all the bulk traps are occupied[18, 19]. However, as shown in figure 5.9, no RIE related defect peaks are observed in the region extending into the SiC epi-layer about 531 nm from the SiO_2/SiC interface. The peaks observed at ∼110 K and ∼180 K are defects in the starting SiC epitaxial layer which could be 'P1/P2' and 'P3' centers reported in the literature[17] or remnant of O2 trap signal. Another peak appears to be located above 500 K for both samples, which may be an epitaxial layer defect but it is not due to the RIE as it appears in both etched and un-etched samples. None of these peaks were associated with RIE or the gate oxidation process.

5.1.4 *I-V* measurements

I-V measurements were carried out to determine oxide quality of etched surface samples. Figure 5.10 shows current density verses electric field characteristics acquired on RIE MOS devices compared with reference devices. As can be seen in the figure 5.10, almost overlapped curves and comparable oxide breakdown fields from the measurements indicate the minimal effects induced by RIE.

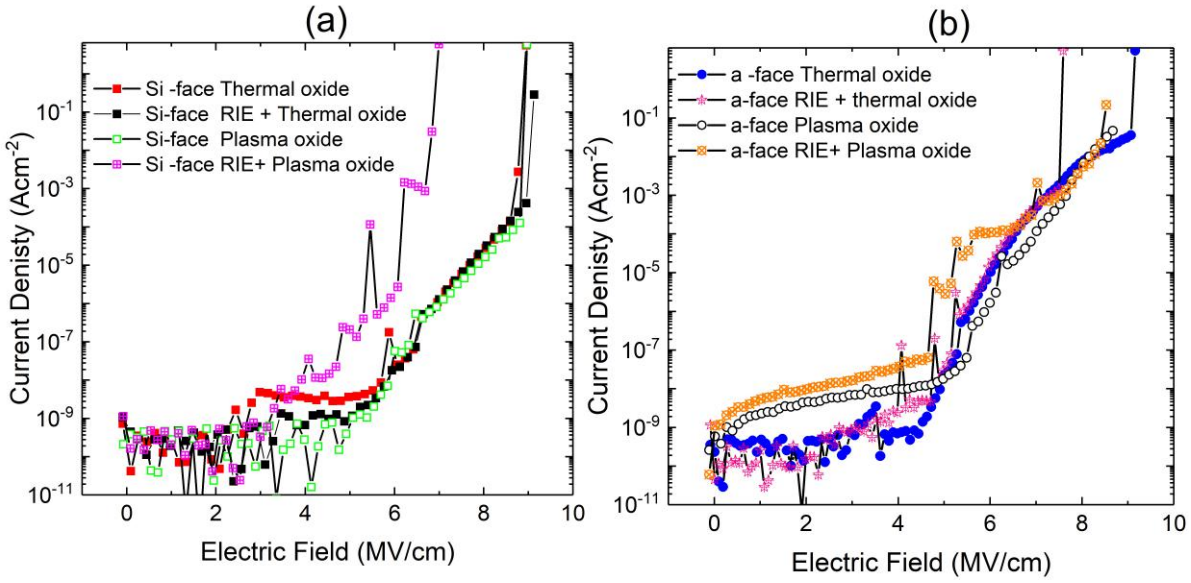

Figure 5.10: Current density- electric field characteristic in accumulation for with/without RIE on Si-face and a-face MOS capacitors.

5.2 Trench formation in 4H-SiC

Trench formation requires mask material to pattern the structures in 4H-SiC by opening the allocated area for RIE etching. Thus, selecting a masking material is important step in the process. Further, due to the requirement of high selectivity against masking material and RIE induced effects, selecting a proper masking material is vital. High selectivity can be obtained by using metals, such as Ni as mask material. However, small metal particles induced by RIE sputtering can be redeposited on the surface (known as 'micro-masking') and led to a higher surface roughness. Figure 5.11 shows Scanning Electron Microscope (SEM) and Atomic Force Microscopy(AFM) images of the 4H-SiC surface after RIE with the use of Ni metal as the mask material. Surface roughness was severe, around 112 nm. Furthermore, SEM images clearly shows the pillar-like hillocks in the 4H-SiC surface. These results strongly suggest the need of different mask material for trench fabrication process. Therefore, SiO_2 mask was considered as the mask material. As shown in figure 5.12, SiO_2 mask did not result in micro-masking and shows a tremendous reduction in surface roughness (RMS=0.6 nm). Use of SiO_2 mask advent new difficulties, such as low selectivity with 4H-SiC (almost 1:1) and requirement of additional RIE step for SiO_2 mask pattern formation. In the remaining of the chapter, this process was used for all etching, trenching experiments.

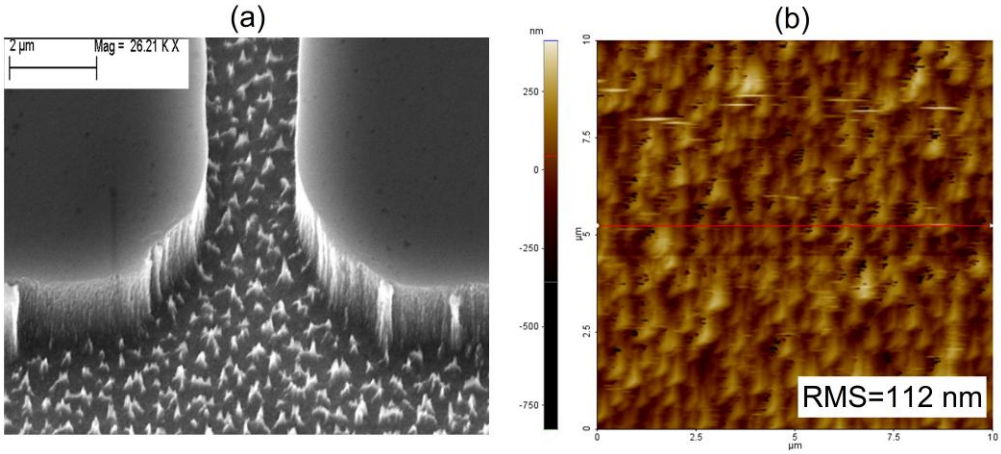

Figure 5.11: Micro-masking due to metal mask (a) SEM image and (b) AFM scan image.

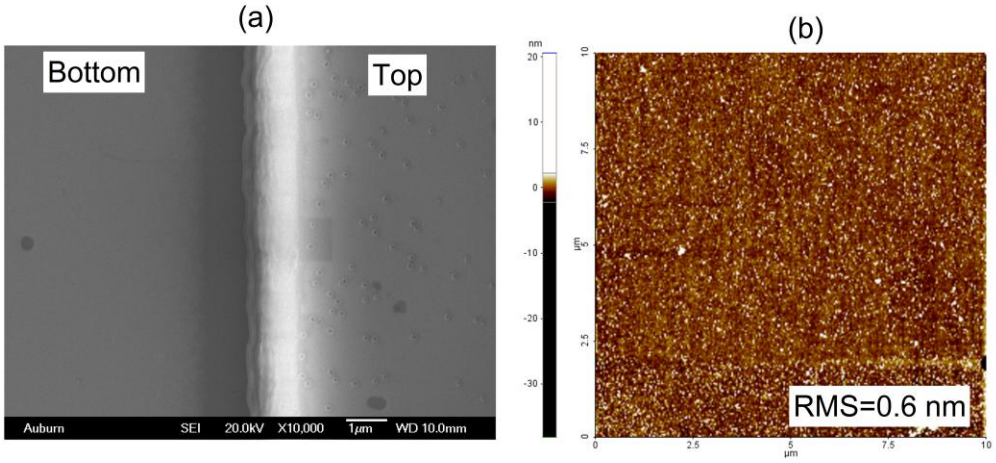

Figure 5.12: Smooth surfaces with SiO_2 mask.(a) SEM image and (b) AFM image.

5.3 Investigation of electronic properties of SiO_2/4H-SiC sidewalls

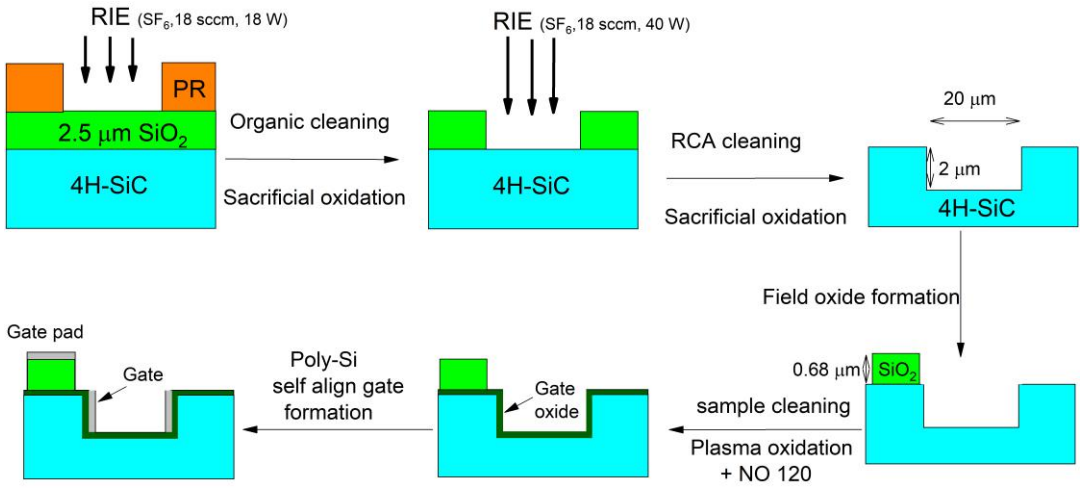

Figure 5.13: The fabrication process flow for trench MOS capacitors.

The trench MOS capacitor fabrication process began carried out with the deposition of 2.5 μm thick plasma-enhanced chemical vapor deposition (PECVD) SiO_2 on 5×10^{15} cm^{-3} doped 5 μm thick epi-layer n-/n+ Si-face 4H-SiC. Thereafter, SiO_2 etch mask was patterned by RIE process with SF_6 as the etch gas (18 sccm) and RF power at 18 W. For this step, thick photoresist ($\sim$5.6 μm, NLOF2070) was used as the mask material. Once the SiO_2 mask was formed, remaining photoresist was striped off by carrying out organic cleaning and sacrificial oxidation in pure O_2 at 1150 $^{\circ}$C for 3 hours. Next, $\sim$2 μm depth trenches on 4H-SiC are formed by using the RIE process with SF_6 as the etch gas (18 sccm) and RF power with 40 W. After dry

etching, remaining SiO_2 hard mask was removed with the use of BOE (Buffered oxide etch). Thereafter, sacrificial oxide was formed by dry oxidation in pure O_2 at 1150 $^{\circ}$C for 3 hours to consume a thin surface layer of etched SiC, which was subsequently etched with BOE. Since the focus is on the electronic characterization of trench sidewall, it is desired to minimize top surface capacitance contribution to total capacitance. In this regard, 0.68μm thick SiO_2 field oxide was deposited on 4H-SiC top surface via LPCVD process. Subsequently, RIE process and wet etch process was carried out to pattern the field oxide. Following that, gate oxidation was performed with optimized plasma oxidation process (chapter 4, section 4.4) and metallic gate was formed by heavily doped Si (Poly-Si gate process). Here, self aligned gate formation was carried out to have large value of sidewall capacitance contribution to the total capacitance. Trench fabrication flow with major fabrication steps are shown in figure 5.13. Also, along with trench MOS capacitors, planar MOS capacitors with poly-Si gates was also fabricated on planar Si-face (0001) and a-face ($11\bar{2}0$) for comparison purpose.

Cross-sectional SEM image of one of the trench structure is shown in the figure 5.14. According to the figure 5.14, trench structures formed by the RIE process result in an $\sim$115 $^{\circ}$ angle (trench taper angle) and a '*V-shape*' structure. However, micro-trenchers are not observed in these structures.

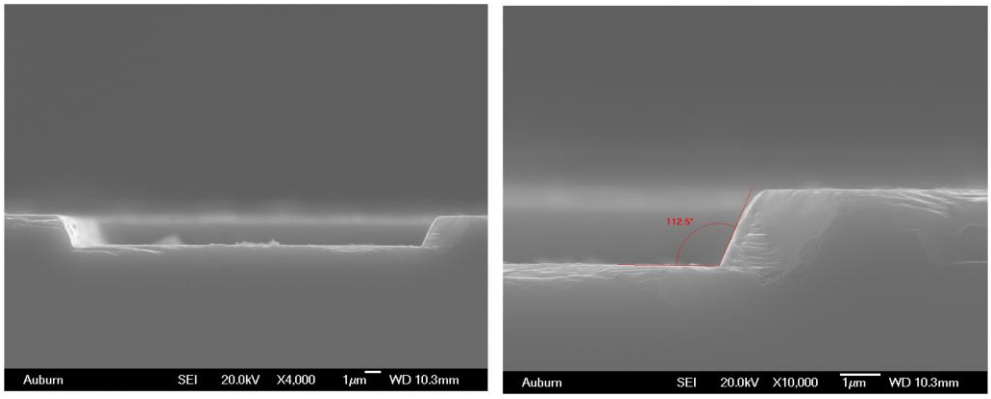

Figure 5.14: Cross-sectional SEM image of trench structure.

Figure 5.15 shows the top view of the trench MOS capacitor with 20 trench fingers (40 sidewalls) and schematic diagram of the trench structure. Calculated area contribution from Si-face and sidewalls are 5.98×10^{-4} cm^2 and 5.96×10^{-4} cm^2 , respectively. However, Si-face capacitance contribution to total capacitance will be small due to the thick field oxide.

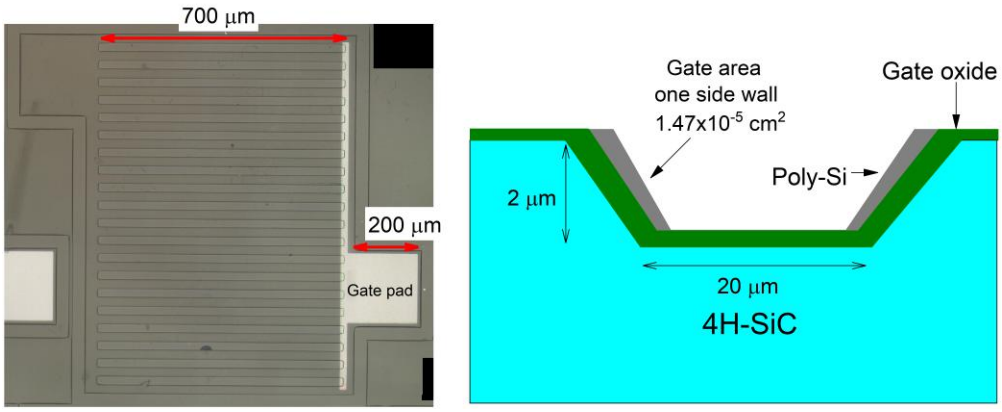

Figure 5.15: Top view of fabricated trench MOS capacitor and schematic of trench structure.

Interface trapping of trench side walls was investigated by the 'Gray Brown' technique (see section 3.2.3 for technique). Figure 5.16 show high frequency (100 kHz) small signal a.c bias *C-V* curves for trench MOS capacitor, in the temperature range 77 K and 298 K. As shown in figure 5.16 low temperature *C-V* curve on trench MOS capacitors show an interface state ledge. The calculated N_{it} values are shown in table 5.3 and shows slightly higher values for the trench MOS capacitors compared to planar devices, which may be an indication of higher interface states on the side wall interface. Higher N_{it} could be due to the surface roughness in the side walls as well as due to the resultant crystal face($\sim$115 $^\circ$ angle is neither a-face $(11\bar{2}0)$ or m-face $(1\bar{1}00)$).

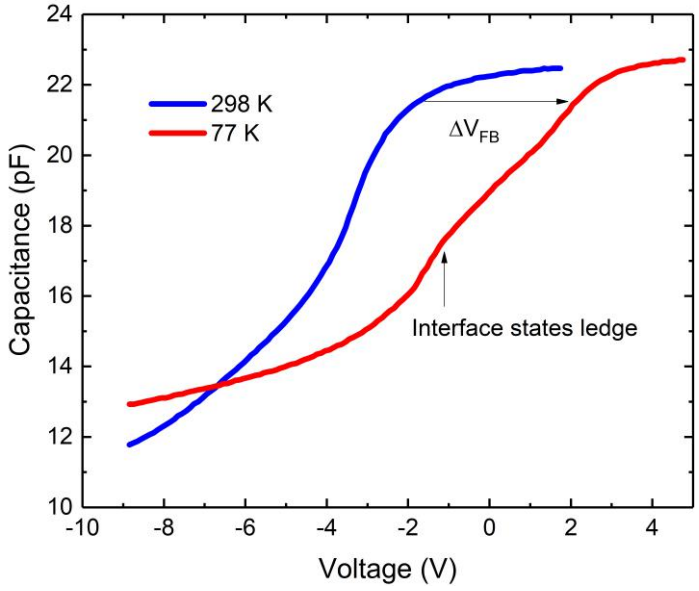

Figure 5.16: Low temperature *C-V* measurements on trench MOS capacitor.

Sample Info	Gray-Brown ~0.05-0.2 eV N_{it} ($\times 10^{11}$ cm^{-2})
Trench MOS capacitor	7.4
Si-face Planar MOS capacitor	6.5
a-face Planar MOS capacitor	6.2

Table 5.3: N_{it} values from Gray-Brown technique comparison for planar and trench MOS capacitors.

5.4 Trench MOSFETs fabrication and characterization

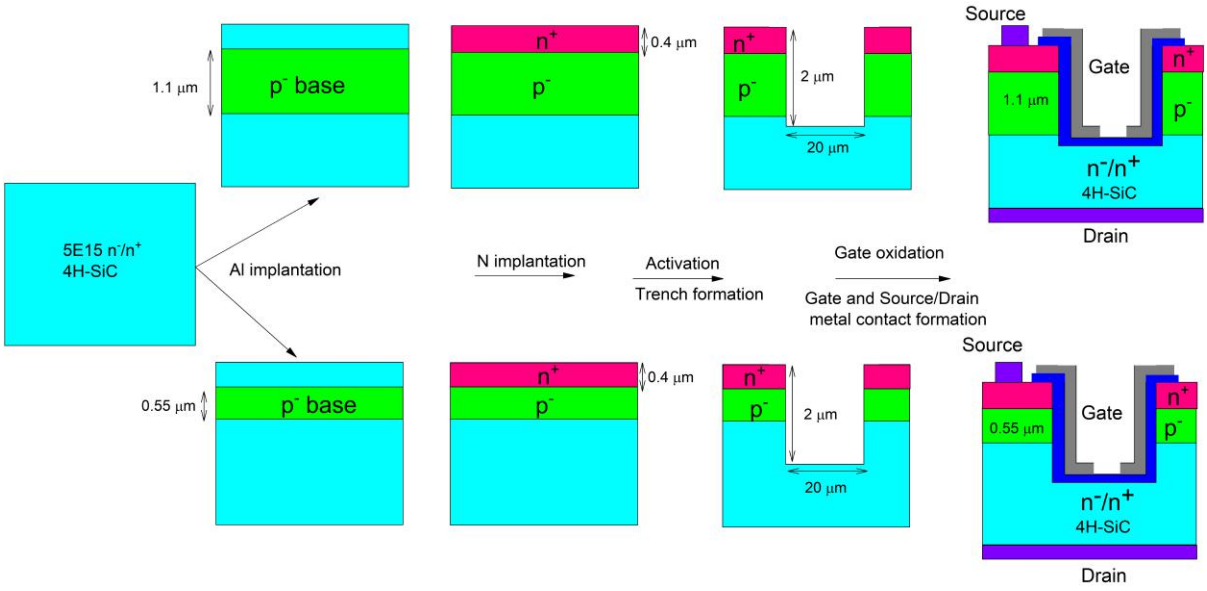

Figure 5.17: Fabrication process flow of 4H-SiC trench MOSFETs.

Using the RIE (section 5.3) and plasma oxidation of process (chapter 4, section 4.4) trench MOSFETs were fabricated on Si-face (0001) of *n*-type, 5 μm thick 4H-SiC epitaxial layers doped at 5×10^{15} cm^{-3}. The p-base region (*n*-channel) was formed by carrying out Al implantation at 700 °C with the dose of 4×10^{16} cm^{-3}. Here, two different implantation depth profiles were used to achieve channel lengths 1.1 μm and 0.55 μm. Implantation of N (8×10^{19} cm^{-3}) at 700 °C was performed with depth profile of 0.4 μm from the Si-face surface. Subsequently, post-implantation activation annealing at 1650 °C using a graphitic carbon cap layer was performed. Following that, trench formation using optimized RIE recipe and gate oxidation with plasma oxidation was carried out as described before. After that, Mo and Ni were sputtered

as the gate and the source/drain(bottom side) contact metals respectively. Ohmic contact annealing was carried out at 800 °C in Argon. Summary of process flow is shown in figure 5.17. Figure 5.18 shows the top view of the fabricated trench MOSFETs. In these MOSFETs, channel width (W) is the number of fingers times 700 μm and channel length (L) is the number of fingers times corresponding p base depth (i.e. shorter channel MOSFETs, L = 0.55 μm $\times$ number of fingers and longer channel MOSFETs, L=1.1 μm $\times$ number of fingers).

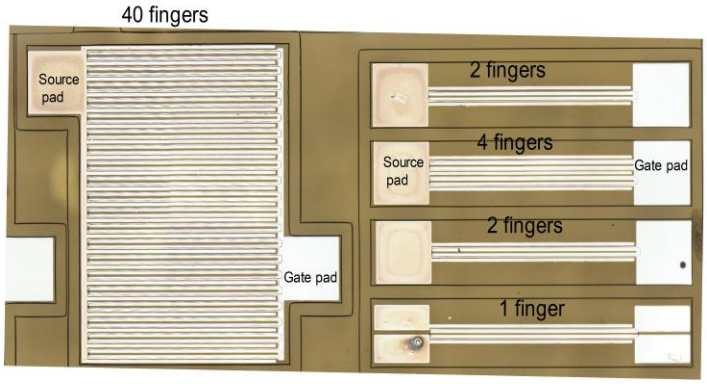

Figure 5.18: Top view of fabricated 4H-SiC trench MOSFETs.

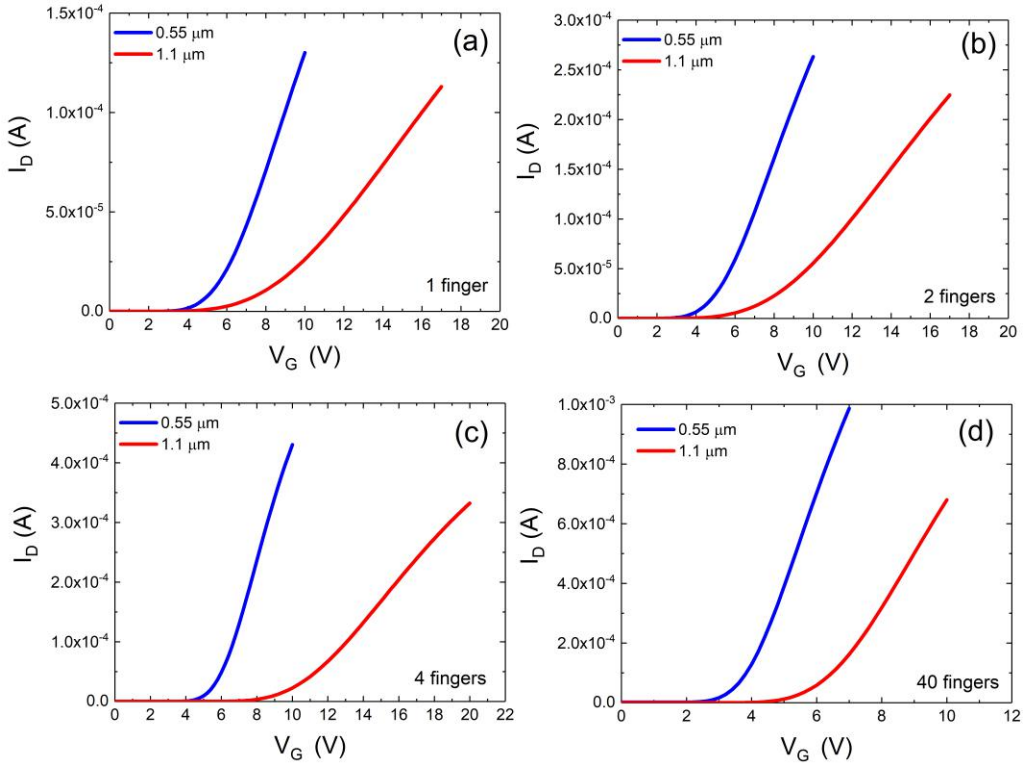

Figure 5.19: I_D-V_G characteristics of (a) 1 finger (b) 2 fingers (c) 4 fingers and (d) 40 fingers 4H-SiC trench MOSFETs with V_D = 100 mV.

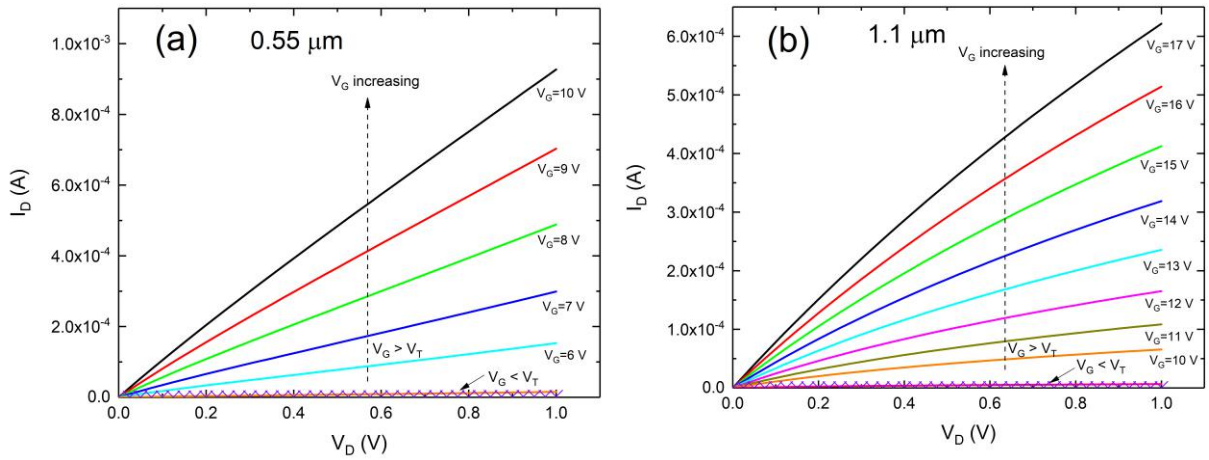

Figure 5.20: Example of I_D-V_D characteristics with V_G increasing for 1 finger trench MOSFETs with (a) Short channel(0.5 μm) and (b) Long channel(1.1 μm).

Figure 5.19 shows drain current vs. gate voltage (I_D-V_G) characteristics at room temperature with fixed drain voltage V_D = 100 mV. As shown in figure 5.19, I_D-V_G characteristics show *normally-off* (enchantment mode) behavior for trench MOSFETs and confirmed the gate bias dependence on transistor characteristics. The characteristics show typical short channel effect, where threshold voltage (V_T) becomes a function of channel length. Qualitatively, decrease in V_T for shorter channel (*p* depth 0.55 μm) can be explained as follows. In a short channel device drain to source voltage depletes the region under the gate. A significant portion of sub-gate depletion region charge is balanced by charge on *pn* junctions on source and drain side. Thus less gate charge is required to reach the start of inversion and this result a decrease in V_T . For the smaller channel length, short-channel effect is severe and further reduces the V_T [20].

Figure 5.20 shows an example of I_D-V_D characteristics for 1 finger trench MOSFETs. These results confirm the "*transistor*" nature of the fabricated trench MOSFET structure. Transistor action appears, where I_D flowing in an output circuit is modulated by an input voltage applied to the gate[20].

5.5 Blocking voltage characteristics

As we discussed in the introduction, a power MOSFET device is capable of supporting high voltage when the drain bias is positive and gate electrode is shorted with source electrode. Therefore, investigation of blocking voltage capability of the trench MOSFET device is important. In this regard, I_D-V_D characteristics were carried out with gate voltage set at zero (V_G=0).

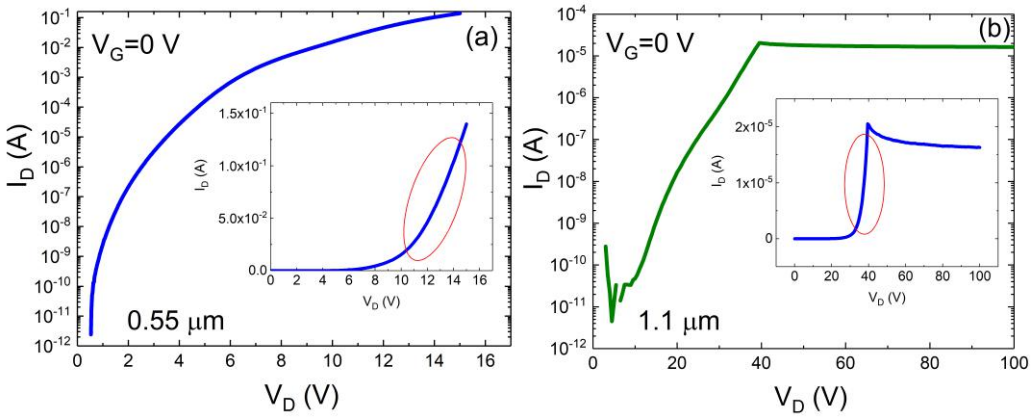

Figure 5.21: I_D-V_D characteristics (blocking voltage characteristics) with V_G=0 for 1 finger trench MOSFETs with (a) Short channel(0.5 μm) and (b) Long channel(1.1 μm).I_D-V_D characteristics in linear scale shows in the insets of the figure.

As shown in figure 5.21, blocking voltage of these devices are well below the theoretically expected values. The main reason this can be explained by the parasitic bipolar transistor action in these structures. The trench MOSFET structure contains a parasitic bipolar transistor (BJT) formed between the n^+ source region, the p^- base region, and the n^- drift region. Since p^- base region has a shorter width, current gain of the *n-p-n* (n^+-p^--n^-) transistor is significant[21]. When source and drift region are separated by few micron or less, it becomes possible for *pn* junction depletion regions around the source and drift layer to touch or *punch-through*[20]. When this occurs, gate loses the control of MOSFET, and I_D-V_D characteristics show turn ON behavior even for V_G=0. In addition, impact of parasitic BJT action is more severe for shorter channel (0.5 μm) devices as shown in figure 5.21. More developed trench MOSFET structures, parasitic BJT action is usually mitigated by introducing p^+ region to short the emitter and the base of *n-p-n* transistor.

5.6 Summary

Interface on dry etched planar surface

Oxides grown on etched 4H-SiC surfaces with optimized etching processes do not result in the creation of additional traps at the SiO_2-SiC interface or in the bulk of SiC. These results provide some useful references and are very encouraging for development of 4H-SiC trench MOSFETs

Interface on dry etched sidewalls

We have discussed trench MOS capacitor fabrication with using methods discussed in chapter 4.4 and section 5.1.1. Cross-sectional images of trench structures have shown the formation of a V-shaped trench structures due to the specific RIE process used in this work. Interface characteristics of trench side walls have been investigated by using 'Gray-Brown' technique and indicate a higher interface traps on the sidewalls interface compared to planar surface interface. Higher interface traps could be due to the surface roughness of the side wall and as well as due to the peculiar crystal face resultant from RIE ($\sim$115 $^\circ$ angle). In addition, we have demonstrated the transistor behavior on fabricated preliminary trench MOSFETs. Electrical characterization of these devices point out the requirement of more complex structures to prevent short channel effects.

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Chapter 6

Electronic properties of dielectric-β-Ga_2O_3 interfaces

As discussed in chapter 1, β-Ga_2O_3 is an attractive semiconductor material due to an ultra-wide energy bandgap (E_G) of 4.6-4.9 eV. The recent demonstration of different device structures illustrates the fast pace of the technological development in this area[1]−[10].While Al_2O_3 and HfO_2 gate dielectrics[1, 2, 3, 4] have been used in β-Ga_2O_3 MOSFETs, relatively less effort has been devoted to use of the SiO_2 gate dielectrics[5, 6, 7, 8, 9, 10]. The conduction band offset between SiO_2 and Ga_2O_3 has been reported to be between 2.8-3.6 eV[11, 12, 13], significantly higher than that of Al_2O_3-Ga_2O_3, which is between 1.5 and 2.2 eV[14, 15, 16] . Therefore, from a point of view of dielectric reliability, SiO_2 could make a better candidate for *n*-channel Ga_2O_3 MOSFETs, provided that low interfacial charge and interface state densities can be obtained for SiO_2-Ga_2O_3 interfaces. Understanding the electrical properties of the oxide-β-Ga_2O_3 interfaces is important for the development of practical Ga_2O_3 MOS devices as these factors impact critical MOSFET parameters such as sub-threshold swing, threshold voltage, channel mobility and device stability. Analyses of the interface state density at the interface between $(\bar{2}01)$ oriented β-Ga_2O_3 and atomic layer deposited (ALD) SiO_2 [17, 18] and ALD Al_2O_3 [19, 20] dielectrics have been reported recently, but have not been compared systematically.

In this chapter, we performed a systematic comparison of the electrical properties of Low-Pressure Chemical Vapor Deposition (LPCVD) SiO_2 and Atomic Layer Deposition (ALD) Al_2O_3 interfaces with β-Ga_2O_3, analyzing the impact of post-deposition annealing (PDA). Five different interfaces are compared in this study: LPCVD SiO_2 as deposited, LPCVD SiO_2 with N_2 anneal at 850 °C, ALD Al_2O_3 as deposited and ALD Al_2O_3 annealed in Forming gas(FG) or N_2, at 500 °C.

6.1 Sample perpetration

Square pieces (5 mm $\times$5 mm) of *n*-type (Si-doped, 2.5×10^{17} $cm^{-}3$) ($\bar{2}01$) oriented β-Ga_2O_3 were diced from a 2-inch diameter wafer from Tamura Corporation, Japan. The samples were cleaned with organic solvents and acid solutions before oxide deposition. Next, a Piranha etch step (H_2SO_4+30%H_2O_2 1:1) was performed for 15 minutes. Tetraethyl orthosilicate (TEOS or Si $(OC_2H_5)_4$) was used as the precursor in the LPCVD SiO_2 process. The deposition process was performed at 650 $^{\circ}$C for 35 minutes under a chamber pressure of 0.5 Torr and a TEOS carrier flow rate of 80 sccm. At elevated temperatures (>600 $^{\circ}$C), TEOS converts to silicon dioxide according to the following chemical reaction: $Si(OC_2H_5)_4 \rightarrow SiO_2 + 2(C_2H_5)_2O$. Following deposition, one sample was annealed at 850 $^{\circ}$C for 2 hours in flowing ultra-high-purity N_2 gas (500 sccm). The ALD Al_2O_3 films were deposited with Trimethylaluminum (TMA, $Al(CH_3)_3$) as the precursor gas. The process temperature was 200 $^{\circ}$C and a precursor pulse time of 0.06 sec was used with a deposition rate of 0.89 Å/cycle. In ALD process, precursor involves $Al(CH_3)_3$ (precursor gas A) and water (precursor gas B) react according to the following chemical reaction: $2Al(CH_3)_3+3H_2O \rightarrow 3Al_2O_3+6CH_4$. After deposition, samples were annealed in a Jipelec JetFirst200 rapid thermal annealing (RTA) furnace for 2 minutes in Forming gas (FG) or N_2 atmosphere at 500 $^{\circ}$C. Here, ALD process was performed at Purdue University, Indiana by Rahul P. Ramamurthy.

Circular gate contacts with a diameter of 500 μm were formed by thermally evaporating 150 nm of Aluminum (Al) through a shadow mask. A large area ohmic contact was formed by depositing $\sim$100 nm of Titanium (Ti) on the backside using DC sputtering. Samples were then attached to a gold plated ceramic plate using conducting silver paint for electrical measurements. Figure 6.1 (a) shows a schematic of the β-Ga_2O_3 MOS capacitor.

6.2 Simultaneous high-low frequency *C-V* characteristics

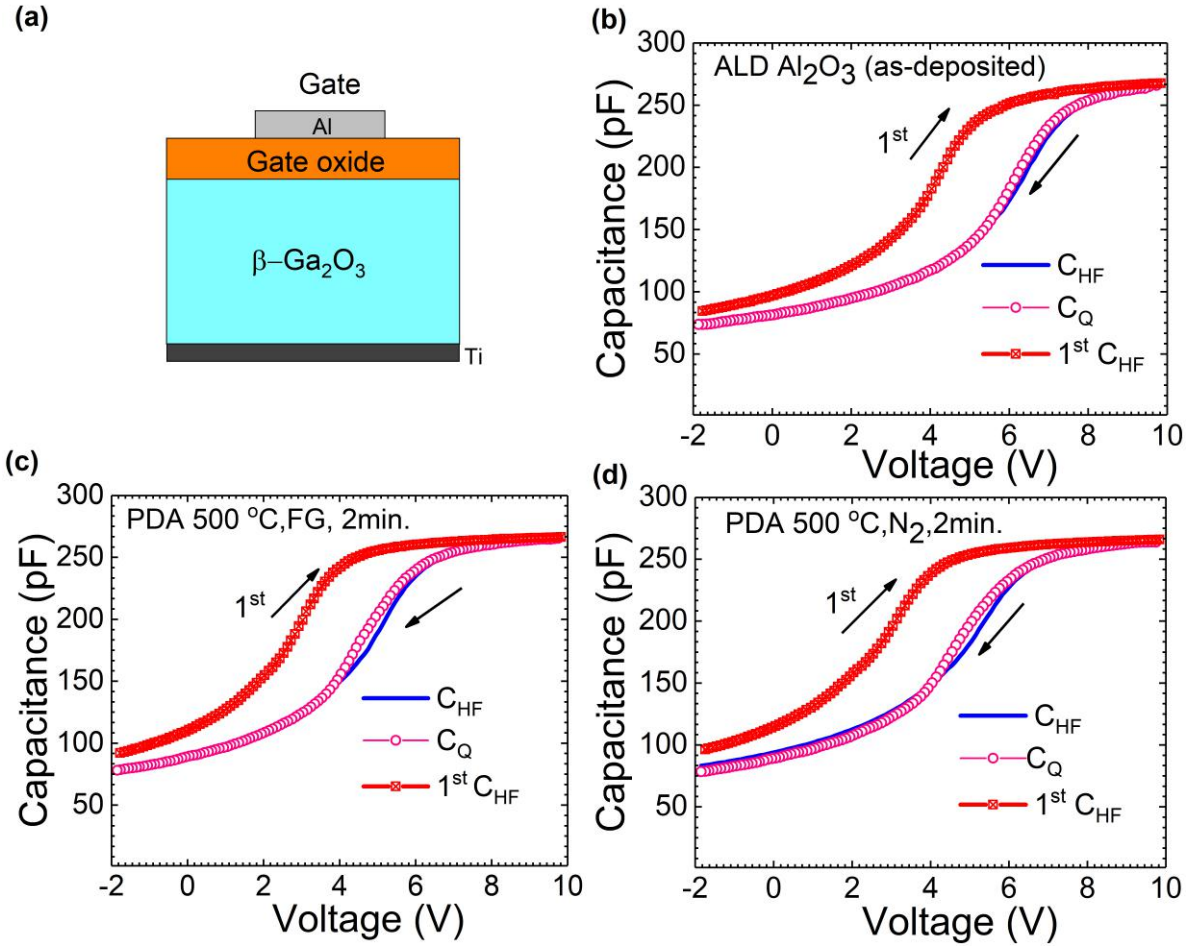

Figure 6.1: (a) Schematic of β-Ga_2O_3 MOS capacitor. (b), (c), (d) measured high frequency (C_{HF}) 100 kHz C_{HF}-V, quasi-static(C_Q) C_Q-V and *C-V* hysteresis curves for different sweep directions on ALD Al_2O_3 dielectric MOS capacitors at room temperature with different post-deposition annealing

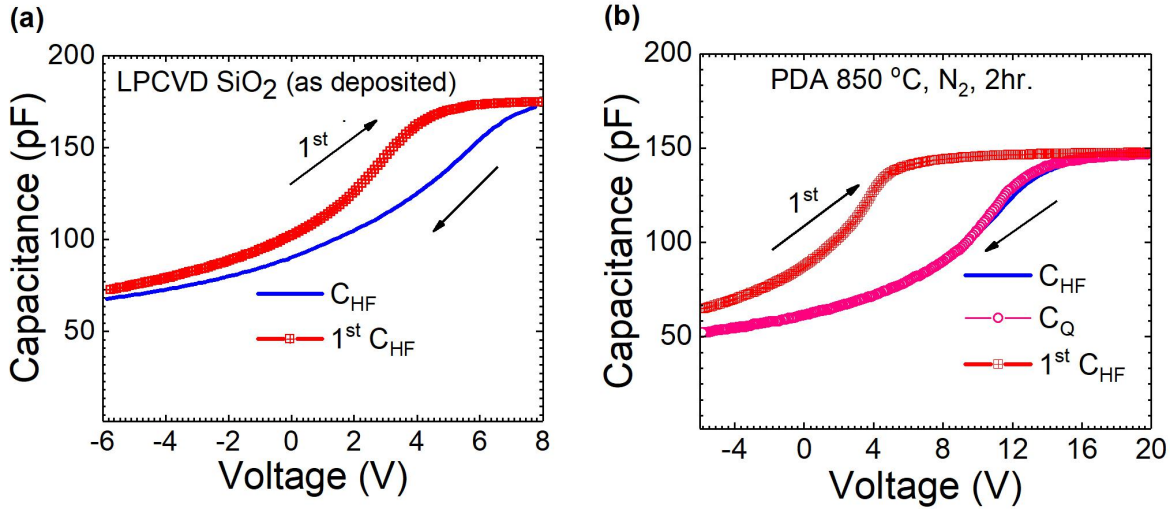

Figure 6.2: (a) Measured high frequency (C_{HF}) *C-V* hysteresis curves for MOS capacitors with as deposited LPCVD SiO_2 which shows the lack of a true accumulation. (b) C_{HF}-*V*, C_Q-*V* and *C-V* hysteresis curves for different sweep directions on LPCVD SiO_2 dielectric MOS capacitors at room temperature with PDA.

Typical simultaneous high-low frequency *C-V* characteristics at room temperature for MOS capacitors with ALD Al_2O_3 and LPCVD SiO_2 gate dielectrics are shown in figures 6.1 and 6.2. As indicated in the figure, the gate voltage was first swept from deep depletion to accumulation and then again in the reverse direction for a given voltage range. High gate leakage current in accumulation for the as-deposited LPCVD SiO_2 MOS capacitors prevented further analysis on this sample. The *C-V* characteristics, independent of gate dielectric, shows hysteresis indicative of slow 'border' traps[21, 22, 23, 24]. The largest hysteresis was observed for the LPCVD SiO_2 sample with PDA, indicating a higher density of 'border' traps compared to ALD Al_2O_3. Effective oxide charge density (N_{EFF}) were extracted from the accumulation to depletion sweep using fundamental equations as follows[25, 26]. First, ideal value of the flat-band capacitance (C_{FB}) has been calculated from

$$C_{FB} = \frac{C_{ox}\left(\epsilon_s A/\lambda_D\right)}{C_{ox} + \left(\epsilon_s A/\lambda_D\right)} \tag{6.1}$$

where λ_D is extrinsic Debye length, which is given by

$$\lambda_D = \left(\frac{\epsilon_s k_B T}{q^2 N_D}\right) \tag{6.2}$$

where C_{ox}, A, ϵ_s, N_D , k_B, q and T are oxide capacitance, gate area, permittivity of β-Ga_2O_3, bulk doping concentration, Boltzmann constant, elementary charge and temperature respectively. The value used for the dielectric constant of the β-Ga_2O_3 was 10.2. Here, value for N_D was extracted from the reciprocal of the slope of the $1/C^2$ vs.V curve. Once, C_{FB} value was calculated, it was used to find the corresponding flat-band voltage (V_{FB}) from experimental 100 kHz *C-V* data. As listed in Table 6.1, extracted flat-band voltage V_{FB} values at room temperature were used to obtain the effective oxide charge density (N_{EFF}) which represents the sum of all deep interface traps, 'border' traps and fixed oxide trapped charges. N_{EFF} values were calculated according to the following equation.

$$N_{EFF} = \frac{C_{ox}|W_{MS} - V_{FB}|}{qA} \tag{6.3}$$

where C_{ox}, A, q and W_{MS} are oxide capacitance, gate area, elementary charge and metal-semiconductor work function difference, respectively. Here, metal-semiconductor work function difference(W_{MS}) was calculated from the following equation.

$$W_{MS} = W_M - \left(\frac{\chi}{q} + \frac{E_G}{2q} - \phi_B\right) \tag{6.4}$$

where W_M is metal-work function (Al=4.28 V), χ= 4.0 eV is electron affinity, E_G =4.6 eV is the energy band gap and $\phi_B = k_B T(N_D/n_i)$ is bulk potential for the Ga_2O_3. Here, intrinsic carrier density(n_i) is obtained from $n_i = 4.9 \times 10^{15}((m_e^* m_h^*)/m_o^2)^{3/4} exp(-E_G/k_B T)$ [25] with the use of effective mass of the electron, $m_e^* = 0.34 m_o$ and effective mass of the hole, $m_h^* = 40 m_o$.

Next, the interface trap density (D_{it}) was extracted by using the simultaneous high-low technique as discussed in chapter 3 section 3.2.1 [21, 26, 27] As mentioned in section 3.2.1, the D_{it} measurements at room temperature performed here are accurate only in a limited energy range, from about 0.2 (flat-band) eV to 0.6 eV below the conduction band (E_C) of Ga_2O_3[18].

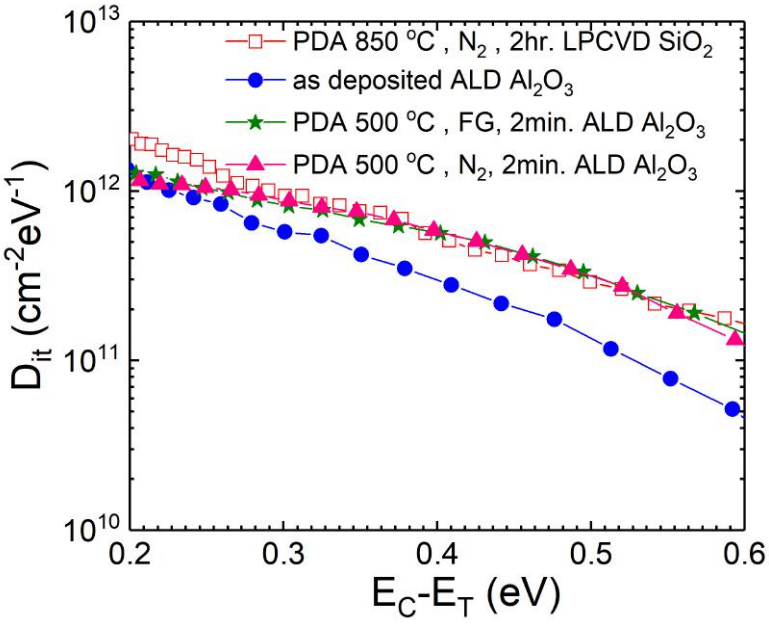

Figure 6.3: Interface trap density (D_{it}) versus energy level from conduction band (E_C-E_T) by simultaneous hi-low *C-V* measurement at room temperature for LPCVD SiO_2 and ALD Al_2O_3.

Sample Info	PDA condition	N_{EFF} ($\times 10^{12}$ cm^{-2})	N_{it} hi-low ($\times 10^{11}$ cm^{-2})
LPCVD SiO_2	850 °C, 2 hr., N2	6.4	2.73
ALD Al_2O_3	as-deposited	5.3	1.58
ALD Al_2O_3	500 °C, 2 min., FG	5.1	2.59
ALD Al_2O_3	500 °C, 2 min., N_2	5.2	2.25

Table 6.1: Extracted effective oxide charge density (N_{EFF}), total concentration of near interface traps (N_{it}) obtained by integrating the D_{it} profiles over the energy ranges of E_C-0.2 to E_C-0.6 eV.

The extracted D_{it} profiles as shown in figure 6.3 indicate a significantly higher interface state density for LPCVD SiO_2-β-Ga_2O_3 compared to the as deposited ALD Al_2O_3-β-Ga_2O_3 interface, which has the lowest D_{it} . Furthermore, increase of D_{it} is observed for ALD Al_2O_3 samples with PDA independent of the annealing ambient. The total density of interface traps, N_{it} was obtained by integrating the D_{it} profiles over the energy ranges of E_C-0.2 to E_C-0.6 eV, as shown in Table 6.1.

6.3 Photo-assisted *C-V* measurements

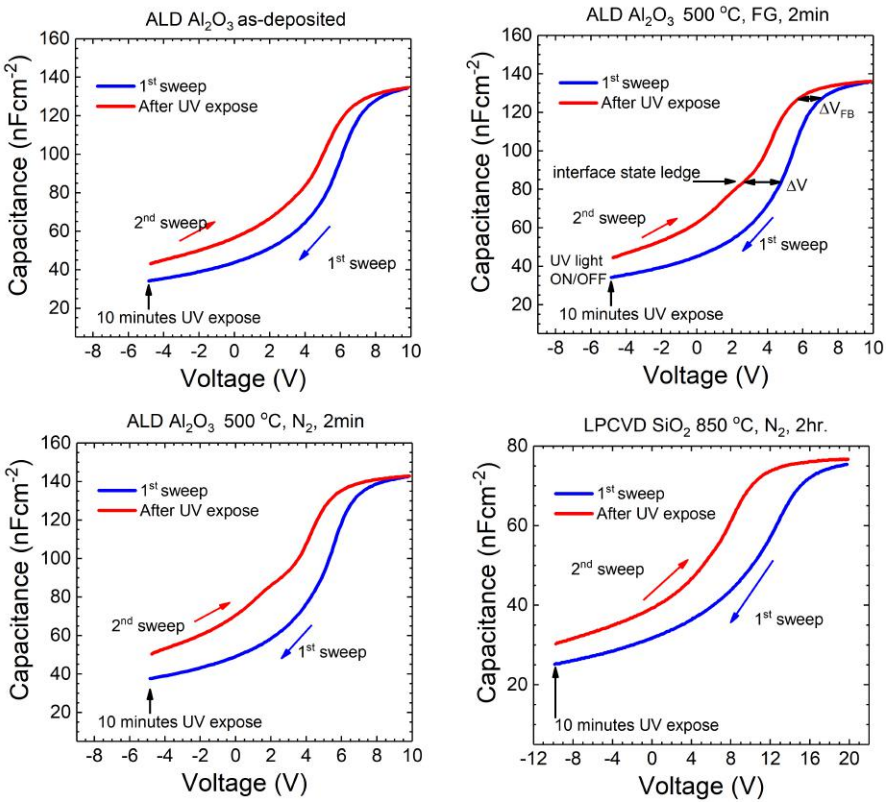

Figure 6.4: Photo assisted high frequency (100 kHz) *C-V* measurement on ALD Al_2O_3-$\beta-Ga_2O_3$ and LPCVD SiO_2-$\beta-Ga_2O_3$ MOS capacitors.

Photo-assisted *C-V* measurements were used to measure energetically deeper interface and border traps[27, 28, 29]. As we have discussed in chapter 3, section 3.2.3, in this technique, occupied deep traps are de-trapped due to the UV generated holes. While the device is swept from depletion to accumulation in the dark, electron traps get refilled. This de-trapping and trapping alters the total charges in the MOS system which in turn, appears as changes in *C-V* characteristics before and after UV illumination. Photo-assisted *C-V* measurement data on these MOS capacitors are shown in figure 6.4. The total number of deep interface traps density (N_{it}^{deep}) and 'border' traps (N_{bt}) was extracted using the following equations (section 3.2.3) [27, 29].

$$N_{it}^{deep} = \frac{C_{ox}\Delta V}{Aq} \tag{6.5}$$

$$N_{bt} = \frac{C_{ox}\Delta V_{FB}}{Aq} \tag{6.6}$$

where C_{ox}, A, q, ΔV, ΔV_{FB} are oxide capacitance, gate area, electron charge, voltage shift at a given capacitance and flat-band voltage shift respectively. The N_{it}^{deep} and N_{bt} values are shown in table 4.2. Photo-assisted *C-V* shows the highest N_{it}^{deep} and N_{bt} for the LPCVD SiO_2 sample. In addition, these results confirm the increase of interface states after the PDA on ALD Al_2O_3, suggesting the high temperature annealing to be detrimental for Al_2O_3-Ga_2O_3 interfaces.

Sample Info	PDA condition	N_{it}^{deep} ($\times 10^{12}$ cm^{-2})	N_{bt} ($\times 10^{12}$ cm^{-2})
LPCVD SiO_2	850 °C, 2 hr., N2	2.2	2.16
ALD Al_2O_3	as-deposited	0.84	0.51
ALD Al_2O_3	500 °C, 2 min., FG	1.99	0.99
ALD Al_2O_3	500 °C, 2 min., N_2	2.12	0.91

Table 6.2: Extracted total number of deep interface traps density (N_{it}^{deep}) and 'border' traps(N_{bt}) density from the photo-assisted *C-V* measurements for dielectric/ β-Ga_2O_3 MOS capacitors.

6.4 *I-V* measurements

Dielectric leakage currents were measured to determine the tunneling barrier height and the oxide breakdown strength. As shown in figure 6.5, among all the samples studied, the LPCVD SiO_2 with PDA had highest breakdown strength. The ALD-Al_2O_3 samples demonstrate significantly higher leakage currents and lower breakdown, independent of the annealing details. This result is consistent with the smaller conduction band offset at the Al_2O_3-Ga_2O_3 interface. Fowler-Nordheim (F-N) tunneling model was used to fit the *I-V* data in the high field region (as shown in figure 6.5 (b)) to extract tunneling barrier heights. Tunneling current density (J_{F-N}) is given by [31, 31, 32]

$$J_{F-N} = \frac{q^3 m_o E_{ox}^2}{8\pi h m_{ox}^* \Phi_B} \exp\left(\frac{-8\pi\sqrt{2qm_{ox}^*}\Phi_B^{3/2}}{3hE_{ox}}\right) \tag{6.7}$$

where m^*_{ox} is the effective electron mass in gate oxide, m_o is the free electron mass, q is the electron charge, h is the Plancks constant, E_{ox} is the electrical field across the gate oxide and Φ_B is the tunneling barrier height for electrons. The values used for the effective electron mass (m^*_{ox}) in the gate oxides were m^*_{ox} =0.42 m_o [30] for LPCVD SiO_2 and m^*_{ox} =0.28 m_o [33] for ALD Al_2O_3. The extracted Φ_B values, from slope of the $ln(J/E^2_{ox})$ vs. $1/E_{ox}$ curves were 2.14 eV for LPCVD SiO_2, and 1.4 eV for ALD Al_2O_3 samples. The Φ_B values determined here is in good agreement with the conduction band offsets at dielectric- β-Ga_2O_3.

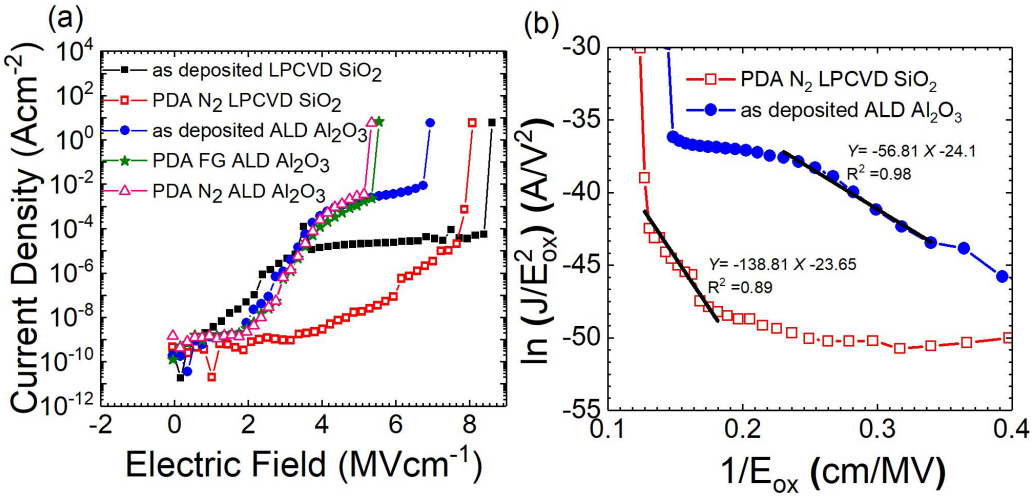

Figure 6.5: (a) Current density (J) vs. oxide electric field (E_{ox}) characteristics acquired on LPCVD SiO_2 and ALD Al_2O_3 MOS devices. (b) Representative FN tunneling plot (ln (J/E^2_{ox}) vs. $1/E_{ox}$) of 850 °C PDA LPCVD SiO_2 and as deposited ALD Al_2O_3 gated MOS capacitors.

6.5 Possible causes for higher density of interface traps in SiO_2-Ga_2O_3 compared to Al_2O_3-Ga_2O_3

The presence of native defects in gate dielectric with energy levels of 2.5∼2.8 eV below the SiO_2 conduction band[34, 35, 36], and 3∼4.3 eV below the Al_2O_3 conduction band [37, 38] can be used to explain higher density of 'border' traps at SiO_2/Ga_2O_3 interface compared to Al_2O_3/Ga_2O_3 interface. Energy band diagrams for Al_2O_3/Ga_2O_3 and SiO_2/Ga_2O_3 are shown in figure 6.6 where the energy levels of the insulator bulk traps are also schematically illustrated. For SiO_2, these defects are energetically located closer to the conduction band of the β-Ga_2O_3 (figure 6.6 (a)) which could be the origin of the higher density of 'border' traps at SiO_2/Ga_2O_3 interfaces. For Al_2O_3 on the other hand, the associated oxide trap levels are located well below

the conduction band of the β-Ga_2O_3 near the semiconductors midgap (figure 6.6 (b)). Furthermore, Guo et al.[38] have suggested that Al_2O_3 related oxide traps are unable to trap excess electrons in amorphous Al_2O_3.

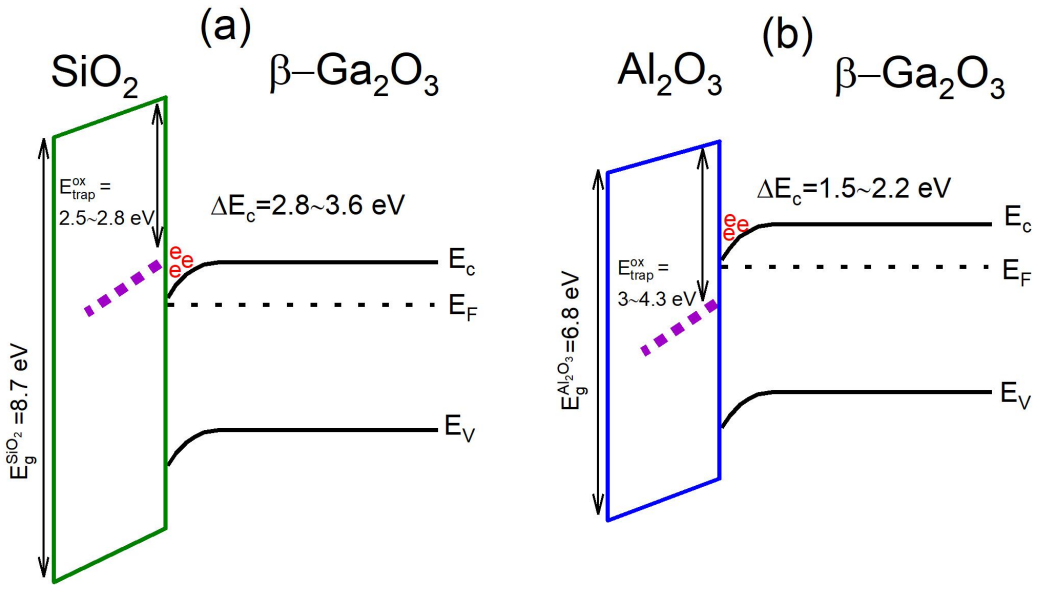

Figure 6.6: Schematic illustration of energy band diagram showing the reported conduction band offsets, oxide traps on (a) SiO_2-β-Ga_2O_3 and (b) Al_2O_3-β-Ga_2O_3 system.

In addition, structural changes of Al_2O_3/Ga_2O_3 system could be the source for changes in device characteristics after PDA. Similar electronic structure of the Al and Ga may facilitate inter-diffusion, leading to the formation of mixed phase β-Ga_{2-x} $Al_{2-x}O_3$, $0 \leq x \leq 2$ [39, 40] which could change the interfacial dielectric layer resulting in different interface trap profile. To this effect, Goyal et al.[41] have observed that at elevated annealing temperatures ($\sim$ 600 °C) Al inter-diffusion into Ga_2O_3 leads to Al substitution on Ga sites resulting in a change of lattice parameters[41]. In addition, Ma et al.[42] recently reported that the incorporation of Al into β-Ga_2O_3 leads to a tendency of forming oxygen interstitial defects. These hypotheses can be qualitatively related to the obtained higher interface trap profiles in ALD Al_2O_3/Ga_2O_3 interfaces after PDA.

6.6 Summary

In summary, this work indicates higher interface state density at the SiO_2-β-Ga_2O_3 interface compared to the Al_2O_3-β-Ga_2O_3 interface. Increase of D_{it} at the Al_2O_3-β-Ga_2O_3 interface

was also observed after post-deposition annealing at 500 °C. In addition, a higher density of 'border' traps were detected in the LPCVD SiO_2-β-Ga_2O_3 compared to the Al_2O_3-β-Ga_2O_3 interfaces. Furthermore, it was shown that LPCVD SiO_2 has a higher oxide field breakdown, which would be an advantage in *n*-channel Ga_2O_3 MOS applications. While the interface state density in both interfaces are reasonable for MOSFET operation, the effective negative charge and the border trap density needs to be further reduce for high performance Ga_2O_3 MOSFET with stable operation.

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Chapter 7

Conclusion and future work

7.1 Conclusion

β-Ga_2O_3 and 4H-SiC based Schottky diodes and MOSFETs are ideal for rectification and conversion of high voltage due to expected low specific on resistance. To have such power devices, it requires forming metal-semiconductor interfaces via metallization and dielectric-semiconductor interfaces via dielectric formation. In addition, advanced MOSFET geometry such as trench MOSFETs in 4H-SiC requires reactive ion etching to form trenches. Such technological steps can alter the WBG semiconductor surface as well as can introduce interface defects. Therefore, electronic characterization of technologically relevant interfaces are mandatory. Furthermore, characterization of inherent bulk defects as well as extrinsic bulk defects are also very important. Therefore, identification and quantification of defects in interfaces as well as in bulk are required for further development of these WBG semiconductors. In this regard, we have studied following interfaces in this work.

• Metal-semiconductor interfaces fabricated by metallization of Al, Mo, Au and Ni on β-Ga_2O_3 shown that Al interface results in Ohmic behavior and Mo, Au and Ni metal interfaces results in rectifying behavior. Temperature dependent electronic properties of Ni/($\bar{2}$01) β-Ga_2O_3 SBDs demonstrate a strong temperature dependence on barrier height and ideality factor. This has been attributed to the Schottky barrier spatial inhomogeneity. In addition, bulk defect investigation on EFG grown β-Ga_2O_3 was shown that presence of electron trap at 0.77 eV below the conduction band of β-Ga_2O_3 with a concentration of 2.6×10^{16} cm^{-3}, which arises from Fe impurity in the substrate.

• Electronic characterization of phosphorus (P) incorporated SiO_2-4H-SiC interface determine two near-interface oxide traps, named O1 (E_C-0.15 eV)(carbon dimer C_O=C_O) and O2 (E_C-0.4 eV) (interstitial Si (Si_i)), that are typically observed in thermal oxides on 4H-SiC. Experimental results in this work and theoretical models for trap passivation confirm that optimum P doping is more effective than nitridation in near-interface trap passivation.

• In this work, it has been demonstrated that standard thermal oxidation anisotropy in 4H-SiC Si-face (0001) and a-face ($11\bar{2}0$) can almost be eliminated by oxidizing 4H-SiC in a plasma afterglow furnace with optimized conditions. Furthermore, it has been shown that resultant SiO_2-4H-SiC interface for both oxides (plasma and standard thermal) has similar electrical properties after interface nitridation.

• Electronic characterization of SiO_2-4H-SiC interface on planar etched surfaces have shown that specific RIE process used in this work does not create an additional interface or bulk traps. Results on SiO_2-4H-SiC sidewall etched interface indicated that higher interface traps compared to the planar SiO_2-4H-SiC interface, which could be due to the physical properties of the side walls (surface roughness or specular crystal plane). In this work, trench MOSFETs have been fabricated based on discussed RIE process and plasma oxidation process. Electrical characterization has shown that, transistor behavior on these devices and also point out the requirement of well developed structures for better results.

• Results of dielectric-Ga_2O_3 interfaces have shown that the SiO_2-β-Ga_2O_3 interface has higher interface and near-interface trap density than the Al_2O_3-β-Ga_2O_3 interface. However, LPCVD SiO_2 was found to have the lowest dielectric leakage and highest breakdown field. Therefore, provided that low traps at SiO_2-β-Ga_2O_3 interfaces, SiO_2 will be a better candidate for *n*-channel Ga_2O_3 MOS applications.

7.2 Future work

Based on the discussion in the dissertation, in order for further development of power electronic devices based on β-Ga_2O_3 and 4H-SiC , more work should be carried out, including

• Electronic characterization of Schottky barrier diodes fabricated on β-Ga_2O_3 epitaxial layers and investigate breakdown characteristics on them. In this work, we have characterized

the SBDs based on the single crystal substrate. However, for the power device application, it requires having voltage rated SBDs which has blocking voltage limits. To develop these SBDs, it needs further investigation of properties on SBDs fabricated on epitaxial layers.

• Adopt low-temperature processes to make SiO_2 interface with β-Ga_2O_3 and study different post-deposition annealing process for reduction of traps in SiO_2-Ga_2O_3 interface. Technological requirements of high breakdown field and low gate leakage favors SiO_2 for MOS applications in the current state of development of these deposition processes. However, trap density is still high for MOS work. In this work, SiO_2 was deposited at a higher temperature compared to ALD process. If electrical properties of different deposition process can compare, deposition method with better electrical properties can be chosen for further investigation. For further reduction of the SiO_2-Ga_2O_3 interface state density, experiments with different post-deposition annealing steps is highly desirable.

• Further interface oxide trap investigation on SiO_2-4H-SiC interface by CCDLTS measurements. In this work, CCDLTS measurements have been used for study the thermally grown SiO_2-4H-SiC interface. However, further investigation with deposited SiO_2 can be used to understand the origin of the O1 and O2 trap. In addition, doing Arrhenius analysis for each V_p runs (probably above V_p=V_FB+2 V, where it can see the peaks) can be used to investigate the effect of tunneling in the extracted activation energies and capture cross-sections. Also, current transient DLTS can be used to examine the depth profile of these traps.

• Investigate electronic properties of different gate oxides/4H-SiC (side wall) interface. In this work, we have only investigated the NO-annealed SiO_2-4H-SiC sidewall interface. However, PSG results on planar capacitors as well as in lateral MOSFETs have shown promising results. Therefore, it is worthwhile to compare PSG and NO-annealed SiO_2-4H-SiC side wall interfaces, which can be use in the future trench devices.

• Adopt the N plasma passivation to avoid the re-oxidation due to NO annealing in the plasma growth oxides. N plasma passivation has shown comparable results to NO annealed samples. If N plasma passivation process used in trench MOSFET fabrication process, re-oxidation due to NO annealing can be mitigated. In that manner, oxide thickness difference between sidewall and bottom of the trench can be further reduced.

• Investigate different RIE recipes (different mask material, etch gas chemistry, different RIE reactors) for trench morphology and shape studies. Herein we have only investigated etched surfaces produced by CCP system with fluorine-based gas. However, as we discussed in chapter 6, other etch reactors and etch gas chemistry may result in different morphology as well as various shape in trenches. In this regard, studying properties of trenches with the different etch reactors, as well as multiple recipes, are required.

Appendices

APPENDIX A

VESTA input parameters

Title= β-**Ga_2O_3**

Lattice type= C

Space group name= C2/m

Space group number= 12

Lattice parameters

a=12.21430,b=3.03719,c=5.79819,

alpha =90.0000,beta=103.8320,gamma=90.0000

Structure parameters

Ga1=(0.09050,0.00000,0.79460)

Ga2=(0.34140,0.00000,0.68600)

O1=(0.16452,0.00000,0.10983)

O2=(0.49570,0.00000,0.25530)

O3=(0.82790,0.00000,0.43650)

Title= 4H-SiC (ABCB)

Lattice type=P

Space group name=P1

Space group number=1

Lattice parameters

a=3.08051, b=3.08051, c=10.08480,

alpha=90.0000,beta=90.0000,gamma=120.0000

Structure parameters

C1=(0.00000,0.00000,0.18784)

C3=(0.66667,0.33333,0.68784)

C2=(0.33333,0.66667,0.43671)

C4=(0.33333,0.66667,0.93671)

Si1=(0.00000,0.00000,0.00000)

Si3=(0.66667,0.33333,0.50000)

Si2=(0.33333,0.66667,0.24983)

Si4=(0.33333,0.66667,0.74983)

Title= 6H-SiC (ABCACB)

Lattice type=P Space group name=P63mc Space group number=186

Lattice parameters

a=3.08129, b =3.08129, c=15.11976

alpha=90.0000, beta=90.0000, gamma=120.0000

Structure parameters

C1=(0.00000,0.00000,0.12540)

C2=(0.33333,0.66667,0.29215)

Si1=(0.00000,0.00000,0.00000)

Si2=(0.33333,0.66667,0.16667)

Si3=(0.66667,0.33333,0.33333)

C3=(0.66667,0.33333,0.45833)

APPENDIX B

β-Ga_2O_3 cleaning process

Organic Cleaning

Each in ultrasonic shaker for 5 minutes

(1)Acetone

(2)Trichloroethylene(TCE)

(3)Acetone

(4)Methanol

(5)Methanol

(6)De-ionized water

Prianha etch (H_2SO_4 : 30% H_2O_2 1:1) for 1 5 minutes

Dry with N_2 gas

4H-SiC cleaning process

1. Use a cotton swab and acetone to remove the glue on 4H-SiC sample surface.

2. Each in ultrasonic shaker for 5 minutes

(a)Acetone

(b)Trichloroethylene(TCE)

(c)Acetone

(d)Methanol

(e)Methanol

(f)De-ionized water

3. Remove sample and place in buffered oxide etch (BOE) for 5min.

4. DI water ultrasonic shaker for 5 minutes.

5. 1:1 H_2SO_4:H_2O_2 for 15 minutes. Rinse sample in DI water 30 seconds, then place sample in BOE for 1min. Rinse sample in DI water 30 seconds.

6. 3:1:1 DI water:H_2O_2:NH_4OH for 15 minutes at 100-115 °C. Rinse sample in DI water 30 seconds, then place sample in BOE for 1min. Rinse sample in DI water 30 seconds.

7. 3:1:1 DI water:H_2O_2:HCl for 15 minutes at 100-115 °C. Rinse sample in DI water 30 seconds, then place sample in BOE for 1min. Rinse sample in DI water 30 seconds.

8. Rinse sample and dry with N_2 gas.

Plasma oxidation of 4H-SiC

1. Flow N_2 (500 sccm) in plasma furnace tube.

2. Turn ON cooling water.

3. Turn ON fans for furnace and magnets.

4. Load the sample.

5. Close N_2 gas and vacuum the furnace tube (0.2 Torr) for 15 minutes.

6. Turn ON microwave generator and wait until it ready to use.

7. Set the furnace tube temperature.

8. Flow O_2 (3000 sccm) and N_2O(300 sccm).

9. Start Microwave generater.

10. Adjust microwave power to 2kW.

11. After plasma ignites, adjust reflectors until reflected power is zero.

12. Let plasma run for 2 hors.

13. After plasma time is completed, turn microwave power down to zero.

14. Close O_2 and N_2O and open N_2 (3000 sccm).

15. Close vacuum. Once furnace tube pressure shows 680 Torr open exhaust.

16. Reduce N_2 flow rate to 500 sccm.

17. Sample densified for 1 hour in N_2 at 900 °C.

18. After densification, ramp down the furnace temperature to 850 °C.

19. Ground yourself since sample has a gate oxide. Unload the sample. Close N_2 and Vacuum furnace tube and fill back with N_2.

20. Turn off microwave power.

21. Turn off cooling water and fans.

22. Close all the gas tanks.

Thermal oxidation of 4H-SiC

1. Vacuum oxidation furnace tube until base pressure is less than 1 torr.

2. Flush oxidation furnace tube with argon for 10-15 min to remove residual gases.

3. Load samples into oxidation furnace tube.

4. Vacuum oxidation furnace tube for 10-15 min.

5. Flush oxidation furnace tube with argon for 15 min.

6. Set oxidation furnace temperature to 1150 °C and the ramp rate to 5 °C/min.

8. When temperature is at 1150 °C, stop argon and flaw oxygen at 500 sccm.

9. Let oxidation run for the desired time.

10. Stop oxygen and begin argon. Sample anneal in Ar for 30 min post oxidation.

12. Set oxidation furnace temperature ramp rate to 10 °C/min and ramp temperature down to oxidation furnace base temperature.

13. Ground yourself since sample has a gate oxide. Remove samples from oxidation furnace tube.

14. Vacuum the furnace tube and fill with Ar.

NO annealing

Ground yourself since sample has a gate oxide.

1. Vacuum oxidation furnace tube until base pressure is less than 1 torr.

2. Flush oxidation furnace tube with argon for 10-15 min to remove residual gases.

3. Load samples into oxidation furnace tube.

4. Vacuum oxidation furnace tube for 10-15 min.

5. Flush oxidation furnace tube with argon for 15 min. Close Vacuum valve. NO is corrosive.

6. Increase temperature to 1175 °C.

7. At 1175 °C , begin NO (575 sccm) 2 hour annealing and turn off argon flow.

8. Set NO regulator to 15 psi.

9. After anneal is done, stop NO (by closing tank top). Flow Ar to the furnace tube.

10. Let NO pressure drop to zero, and then flush NO lines with argon.

11. Set furnace temperature ramp rate to 10 °C/min and ramp temperature down to furnace base temperature (900 °C).

12. Unload the sample.

13. Vacuum the furnace tube and fill with Ar.

14. Stop argon flow in NO lines and vacuum NO lines until pressure is zero.

15. Stop vacuum of NO lines.

16. Close Ar tank top.

Al thermal evaporation procedure

Ground yourself if sample has a gate oxide.

1. Turn OFF the Ion Gauge.

2. Check roughing pump closed.

3. Check fore-line open.

4. Close the high vacuum.

5. Open the Nitrogen (N_2) gas to chamber.

6. Load Al pellets in the bridge holder.

7. Load samples facing down with the shadow mask.

8. Slowly open the roughing pump and hold tightly chamber down.

9. At 100 mtorr, close rouging pump, open fore-line.

10. Slowly open high vacuum to the chamber.

12. When pressure is 1×10^{-6} torr, turn on Voltmeter and Ammeter. Turn on AC power(60%).

13. Pre-evaporate Al for 20 seconds.

14. Remove the cover plate and expose samples for 4 minutes.

15. Turn off AC power.

16. Repeat step 1 to 5 . Remove samples

17. Repeat step 7 to 10 and return the system to stand-by mode.

Mask aligner and spinner procedure

Ground yourself if sample has a gate oxide.

1. Clean the Si wafer(use H_2O_2 to remove Mo, acids to remove metal) Or just clean by organic cleaning (Acetone, Methanol, Di water) 2. Get funnel and blow N_2 gas.

3. Small amount of 5214E photoresist and attached the sample. Attached extra edge plate samples for avoid edge beads.

4. 15 minutes bake in oven at 105 °C

5. 10 minuets in HMDS for NLOF 2070 (negative) or 4620(positive)

6. ON Vacuum switch, open N_2 gas valve to the spinner. Turn ON spinner. Select the proper revolutions per minute(rpm) and spin time. For NLOF 2070 5000 rpm and 30 sec. For 5214 and 4620 4000 rpm and 30 sec.

7. Align (center the sample) wafer in the spinner. Vacuum the sample to stick in to rotator.

8. Use new funnel and pipet to get desired photo resist. Sample cover with photoresist without air bubbles.

9. Run spinner with selected program.

10. Perform the soft bake procedure. For 5214 , 1 minute at 105 °C. For 2070, 90 seconds at 105 °C. For 4620, 20 minutes starting from 65 °C to 95 °C.

12. Remove edge plates.

11. Mask aligning and UV expose by using a MJB3 Karl Suss mask aligner. UV expose time varies with photoresist type. Usually 5214 and 2070 require 30 second expose. 4620 require 90 second expose.

If 2070 used, 90 second bake required after UV expose.

12. Use AZ 726 MIF to develop the exposed photoresist and the sample was finally rinsed in DI water and dried in nitrogen.

DC sputtering

1. Turn off the ion gauge.

2. Close the High vacuum.

3. Check high vacuum partial valve is Open.

4. Filling nitorgen gas (Open valve on wall, Open the gas intake on vacuum system)

5. 790 torr (digital display) close nitrogen gas.

7. Open the chamber and place the sample. Change desired target and chimney. (Ground yourself if sample has a gate oxide)

8. Close the chamber. Open roughing pump slowly. When presser get down to 30 mtorr. Close roughing pump. open fore-line. Slowly open high vacuum valve.

9. At 3×10^{-7} torr, turn off ion gauge. Close high turbo pump partial valve. Open Ar (95 sccm, 17 mtorr). Wait until turbo pump power settle down. Check power line for target and cooling water is open.

10. Turn on power and increase voltage up to plasma ignition.

11. Once plasma ON maintain current(Mo=0.4 A, Ti=0.25 A, Ni=0.2 etc) by voltage knob.

12. Pre sputter 2 minutes and sputter desired time to sample.

13. Turn down voltage and power off. Close Ar. Close high vacuum and open nitrogen.

14. Take the sample out. Clean the sputtering chamber by vacuum cleaner.

15. Pump down the chamber for steady state of the system.

Reactive ion etch procedure (CCP system)

1. Sample attached to Si 2 inch wafer (covered with NLOF 2070) or graphite plate

2. Open glass window of etcher.

3. Place wafer on electrode. Try to center the sample.

4. Use large tweezers to press down on wafer to ensure it is securely in place.

5. Close the glass window and tighten until snug.

6. Open nitrogen for 1 minute.

7. Vacuum system for 30 minutes until system reaches base pressure (5 mtorr).

8. Open all valves to etch gas line and turn on the appropriate switch on the flow controller. If necessary change the flow rates.

9. Flush the gas line for 5 minutes.

10. Turn on RF power supply.

11. Adjust power setting to about three watts higher than the desired power.

12. Turn ON RF power.

13. If necessary, adjust power to appropriate level and adjust matching network to obtain the lowest possible reflected power.

14. After desired etch time, turn off the RF power.

15. Turn off the etchant gas and allow system to vacuum to base pressure.

16. Fill chamber with nitrogen for 1 minute and vacuum again. Repeat this step at least two times. etch gases are toxic gases.

17. Close vacuum valve and fill chamber with nitrogen to get atmospheric pressure.

18. Remove the wafer with the sample.

19. Fill chamber with nitrogen for 1 minute. Close all the gas tanks.

20. If no other etching is required, turn off the vacuum pump.

APPENDIX C

DLTS technique : Detail derivation

Rate change in trap center occupancy

When electrons are captured and emitted by the electron traps, the trap occupancy rate of change can be written as follows

$$\begin{gathered}\frac{dn_T}{dt} = \text{electron capture rate-electron emission rate} = c_n n(N_T - n_T) - e_n n_T \\ \frac{dn_T}{dt} = c_n n N_T - (c_n n + e_n) n_T\end{gathered} \tag{1}$$

where c_n is electron capture coefficient, e_n is electron emission coefficient, N_T is total electron trap density (cm^{-3}) , n_T is occupied electron trap density (cm^{-3}) and n is electron density in conduction band.

Solving the equation 1 (first order differential equation), expression for $n_T(t)$ can be found as follows.

$$\begin{gathered}\frac{dn_T}{dt} = c_n n N_T - (c_n n + e_n) n_T \\ \frac{dn_T}{dt} + (c_n n + e_n) n_T = c_n n N_T \\ \text{considering constants } A = (c_n n + e_n) \text{ and } B = c_n n N_T \\ \frac{dn_T}{dt} + A n_T = B\end{gathered} \tag{2}$$

$$
\begin{aligned}
\tfrac{dn_T}{dt} + An_T &= B \\
U(t) &= e^{\int A dt} = e^{At} \\
e^{At}\tfrac{dn_T}{dt} + e^{At}n_T &= Be^{At} \\
\Rightarrow \tfrac{d}{dt}\left[e^{At}n_T\right]_0^t &= \int_0^t Be^{At}dt \\
\Rightarrow e^{At}n_T(t) - n_T(0) &= \left[\tfrac{Be^{At}}{A}\right]_0^t \\
\Rightarrow e^{At}n_T(t) - n_T(0 &= \tfrac{Be^{At}}{A} - \tfrac{B}{A} \\
n_T(t) &= n_T(0)e^{-At} + \tfrac{B}{A} - \tfrac{B}{A}e^{-At}
\end{aligned}
\tag{3}
$$

The time dependence of $n_T(t)$ during the *capture period* can be found by setting $e_n = 0$, $A = c_n n$,$B = c_n n N_T$ and $\frac{B}{A} = N_T$

$$
\begin{aligned}
n_T(t) &= n_T(0)e^{-c_n nt} + nN_T - nN_T e^{-c_n nt} \\
n_T(t) &= N_T - (N_T - n_T(0))e^{-c_n nt}
\end{aligned}
\tag{4}
$$

The time dependence of $n_T(t)$ during the *emission period* can be found by setting $c_n = 0$, $A = e_n$,$B = 0$

$$
n_T(t) = n_T(0)e^{-e_n t} \tag{5}
$$

Capacitance transient

In Schottky diode, the transient measurement is time-varying capacitance, which is corresponding to time-varying depletion width(W). The capacitance transient can be found by considering the time-varying charge,$N_{scr}(t)$, in the space charge region as follows.

$$
C(t) = A\sqrt{\tfrac{q\epsilon_s}{2}}\sqrt{\tfrac{N_{scr}(t)}{V_{bi}-V}} \tag{6}
$$

where A is device area, q is elemental charge, ϵ_s is permittivity of the semiconductor, V_{bi} is built in potential, V is applied bias. With the time varying charge in space-charge region $N_{scr}(t) = N_D^+ - n_T(t)$

$$
\begin{aligned}
C(t) &= A\sqrt{\tfrac{q\epsilon_s}{2}}\sqrt{\tfrac{N_D^+ - n_T}{V_{bi}-V}} \\
\Rightarrow C(t) &= A\sqrt{\tfrac{q\epsilon_s N_D}{2(V_{bi}-V)}}\sqrt{1-\tfrac{n_T(t)}{N_D}} \\
C(t) &= C_0\sqrt{1-\tfrac{n_T(t)}{N_D}} \qquad (7) \\
&\text{where} \\
C_0 &= A\sqrt{\tfrac{q\epsilon_s N_D}{2(V_{bi}-V)}}
\end{aligned}
$$

C_0 is the capacitance of the Schottky diode at reverse bias voltage $-V$.

With Taylor series expansion, $(1-x)^{\frac{1}{2}} = 1 - \frac{1}{2}x + - - -$

$$
C(t) = C_0\Big(1 - \tfrac{n_T(t)}{2N_D}\Big) \qquad (8)
$$

Then capacitance transient during the *emission period* can be found by substituting the expression for $n_T(t)$ from the equation 5 as follows

$$
\begin{aligned}
C(t) &= C_0\Big(1 - (\tfrac{n_T(0)}{2N_D})\exp(-e_n t)\Big) \\
&\text{or with } e_n = 1/\tau_n \qquad (9) \\
C(t) &= C_0\Big(1 - (\tfrac{n_T(0)}{2N_D})\exp(-\tfrac{t}{\tau_n})\Big)
\end{aligned}
$$

Therefore, DLTS signal (capacitance transient measured at two different time) can be written as follows

$$
S(T) = C(t_1) - C(t_2) = C_0\frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{t_2}{\tau_n}\Big) - \exp\Big(-\frac{t_1}{\tau_n}\Big)\Big] \qquad (10)
$$

Relation of the rate window (τ_{max}^{-1}) of the spectrometer and trap emission coefficient (e_n)

When DLTS spectra shows a peak (maximum or minimum) at temperature *T*, emission rates (e_n) of the traps will be equal to rate window of the spectrometer(τ_{max}^{-1}). Set values of t_1 and t_2 in spectrometer determine the rate window of the spectrometer. Therefore, relationship between τ_{max} and t_1 and t_2 is derived by finding the maximum (or minimum) for $S(T)$ (differentiating $S(T)$ with respect to τ_n and setting the result equal to zero).

$$
\begin{aligned}
&\frac{dS(T)}{d\tau_n} = 0 \\
\Rightarrow C_0 \frac{n_T(0)}{2N_D} \Big[-t_2(-1)\exp\Big(-\frac{t_2}{\tau_{max}}\Big) - -t_1(-1)exp\Big(-\frac{t_1}{\tau_{max}}\Big)\Big] &= 0 \\
\Rightarrow t_1 \exp\Big(-\frac{t_1}{\tau_{max}}\Big) &= t_2 \exp\Big(-\frac{t_2}{\tau_{max}}\Big) \\
\Rightarrow \exp\Big(\frac{(t_2-t_1)}{\tau_{max}}\Big) &= \frac{t_2}{t_1} \\
\Rightarrow \frac{(t_2-t_1)}{\tau_{max}} &= ln\Big(\frac{t_2}{t_1}\Big) \\
\tau_{max} &= \frac{t_2-t_1}{\ln(t_2/t_1)}
\end{aligned}
\tag{11}
$$

Thus, the emission rate (e_n) corresponding to the maximum of a trap peak observed in a DLTS spectra is a precisely defined quantity which is given by $\tau_{max}^{-1} = \frac{\ln(t_2/t_1)}{t_2-t_1}$.

Trap concentration, N_T

When DLTS spectra shows a peak (maximum or minimum) at temperature *T*,DLTS signal is $S(T) = \Delta C_{max}$, which is given by,

$$
\begin{aligned}
\Delta C_{max} = C(t_1) - C(t_2) &= C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{t_2}{\tau_n}\Big) - \exp\Big(-\frac{t_1}{\tau_n}\Big)\Big] \\
&\text{with } \tau_n = \tau_{max} \\
\Delta C_{max} = C(t_1) - C(t_2) &= C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{t_2}{\tau_{max}}\Big) - \exp\Big(-\frac{t_1}{\tau_{max}}\Big)\Big]
\end{aligned}
\tag{12}
$$

Further simplification

$$
\begin{aligned}
\Delta C_{max} &= C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{t_2}{\tau_{max}}\Big) - \exp\Big(-\frac{t_1}{\tau_{max}}\Big)\Big] \\
&\text{Let } \frac{t_2}{t_1} = r, \text{ then } t_2 = rt_1 \text{ and } \tau_{max} = \frac{(r-1)t_1}{\ln(r)} \\
\text{first } t_2 \text{ replace by } rt_1 \Rightarrow \Delta C_{max} &= C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{rt_1}{\tau_{max}}\Big) - \exp\Big(-\frac{t_1}{\tau_{max}}\Big)\Big] \\
&\text{Let } x = \exp\Big(-\frac{t_1}{\tau_{max}}\Big), then
\end{aligned}
\tag{13}
$$

$$\Delta C_{max} = C_0 \frac{n_T(0)}{2N_D}\Big[x^r - x\Big]$$
$$\Rightarrow \Delta C_{max} = C_0 \frac{n_T(0)}{2N_D}\Big[x^r\Big(1 - x^{(1-r)}\Big)\Big]$$
Now x is replace back ,$x = \exp\Big(-\frac{t_1}{\tau_{max}}\Big)$, and with the $t_1 = \frac{\ln(r)\tau_{max}}{(r-1)}$
$$\Rightarrow \Delta C_{max} = C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{r\ln(r)\tau_{max}}{(r-1)\tau_{max}}\Big)\Big]\Big[1 - \exp\Big(-\frac{(1-r)\ln(r)\tau_{max}}{(r-1)\tau_{max}}\Big)\Big] \quad (14)$$
$$\Rightarrow \Delta C_{max} = C_0 \frac{n_T(0)}{2N_D}\Big[\exp\Big(-\frac{r\ln(r)}{(r-1)}\Big)\Big]\Big[1 - r\Big]$$
Assuming $n_T(0) = N_T$
$$N_T = \frac{\Delta C_{max}}{C_0}\frac{2N_D[\exp(\frac{r\ln(r)}{(r-1)})]}{(1-r)}$$

Where r is proportionality factor of spectrometer detection time t_1 and t_2, which determine the rate window. Hence,

$$N_T = \frac{f(r)\cdot 2\cdot \Delta C_{max} N_D}{C_0} \quad (15)$$
where f(r) is

$$f(r) = [\frac{\exp(\frac{r\ln(r)}{(r-1)})}{(1-r)}] \quad (16)$$

Incomplete trap filling

For the above derivations, we have assumed that all the traps within the depletion width (W_R) corresponding to revers bias voltage (-V_R) has been filled with electrons during the filling pulse (up to zero bias) and emitted back during the emission period . However, for zero bias device, traps within $\lambda(E_T)$ from the metal-semiconductor interface do not fill because they are located above the fermi level. Furthermore, when the device bias switch to revers bias -V_R, traps within the $\lambda(E_T)$ from the tail of the space charge region do not emit electrons because they are below the fermi level.

This transition distance $\lambda(E_T)$ is given by

$$\lambda(E_T) = \sqrt{\frac{2\cdot \epsilon_{rs}\epsilon_o\Big(E_T - E_F)\Big)}{qN_D}} \quad (17)$$

where q is the elementary charge, ϵ_{rs} is relative dielectric constant, ϵ_o is the vacuum permittivity 8.8×10^{14} Fcm^{-2}, E_F is the position of the Fermi level from bottom of the conduction band at the temperature of the DLTS peak and E_T is the trap energy level from the bottom of the conduction band edge.

Therefore, considering the spatial dependence, DLTS signal can be written as follows.

$$\begin{aligned} S(T) = C(t_1) - C(t_2) &= C_0 \frac{\int_{W_P-\lambda}^{W_R-\lambda} n_T(0,x)xdx}{2\int_0^{W_R} N_D(x)xdx} \left[\exp\left(-\frac{t_2}{\tau_n} \right) - \exp\left(-\frac{t_1}{\tau_n} \right) \right] \\ S(T) &= C_0 \frac{n_T[(W_R-\lambda)^2-(W_P-\lambda)^2]}{2N_D W_R^2} \left[\exp\left(-\frac{t_2}{\tau_n} \right) - \exp\left(-\frac{t_1}{\tau_n} \right) \right] \end{aligned} \tag{18}$$

where W_P is the depletion layer width during the filling pulse and W_R is the depletion layer width for constant voltage.

Accordingly, N_T values can be calculated from the

$$\begin{aligned} N_T &= \frac{f(r)\cdot 2\cdot \Delta C_{max} N_D W_R^2}{C_0[(W_R-\lambda)^2-(W_P-\lambda)^2]} \\ &\text{where f(r) is} \\ f(r) &= [\frac{\exp(\frac{r\ln(r)}{(r-1)})}{(1-r)}] \end{aligned} \tag{19}$$

SULA System: DLTS instrument in our lab

During the DLTS measurements, t_1 and t_2 is automatically set by SULA system for pre selected (by user) correlator IDs (initial delay times). Figure C.1 shows illustration of applied charging pulse, capacitance transient and capacitance transient detection points(t_1 and t_2) corresponding to correlator timing. As shown in figure, SULA system maintains the $t_1 = 2.8ID$ and $t_2 = 7.0ID$.

Therefore, r factor which is determined the relation between t_1 and t_2 is equal to 2.5 as shown bellow.

$$r = \frac{t_2}{t_1} = \frac{7.0ID}{2.8ID} = 2.5 \tag{20}$$

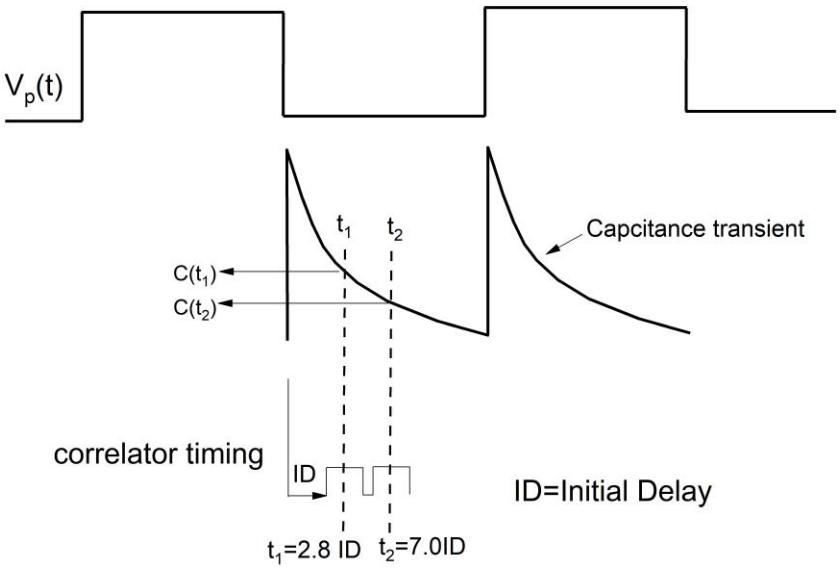

Figure C.1 : Initial delay and sampling timing of SULA system

Accordingly, calculated $f(r)$ for SULA system extracted data is

$$|f(r)| = |[\frac{\exp(\frac{r\ln(r)}{(r-1)})}{(1-r)}]| = |[\frac{\exp(\frac{2.5\ln(2.5)}{(1.5)})}{(-1.5)}]| = 3.0700 \simeq 3 \tag{21}$$

This is how factor 3 arise in the N_T calculation equation. Since factor 3 directly related to t_1 and t_2, it is a property of the instrument. Now, with the $f(r) = 3$, N_T calculation equation can be written as follows.

$$N_T = \frac{3 \cdot 2 \cdot \Delta C_{max} N_D W_R^2}{C_0[(W_R - \lambda)^2 - (W_P - \lambda)^2]} \tag{22}$$

Relation between correlator ID and emission rates (e_n)

As we discussed the emission rate (e_n) is equal to the spectrometer rate window τ^-1_{max}, for the trap peak observed in a DLTS spectra. τ_{max}^{-1} is given by $\frac{\ln(t_2/t_1)}{t_2-t_1}$. Therefore, for given ID (initial delay) τ_{max}^{-1} in SULA system can be found by with $t_1 = 2.8ID$ and $t_2 = 7.0ID$ as follows

$$\begin{gathered} \tau_{max} = \frac{t_2-t_1}{\ln(t_2/t_1)} = \frac{(7-2.8)ID}{\ln(2.5)} = 4.583ID \\ \tau_{max}^{-1} = \frac{1}{4.583ID} \end{gathered} \tag{23}$$

However, SULA system instrumentation manual is given different relation as follows. This is the relation we have used in this work.

$$\tau_{max}^{-1} = \frac{1}{4.3ID} \tag{24}$$

Accordingly, relation between ID and DLTS detected trap emission rate (e_n) is 2.1.

ID (ms)	e_n (s^{-1}) $=1/(4.3 \times ID \times 1000)$
100	2.325
50	4.651
20	11.627
10	23.255
5	46.511
2	116.279
1	232.558
0.5	465.116
0.2	1162.790
0.1	2325.581
0.05	4651.162
0.02	11627.906

APPENDIX D

CCDLTS signal: Voltage transient

When MOS capacitor bias in depletion bias, high frequency capacitance of the MOS capacitor can be written as the series combination of oxide capacitance C_{ox} and semiconductor depletion capacitance C_s as follows.

$$\begin{aligned} \frac{1}{C_{HF}} &= \frac{1}{C_{ox}} + \frac{1}{C_s} \\ C_{HF} &= \frac{C_{ox}C_s}{C_{ox}+C_s} \end{aligned} \tag{25}$$

In CCDLTS, capacitance of the MOS device held at a constant capacitance. In addition, oxide capacitance is independent of the gate voltage. Therefore, during the transient measurements in CCDLTS, semiconductor depletion capacitance C_s held at constant.

Considering the applied gate voltage, which divides across the oxide and semiconductor, can be written according to the following equation.

$$V_G = V_{ox} + \psi_S + \psi_{MS} \tag{26}$$

where V_{ox} and ψ_S are potential across the oxide and surface potential, respectively. From Gauss' law, V_{ox} depends on the net charge at the oxide-semiconductor interface and can be written as follows.

$$V_{ox} = -\frac{A(Q_{is} + Q_s)}{C_{ox}} \tag{27}$$

where Q_{is} is interface charge and *A* is device gate area. Herein charge densities are in per unit area. As we discussed in the chapter 3, if C_s is constant, then semiconductor band

bending will be constant and corresponding surface potential, ψ_S, is constant. Because of that semiconductor depletion region charge density per unit area, Q_s, is constant.

Now, equation 26 can be written as follows,

$$V_G = -\frac{A(Q_{is} + Q_s)}{C_{ox}} + \psi_S + \psi_{MS} \tag{28}$$

In CCDLTS technique, the voltage transient after the filling pulse is monitored as a function of temperature and measured at two different times t_1 and t_2. This signal, $\Delta V = V_G(t_1) - V_G(t_2)$ is linearly dependent on the deference of the net interface charge as follows.

$$\Delta V = V_G(t_1) - V_G(t_2)$$
$$\Rightarrow \Delta V = (-\tfrac{A(Q_{is}(t_1)+Q_s)}{C_{ox}} + \psi_S + \psi_{MS}) - (-\tfrac{A(Q_{is}(t_2)+Q_s)}{C_{ox}} + \psi_S + \psi_{MS})$$

Since ψ_S, Q_s are constant for constant capacitance as shown above and ψ_{MS} is constant

$$\Rightarrow \Delta V = -\tfrac{A}{C_{ox}}\Big[Q_{is}(t_1) - Q_{is}(t_2)\Big] \tag{29}$$

In DLTS measurements, $S(T) = C(t_1) - C(t_2)$ signal shows minimum for major (electron) traps (peak minima) when monitored as a function of temperature. However, in CCDLTS measurements, $\Delta V = V_G(t_1) - V_G(t_2)$ signal shows maximum for major (electron) traps (peak maxima) when monitored as a function of temperature. Negative sign in the equation 29 mathematically explain this.

Considering the voltage transient without the sign conversion, equation 29 can be written as follows.

$$\Delta V = \frac{A}{C_{ox}}\Big[Q_{is}(t_1) - Q_{is}(t_2)\Big] \tag{30}$$

As we discussed in the DLTS section appendix C, time dependence of trap occupancy ,$N_{IT}(t)$, during the *emission period* can be found by

$$N_{IT}(t, E) = N_{IT}(0, E)\exp(-e_n t) \tag{31}$$

Therefore, time variation or time dependent net interface charge can be written as

$$Q_{is} = qN_{IT}(E)\exp(-e_{n,T_P}t) \tag{32}$$

Accordingly, equation 30, CCDLTS signal for electron emission form the single energy level can be written as follows.

$$\Delta V = \Big(Aq/C_{ox}\Big)N_{IT}(E)\Big[\exp(-e_n t_1) - \exp(-e_n t_2)\Big] \tag{33}$$

Furthermore, trap density for single energy level can be found when $\Delta V(T_0)$ is the maximum of the CCDLTS signal for peak temperature T_0 as follows. This is similar to DLTS analysis.

$$\begin{gathered} N_{IT} = f(r)\frac{(C_{ox}/A)\Delta V(T_o)}{q} \\ \text{where f(r) is} \\ f(r) = [\frac{\exp(\frac{r\ln(r)}{(r-1)})}{(1-r)}] \\ \text{where f(r)=3 for } t_2\text{=2.5}t_1 \end{gathered} \tag{34}$$

However, CCDLTS spectra shows broader peak signal which is due to the interface state distribution. Therefore, it requires to consider time dependent net interface charge density, which can be written as

$$Q_{is} = \int qN_{IT}(E)\exp(-e_{n,T_P}t)dE \tag{35}$$

Then CCDLTS signal for electron emission form the interface state distribution can be written as follows.

$$\Delta V = \Big(Aq/C_{ox}\Big)\int N_{IT}(E)\Big[\exp(-e_n t_1) - \exp(-e_n t_2)\Big]dE \tag{36}$$

where e_n is electron emission rate which is given by

$$e_n = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-E}{kT}\right) \tag{37}$$

For the trap emission at the peak temperature T_P can be written as

$$e_{n,Tp}(E) = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-E}{kT_P}\right) \tag{38}$$

For further analysis of equation 38 (since experimental CCDLTS signal is given by scanning the temperature range, not over the energy range), it requires to change the variable E to T.

In this regard, equation 38, emission rate from single energy level E_P can be written as follows

$$e_{n,Ep}(T) = \sigma_n \upsilon_{th} N_C \exp\left(\frac{-E_P}{kT}\right) \tag{39}$$

Then CCDLTS signal can be written as follows.

$$\begin{aligned} \Delta V &= \Big(Aq/C_{ox}\Big) \int N_{IT}(E) \Big[\exp(-e_{n,Ep}t_1) - \exp(-e_{n,Ep}t_2)\Big] \tfrac{dE}{dT} dT \\ &\Rightarrow \tfrac{\Delta V}{\int [\exp(-e_{n,Ep}t_1) - \exp(-e_{n,Ep}t_2)] dT} = \Big(Aq/C_{ox}\Big) N_{IT}(E) \tfrac{dE}{dT} \\ &\Rightarrow \tfrac{\int \Delta V dT}{\int [\exp(-e_{n,Ep}t_1) - \exp(-e_{n,Ep}t_2)] dT} = \Big(Aq/C_{ox}\Big) \int N_{IT}(E) dE \\ &\tfrac{\int \Delta V dT}{\int [\exp(-e_{n,Ep}t_1) - \exp(-e_{n,Ep}t_2)] dT} = \Big(Aq/C_{ox}\Big) N_{IT} \end{aligned} \tag{40}$$

Introducing $f(T)$ as follows

$$f(T) = \int [\exp(-e_{n,Ep}t_1) - \exp(-e_{n,Ep}t_2)] dT \tag{41}$$

$$N_{IT} = \tfrac{C_{ox}}{Aq} \tfrac{\int \Delta V dT}{f(T)} \tag{42}$$

However, to compare the experimental CCDLTS signal with the CCDLTS signal corresponding to a single energy level having the same peak temperature and amplitude, equation 42 has to be further modified.

CCDLTS signal $S(T)$ (equation 43) for single energy level, peak amplitude will be equal to $\Delta V(T_p)$ at peak temperature, when $A(T)$ is equal to $3\Delta V(T_p)$ (rate window with t_2=2.5t_1 will be result in $[\exp(-e_n t_1) - \exp(-e_n t_2)] = 1/3$ as shown in DLTS section)

$$\Delta S(T) = A(T)[\exp(-e_n t_1) - \exp(-e_n t_2)] \tag{43}$$

Therefore, equation 42 can be modified to compare the experimental CCDLTS signal and CCDLTS signal for having one energy peak as follows

$$\begin{gathered} N_{IT} = \frac{3\Delta V(T_P)C_{ox}}{Aq}\frac{\int \Delta V dT}{3\Delta V(T_P)f(T)} \\ \text{By intrducing the } \Delta W \text{ as} \\ \Delta W = \frac{\int \Delta V dT}{3\Delta V(T_P)f(T)} \\ N_{IT} = \frac{3\times\Delta V(T_P)C_{ox}\Delta W}{Aq} \end{gathered} \tag{44}$$

where ΔW is the broadening factor given by the ratio of the integral of the experimental CCDLTS signal ΔV and the integral of the function S(T)(CCDLTS signal for single energy level) over temperature.

MATLAB Code

%Asanka Jayawardena CCDLTS ideal spectra

clc

clear all;

close all;

%constants and parameters

h = 6.62617E-34; %Js(Plank Constant)

mo = 9.1095E-31; % kg (electron Rest mass)

k = 1.38066E-23 ; %J/K (Boatsman Constant)

q = 1.60E-19; %C (charge)

Eo = 8.85E-14; %F/cm (permittivity in vacuum)

%Semiproperties

SiC4H =$[0.42, 0.66, 3.26, 3.7, 9.7]$;

Semi=SiC4H;

me = Semi(1); %effective mass of the electron

```
mh = Semi(2); %effective mass of the hole
Eg = Semi(3); % energy band gap
Xs = Semi(4); % electron affinity
Er = Semi(5); % dielectric constant
Es=Er*Eo;%unit:F/cm
% Inputs from User
gamA=((mo*k^2*2*((2*pi)^(3/2))*sqrt(3))/(h^3))*1E-4;
%cm-2.s-1.K-2 Schroder page 262 gama simplification
gamn=gamA*me; %cm-2.s-1.K-2 for SiC
prompt ='Correlator ID for experimental data (ms)=';
CID=input(prompt);
CID=CID*1E-3;
prompt ='Trap level 1 (Ec-ET)(eV)= ';
ET1=input(prompt);
prompt ='Capture cross-section for trap level 1 (Ec-ET) (cm^2)= ';
S1=input(prompt);
prompt ='Maximum CCLDTS peak amplitude for trap lavel 1 (ET1) from experiment data(
correlator ID should be same) (mV)=';
DV1=input(prompt);
prompt ='Trap level 2 (Ec-ET)(eV)= ';
ET2=input(prompt);
prompt ='Capture cross-section for trap level (Ec-ET) 2 ?(cm^2)= ';
S2=input(prompt);
prompt ='Maximum CCLDTS peak amplitude for trap lavel 2 (ET2) from experiment data(
correlator ID should be same) (mV)=';
DV2=input(prompt);
% correlator timing in SULA system
t1=2.8*CID;
t2=7.0*CID;
```

```
%Temperture range(K)
T1=77:0.1:300;
[m,n]=size(T1);
for i=1:n
T(i)=T1(i);
kT(i)=k*T(i)./q;%kT in eV
%Trap level 1%
en1(i)=S1*gamn*((T(i)).^2).*exp(-ET1/(kT(i)));% trap level 1
ST1(i)=3*DV1*(exp(-en1(i)*t1)-exp(-en1(i)*t2));% tap level 1
% Trap level 2% en2(i)=S2*gamn*((T(i)).^2).*exp(-ET2/(kT(i)));% trap level 2
ST2(i)=3*DV2*(exp(-en2(i)*t1)-exp(-en2(i)*t2));%tap level 2
end
plot (T,ST1,'b',T,ST2,'r')
title('Simulated CCDLTS')
xlabel('T(K)')
ylabel('CCDLTS signal (mV)')
ST11=ST1';
ST22=ST2';
Tnew=T';
Data=[Tnew ST11 ST22];
save name Data -ascii -tabs;
```