Superconducting Digital Logic Families Using Quantum Phase-slip Junctions

by

Uday Sravan Goteti

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Approved by

Michael C. Hamilton, Chair, Associate Professor of Electrical and Computer Engineering
Masoud Mahjouri-Samani, Assistant Professor of Electrical and Computer Engineering
Mark L. Adams, Assistant Professor of Electrical and Computer Engineering
Ryan B. Comes, Assistant Professor of Physics
Minseo Park, Professor of Physics

Abstract

Superconducting electronics based computing is being actively pursued as an alternative to CMOS-based computing for high performance computing due to their inherent advantages such as low-power and high switching speed. These circuits are predominantly based on Josephson junctions. In this work, superconducting digital electronic circuits based on a device called quantum phase-slip junction are explored. Quantum phase-slip junctions are dual to Josephson junctions based on charge-flux duality of Maxwell's equations. Therefore, incorporating these devices into superconducting computers could lead to certain advantages that may overcome some of the challenges currently faced by Josephson junction based circuits, as explained in later chapters in this document.

Three different superconducting logic circuit families are introduced using quantum phase-slip junctions and Josephson junctions, namely charge-based logic family, complementary quantum logic family and adiabatic quantum charge parametron logic family, with different advantages and challenges for each of the circuit families. The various circuits comprising these logic families have been demonstrated using circuit simulations in a program called WRSPICE. For this purpose, a SPICE model has been developed for quantum phase-slip junctions that can be loaded into WRSPICE.

Charge-based logic family using quantum-phase-slip junctions is inspired from single-flux quantum family based on Josephson junctions. The presence or absence of a single charge pulse (i.e. a current pulse of a constant area equal to $2e$ where e is the charge of an electron, generated by switching a quantum phase-slip junction) constitutes the logical bit 1 and 0 respectively. Several circuits in this logic family are exact dual versions of single-flux quantum family, while several additional circuits are designed that are exclusive to charge-based logic family. It is comprised of logic gates such as AND, OR, XOR, NAND, NOR etc.,

and various data manipulation circuits such as buffer circuits, fan-out circuits and merger circuits.

Complementary quantum logic family combines the charge-based logic with quantum phase-slip junctions and flux-based logic with Josephson junctions. Therefore, it consists of circuits that convert flux to charge and vice-versa. Additionally, a control circuit has been designed that has a gate input to turn the output signal ON or OFF. Logic and fan-out circuits have been demonstrated using circuit simulations that comprise of basic principles introduced in flux-charge conversion circuits and control circuit.

Adiabatic quantum charge parametron family is a variation of charge-based logic family that when operated in a certain mode of operation allows switching from logical bit 1 to 0 and vice-versa while dissipating energy less than the thermal energy at that temperature. Therefore, these circuits are compatible with reversible computing. The switching energy calculations that correspond to the circuit parameters and its operating conditions required for adiabatic switching (i.e. when switching energy is below the thermal energy K_BT) are shown. Universal logic gates such as the Majority gate has been designed and demonstrated in simulation. Several examples that use Majority gate to achieve logic operations such as AND, OR, XOR etc. are shown.

Theoretical calculations were performed based on existing physics models for quantum phase-slip junctions to extract the physical design parameters of the devices based on required circuit parameters according to simulation. Using the same calculations, materials suitable for these devices were estimated that provide highest probability of exhibiting quantum phase-slips. Additionally, the operating temperature of the circuit families introduced for several materials of interest are obtained from these calculations. The switching speeds versus power dissipation for varying device parameters are calculated and compared to existing superconducting technologies using Josephson junctions.

The work presented in this dissertation is intended to generate interest in a new field of digital logic circuits using quantum phase-slip junctions, the devices that were not previously

explored for use in classical computing systems. The new circuit families introduced exhibit several potential advantages over the existing circuits in terms of higher energy efficiency, faster switching speed as well as ease of operation that may lead to a possibility of higher integration density.

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Abbreviations

AQFP Adiabatic Quantum Flux Parametron

JJ Josephson Junction

QPSJ Quantum Phase-slip Junction

RCSJ Resistively and Capacitively Shunted Junction

RLSJ Resistive and Inductive Series Junction

RQL Reciprocal Quantum Logic

RSFQ Rapid Single Flux Quantum

SFQ Single Flux Quantum

SPICE Simulation Program with Integrated Circuit Emphasis

SQUID Superconducting Quantum Interference Device

Chapter 1

Introduction

1.1 Background and Motivation

Digital computers based on superconducting materials and devices have been of interest since the discovery of phenomenon called Josephson tunneling in 1962 by B.D Josephson [7] and their experimental realization [8]. Since then, several electronics applications were proposed using Josephson junctions (JJs) and related devices known as superconducting quantum interference devices (SQUIDs superconducting loops comprising JJs) in practical systems such as qubits [9], milli-meter wave receivers [10], the volt standard [11], magnetometers [10] and as fast switches for use in digital circuits [12] and memories [13]. Several of these applications, particularly with respect to logic applications, were realized very early after discovery of JJs as suggested by the cited references.

The digital logic circuits using Josephson junctions were viewed as an alternative to CMOS based circuits for ultra-low power computing with significantly faster switching speeds [12, 14, 13]. Therefore, In the 1970s and early 1980s, the project involving development of a prototype computer by IBM Corporation, based on a family of circuits called voltage-state logic, attracted significant attention [15]. These circuits used zero-voltage of JJs during its superconducting state as logical '0' and corresponding non-zero voltage of its normal state as logical '1' [16, 17]. This logic family could not compete with CMOS logic due to several disadvantages including poor choice of superconducting materials, and mainly, the use of under-damped Josephson junctions which latch into the voltage state, once switched

[18], although several improvements were suggested [19, 20]. The drawbacks of a voltage-state logic family were addressed using single flux quantum (SFQ) logic, which employs over-damped JJs, which was introduced in 1985 [21] and later experimentally demonstrated in 1987 [22]. Later, several improvements were suggested for circuits in this logic family [23, 24, 25].

Superconducting digital electronics is re-gaining interest for high-performance and energy efficient computation due to potential for high clock rates and low energy operation [26, 27, 28, 29] as concerns about scaling to exa-scale computing grow with traditional CMOS based electronic circuits [30, 31]. SFQ logic family and related circuits can offer up to 3 to 4 orders of magnitude of energy efficiency compared to state-of-the-art silicon CMOS technology [32, 33, 34, 35] and therefore is more efficient than other beyond-CMOS technologies as shown in Figure. 1.1 [1]. Additionally, superconducting electronics is also gaining interest in the area of quantum computing [36, 37, 38, 39] and inter-connectivity. Flexible superconducting transmission lines can transfer data with significantly low loss at high-speeds [40, 41, 42, 43, 44, 45, 46, 47].

Furthermore, JJs are known to perform arithmetic and logic operations at compellingly high clock speeds (a few hundred GHz) [48, 49] as the junctions are scaled to higher critical current densities. Circuits operating at clock frequencies above 750 GHz have been reported [50, 51]. The circuits of this technology employ superconducting loops broken with JJs that store flux quanta as its basic logic element. The state of the element can be measured as voltage pulses with quantized area [18], as the junction is switched. Therefore, these devices do not latch on to a state due to switching, and go back to their default state. However, RSFQ logic has disadvantages in having static power dissipation and in requiring large DC current biases to supply all the junctions, which, in-turn, introduce difficulties in design. These two disadvantages were overcome by other technologies that use the same quantized flux logic but with improved biasing techniques such as low voltage RSFQ [35, 52], energy-efficient RSFQ (/eSFQ) [33, 53, 34], reciprocal quantum logic (RQL) [54, 55] and adiabatic quantum

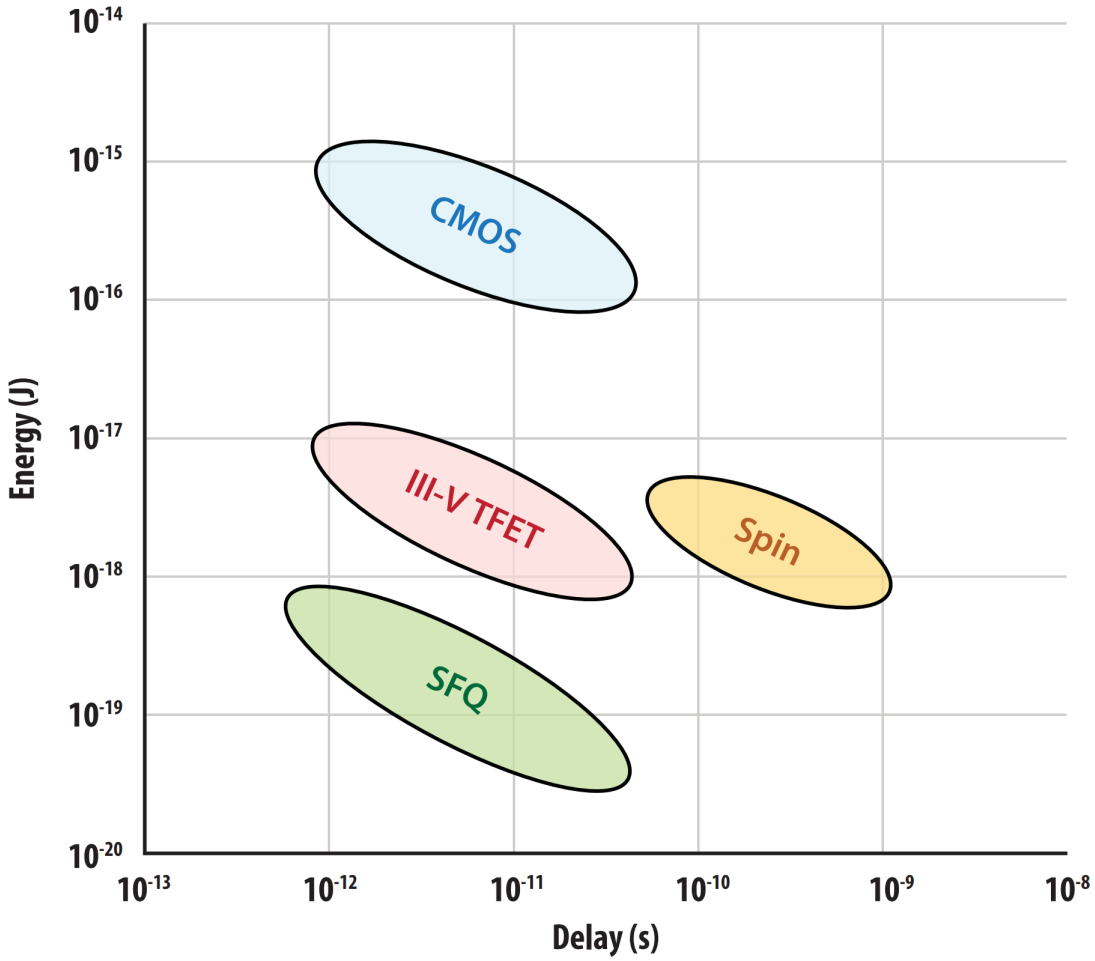


Figure 1.1: The projected gate-switching energy and delay time for several beyond-CMOS technologies (i.e., SFQ, III-V TFET, and Spin) compared with state-of-the-art silicon CMOS illustrates that SFQ switching energy is nearly an order of magnitude lower than state-of-the-art CMOS. [III-V refers to compounds with elements from both columns III and V of the periodic table.][1]

flux parametron (AQFP) [4, 56]. Although these variations of SFQ circuits overcome several challenges, there are some challenges that may inhibit scaling of these computers to peta and exa-scales [28]. Superconducting loops that can store flux quantum occupy a substantial area. It is challenging to scale existing JJs to junction sizes of a few nanometers, because as critical current of JJs get smaller, larger inductances, and therefore larger logic cells, are needed for SFQ loops. A single SFQ logic cell currently, is a loop made of two JJs and an inductor with an area of Γ20μm x 10 μm.

In this work, alternative superconducting logic circuit families that are based on superconducting devices known as quantum phase-slip junctions (QPSJs) are introduced. QPSJs are superconducting nano-wire based devices that have been identified as exact duals to Josephson junctions, based on charge-flux duality [57, 2] of Maxwell's equations. Due to this duality, the QPSJs generate quanta of charge that can be used as basic information elements, instead of quanta of flux (i.e. in circuits with only QPSJs), or in conjunction with quanta of flux (i.e. in circuits with QPSJs and JJs together). It is possible that this such circuits can inherently solve the drawbacks of RSFQ [2], along with providing several new possibilities for high-speed computing. Three new logic circuit families are introduced and demonstrated using circuit simulations in this dissertation. A brief outline of the dissertation is described in the following section.

1.2 Outline of Dissertation

In this dissertation, superconducting digital electronic circuits using QPSJs are introduced in the form of three different families of logic circuits. A SPICE model has been developed for a QPSJ to be able to demonstrate various circuits that were designed. The logic families comprise of basic switching circuits that generate quantized area (equal to charge of a Cooper pair $2e$) current pulses that define logic bits '1' and '0'. Then the basic cells are used to design various logic gates such as AND, OR, XOR, NAND etc., that together form a set of universal logic gates. Additional circuits that enable data manipulation circuits suitable for buffer, fan out etc., are also designed for each of the families. These are described in detail in various chapters in the dissertation, the outline of which is given below.

- In chapter 2, the theoretical background of the QPSJ will be described in detail. The current density calculation that outlines the definition of phase-slip is shown. Then the compact circuit model the QPSJs that was used in the SPICE model is introduced with the help of parallel comparison of the model for JJs. Additional background description

and the practical implementation examples of a QPSJ available in the literature are discussed and referenced.

- Chapter 3 describes the SPICE model that has been used for the QPSJ simulations. The details of development of the SPICE model are available in my master's thesis [58]. This chapter describes the basic model with additional features that were added to the model to be able to simulate the quantized area charge pulses necessary for logic circuits described. Some example simulations of I-V characteristics are presented that reproduce some of the measurement results available in literature. The quantized charge-pulse generation and the switching dynamics of the QPSJ are also demonstrated in simulation in this chapter.

- Chapter 4 introduces the first of the digital logic circuit families using QPSJs, namely the quantized charge-based logic family. Several circuits in this family are dual versions of single-flux quantum (SFQ) circuits, but there are several additional circuits introduced that are exclusive to QPSJ based circuits. The basic logic cell called the charge island is introduced, and several basic data manipulation circuits are presented, along with corresponding simulation results. Then the logic gates and flip-flops are included that follow the operational principles that are similar to SFQ circuits as well as additional circuit operational principles that are exclusive to QPSJ based circuits that simplify certain circuit operations. Some circuits of higher complexity that combine several of the logic and data manipulation circuits introduced, such as adders, ring oscillators etc., are demonstrated.

- In chapter 5, a digital logic circuit family known as "Complementary quantum logic family" that combines both SFQ logic and charge-based QPSJ logic family. Therefore, circuits that perform flux-to-charge conversion and vice-versa are introduced. Switching circuits and fan-out circuits are designed. Several logic gates using these circuit are presented.

- In chapter 6, a new set of logic circuits that are compatible with reversible computing are introduced. These circuits are similar to the adiabatic quantum flux parametron circuits based on JJs. A basic charge parametron circuit has been designed using QPSJs and capacitors. The potential energy of the circuit has been calculated to extract the range of parameters that allow adiabatic switching. Then the majority gate design is introduced using the parametron circuit. Several different logic gates are then obtained by programming the parametron circuit appropriately.

- In chapter 7, the theoretical calculations are presented to facilitate the physical design, material choice and measurement conditions for physical implementation of a QPSJ using a physics model presented by [5].

- Chapter 8 is the final chapter in the dissertation that summarizes various circuits introduced in the dissertation and compares them with other existing technologies such as SFQ circuits. A detailed list of advantages and challenges of this technology and the comparison of energy dissipation and switching delay with other circuit families is discussed.

Chapter 2

Theoretical Background of QPSJs

2.1 Superconductivity

The field of superconductivity has been originated with the observation of zero DC resistance in mercury (Hg) low temperatures close to absolute zero by Kamerlingh Onnes in 1911[59]. Several metallic elements, compounds and alloys were then observed to undergo phase transformations at a low temperature, which is characteristic of the material and is called the transition temperature (T_C) below which, the characteristics of superconductivity are observed. Superconductivity can be mainly described by two properties in the macroscopic scale, namely persistent currents without dissipation and Meissner effect[60, 61].

In this dissertation, the device of interest is known as a quantum phase-slip junction (QPSJ) based on superconducting nano-wires. The superconducting properties mentioned above are altered in sufficiently thin nano-wires of certain materials where superconductivity is suppressed well below transition temperature. These phenomena, namely phase-slips, are observed as resistive tails below transition[62]. The phenomenon of a quantum phase-slip, i.e. phase-slip occurring due to quantum tunneling of flux across the nano-wire, explained later, has been identified as a dual process to Josephson tunneling [7] based on flux-charge duality [57].

In this chapter, we discuss the theoretical background starting from the basics of superconductivity using Ginzburg-Landau theories[63], which will lead to the origin of the idea of a phase-slip. Various experiments that lead to the understanding of quantum phase-slip

phenomenon are then briefly discussed. The idea of flux-charge duality explaining relationship between a Josephson tunneling and a quantum phase-slip will then be presented in some detail. The resistively and capacitively shunted junction (RCSJ) model of a Josephson junction (JJ) [10] will be discussed in detail in parallel with the QPSJ to facilitate the explanation of its complementary model. A basic introduction to some circuit applications of JJs will be examined which in later chapters is further explored in the context of QPSJs.

The change in behavior in terms of resistance to electrical current dropping to zero in some materials at low temperatures close to zero is interpreted as a phase-transition as explained by Ginzburg-Landau (GL) theories[63] in the macroscopic sense. This theory is valid for explanation of several phenomena in superconductors, including Josephson tunneling and phase-slips, sufficient for understanding the circuit models used in this dissertation. Therefore, in this chapter, the phase-slips are described using GL theory and the microscopic theory of superconductors (i.e. BCS theory[61]) is not considered.

2.2 Macroscopic Wave Function Description of Superconductors

According to the Ginzburg-Landau theory of superconductivity [64], a phase transition takes place in superconducting materials below transition temperature T_C, where it is energetically favorable for electrons to form a condensate, which is highly ordered compared to a normal metal phase. In this phase, the superconducting state is defined by a complex order parameter given by:

$$\Psi(r) = \sqrt{n(r)}e^{i\phi(r)} = \psi(r)e^{i\phi(r)} \tag{2.1}$$

Here, $|\psi(r)|^2 = n(r)$ is the density of the electrons condensed in the superconducting state and ϕ is the position dependent phase factor of the state.

This implies that all the condensed electrons occupy a single quantum state with their phases overlapped making it continuous while in this condensate. It is noteworthy that the

phase factor enters the macroscopic wave function. This factor of phase can only have values modulo 2π and is usually wiped out when averaged over billions of electrons in distinct quantum states in a normal metal phase. But, in a superconductor, this becomes an element which gives rise to detectable macroscopic quantum phenomena. We will see later that this property of superconductors is significant in explaining the behavior of JJs and QPSJs.

2.2.1 Phase-slip in Superconductors

In this section, we discuss the origin of a phase-slip in superconductors. By using the above description of a macroscopic wave function, we can calculate the current density of the dissipation-less currents induced in a superconductor by assuming an induced supercurrent due to an applied magnetic potential (external magnetic field) with the help of time dependent Schrodinger equation. This simple calculation will facilitate the explanation of the origin of a phase-slip due to Josephson tunneling or a quantum fluctuations, which are responsible for quantum phase-slips that will be discussed in detail in later sections. Details of calculations (can be found in [65]) are not shown here, and only a simple description of the flow of calculation is given below.

Let us consider motion of a particle in the presence of a magnetic potential. In our example, the particle is moving in a superconductor. Therefore, the momentum of particles in the superconducting state described by equation 2.1 in case of magnetic potential is given by:

$$\bar{p} = -i\hbar\nabla - eA(r) \tag{2.2}$$

Here, $\bar{p}$ is the momentum operator of the particle, $\hbar$ is the reduced Planck's constant, ∇ is the divergence operator and A is the magnetic vector potential.

The behavior in the presence of magnetic potential is considered only for illustrating supercurrent flow in an example that follows. In practice, a supercurrent can be setup using either an electric or a magnetic field.

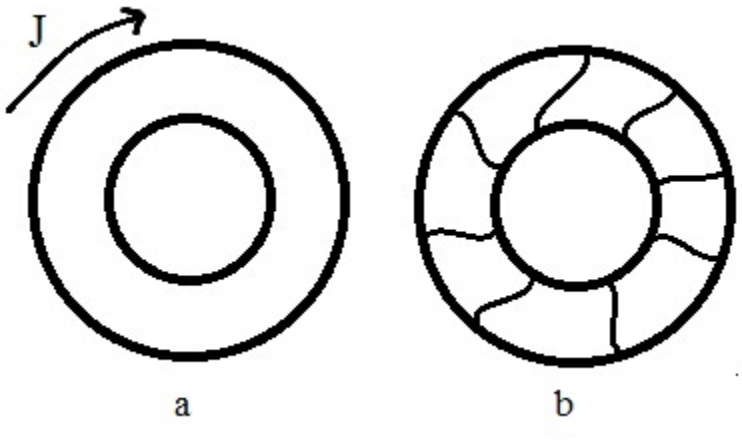


Figure 2.1: a. Persistent current in a superconducting ring. b. Phase of macroscopic wave function around the ring.

Now, let us imagine that we setup a supercurrent in a closed ring shown in the Figure 2.1 using an external magnetic field and then turning it down. We see that a persistent current is setup in the ring, which will take infinite time to decay. Using both equations 2.1 and 2.2, the supercurrent can be calculated as shown in equation 2.3:

$$j(r) = \frac{e}{2m}\psi(r)|\bar{p}|\psi(r) \tag{2.3}$$

$j(r)$ is the current density as a function of position and m is the mass of the electron.

Substituting equation 2.2 in equation 2.3 gives equation 2.4:

$$j(r) = \frac{e}{2m}\left|\psi(r)\right|^2\left|\nabla\phi(r) - eA(r)\right| \tag{2.4}$$

In the presence of a magnetic field, $\phi(r)$ is constant and therefore $\nabla\phi(r)$ is zero. Current is only a function of magnetic field in the loop shown in Figure 2.1a. But when the magnetic field is turned off, supercurrent persists in the loop without dissipation unless significant changes to the environment are made. In this situation, the supercurrent is a function of $\nabla\phi(r)$, which now cannot be zero and must have a constant value. $\phi(r)$ has values modulo

2π which means $2\pi \pm k$ is equivalent to k. Therefore, in this case of a loop, we can write:

$$\int \nabla\phi(r)dl = 2\pi n \tag{2.5}$$

where n is the winding number.

This is the constant value that is directly proportional to the supercurrent in the loop. The number n is called the winding number of the loop and is illustrated in the Figure 2.1b as the number of times the phase of the wave function goes over 2π. This example has been of a superconducting loop but this equation is valid for any continuous superconductor.

Now, the persistent supercurrent without decay is the result of constant winding number as shown in equations 2.4 and 2.5. When the superconducting order parameter is zero at a point in the loop, winding number changes to $n \pm 1$ and this is called as a phase-slip.

Phase-slips are therefore identified as events in the superconductor where the order parameter goes to zero and the winding number changes. This also causes a voltage to develop across the phase-slip region. These events causing suppression of superconductivity in this way are observed in different situations. Some examples include: phase diffusion through thermal fluctuations in JJs, when their Josephson energy is in the regime $E_J \gg e^2/2C_J$ shown in [66]; macroscopic quantum tunneling in JJs whose capacitive energy is much larger than Josephson energy[67], $E_J \ll e^2/2C_J$; thermally activated phase-slips in superconducting nano-wires whose theory is described in [68, 69, 70] and observed in experiments just below critical temperatures in superconducting nano-wires [71, 72]; along with quantum phase-slips due to quantum tunneling of superconducting order parameter between the states whose phases differ by 2π, experimentally observed in [62, 3, 73, 74, 75, 76, **?**, 77, 78]. In this dissertation, we are mainly interested in quantum phase-slips and the SPICE model that primarily describes the electronic device based on this phenomenon. The theory describing the physics of this phenomenon leading to the formulation of a compact model of the

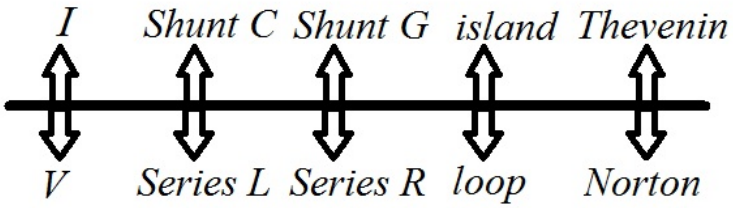


Figure 2.2: Flux-charge duality in electrical circuits (adapted from [2]).

aforementioned QPSJ device is described in the subsequent sections. Thermally activated phase-slips based on LAMH[68, 69, 70] are also briefly explained as they are relevant in a part of the model.

2.3 Flux-charge Duality and Quantum Phase-slips

Quantum phase-slip phenomenon can be described as a dual phenomenon to Josephson tunneling based on flux-charge duality of Maxwell equations, originally described by Mooij and co-workers [57]. Later on, this has been extended to define the QPSJ as a dual device to Josephson junction. In the following sub-section, the idea of flux-charge duality in Maxwell's equations, in the context of superconductors will be discussed.

2.3.1 Flux-charge duality

Classical flux-charge duality based on Maxwell's equations can be observed in lumped element circuits as shown in Figure 2.2. In continuous case, superconductors and insulators can be shown to be the exact duals of each other, based on charge-flux duality [79, 80, 81, 82, 83, 84]. The quantities charge and flux current densities can be interpreted as sum of bound and free quantities based on Maxwell equations as shown below [2]:

$$J_Q = \rho_Q v_Q + \frac{dD}{dt} \tag{2.6}$$

$$J_\phi = v_\phi \times B_f - \frac{dA}{dt} \tag{2.7}$$

where, J_Q is the current density corresponding to charge, ρ_Q is the charge density moving at velocity v_Q, D is the electric displacement, J_ϕ is the current density corresponding to flux, B_f is the magnetic flux density moving at velocity v_ϕ and A is the vector potential and can be defined in case of superconductors using equation 2.8:

$$A = \wedge \rho_Q v_Q \tag{2.8}$$

where,

$$\wedge = \mu_0 \lambda^2 \tag{2.9}$$

Here, μ_0 is the magnetic permeability and λ is the magnetic penetration depth in superconductors.

Using the equations 2.8 and 2.9 along with $D = \epsilon E$, we can define charge and flux transport in case of superconductors using equations 2.10 and 2.11 respectively [2].

$$\wedge \frac{dJ}{dt} = E \rightarrow L_k \frac{d^2Q}{dt^2} = V \tag{2.10}$$

$$\epsilon \frac{dE}{dt} = J \rightarrow C \frac{d^2\Phi}{dt^2} = I \tag{2.11}$$

Here, L_k is called the kinetic inductance and C is the kinetic capacitance.

These quantities will be encountered in the context of JJs and QPSJs. These equations take the duality between charge and flux to illustrate the dual relation in charge/flux transport in superconductors/insulators.

2.3.2 Josephson Junctions and Quantum Phase-slip Junctions

A QPSJ, which is an exact dual to a Josephson junction can now be introduced and defined based on the theoretical description so far. Consider the Figure 2.3. A JJ, shown in

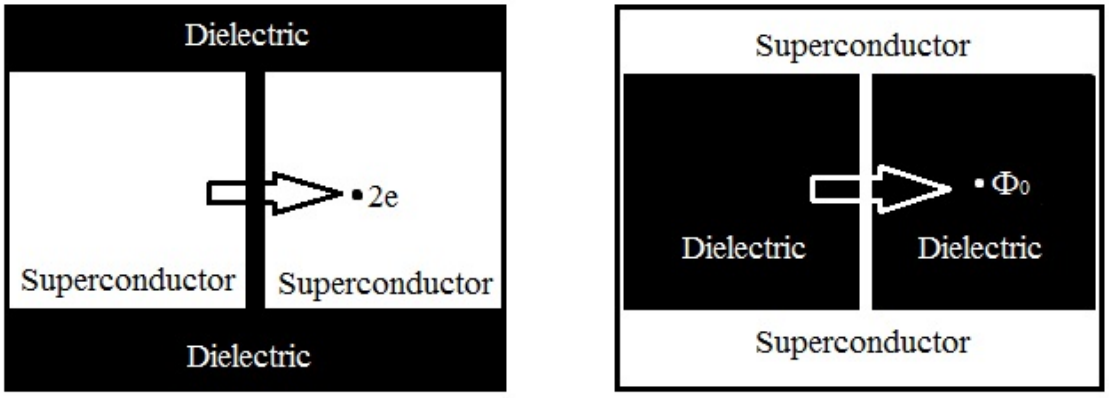


Figure 2.3: Duality between Josephson tunneling in JJs and Fluxon tunneling in QPSJs (adapted from [3]).

the left, consists of two superconducting islands of cooper pairs separated by an insulating potential barrier, while a QPSJ, shown in right, can be viewed as two insulating *islands* of flux-quanta (referred to as $fluxons$ [2]) separated by a superconducting potential barrier. Therefore, the suppression of superconductivity, discussed earlier, associated with a quantum phase-slip is due to tunneling of fluxons across a superconducting nano-wire. The idea of charge-flux duality is not just a classical concept, but the variables-charge and flux, also obey commutation relations when treated as quantum operators.

The behavior of Josephson junction depends mainly on the phase difference between the two superconducting electrodes which are separated by an insulating potential barrier. The tunneling of charges between them is a coherent process, and the current through the junctions is a function of phase difference between these electrodes. Similarly, the tunneling of a fluxon across the superconducting potential barrier sets up voltage between the ends of nano-wire which is a function of charge travelling through the wire. This tunneling of fluxons is also a coherent process. But dissipation occurs in both JJs and QPSJs causing this an incoherent process which will be discussed in detail in later sections.

2.4 Quantum Phase-slip Junctions

QPSJs are therefore formed from superconducting nano-wires, linking two superconducting electrodes in dielectric region. They show suppression of superconductivity, resulting in dissipation and voltage drop across the nano-wire associated with a phase difference of 2π between the ends of the nano-wire, below the transition temperature. In experiments, these are observed as resistive tails below superconducting transition [85, 86, 75, **?**, 87] similar to thermally activated LAMH phase-slips [68, 69, 70, 71, 72]. Josephson tunneling, however is a coherent process without dissipation. Therefore, the Quantum phase-slip which is described by a dual process is also coherent, and has been identified [3, 88] with experimental setups similar to the approach described in section 1.1.2. Using its quantum nature, a quantum phase-slip based qubit has also been proposed [89] which is dual to the charge qubit using Josephson junctions [90]. Nevertheless, we are interested in using QPSJ device in SPICE for use with classical circuits similar to JJs and therefore, will consider the incoherent process where dissipation can be measured. This involves usage of the model for QPSJ similar to RCSJ based device model for a JJ[91]. This model includes parameters to account for dissipation, along with the inductance of the nano-wire, similar to the capacitance in JJ along with the voltage term depicting the coherent quantum phase-slip. A short description of the RCSJ model of a Josephson junction will be explained to facilitate the derivation of QPSJ device model.

2.4.1 Josephson Junction and RCSJ Model

In this section, we explain and briefly derive the equations governing supercurrent, voltage and phase in DC Josephson effect. Later on, the canonical transformation based on commutation relation between q and ϕ will be used to obtain a model for the QPSJ from the JJ equations [91]. As explained earlier, equation 2.1 defines the charge carriers in superconducting state and can be used to describe either side of the superconducting regions of insulating barrier in a JJ (see Figure 2.3). Let us consider the case where voltage V

is applied between the two superconductors. Then the energy and wave function of both superconductor regions are eV, ψ_1 and $-eV$, ψ_2 respectively. We can write time-dependent Schrodinger equation on either side of the superconductor as given by equations 2.12 and 2.13 below:

$$i\hbar\frac{d\psi_1}{dt} = eV\psi_1 + k\psi_2 \tag{2.12}$$

$$i\hbar\frac{d\psi_2}{dt} = -eV\psi_2 + k\psi_1 \tag{2.13}$$

where ϕ is the phase difference across the junction.

Substituting equation 2.1 in the above equations and separating it into real and imaginary parts gives the result:

$$\frac{d\phi}{dt} = \frac{2e}{\hbar}V \tag{2.14}$$

for the imaginary part, and

$$I = I_C sin\phi \tag{2.15}$$

for the difference of real parts. I_C is the critical current of a JJ. It is the maximum supercurrent that can be carried across the junction.

Equations 2.14 and 2.15 define DC Josephson effect at the device level.

The JJ used in circuits does not behave completely like the equation 2.15 describes. It has dissipation and therefore deviation from completely coherent behavior as described by equations 2.14 and 2.15. The description which includes this behavior of a JJ is called RCSJ model. Resistively and capacitively shunted junction (RCSJ) model of a JJ takes into consideration, the junction's intrinsic resistance and capacitance. The current biased

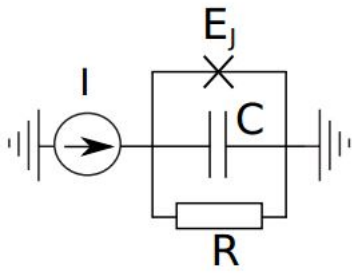


Figure 2.4: Current biased resistively and capacitively shunted Josephson junction (RCSJ model).

junction shown in Figure 2.4 represents an equivalent circuit model. When the current applied is above the critical current of the junction, the additional current passes through the elements R and C of the junction. Total current is hence given by:

$$I = I_J + I_R + I_{Cap} \tag{2.16}$$

which gives:

$$I = I_C sin\phi + \frac{V}{R} + C\frac{dV}{dt} \tag{2.17}$$

2.4.2 Charge Transport in a Quantum Phase-slip

A very useful explanation of charge transport in JJs can be derived from RCSJ model. By replacing V in equation 2.17 with its substitute from equation 2.14, we can get a description of JJ in terms of a second order equation in phase. An energy versus phase plot with this description of the model is called as washboard potential shown in the Figure 2.5. The slope in the plot is due to the applied bias current. In a JJ, the charge carrier oscillates in a potential well, giving rise to sinusoidal current description given by equation 2.15. But with enough bias current, the height of the potential well is decreased and the charge carrier rolls off to lower potential wells, losing energy due to dissipation. Under low bias current, the charge carrier can still travel into next potential well through a process called phase diffusion [66], where thermal activation is responsible for the particles to cross the energy barrier.

In highly capacitive Josephson junctions, another possible way exists for charge carriers to transport via tunneling through the potential barrier between potential wells which are stimulated by zero-point fluctuations. These fluctuations are caused due to the energy oscillations between kinetic inductance (see equation 2.10) and junction capacitance. This phenomenon is called as macroscopic quantum tunneling [67].

In superconducting nano-wires, the thermally activated phase-slips can be described by a similar process to that of phase diffusion but at a different energy scale proposed by LAMH [68, 69, 70]. These phase-slips are observed as resistive tails below superconducting transitions in nano-wires, where the value of resistance is given as a function of potential barrier (Figure 2.5), which is further defined as proportional to the energy needed to destroy superconductivity, as shown in the following equations.

$$R(T) \propto e^{-U/T} \tag{2.18}$$

$$U \approx \frac{\nu {\Delta_0}^2(T)}{2} S\xi(T) \tag{2.19}$$

where, Δ_0 is the superconducting energy gap , ν represents density of states and ξ is the cross-section of the wire and coherence length at a given temperature T.

Quantum phase-slips follow a similar process as that of macroscopic quantum tunneling but at a different energy scale derived in detail in [2]. The zero-point fluctuations arise as a result of oscillations between inductance of the nano-wire and kinetic capacitance (see equation 2.11). The dissipation in a quantum phase-slip process which allows the charge carrier to settle in lower-energy potential well arises due to the dielectric constant of the conducting material, which acts as an effective mass for the fluxon tunneling across the nano-wire. Therefore, the resistance term that will be shown in resistive and inductive series junction (RLSJ) model of a QPSJ in next section corresponds to the loss due to dielectric for

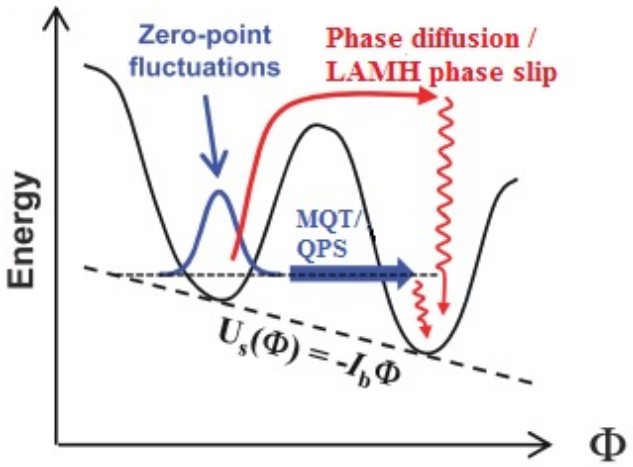


Figure 2.5: Washboard potential description of Phase diffusion/LAMH phase-slip (shown in red) and Macroscopic quantum tunneling/Quantum phase slip (shown in blue) [2].

the electric field (or voltage drop) along the nano-wire due to the fluxon tunneling across the wire. This microscopic description manifests as lumped element model in the next section derived from the dual model to JJ which will be ready to implement in a SPICE model.

2.4.3 Resistive and Inductive Series Junction Model of a Quantum Phase-slip Junction

As we have already seen, phase-slips are observed when superconductivity is suppressed and a quantum phase-slip phenomenon can be explained as a dual to Josephson tunneling. Mooij and Nazarov are the first to realize that a quantum phase-slip process can be described by the charge-flux duality using quantum conjugates q and ϕ [57]. Charge and phase quantum operators satisfy the commutation relation:

$$[\hat{q}, \hat{\phi}] = -i \tag{2.20}$$

where q is the electric charge and ϕ is the magnetic flux.

They also proposed a phase-slip energy dual to the Josephson energy which was later derived by [2]. In description given by Mooij et. al. [57], they performed canonical transformation, which satisfies the commutation relations between the resulting expressions, to the Josephson Hamiltonian to arrive at a qualitative description of a coherent quantum phase-slip. The details are not discussed here, but the canonical transformations performed are given below.

$$(\hat{q}, \hat{\phi}) \rightarrow (-\hat{\phi}/2\pi, 2\pi\hat{q}) \tag{2.21}$$

$$E_s \rightarrow E_J; E_L \rightarrow E_C; I \leftrightarrow {R_q}^{-1}V; Y(\omega) \leftrightarrow {R_q}^{-1}Z(\omega) \tag{2.22}$$

where E_s is the phase-slip energy, E_J is the Josephson potential energy, E_L and E_C are the inductive and capacitive energies of a QPSJ and a JJ respectively.

Using the above equations, we can perform canonical transformation of equation 2.15 to obtain

$$V = V_C sin(2\pi q) \tag{2.23}$$

with V_C being the critical voltage of the junction and V, the measurable voltage drop across the junction.

The compact model describing the dissipation and inductance of the wire [57, 73] is shown in the Figure 1.6. Notice that this is a series circuit as opposed to parallel circuit as that of a JJ, which is a result of canonical transformation.

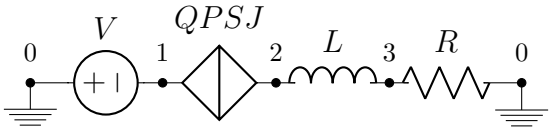


Figure 2.6: Voltage biased QPSJ in RLSJ model

The capacitance and resistance terms from the equation 2.17 transform into the following equations.

$$\frac{V}{R} \rightarrow IR, C\frac{dV}{dt} \rightarrow L\frac{dI}{dt} \tag{2.24}$$

The I-V description of a lumped element model of a QPSJ defined by RLSJ model is therefore given by:

$$V = V_C sin(2\pi q) + L\frac{dI}{dt} + RI \tag{2.25}$$

Equation 2.25 has been used to develop a SPICE model for a QPSJ with additional modifications to incorporate transition between normal and superconducting states through generating constant-area current pulses corresponding to quantized charge of $2e$ etc., explained in detail in the next chapter.

2.4.4 Notes

The physics of quantum phase-slips is still an evolving subject and has several unanswered questions related to the microscopic operation of the device. Particularly, there are multiple but similar theories that explain the origin of phase-slip energy such as in [57, 2] etc. An established theory strongly connected to the material and design aspects of the QPSJs will enable exploration of these devices for further electronic applications.

Chapter 3

SPICE Model of a QPSJ

3.1 Quantum Phase-slip Junction

3.1.1 SPICE Model of a Quantum Phase-slip Junction

Quantum phase-slip junctions are superconducting phenomenon where the phase difference across a nano-wire changes by 2π with the suppression of superconducting order parameter to zero. This has been observed as a resistance tail below superconducting transition in experiments [86, 62, 77]. This phenomenon has been identified as a dual process to Josephson tunneling. While a charge tunnels between two superconducting regions across an insulating barrier in a Josephson junction, inducing a flux quantum in the corresponding loop, a QPSJ can be viewed as flux tunneling across a superconducting nano-wire (barrier for flux) creating a voltage drop at the ends of the wire [2]. Therefore an I-V relationship of a QPSJ can be obtained by replacing phase by charge, current term by voltage term and capacitance term by inductance term [57]. The two equations that were used to describe a QPSJ in the compact model for SPICE are therefore given by:

$$V = V_C sin(q) + L\frac{dI}{dt} + RI \tag{3.1}$$

where,

$$I = \frac{2e}{2\pi}\frac{dq}{dt} \tag{3.2}$$

Here, V is the voltage across the junction, V_C is the critical voltage of the junction, L is the geometric inductance of the junction, I is the current through the junction, R is the

normal resistance of the junction and q is the charge equivalent in the QPSJ normalized to the charge of a Cooper pair ($2e$) and the term $\frac{1}{2\pi}$ to represent q as a phase corresponding to charge. Therefore, q's relation to charge $2e$ is equivalent to relation of superconducting phase ϕ and flux quantum Φ_0, with e being charge of an electron. In practical implementation, the various parameters of the junction can be varied by varying the physical dimensions and material of the junction.

The mathematical description above can be described in a circuit model as shown in Figure 3.1. The first term in equation (1), which represents voltage across a quantum phase-slip event, can be re-written to describe the device as a capacitor with kinetic capacitance C_k, given by:

$$C_k = \frac{2e}{2\pi V_C cos(q)} \tag{3.3}$$

Hence, the circuit in Figure 3.1 can be treated as a series RLC circuit. We describe an over-damped QPSJ for the charge-based logic family analogous to the JJ in RSFQ logic, which will be discussed later. From the circuit and the description given by equations (1) and (2), we can obtain a damping parameter for a QPSJ, which is given by:

$$\beta_L = \frac{2\pi V_C L}{2eR^2} \tag{3.4}$$

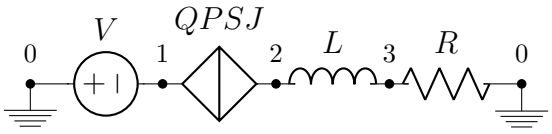


Figure 3.1: Compact circuit model for QPSJ used in SPICE model development.

$\beta_L << 1$ indicates an over-damped junction and $\beta_L >> 1$ represents an under-damped junction. With $\beta_L \sim 1$, the junction is critically damped.

The mathematical definition given for a QPSJ above, along with the circuit description, has been used to develop a SPICE model for a QPSJ in WRSPICE [92]. In addition to the

equations above, the time step in solving these equations using numerical methods must be limited to be smaller than the time scale corresponding to plasma frequency of the junction. The time step limit Δt applied to the simulations is given by:

$$\Delta t = \frac{0.1}{(\frac{2\pi}{2e}\frac{V_C}{L})^{1/2}} \tag{3.5}$$

The details required for simulating a QPSJ have been setup, enabling simulations of more complex circuits, which are described in the following section.

3.1.2 SPICE Model Implementation in WRSPICE

The compact model described above is used to develop a SPICE model compatible with WRSPICE and JSPICE, two programs that are capable of simulating superconducting circuits involving Josephson junctions along with other devices. A verilog model has been developed first using the equation and constraints described in the previous section. However, the ADMS compiler of WRSPICE could not compile the verilog model for QPSJs. Therefore, the compiler was only used to generate the C++ source files that were then edited to describe the model accurately according to the compact model equations. The modified nodal analysis (MNA) stamp of the device is given by the Equation 3.6 and 3.7 below. The time-step limit equation is added separately to the model and is not part of the MNA stamp. The details of the development of the SPICE model are described in my master's thesis [58] and the paper [92].

$$[I] = [Y]\,[V] + [RHS] \tag{3.6}$$

$$\begin{bmatrix} I_3 \\ I_0 \\ V \end{bmatrix} = \begin{bmatrix} g & -g & 1 \\ -g & g & -1 \\ 1 & -1 & \frac{-2L}{\Delta} + V_C \left(\frac{2\pi}{2e}\right) \left(\frac{\Delta}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) \end{bmatrix} \begin{bmatrix} V_3 \\ V_0 \\ I \end{bmatrix}$$
$$+ \begin{bmatrix} -G\left(I\right) + gI \\ G\left(I\right) - gI \\ -L\left(I' + \frac{-2I_L}{\Delta}\right) + V_C \left[\left(\frac{2\pi}{2e}\right) \left(\frac{\Delta L}{2}\right) cos\left(\frac{2\pi q_L}{2e}\right) + sin\left(\frac{2\pi q_L}{2e}\right)\right] \end{bmatrix} \tag{3.7}$$

3.2 Example simulations of QPSJ in WRSPICE

3.2.1 Current Pulses With Quantized Area

The single quantized charge-based logic uses short, pico-second, current pulses as the basic logic signals. These current pulses have quantized area under the curve, which represent the total charge traveled along the nano-wire. Therefore, the presence and absence of the current pulse can form the two logic states, similar to the voltage pulse in RSFQ logic [21].

The explanation for quantized area under the current pulse curve is given by rewriting equation 3.8 below:

$$\int I dt = \int_0^{2\pi} \frac{2e}{2\pi} dq = 2e = 3.204... \times 10^{-19}\ \text{C} \tag{3.8}$$

From equation 3.8, the charge of $2e$ corresponds to the immediate excited energy state of a fluxon tunneling across the nano-wire which is QPSJ [2]. If the junction is over-damped (or critically damped), the total charge through the junction with a bias voltage slightly over V_C is restricted to charge $2e$ through it, with further oscillations damped, without further excitations. The treatment of charge variable q of a QPSJ is analogous to the treatment of Josephson junction phase ϕ.

$$\frac{2e}{2\pi} \longleftrightarrow \frac{\Phi_0}{2\pi} \text{ or } q \longleftrightarrow \phi$$

To illustrate this idea, in Figure 3.2 we show numerical simulation results of a single current pulse with area of $2e$ under the curve. Simulation of an RSFQ pulse is also presented for comparison. Both the junctions are also simulated in under-damped (without a damping resistor) and over-damped (with a damping resistor) configurations. The circuit setup for both under-damped and over-damped QPSJs consist of a voltage bias of $0.7V_C$ and a pulse voltage input in series with a QPSJ. Addition of a series resistor makes it over-damped. A similar setup has been used for JJ, where a current bias of $0.7I_C$ and a current pulse driving it. Addition of a parallel resistor makes the junction over-damped. Simulation results for all the cases (over-damped and under-damped JJ and QPS) are shown in Figure 3.2.

The plot shows quantized area current pulse of a QPSJ very similar to the quantized area voltage pulse of a JJ, when both the junctions are over-damped. In under-damped state, both the junctions switch when the input current or voltage goes above the critical current or critical voltage values and are then latched in that state. This is characteristic of the hysteresis behavior of both the junctions, where, once switched to a resistive state above their respective critical voltages or currents, the junctions do not revert back to their superconducting states until the bias across them is completely zero. In the under-damped switching behavior of a QPSJ in Figure 3.2, the current across the junction is non-zero even after its switching state due to the presence of voltage bias and a quasi-particle resistance across the device.

With over-damped QPSJs, a quantized charge of $2e$ flows through the junction, similar to the flux developed across a JJ. Therefore, as in RSFQ, where a loop made of JJs and an inductor stores one quantum of flux Φ_0, an island formed by two QPSJs and a capacitor can store quantum of charge $2e$. An ideal QPSJ is similar to a tunnel barrier, and therefore the node formed between two QPSJ devices is similar to an island [93, 74].

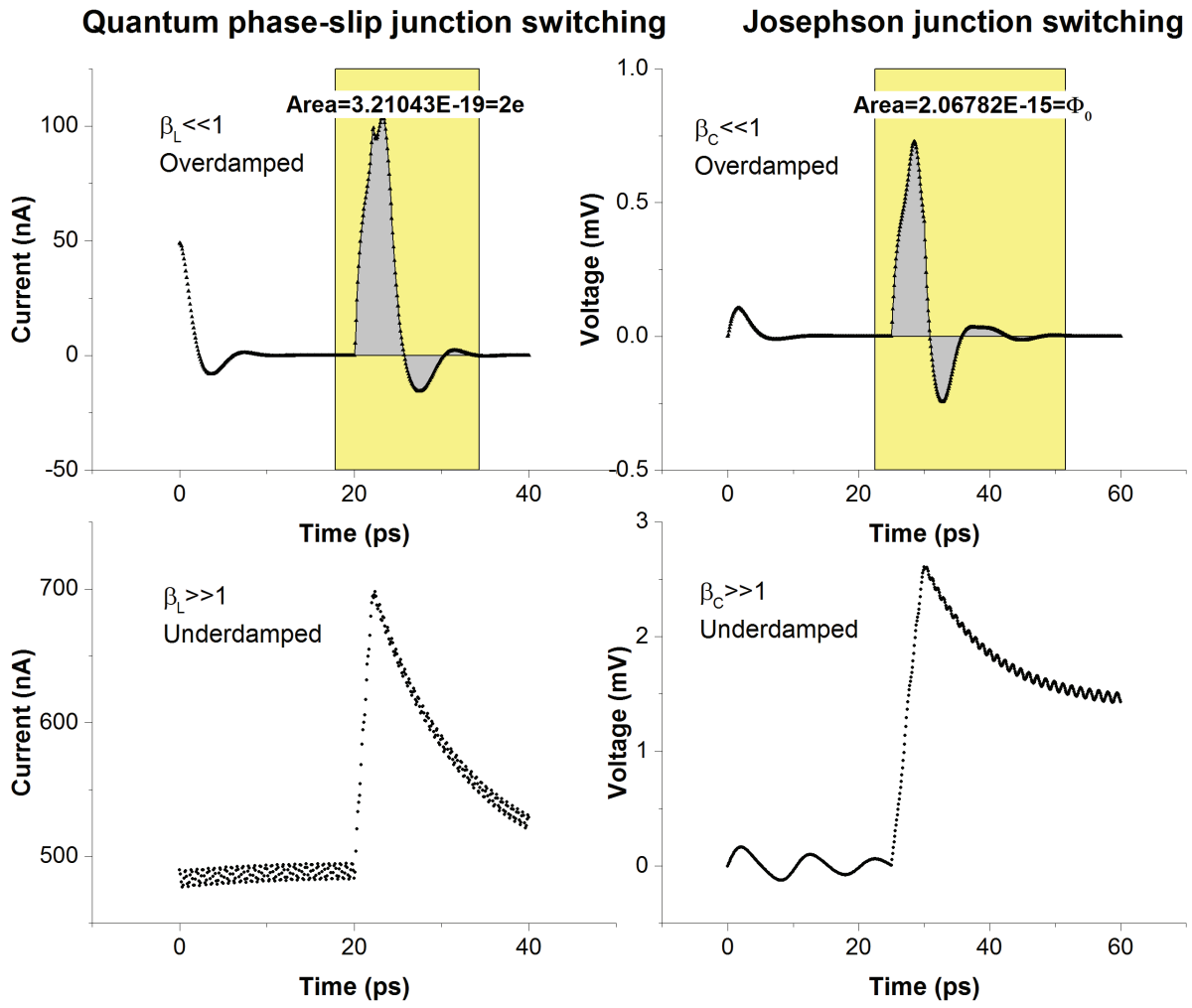


Figure 3.2: Comparison of Switching Dynamics of Quantum Phase-slip Junction and Josephson Junction.

3.3 SPICE Simulation of QPSJ I-V Characteristics

In this section, the SPICE simulations of I-V characteristics of a device are presented for an example quantum phase-slip junction. The operation of a QPSJ can be illustrated using the equivalent circuit model shown in Figure 3.1. This circuit model can be characterized by Equations 3.1 and 3.2, and was realized in a SPICE model in WRSPICE [92]. The coefficients of Equation 3.1 are device parameters that depend on material and dimensions

of the junction where V_C is critical voltage, L is geometrical inductance and R is normal resistance. Nominal simulated I-V characteristics of a QPSJ are shown in Figure 3.2. Note that a linear resistance function with a resistance value equal to the normal resistance of the junction is used here, as opposed to a non-linear, two-part resistance function described in [92]. This is not expected to have a significant impact on the quantized-charge logic operation of the devices.

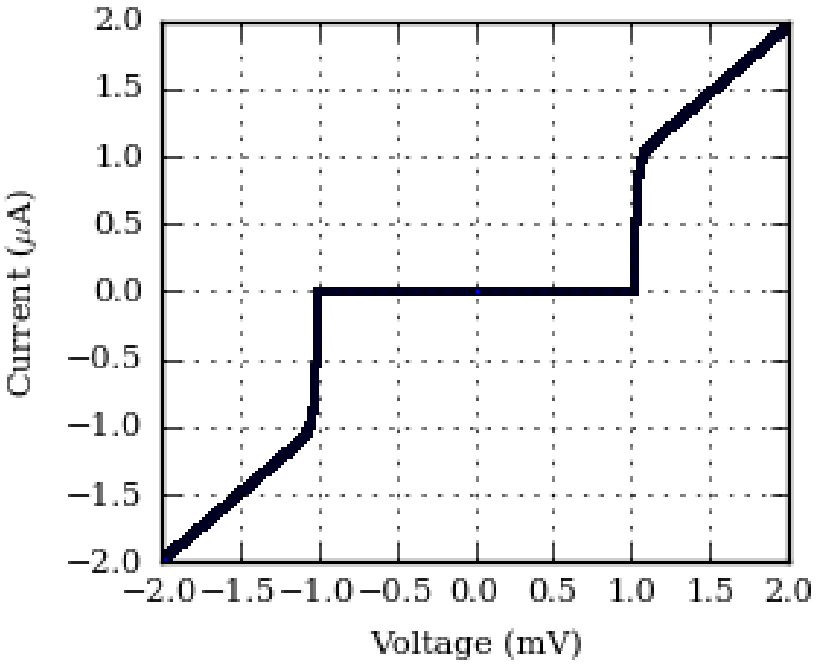


Figure 3.3: I-V characteristics of a quantum phase-slip junction with $V_C = 1mV$, $L = 20nH$ and $R = 1k\Omega$.

3.4 Device Parameter Evaluation

The junction parameters used to obtain the characteristics shown in Figure 3.2 are somewhat arbitrary and, therefore, they may or may not be applicable for a practical junction. These parameters depend on the material properties and physical dimensions of the device and have constraints depending on parameter values that can produce quantum-phase slips.

These constraints are detailed in [5, 2] in the form of models associating various material and design parameters to characteristic energies corresponding to quantum phase-slip processes.

The critical voltage V_C is related to phase-slip energy by:

$$V_C = \frac{2\pi E_s}{2e} \tag{3.9}$$

where E_s is the phase-slip energy, which can be calculated using the model by Mooij et al. [5]. The normal resistance R is calculated from normal-state resistivity of the given material and physical dimensions of the nano-wire that forms the QPSJ. The inductance L of the junction is related to inductive energy E_L, which is a function of normal resistance R and critical temperature of the material [5]. As explained in [5], the parameters satisfying the condition $0.1 \leq \alpha \leq 1$, where $\alpha = \frac{E_s}{E_L}$, are expected to be suitable for quantum phase-slip junctions.

Two different materials, among others hypothesized as suitable for QPSJs [3, 88, 73, 5], $InOx$ and NbN, are considered for parameter evaluation in this section. Values of a subset of design parameters satisfying the $0.1 \leq \alpha \leq 1$ condition for both materials are represented in Figure 3.4 and Figure 3.5. The details of these calculations are explained in Chapter 7. Note that there is a range of combinations of design parameters satisfying the conditions for each material.

By considering an $InOx$ junction of length = 3μm, width = 70 nm and thickness = 20 nm, from the shaded region of Figure 3.4, we obtain the device parameters of critical voltage $V_C = 14.7mV$, normal resistance $R = 300k\Omega$ and inductance $L = 2.8nH$. Similarly, when we consider an NbN junction of length = 3μm, width = 10 nm and thickness = 5 nm, we obtain the device parameters of critical voltage $V_C = 2.94mV$, normal resistance $R = 37.2k\Omega$ and inductance $L = 14.2nH$. These parameters are directly used with the QPSJ SPICE model in WRSPICE to obtain I-V characteristics of both the junctions. Figure 3.4 shows the characteristics of an $InOx$ junction while Figure 3.5 shows the characteristics of an NbN

junction. The curves are obtained by sweeping voltage across the junctions and measuring currents in WRSPICE. The Coulomb blockade characteristic of QPSJs [73, 5] are clearly seen. Since the SPICE model is valid only for transient analysis [92], the curves demonstrate oscillatory characteristics in some regions.

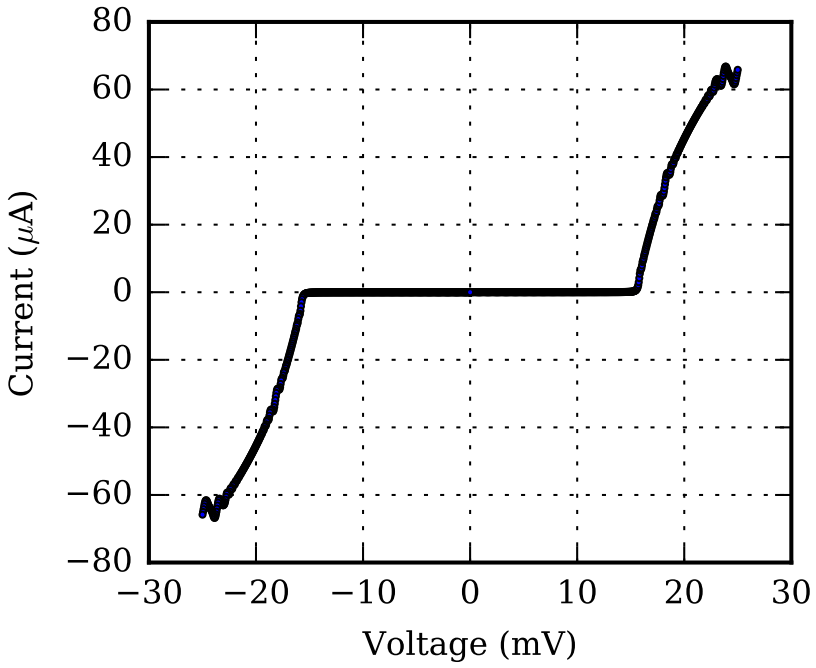


Figure 3.4: I-V characteristics of $InOx$ based QPSJ simulated in WRSPICE. $V_C = 14.7mV$, $R = 300k\Omega$, $L = 2.8nH$.

Based on the device model described in Figure 3.1 and Equations 3.1 and 3.2, the QPSJ is equivalent to a series RLC oscillator. This oscillator must be over-damped in order to produce quantized-area switching characteristics similar to a Josephson junction in SFQ logic [18]. Switching characteristics with quantized-area current pulse are demonstrated by exciting a QPSJ circuit, biased below its critical voltage, using a short voltage pulse that drives the junction above its critical voltage.

Plots demonstrating current pulses with quantized area equal to $2e$, for both $InOx$ and NbN junctions with parameters taken from Figures 3.4 and 3.5, respectively, are shown in

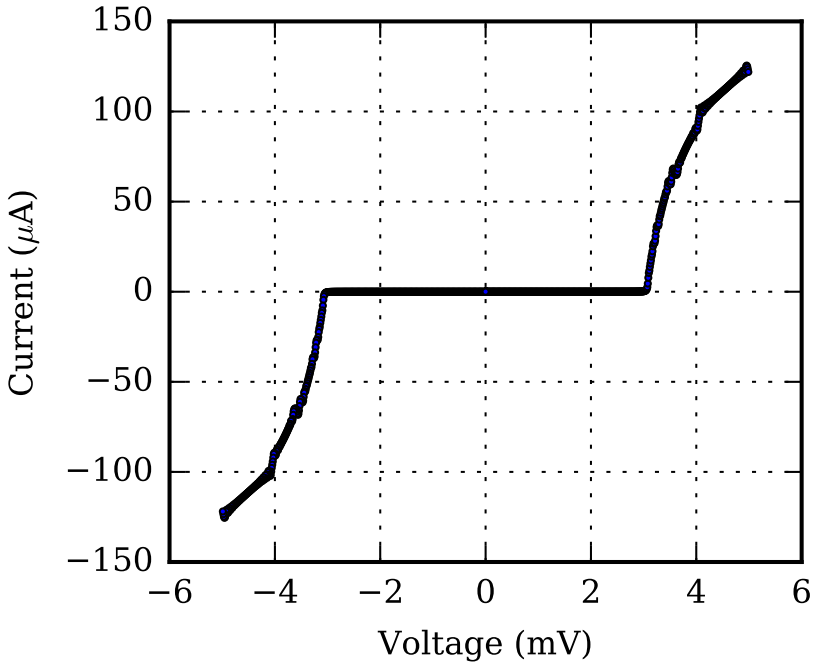


Figure 3.5: I-V characteristics of NbN based QPSJ simulated in WRSPICE. $V_C = 2.94mV$, $R = 37.2k\Omega$, $L = 14.2nH$.

Figure 3.9. These junctions are inherently over-damped and do not require additional damping resistors in series.The integrated area under these curves is equal to $2e$, demonstrating the proper charge pulse.

3.5 Transient Switching Characteristics of a QPSJ Island

A QPSJ can be designed and operated in an appropriate configuration to produce quantized-area current pulses demonstrating tunneling of a Cooper pair at an instant. This is similar to a Josephson junction producing a constant area voltage pulse indicating movement of flux quanta across them. This can be achieved by over-damping the plasma oscillations of the junction. The QPSJ can be treated as a series RLC oscillator and a damping parameter can be derived from its characteristic equation as shown in equation below:

$$\beta_L = \frac{2\pi V_C L}{2eR^2} \tag{3.10}$$

where β_L is the damping parameter, V_C is the critical voltage of the QPSJ, L is the geometrical inductance and R is the normal resistance of the nano-wire. The junction is under-damped if $\beta_L >> 1$ and over-damped if $\beta_L << 1$. In order to produce quantized-area current pulses, the SPICE model and simulation of QPSJ must be modified to recognize plasma oscillations of the junction. Therefore, the time-step in the device model must be limited to below the time corresponding to the plasma frequency. The QPSJ model in WRSPICE is therefore modified to limit the time step given by:

$$\Delta t = \frac{0.1}{(2\pi V_C/2eL)^{1/2}} \tag{3.11}$$

A QPSJ may be designed to be either in under-damped or over-damped mode using Equation 3.4 and by appropriate choice of material properties and dimensions. Analogous to an SFQ circuit, the island circuit is biased with a DC voltage source V_b as shown in Fig. 3. The DC voltage biases both the junctions to 70% of their critical voltages and therefore has a value of 140% of V_C. An input square voltage pulse is provided as V_{in}, with sufficient magnitude, i.e. greater than 150%, to switch the junction.

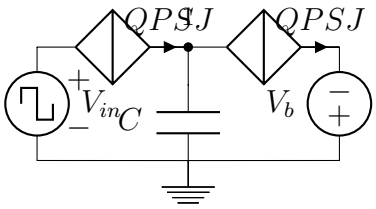


Figure 3.6: Island circuit configuration that is implemented as a quantized charge logic circuit. Note that the capacitance C can be a parasitic capacitance associated with the particular circuit design and layout.

When the junction is under-damped, the switching event causes the junction to switch and latch to a normal state. A result from simulation of the island circuit with both junctions under-damped is shown in Figure 3.2, where the area under the curve is greater than $2e$. A quantized charge pulse, with area under the curve $2e$ can be produced by using over-damped junctions. This is achieved by adding a series resistor to each of the junctions, thereby

increasing the value of R in Equation 3.1. The simulation result of an over-damped junction is shown in Figure 3.2, where the area is quantized to $2e$.

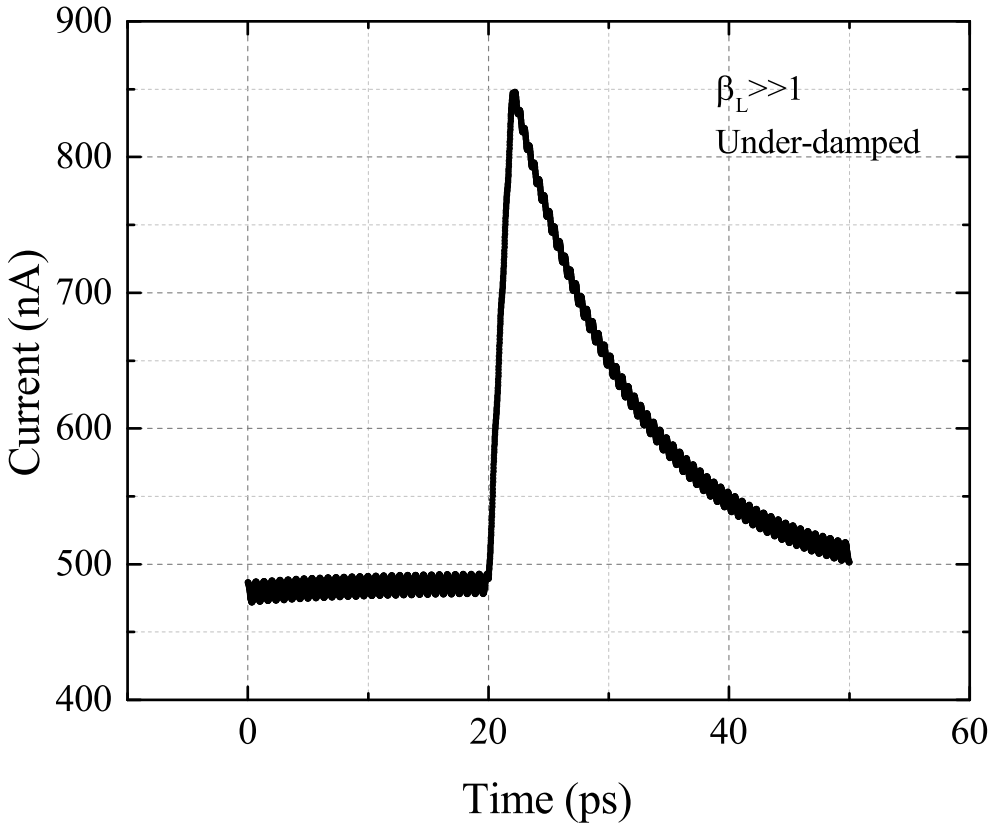


Figure 3.7: Simulation result of switching of an island with under-damped junctions.

3.6 Summary

Using the SPICE model developed for a QPSJ, an operation mode of the device feasible for logic implementation is proposed and demonstrated in simulation. The operation is based on quantized-charge and is a dual to flux-based logic in SFQ circuits. We have demonstrated this operation using estimated junction and material parameters of QPSJ that can be practically implemented. The estimated parameters are an approximation based on a set

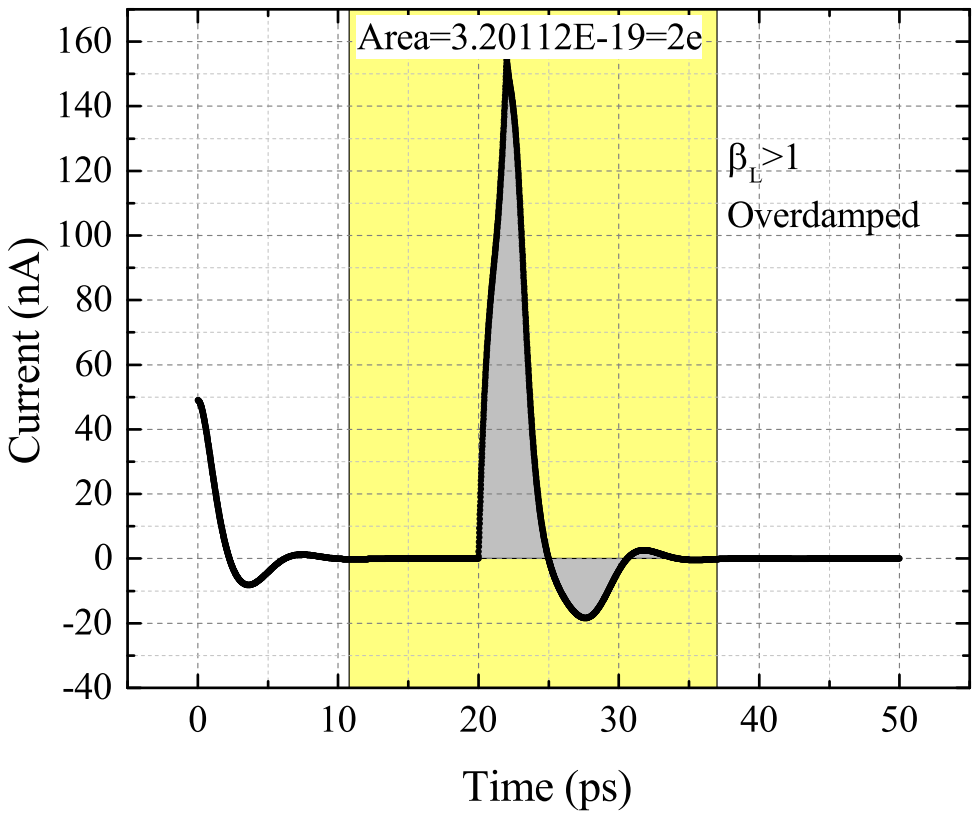


Figure 3.8: Simulation result of switching of an island with over-damped junctions.

of assumptions and we expect that significant experimental work will be needed for experimental verification [5]. The parameter details for obtaining charge pulses in an experiment are outlined.

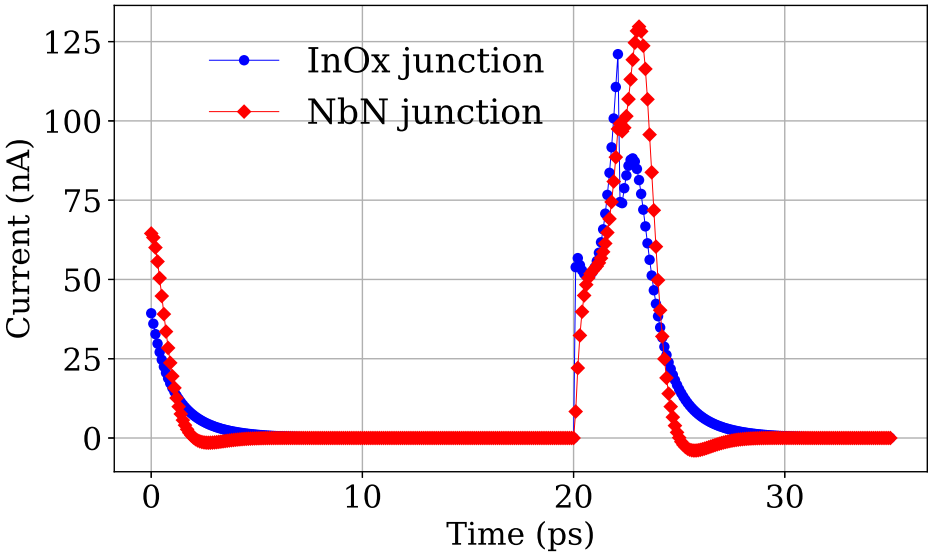


Figure 3.9: Switching characteristics of a QPSJ device demonstrating quantized-area current pulse for charge-based logic for two material systems. Area under each pulse is $2e$.

Chapter 4

Charge-based logic circuits using quantum phase-slip junctions

4.1 Introduction

A QPSJ can be viewed as flux tunneling across a superconducting nano-wire (barrier for flux) creating a voltage drop at the ends of the wire [2]. Therefore, under the appropriate operating conditions, QPSJs can be configured to generate quantized-area current pulses analogous to constant-area voltage pulses in SFQ circuits [18], as described in the previous chapter. We have developed a SPICE model for QPSJs based on a dual model to JJs [92] and demonstrated in simulations, the constant-area pulses that demonstrate quantized charge transport, corresponding to a Cooper pair in QPSJs [94, 95, 96]. In order to implement logic circuits with these devices, a charge-island circuit element, analogous to an SFQ loop [18, 21, 22, 23, 24], has been presented in [97], based on single-charge transistor circuits [93, 74].

In the next section, the basic circuit elements for charge-based superconducting logic are presented along with design and operation requirements that can be expected to produce and manipulate the quantized-charge pulses. These circuits represent the building blocks, that, when used together in different combinations, can form various logic gates that can be used to scale-up the logic operations to perform more complex computations. In the following section, design examples and simulation results of some of the logic gates using the basic components is presented. Finally, differences between SFQ and charge-based logic is presented, based on simulation and highlighting possible advantages and challenges, with comparison of speed of operation and energy requirements per switching event.

4.2 Logic Circuit Elements

The current pulses representing Cooper pair transport across the phase-slip center in the superconducting nano-wire form the logic bits, with the presence of the pulse representing logic "1" and absence of the pulse representing logic "0". When a QPSJ is operated below its critical voltage V_C, the current through the device is zero, and the phase-slip center acts as an insulating barrier between the two electrodes of the device. As an input voltage pulse above the critical voltage is applied to an over-damped QPSJ, an electron pair tunnels across the phase-slip center generating a current pulse with a constant area equal to the charge of two electrons. Therefore, this operation corresponds to a switching from "0" to "1" in charge-based logic. All the other logic operations can be performed by using one or a combination of several logic circuits discussed below.

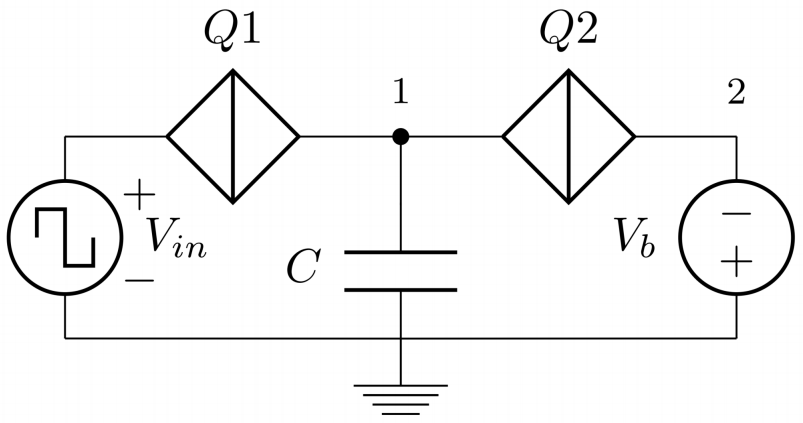


Figure 4.1: Charge island circuit schematic to generate and/or latch charge on node 1. Note that the capacitance C can be a parasitic capacitance associated with the particular circuit design and layout.

4.2.1 Charge Island

The charge-island is comprised of two QPSJs and a capacitor. The two junctions can be identical or different depending on the application in the logic circuit. A circuit schematic of the island is shown in Figure 4.1. When phase-slip occurs in both the junctions, the node 1 between both the QPSJs is isolated from the rest of the circuit acting as an island that

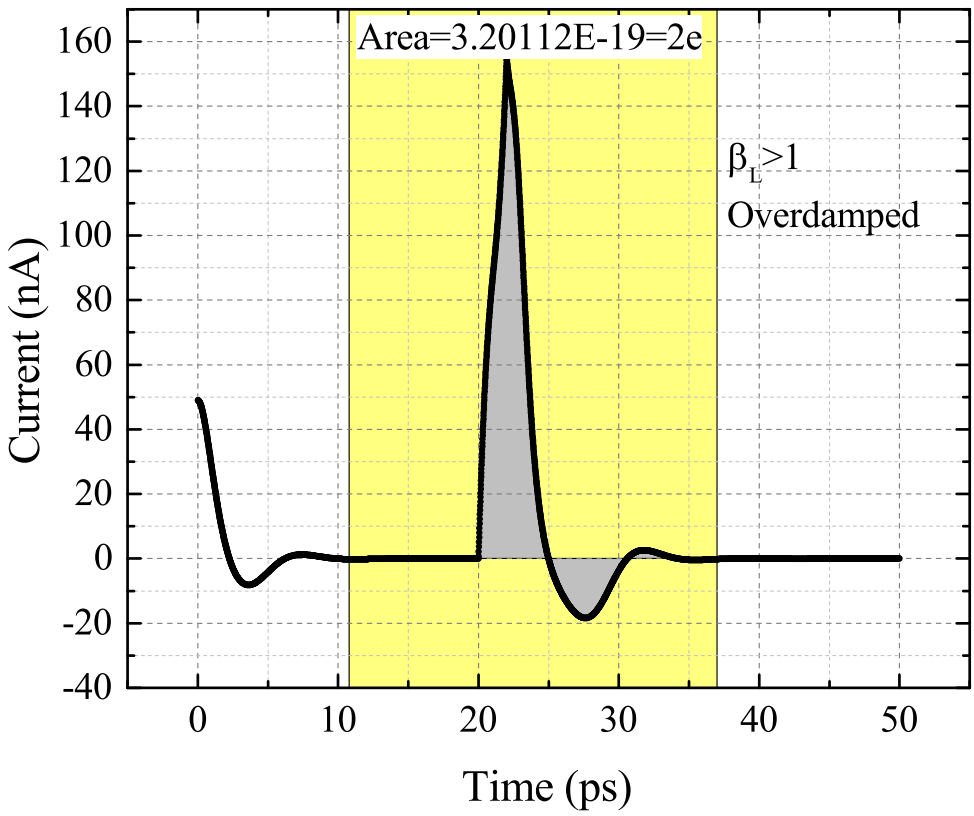


Figure 4.2: Simulation result of an island circuit shown in Fig. 1, illustrating constant-area current pulse of area = $2e$. The critical voltage of both junctions given by $V_C = 0.7$ V. Capacitance $C = \frac{1}{2}2e/V_C$, voltage bias $V_b = 1$ mV, and magnitude of the pulse input voltage $V_in = 2$ mV.

can hold a charge of $C.V_C$, where C is the capacitance of the capacitor. This circuit is a superconductor analog to a single-electron transistor [98]. In this logic operation, the charge on the island will be restricted to a single Cooper pair, i.e. $2e$. Both the junctions $Q1$ and $Q2$ are biased by DC voltage V_b such that the voltage across each junction does not exceed the critical voltage V_C of either junction. The input voltage V_{in} is a pulse signal that can drive the junction $Q1$ above its critical voltage V_C and generate a current pulse. The circuit shown in Figure 4.1 can be designed to accommodate either no charge on the island at an instant, or one Cooper pair depending on the application by appropriately designing the capacitor. If the capacitance $C < 2e/V_C$, the capacitor cannot hold the charge generated by

exciting $Q1$ above its critical voltage, and therefore immediately switches the junction $Q2$. But if the capacitance $C > 2e/V_C$, then the island traps the charge until another pulse signal drives it to the output. Note that this circuit can be connected to another circuit instead of V_{in} to use the incoming current pulse to $Q1$ to drive the connected circuit.

The circuit operation is illustrated using WRSPICE simulation, through demonstration of a constant-area current pulse as shown in Figure 4.2. Different configurations of this circuit can be used in conjunction with other circuits to design several logic gates, some of which are shown in the following sections.

4.2.2 QPSJ Transmission Line

Basic operation of QPSJ circuits can be demonstrated by simulating a QPSJ transmission line which propagates quantized charge of $2e$ along the islands similar to that of Josephson transmission lines [99, 100, 101, 102]. A QPSJ transmission line can be formed using a series of islands with a voltage bias and input voltage signal, similar to the single-electron tunnel junction array reported in [103]. The circuit is shown in Figure 4.3.

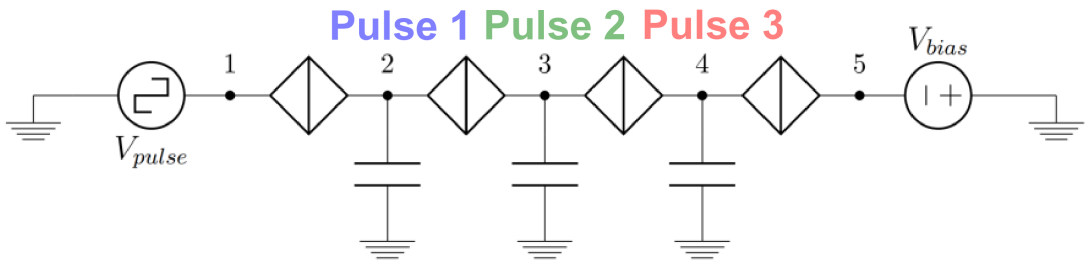


Figure 4.3: QPSJ transmission line with a DC voltage bias of $4 \times 0.7V_C$ and pulse input signal, where V_C is the critical voltage of each of the junctions.

In the circuit, all the junctions have an equal critical voltage of V_C. A DC voltage bias has been used, at node 5, the value of which is equal to $4 \times 0.7V_C$ to be able to bias all four junctions in series. Since each junction, cannot conduct any current until the applied voltage is above its critical voltage, the charge in the islands is zero at this instant. When the input pulse signal is applied, the first junction switches as the voltage across it goes above the

critical voltage of the junction. If the junction is over-damped, a charge of $2e$ is generated, which is stored on the first island, i.e. node 2 of Figure 4.3. This charge in turn generates voltage across the second junction causing it to overcome its critical voltage. Thus, the charge of $2e$, or the current pulse with quantized area of $2e$ travels along the transmission line. The simulation result of this circuit with the input voltage and current at each node is shown in Figure 4.4. A simulation result with multiple current pulses along the transmission line is shown in Figure 4.5. It is possible to obtain amplification or attenuation of current pulse amplitude by using junctions of different critical voltage and different capacitor values similar to that of RSFQ circuits.

4.2.3 QPSJ Pulse Splitter

Fan-out is generally required for implementation of useful digital logic. It is possible to split the current pulses for fan out with the help of a pulse splitter circuit shown in Figure 4.6, which employs charge propagation in islands similar to a QPSJ transmission line, employing different sized junctions. In the circuit shown, the first junction $Q1$ has a critical voltage of $0.7V_C$, where V_C is the critical voltage of $Q2$ and $Q3$. Both the bias voltages are equal to $1.7V_C$. Without decrease in the amplitude of the current pulse, the input pulse is split into two output pulses. The simulation result for this circuit is shown in Figure 4.7.

4.2.4 Control Circuit

The control/buffer circuit configuration is unique to charge-based logic, while the charge island is analogous to a flux loop in SFQ circuits [18].

In the simplest version of this circuit, three QPSJs of different device parameters are used along with two capacitors. It has two input terminals for DC/pulse voltage sources and a DC voltage source for biasing the junctions. This circuit is shown in Figure 4.8. The junctions are designed such that the critical voltage of $Q2$ is higher than the critical voltage of $Q3$. The input voltage V_{in2} has magnitude of $0.7V_C$ where critical voltage of $Q3$ is V_C.

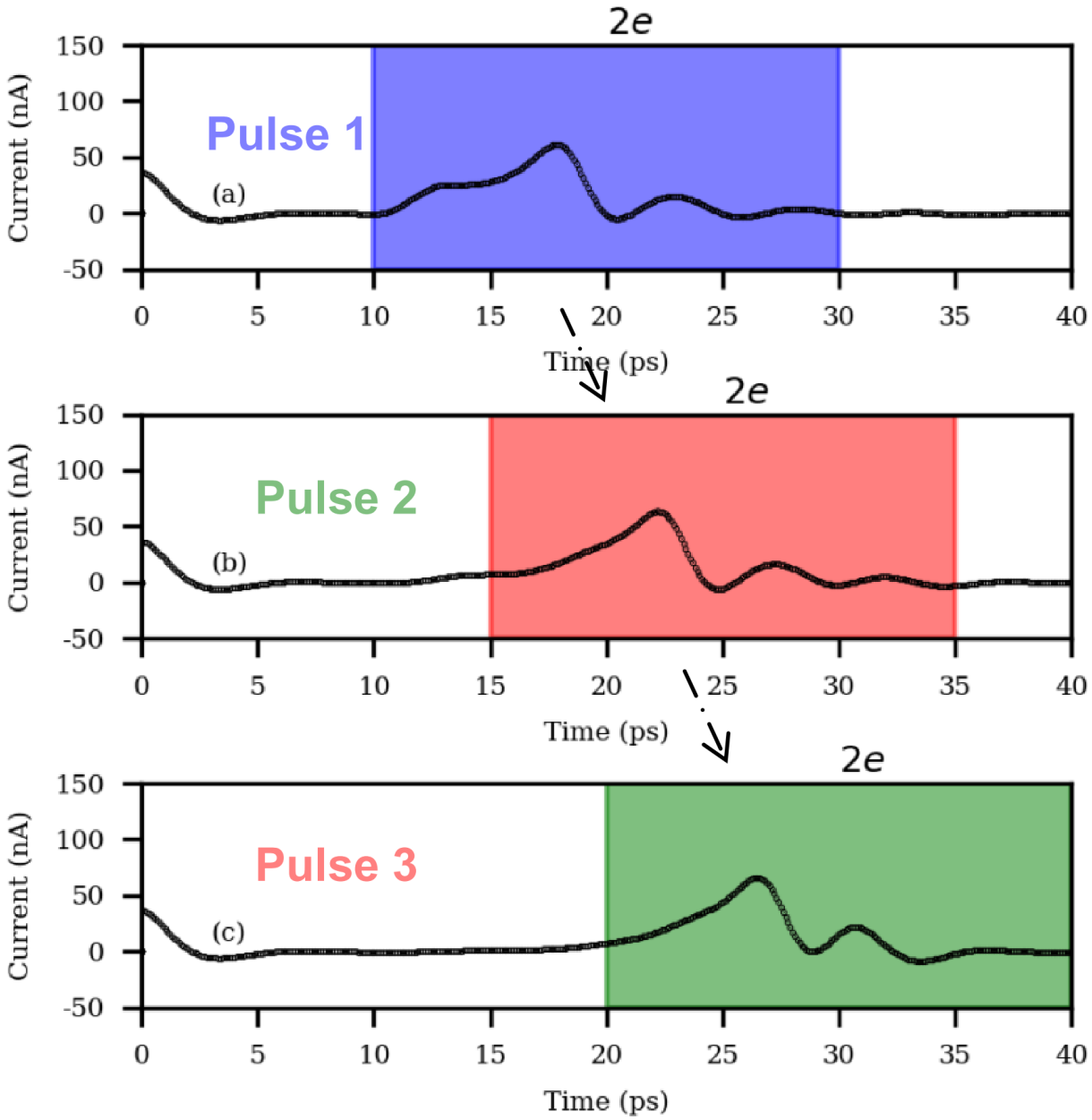


Figure 4.4: Simulation results of QPSJ transmission line illustrating charge $2e$ traveling across islands. (a) Total input voltage signal at node 1. (b) Current at node 1. (c) Current at node 2. (d) Current at node 3.

The input voltage V_{in1} is significantly higher than the critical voltage of $Q1$ to be able to generate the current pulse. Therefore, when the current pulse is generated at $Q1$, it switches $Q3$ before $Q2$ when the input V_{in2} is high and produces the output "0" at node 4. But when the input V_{in2} is low, the output is the same as the input V_{in1}, as the junction $Q2$ is

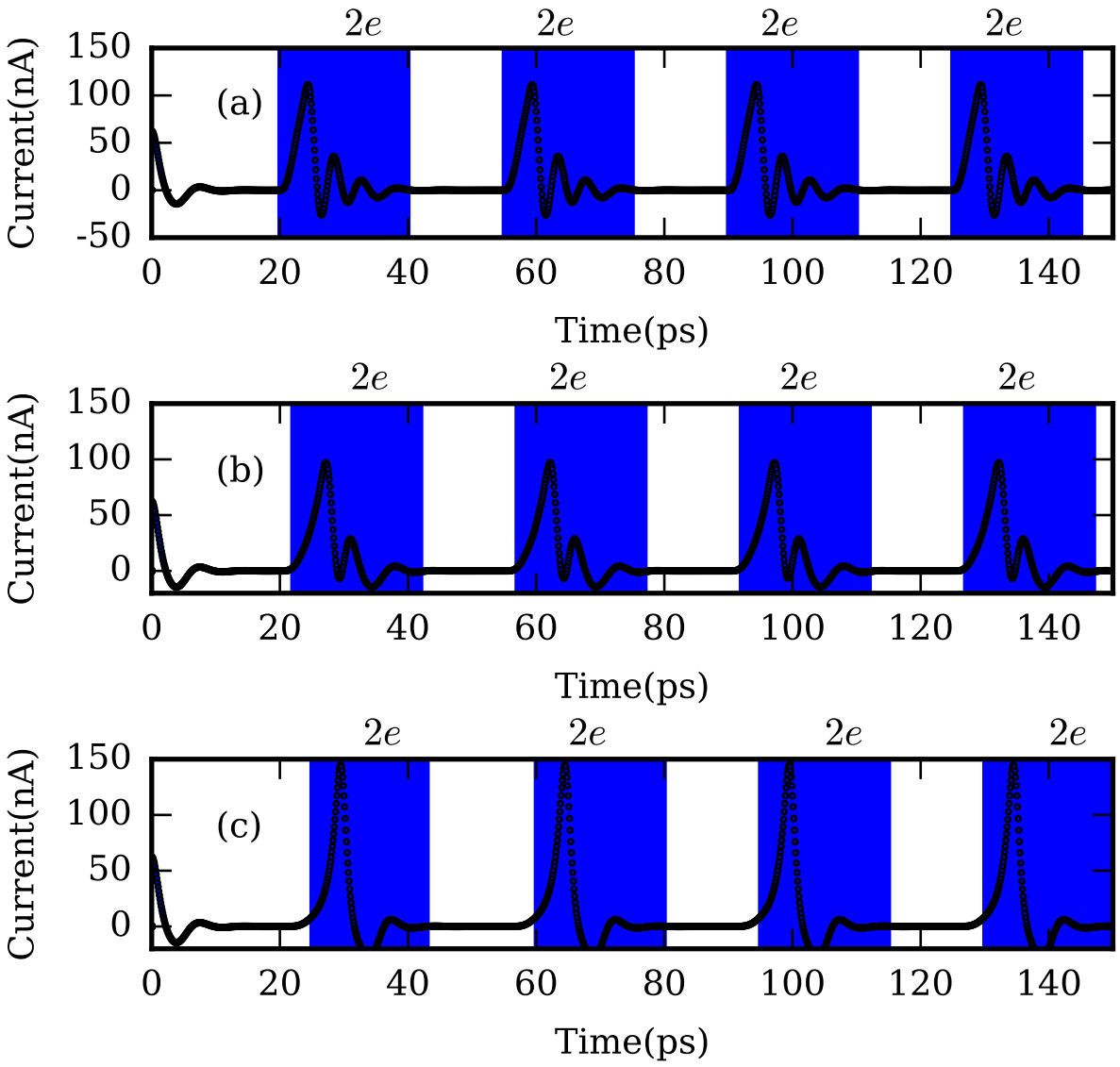


Figure 4.5: Simulation results of QPSJ transmission line with multiple pulses. (a) Current at node 1. (b) Current at node 2. (c) Current at node 3.

biased by V_b. Hence, the input V_{in2} acts as the enable/control input. Furthermore, if the critical voltage of $Q1$ is lower than critical voltages of $Q2$ and $Q3$, then the circuit becomes unidirectional, only allowing the current from node 1 to node 4. The input V_{in2} can be a DC bias to use this circuit as a buffer. The simulation result of an example operation of this circuit is illustrated in Figure 4.9, with circuit parameters chosen to satisfy the conditions mentioned above.

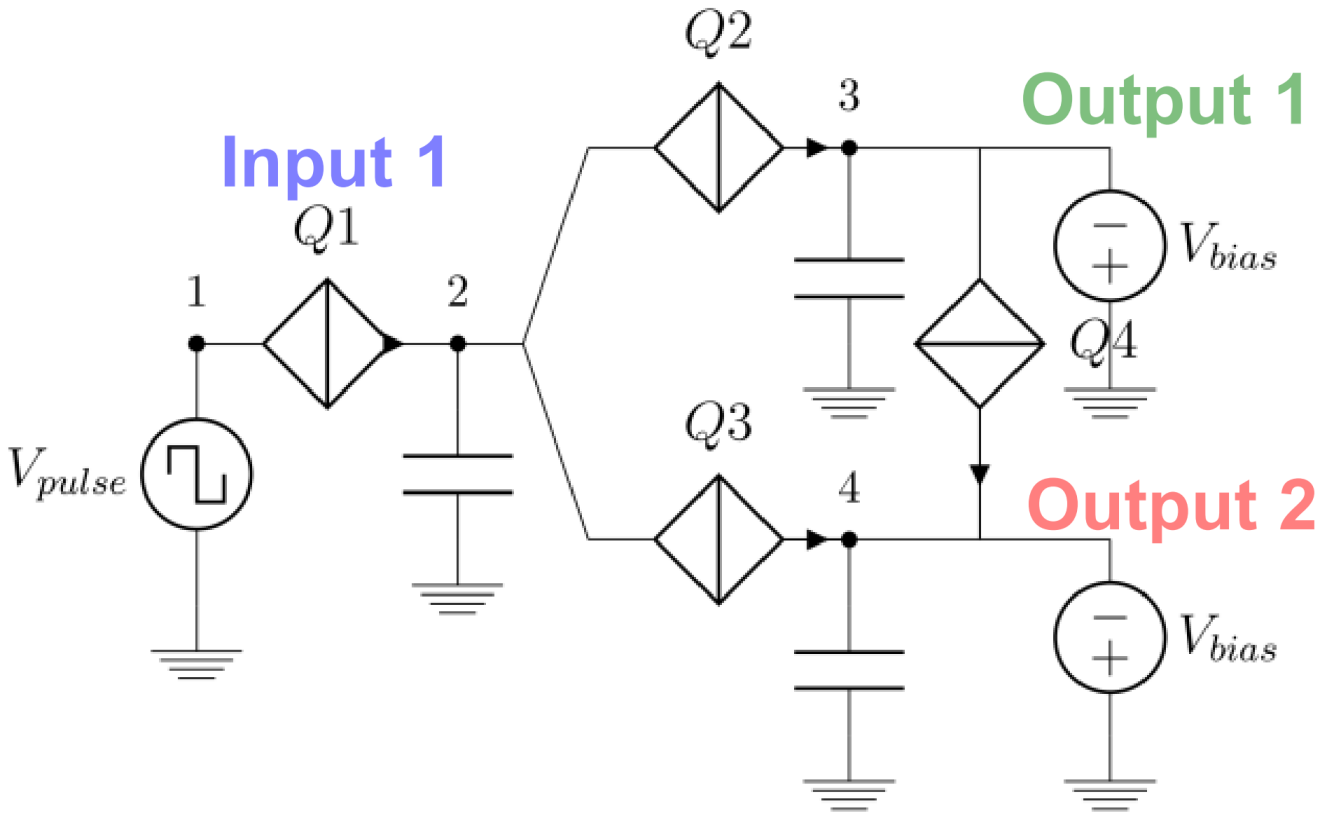


Figure 4.6: Pulse splitter: critical voltage of $Q1 = 0.7V_C$ and critical voltage of $Q2$, $Q3 = V_C$.

4.2.5 QPSJ Buffer

In both the circuits shown so far, the input and output pulses are reciprocal, i.e. the current, and hence the quantized charge $2e$ can flow in both directions. A buffer stage can be designed, as shown in Figure 4.10, and can prevent this reciprocity when introduced in the transmission lines or in logic circuits. In the circuit, the critical voltage of junction $Q1$ is $0.7V_C$, that of junction $Q2$ is V_C and that of junction $Q3$ is $1.4V_C$. Therefore, the current pulse from $Q1$ switches $Q3$, before it switches $Q2$ and prevents signal flow in the direction from node 1 to node 4. Whereas, when current arrives from the opposite direction, as shown in Figure 4.11, junction $Q1$ switches before $Q3$, allowing the signal through. The bias voltage at node 4 is equal to $1.5V_C$ to bias both $Q1$ and $Q2$. $Q3$ is biased using a different voltage

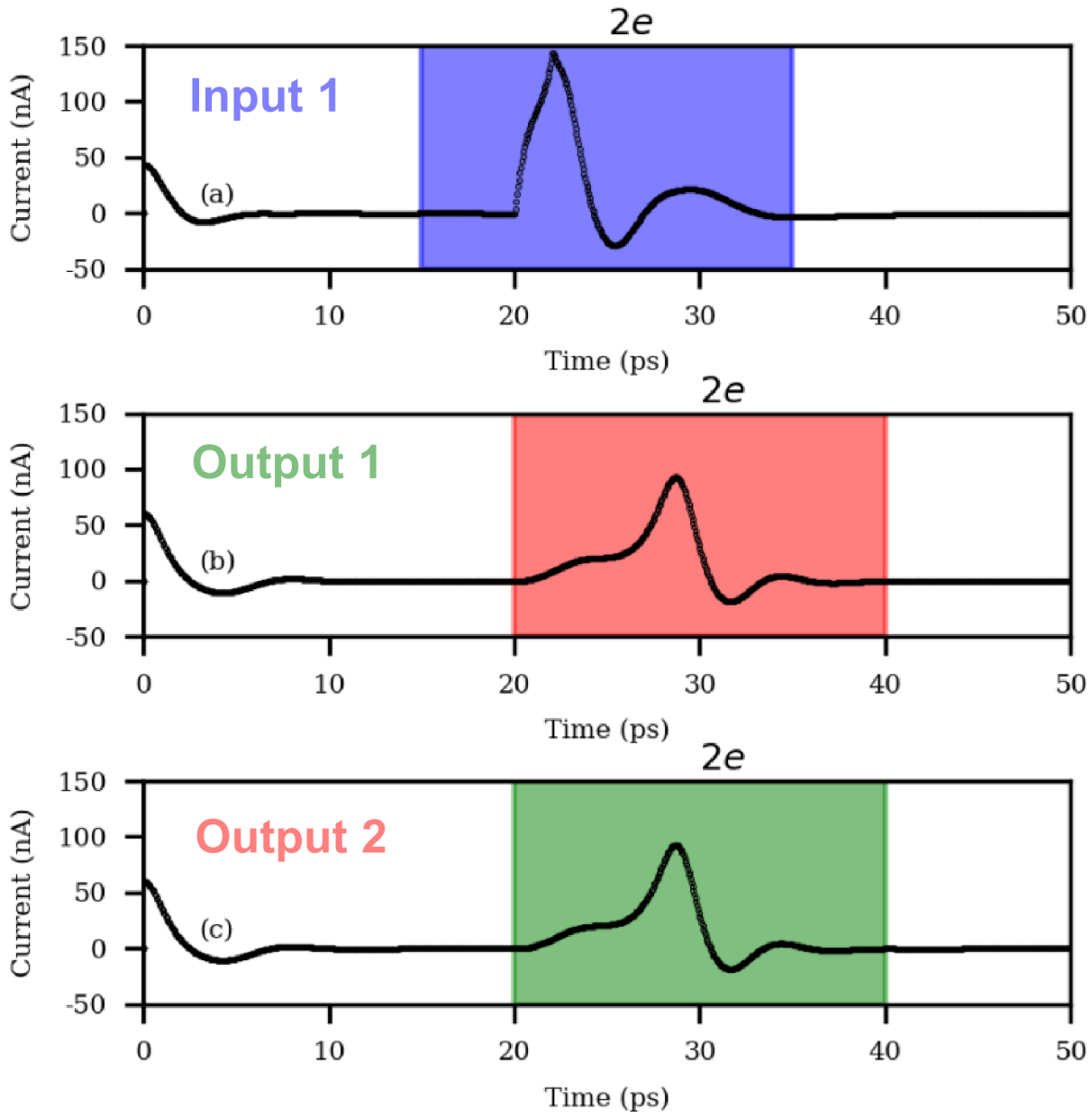


Figure 4.7: Simulation result of pulse splitter circuit shown in Figure 4.6. (a) Total input voltage signal at node 1. (b) Current at node 1. (c) Current at node 3. (d) Current at node 4.

source, the value of which is equal to $0.7V_C$. The simulation results for both situations are shown in Figure 4.11 and Figure 4.12, respectively.

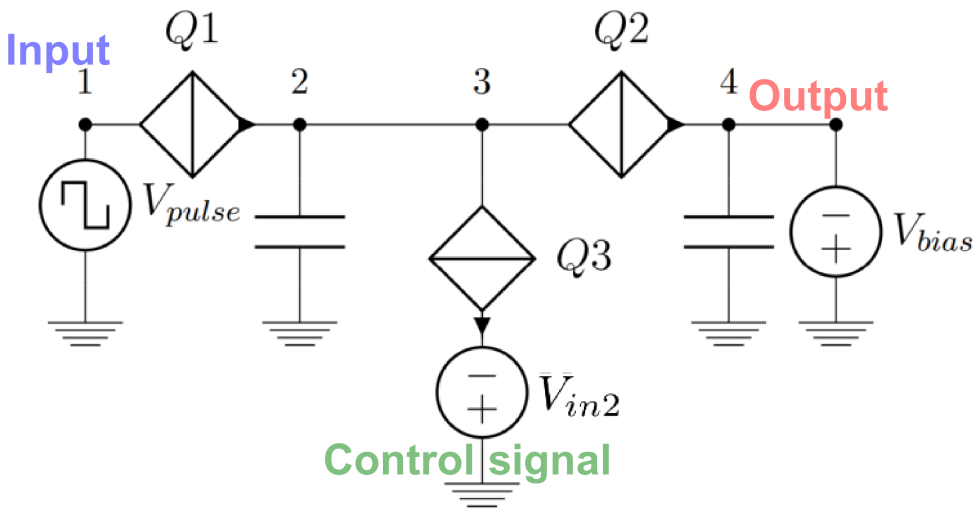


Figure 4.8: Two input control/buffer circuit with input V_{in2} acting as enable/control signal. This circuit can be used as a direction control buffer circuit when V_{in2} is DC bias. $V_C(Q2) > V_C(Q3) > V_C(Q1)$.

4.2.6 QPSJ Confluence Buffer/Merger Circuit

A confluence buffer circuit is an extension of the buffer circuit with two inputs and an output. This circuit can be used to merge two signals and generate a corresponding output pulse without current pulses from one input going to another input. This circuit is shown in Figure 4.13. Here, $Q1$ and $Q2$ have critical voltages of $1.4V_C$, that of $Q3$ is V_C and that of $Q4$ is $0.7V_C$. The simulation result of this circuit is shown in Figure 4.14.

The circuits discussed so far can be used to manipulate the current pulses, control direction, fan-in and fan-out of signals. In the next sections, basic flip-flops and other logic circuits will be presented and discussed.

4.2.7 RS Flip-flop/D Flip-flop

An RS flip-flop or the DC squid of the SFQ logic family is a key component which can be used in other higher level logic circuits. The corresponding configuration in charge-based logic has been implemented in a simplest possible circuit using QPSJs, which is an island formed between two QPSJs. The circuit shown in Figure 4.15 consists of two QPSJs forming an island with a capacitor along with voltage biases and signals at its two terminals

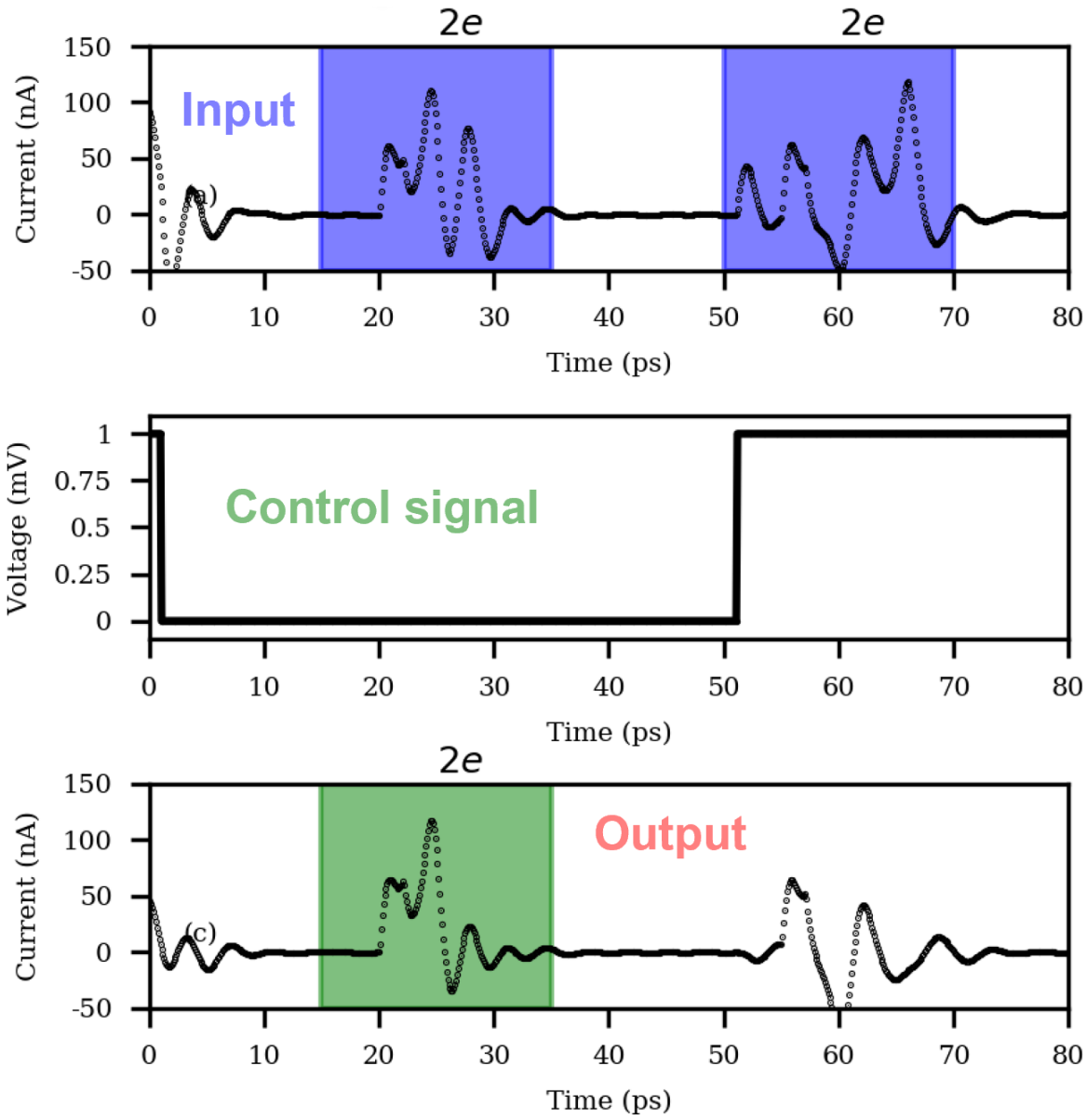


Figure 4.9: Simulation result of a control circuit shown in Figure 4.8, illustrating current pulse at the output only when the control signal is low. The critical voltage of junction $Q1$ is 0.7 mV, $Q2$ is 1 mV and $Q3$ is 1.5 mV. Capacitance $C = 0.23$ fF, Voltage bias $V_b = 1.1$ mV, magnitude of the pulse input voltage $V_{in1} = 1.5$ mV and magnitude of the control input voltage is $V_{in2} = 1$ mV. (a) Input current pulses. (b) Control voltage signal. (c) Output current pulses.

corresponding to $RESET$ and SET. Both the junctions $Q1$ and $Q2$ have critical voltages of V_C. The capacitor between node 3 and ground has a value of $1.5V_C/2e$, enabling it to store a charge corresponding to a single Cooper pair at the island, when SET signal is applied.

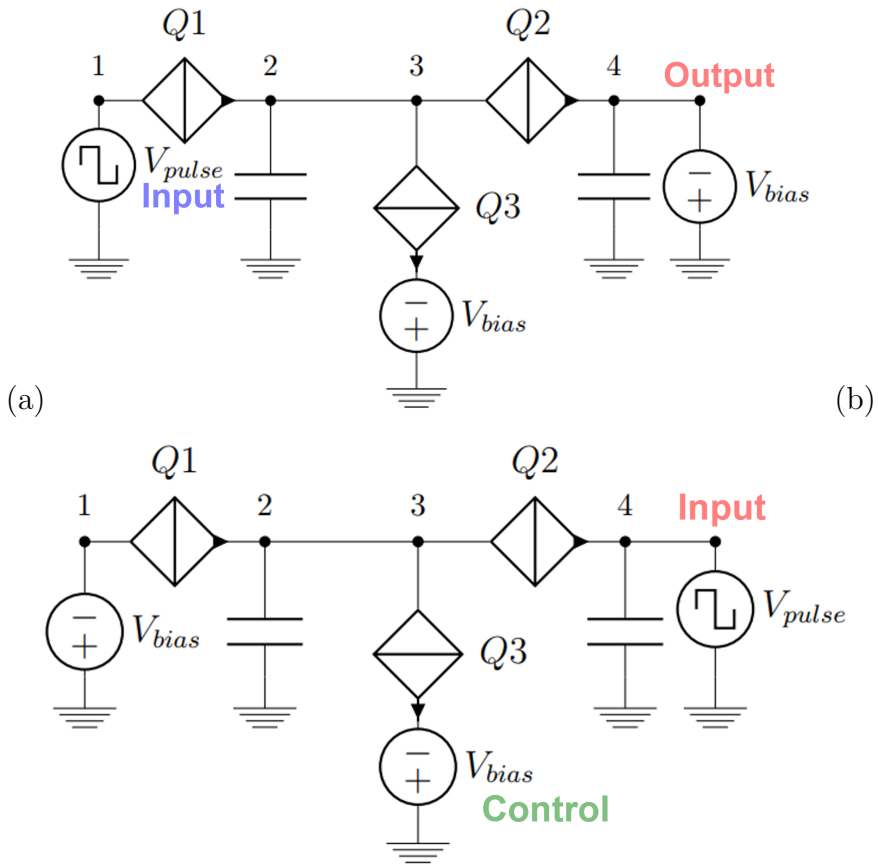


Figure 4.10: Buffer circuit showing current flow situations in both directions. Critical voltage of $Q1 = 0.7V_C$, $Q2 = V_C$ and $Q3 = 1.4V_C$

A DC voltage source biases both the junctions. The input signal at SET, which is V_{pulse} at node 1, induces a charge of $2e$ to the island, and the input signal at $RESET$, which is V_{pulse} at node 4, induces charge opposite to SET and therefore resets the charge on the island. The simulation result illustrating the function of this circuit is shown in Figure 4.16.

A D flip-flop can be implemented using a similar circuit. The input at $RESET$ is replaced by a clock signal. Therefore, the input signal switches the first junction and induces a charge $2e$ on the island. With the next clock pulse, the charge flows through the OUT terminal in the circuit performing the function of a D flip-flop.

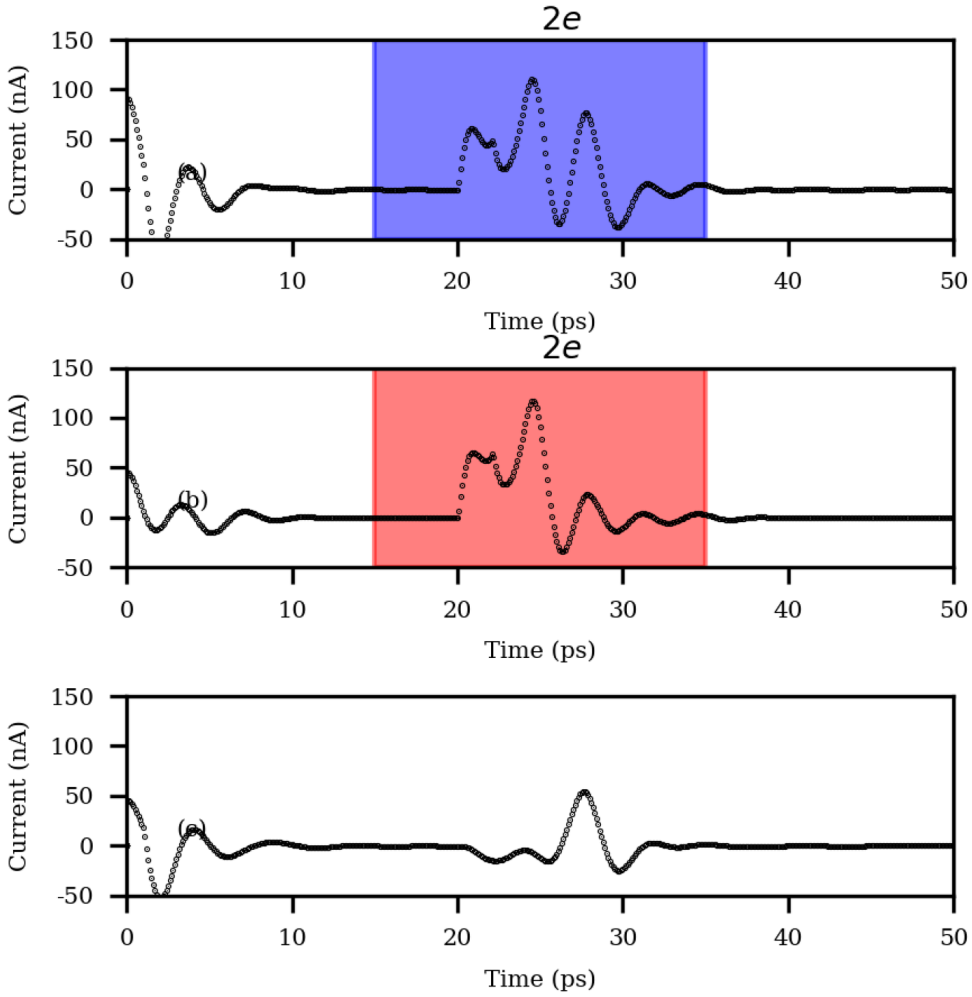


Figure 4.11: Simulation result corresponding to circuit in Figure 4.10(a). (a) Signal at node 1. (b) Signal through $Q3$. (c) Signal at node 4.

4.2.8 T Flip-flop

A T flip-flop can also be implemented using a very similar circuit to RS flip-flop. Both the *RESET* and *SET* inputs are connected to a single clock signal, with the bias voltage connected as shown in the circuit in Figure 4.17. At each clock pulse, the current pulse toggles from ON to OFF and vice-versa indicating the presence and absence of charge on the island with each clock pulse. The simulation result of the circuit is shown in Figure 4.18. The output current pulse is very similar to the output pulse of RS flip-flop circuit simulation.

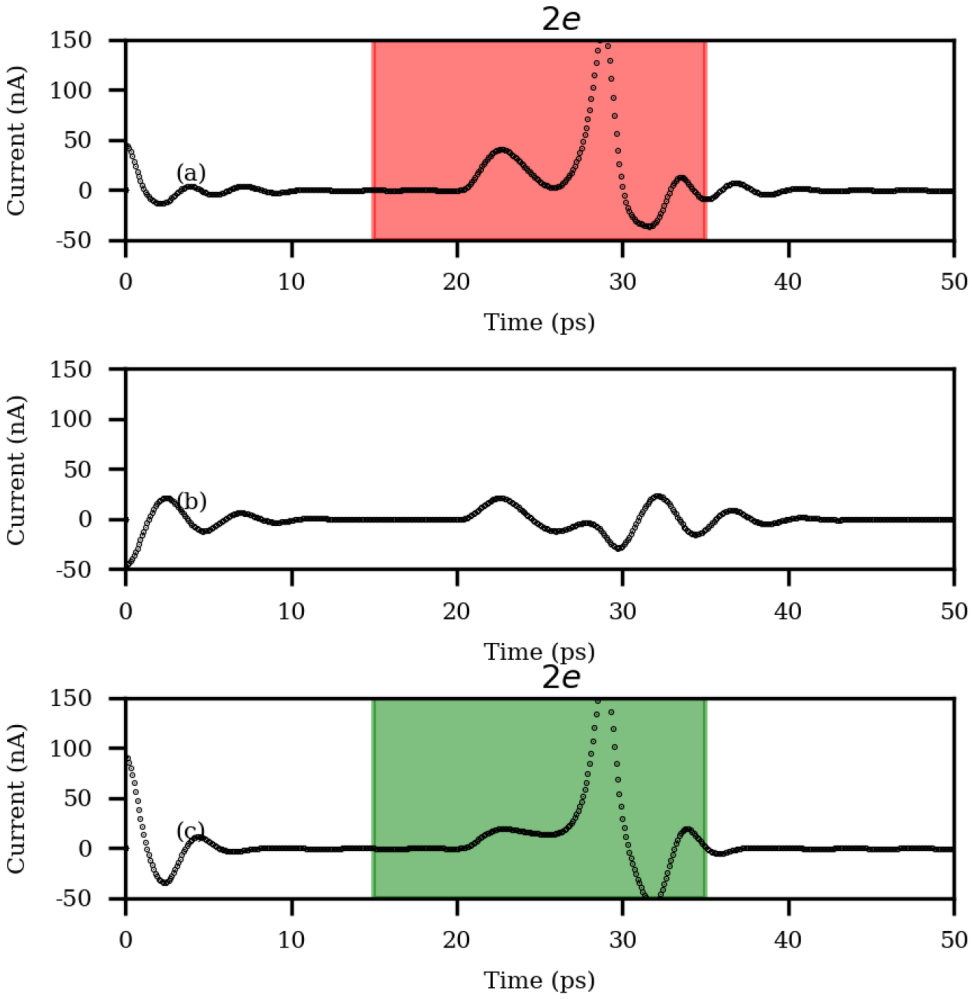


Figure 4.12: Simulation result corresponding to circuit in Figure 4.10(b). (a) Signal at node 1. (b) Signal through $Q3$. (c) Signal at node 4.

4.3 Logic Gates

The charge island and the control/buffer circuit, in their different configurations, can be used in various possible configurations to design several logic gates or memory circuits. In some cases, it is possible to realize the same logic operations in different circuits. Some examples of logic gates designed using combinations of logic elements discussed in the previous section are presented below.

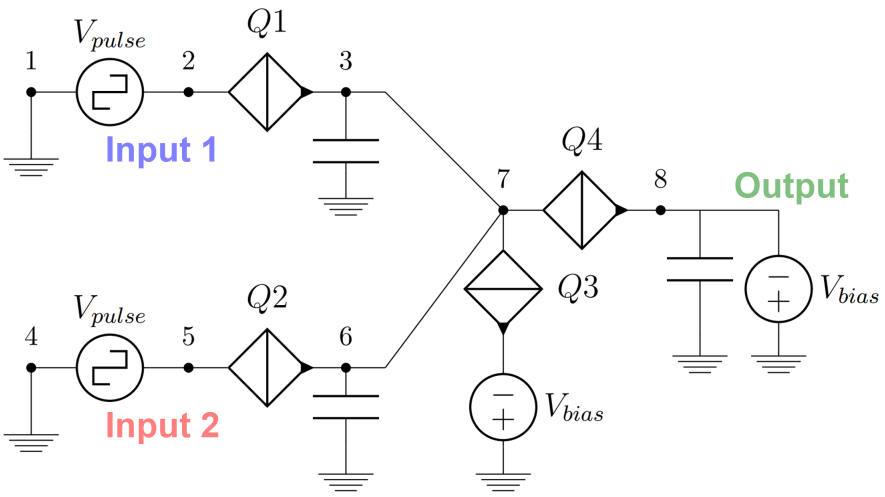


Figure 4.13: QPSJ merger/confluence buffer. Critical voltage of $Q1$, $Q2 = 1.4V_C$, $Q3 = V_C$, $Q4 = 0.7V_C$.

4.3.1 QPSJ Based OR Gate

We will observe that any logic operation can be performed by combining two or more basic elements discussed so far. An OR gate can be formed by cascading a confluence buffer and an island formed by QPSJs similar to an RS flip-flop in series. The junctions with same critical voltages as that of RS flip-flop and confluence buffer. This implementation is identical to the RSFQ based OR gate. The circuit diagram is given in Figure 4.19. This is a timed OR gate, and hence has a clock input.

When one or both the inputs are high, the confluence buffer produces a current pulse corresponding to a charge of $2e$ at the island, which is the input to the RS flip-flop. With the next clock pulse, the charge stored on the island can be seen in the current pulse at the output. When both the inputs are low, there is no charge flow through the output. The simulation result of this circuit is shown in Figure 4.20.

4.3.2 QPS Based AND Gate

An AND operation in charge-based logic can be obtained by slightly modifying the OR gate. The confluence buffer part of the circuit is still used here to have a buffered two-input

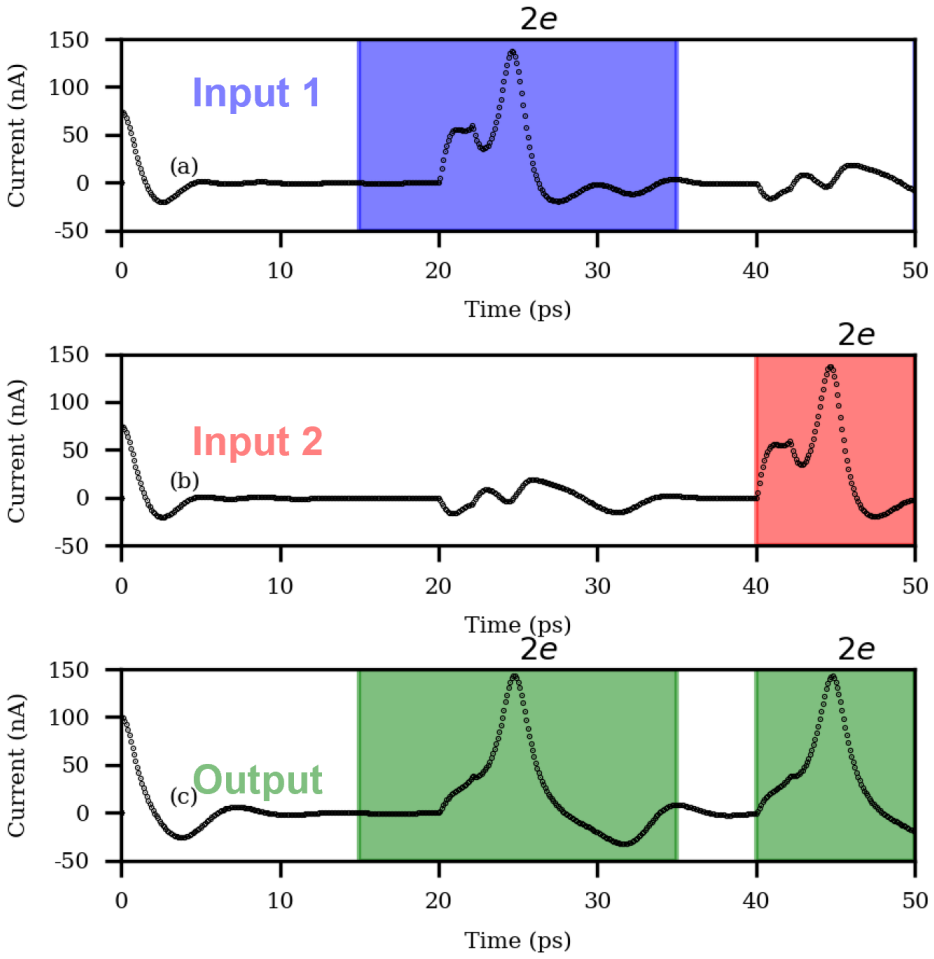


Figure 4.14: Simulation results of a QPSJ merger. (a) Total input voltage signal at node 1. (b) Current pulse at node 3. (c) Current pulse at node 6. (d) Output signal at node 8.

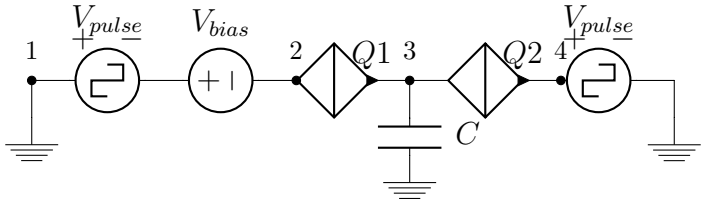


Figure 4.15: RS flip-flop using QPSJs forming an island with a capacitor. Critical voltage of $Q1$, $Q2 = V_C$, $C = 1.5V_C/2e$.

gate, but the island part of the circuit which operates as an RS flip-flop has been replaced with a buffer circuit from Figure 4.10. At the output node, a clock has been added in series with the DC bias which makes this circuit a synchronized AND gate. The clock is necessary for the operation of this gate and a version without clocked gates has not been designed yet.

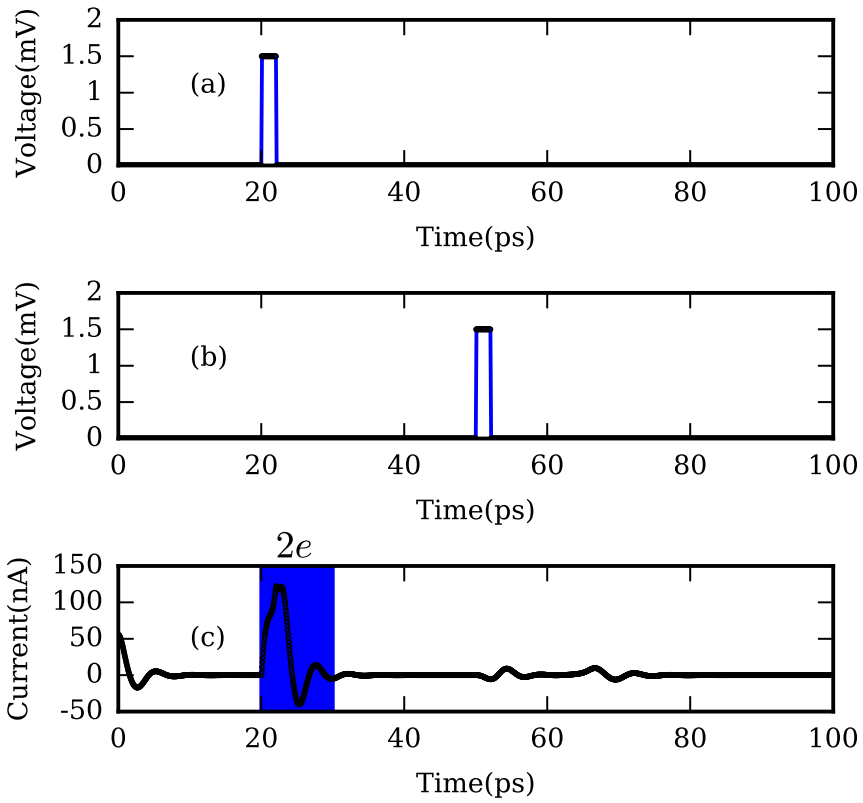


Figure 4.16: Simulation results for RS flip-flop circuit in Fig. 14. (a) Input voltage pulse at SET, i.e. node 1. (b) Input voltage pulse at $RESET$, i.e. node 4. (c) Output current pulse at node 4.

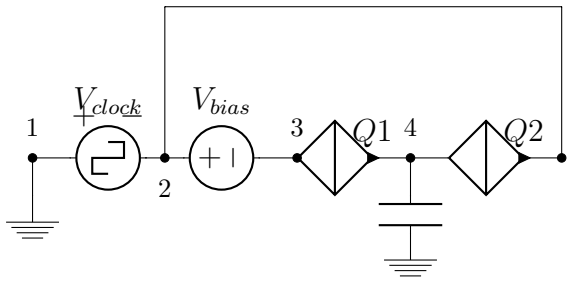


Figure 4.17: T flip-flop circuit obtained from QPSJ island and clock input. Critical voltage of $Q1$, $Q2 = V_C$, $C = 1.5V_C/2e$.

It is possible to extend these gate to more than two inputs by adjusting the parameters of the junctions accordingly. The circuit is shown in Figure 4.21 and the simulation results are shown in Figure 4.22.

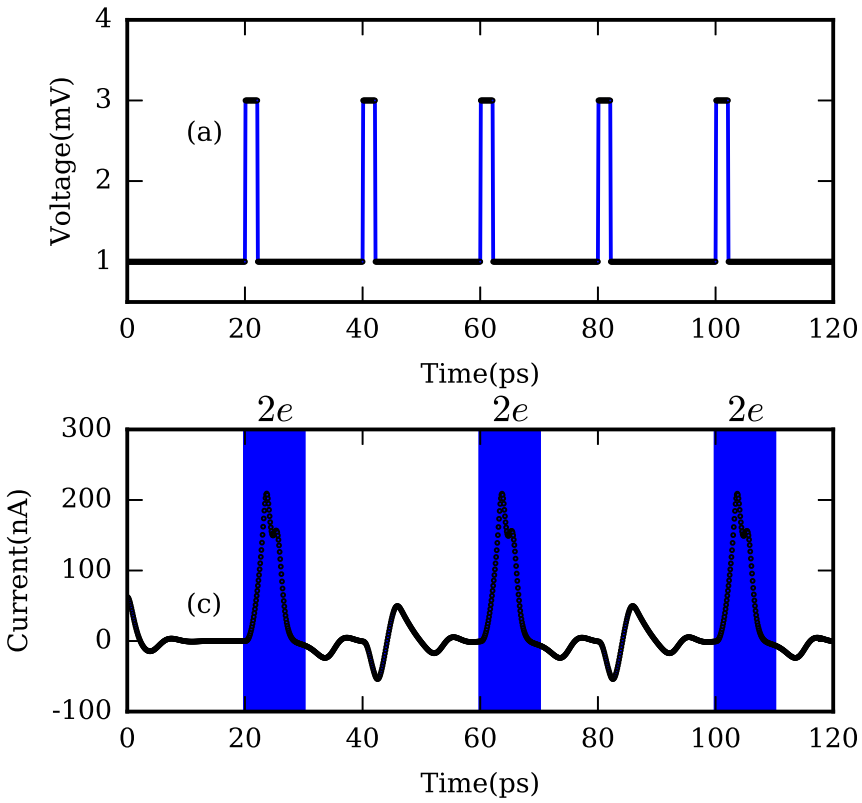


Figure 4.18: Simulation results for T flip-flop. (a) Clock signal input at node 1. (b) Output current signal coming out of node 2.

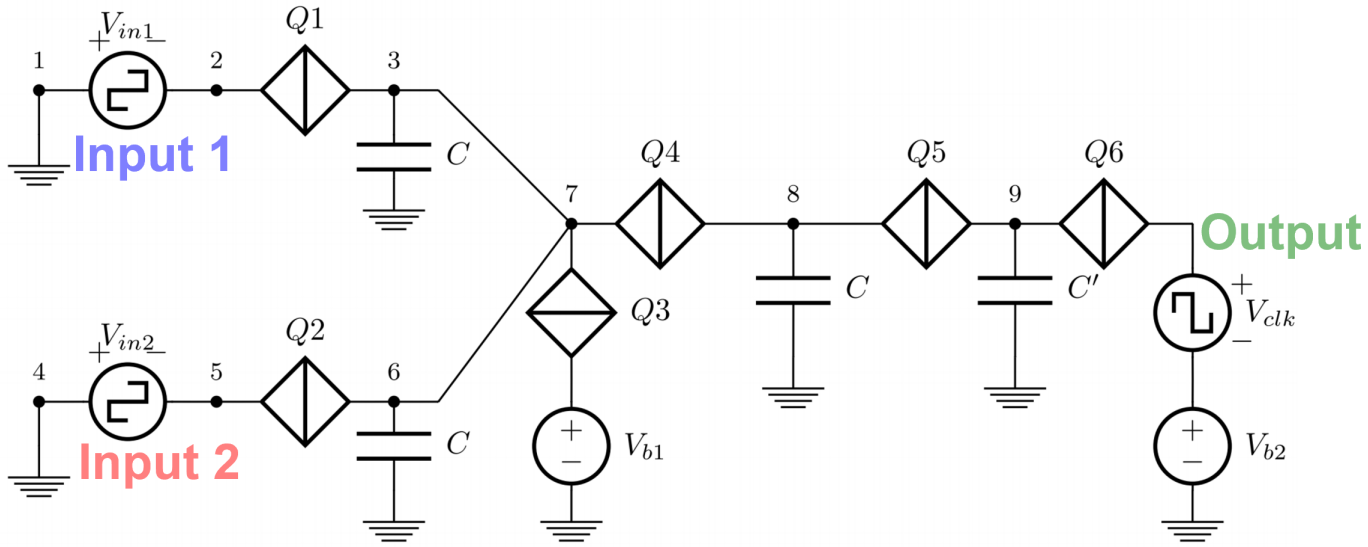


Figure 4.19: QPSJ based OR gate formed by combining a confluence buffer and RS flip-flop.

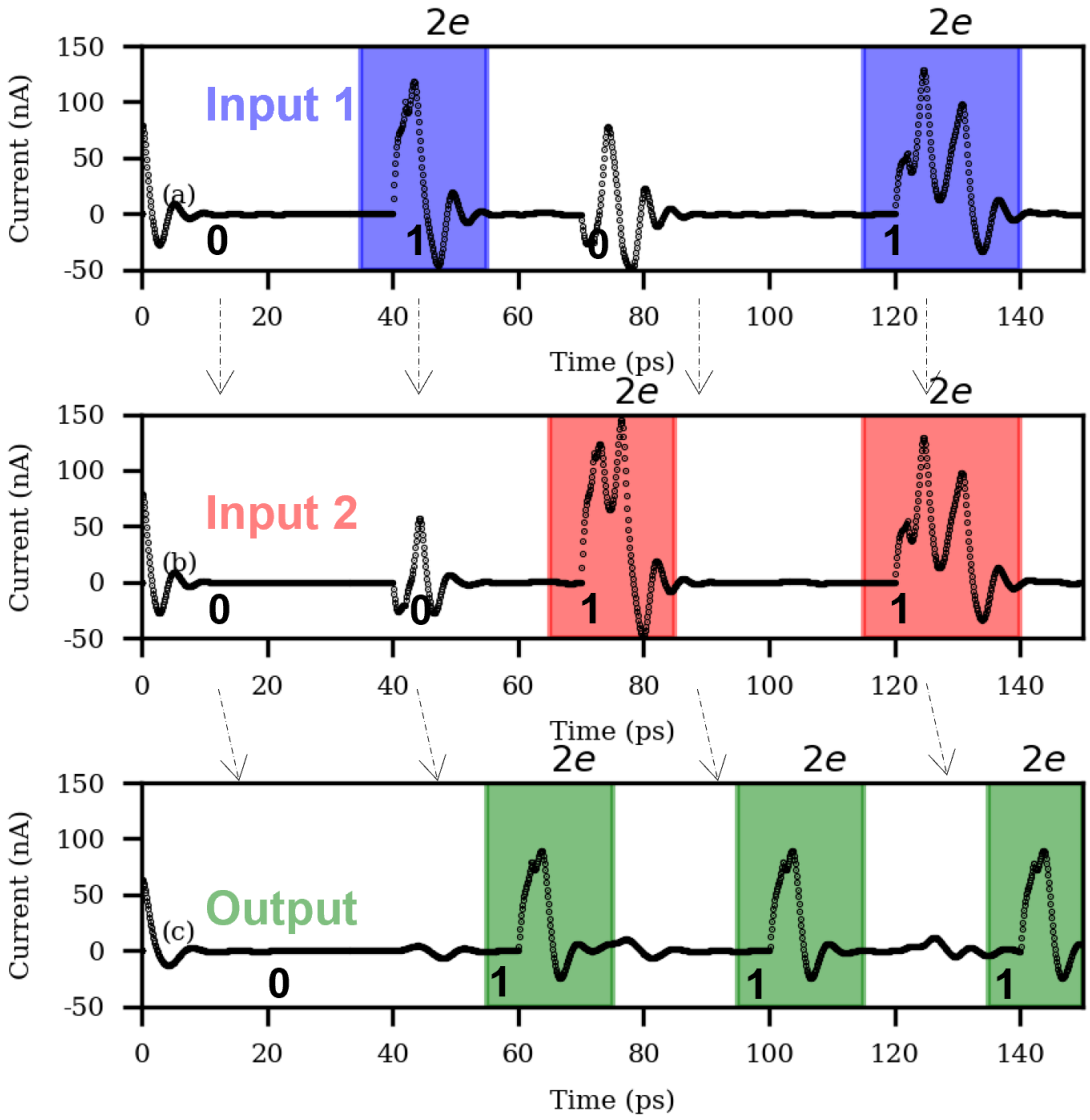


Figure 4.20: Simulation results of OR gate implementation using QPSJs. (a) Input current pulse at node 1. (b) Input current pulse at node 2. (c) Output current pulse at node 9.

When either one of the inputs is high, the junction in the buffer circuit $Q5$ switches therefore ensuring the output to be low. When both the inputs are high during the same clock period, only one of the junctions are negated by the buffer circuit and the output is still high.

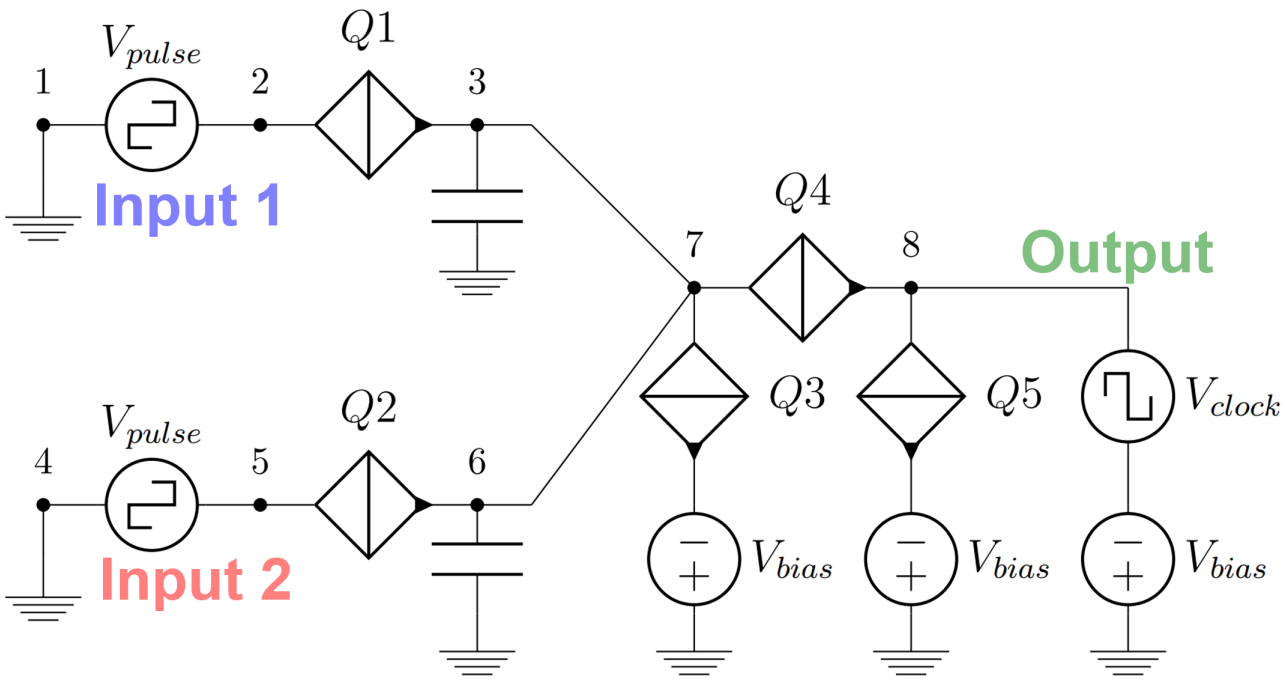


Figure 4.21: AND gate circuit implemented by replacing RS flip-flop in OR gate with a buffer circuit.

4.3.3 QPSJ Based XOR Gate

A two input XOR operation using charge-based logic can be implemented in a way very similar to the OR gate and the AND gate discussed above. A confluence buffer is used for the two input pulses and the additional buffer gate that has been included for AND operation has been removed. This ensures two identical inputs cancel each other out, but only a single pulse at either of the gates will not be affected by a buffer circuit. The circuit is shown in Figure 4.23 and the simulation result is shown in Figure 4.24.

4.3.4 Alternative Design for XOR Gate

The XOR operation can also be achieved by using the control gate circuit operation discussed in section 4.4.

Two identical control gates are used in parallel, with both having the data inputs at both input terminals but their positions swapped from one circuit to another. A simple

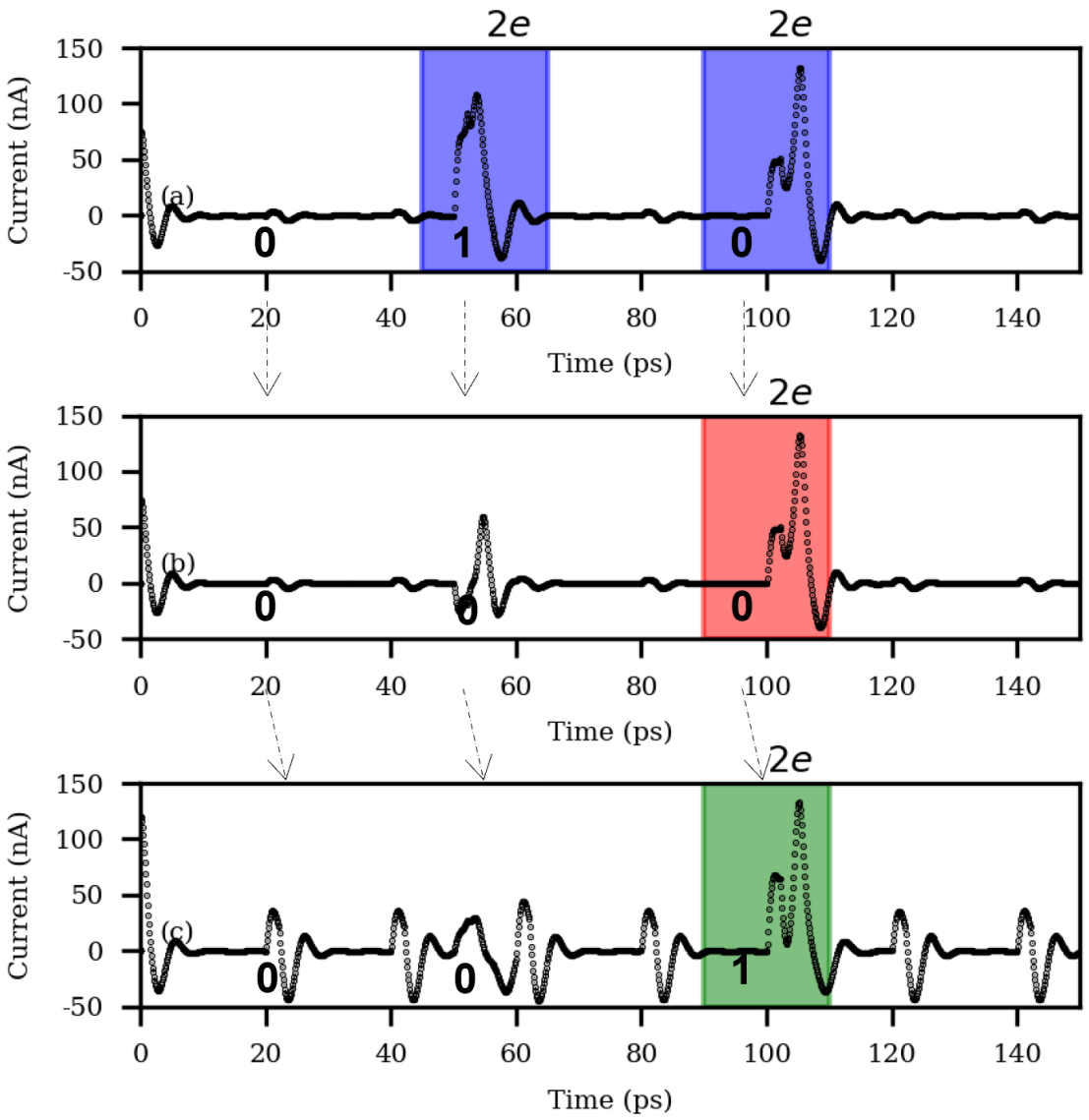


Figure 4.22: Simulation results of AND gate implementation using QPSJs. (a) Input current pulse at node 1. (b) Input current pulse at node 2. (c) Output current pulse at node 8.

version of the circuit schematic is shown in Figure 4.25, though additional buffer circuits may be added at the input or output terminals depending on the application of this circuit. As shown in Figure 4.25, the circuit has two nominally identical control circuits with $Q1$ and $Q4$ identical, $Q2$ and $Q5$ identical and $Q3$ and $Q6$ identical, along with all identical capacitors. The input voltage signal $V_{in1}$is connected to the junctions $Q1$ and $Q6$, and V_{in2} is connected to $Q2$ and $Q4$. When both the inputs are low, no charge transport occurs through the junctions generating output "0".

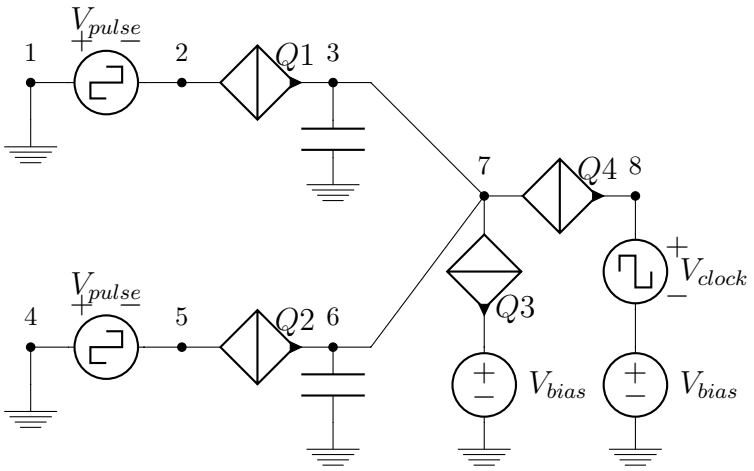


Figure 4.23: XOR gate circuit implemented by removing the buffer circuit in AND gate.

When both the inputs are high, the charge $2e$ is generated at $Q1$ and $Q4$, but the corresponding current pulse signals take the paths through $Q3$ and $Q6$, respectively, enabled by the input signals at these junctions, thereby generating output "0". When one of the inputs is high, the current pulse travels to the output node 4 corresponding to output "1". The simulation results of this circuit with parameters chosen to satisfy the conditions stated is shown in Figure 4.26. Note that this circuit can also be used as an inverter with one of the inputs set as clock, or a DC voltage bias. Furthermore, the input signals can be tied together in different configurations to achieve NAND and NOR gates with more than two inputs.

4.4 Higher-level Digital Operations

4.4.1 QPSJ Based Half-adder

In order to demonstrate that these individual gate designs shown so far can be used to perform more complicated logic operations, a half adder has been demonstrated by combining the AND and XOR gates along with splitters to split the input pulses to both XOR and AND gates. Figure 4.27 illustrates the schematic of the half-adder circuit. Figure 4.28 shows the simulation results of the two-input half-adder circuit.

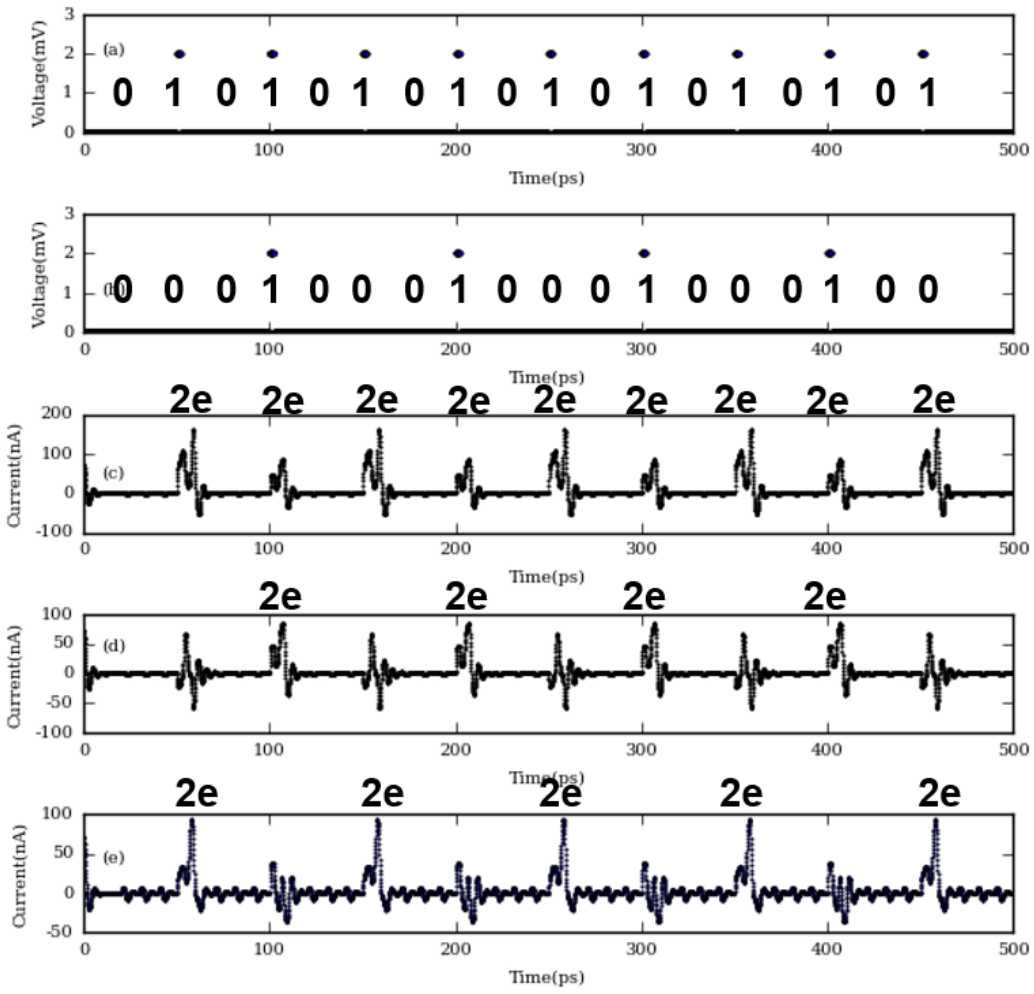


Figure 4.24: Simulation results of XOR gate implementation using QPSJs. (a) Input current pulse at node 1. (b) Input current pulse at node 2. (c) Output current pulse at node 8.

4.4.2 QPSJ Based Shift Register

A D flip-flop demonstrated in the previous section can be used to construct a shift register with identical clocks at each stage. A block diagram demonstrating the entire circuit is shown in Figure 4.29. The circuit has four shift stages with each stage using a different but identical clock input. The simulation result of the shift register is shown in Figure 4.30.

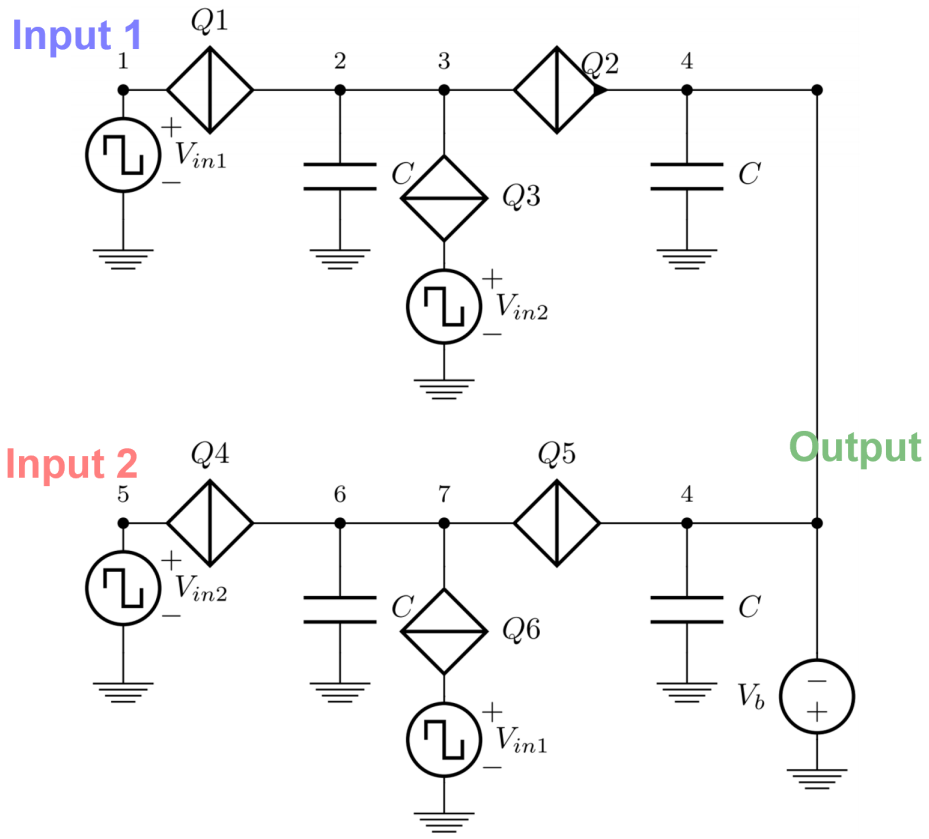


Figure 4.25: Two input XOR gate with both inputs V_{in1} and V_{in2} connected to two different terminals of the circuit each. $V_C(Q2, Q5) > V_C(Q3, Q6) > V_C(Q1, Q4)$. V_{in1}, V_{in2} have magnitudes of $1.5V_C(Q1, Q4)$. $C < 2e/V_C$

4.4.3 QPSJ Based Ring Counter

A ring counter can be constructed using the D flip-flops in a very similar way as a shift register. A single input pulse is needed to trigger the circuit. An identical clock triggers each stage and a counter operation can be observed in the simulation result shown in Figure 4.32 for the block diagram of the circuit being shown in Figure 4.31.

4.4.4 QPSJ Based OR-AND Circuit

An OR-AND circuit shown in Figure 4.33 has been implemented. The gates used in this circuits are all synchronized and therefore use an identical clock. This illustrates that any other higher-level logic circuits for complicated operation can be implemented using charge-based logic. The simulation results of this circuit are shown in Figure 4.34.

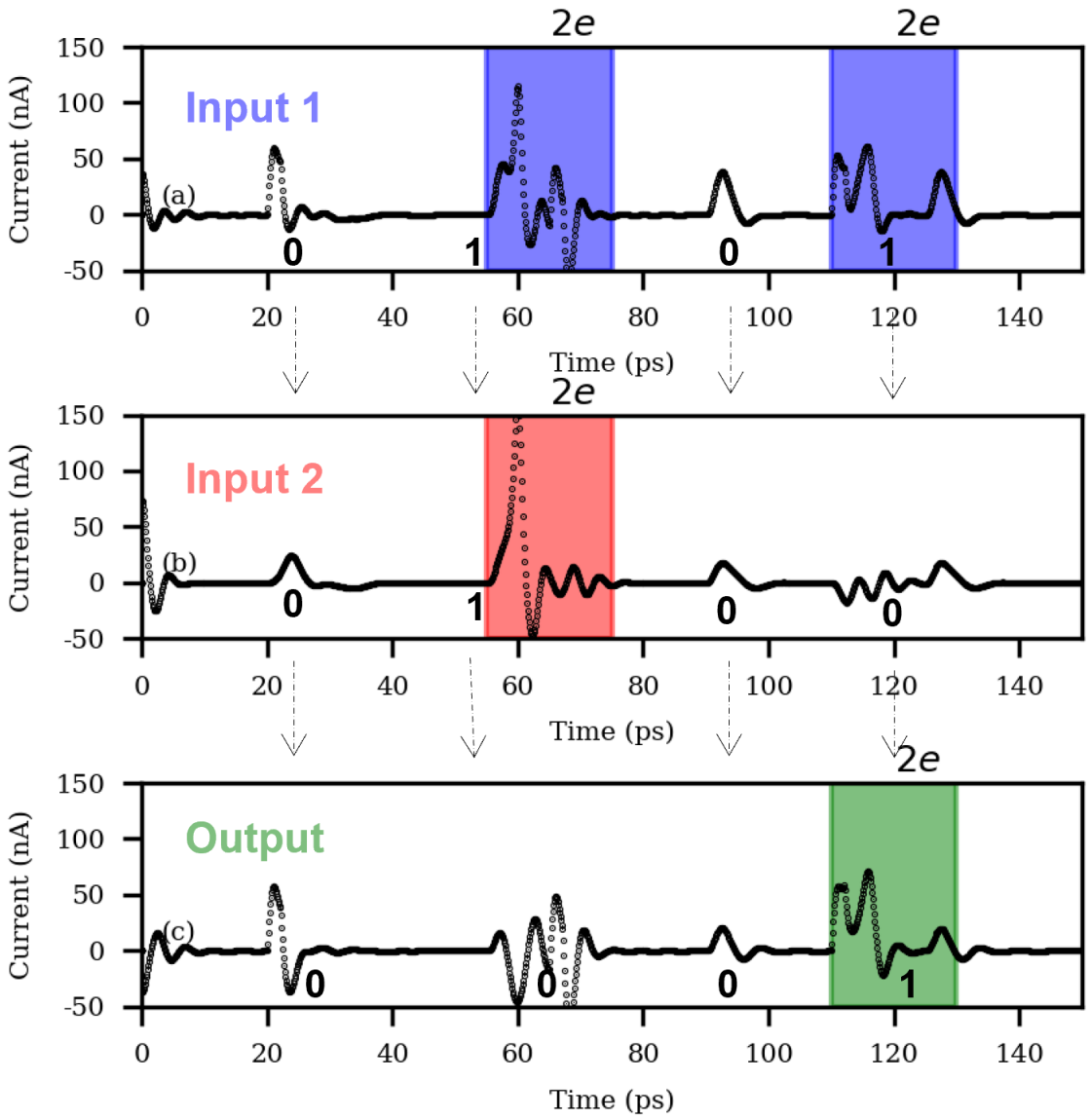


Figure 4.26: Simulation result of a two-input XOR gate shown in Figure 4.25. The critical voltages of junctions $Q1, Q4$ is 0.7 mV, $Q3, Q6$ is 1 mV and $Q2, Q5$ is 1.5 mV. Capacitance $C = 0.23$ fF, Voltage bias $V_b = 0.7$ mV and magnitude of the pulse input voltages V_{in1}, V_{in2} = 1.5 mV. (a) Input current pulses from $Q1$. (b) Input current pulses from $Q4$. (c) Output current pulses at node 4.

4.4.5 QPSJ Based Ring Oscillator

The logic blocks discussed in the previous section can be treated as the fundamental building blocks for the logic family being discussed. The elements of these blocks can be combined to form more complicated circuits. To illustrate this, an example of ring oscillator is implemented. Figure 4.35 shows the block diagram for the ring oscillator. This is based

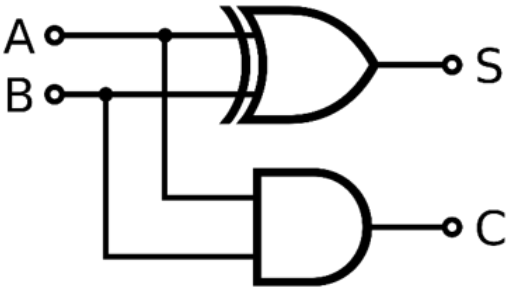


Figure 4.27: half-adder circuit schematic

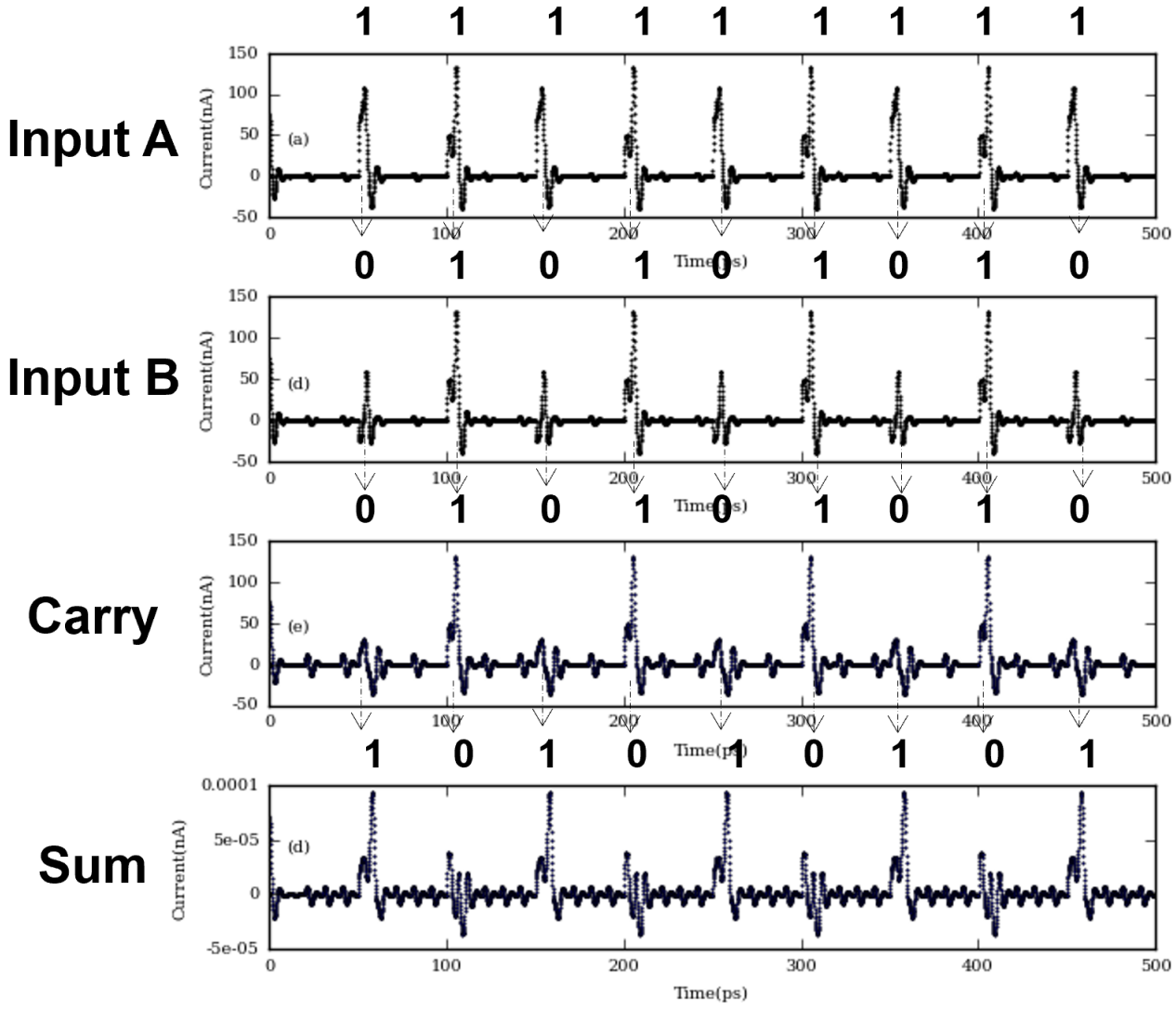


Figure 4.28: Simulation results of Half-adder using XOR and AND gates. (a) Input A. (b) Input B. (c) Sum (d) Carry.

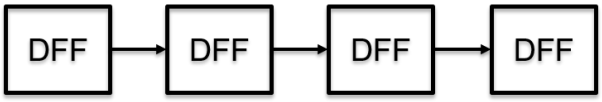


Figure 4.29: 4-stage shift register using D flip-flops.

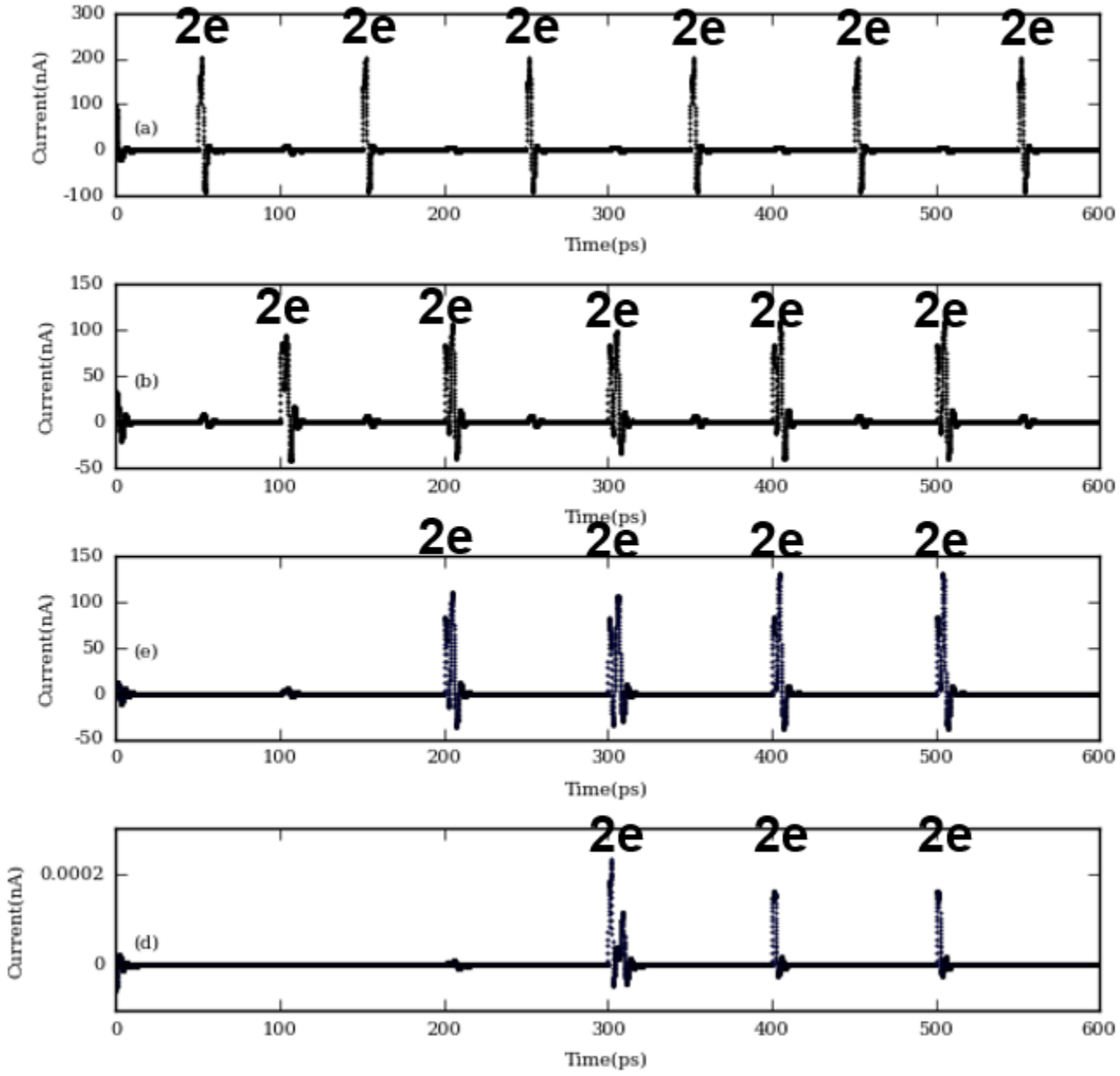


Figure 4.30: Simulation results of shift register. (a) Input data pulses. (b) Output after stage 1. (c) Output after stage 2. (d)Output after stage 3.

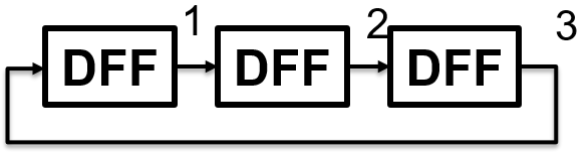


Figure 4.31: Ring counter using D flip-flops.

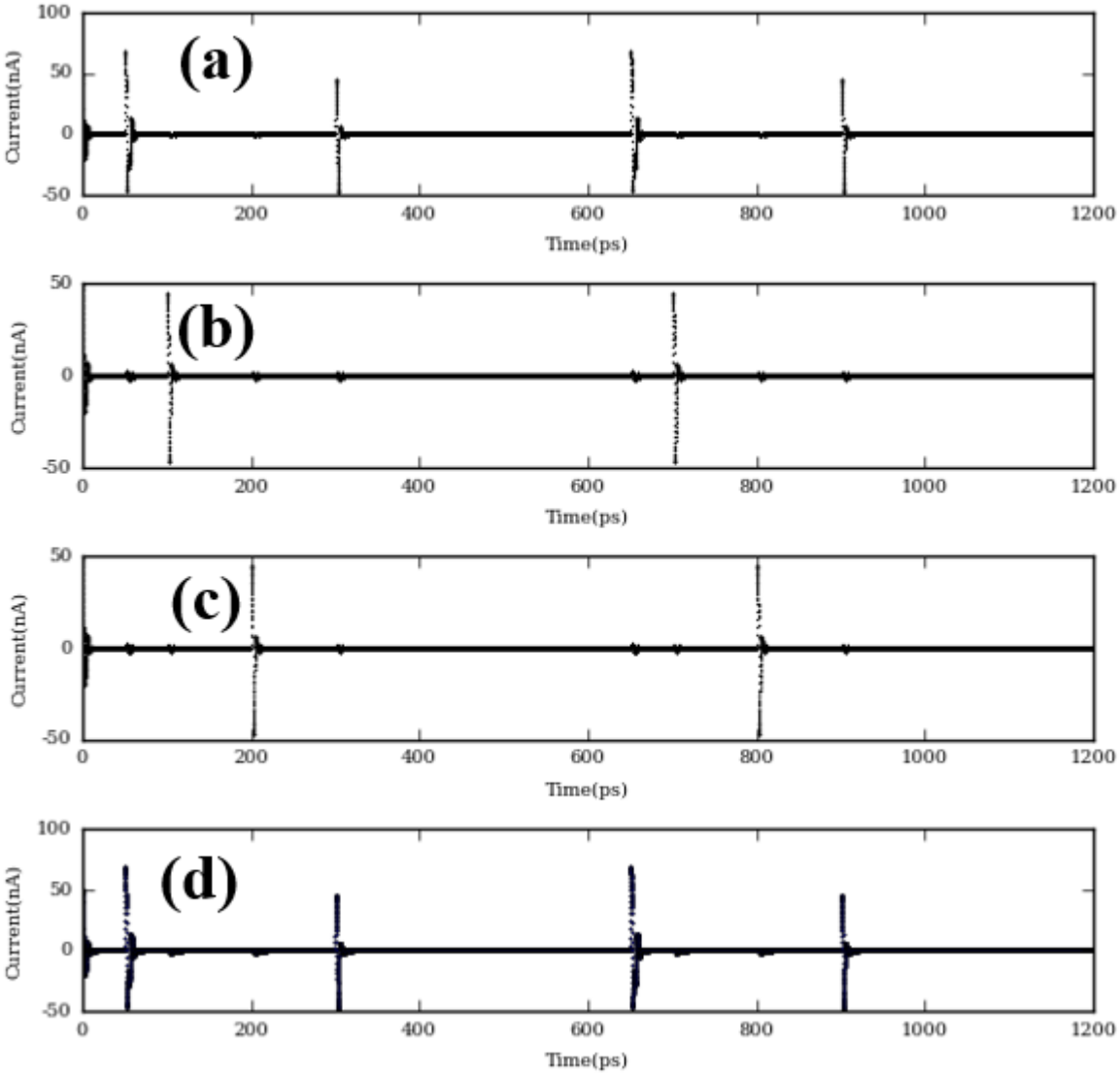


Figure 4.32: Simulation results of ring counter. (a) Output after stage 1. (b) Output after stage 2. (c) Output after stage 3. (d)Output after stage 4.

on Josephson junction based ring oscillator [104]. The corresponding simulation result with a single voltage pulse input triggering the oscillations in the ring is shown in Figure 4.36.

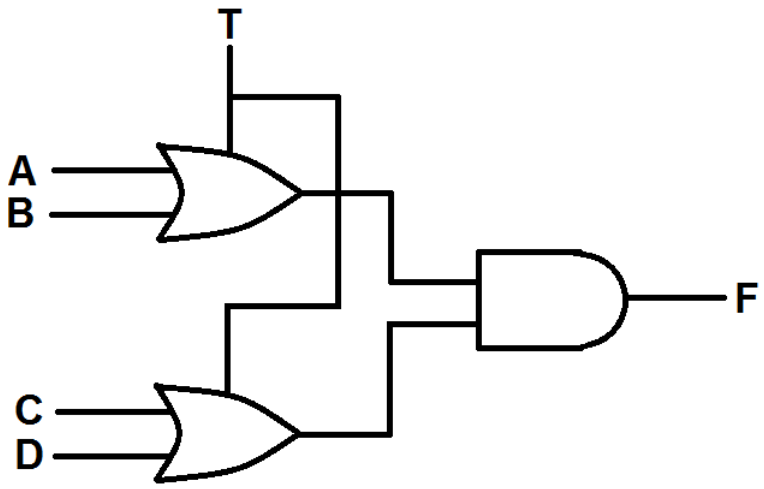


Figure 4.33: OR-AND logic circuit implementation.

4.5 Parameter Margin Analysis of Charge-based Logic Circuits

Quantum phase-slip junctions, because of their extremely small junction dimensions and parameters values like critical voltage, kinetic capacitance and voltage bias required for each island, can pose a challenge in circuit design if the parameter margins are small. Hence, worst case analysis of parameters of an island and a series of islands as that of a QPSJ transmission line has been performed to determine the feasibility of practical implementation charge-based logic circuits that are presented here. The margins are found to be up to 30% on parameters like normal resistance of the junction, kinetic capacitance and the series damping resistance, but only 10% on inductance and bias voltage. In several cases, adjusting the bias voltage is sufficient to make the circuit function as expected. The parameter margins depend on the circuit design and can vary, but in principle, the charge-based logic circuits can be designed have similar parameter margins as RSFQ based circuits. All the circuits that are presented here have junction sizes and switching parameters in common, and therefore are therefore expected to have parameter margins of up to 30% on all their parameters except bias voltage and inductance of nano-wire.

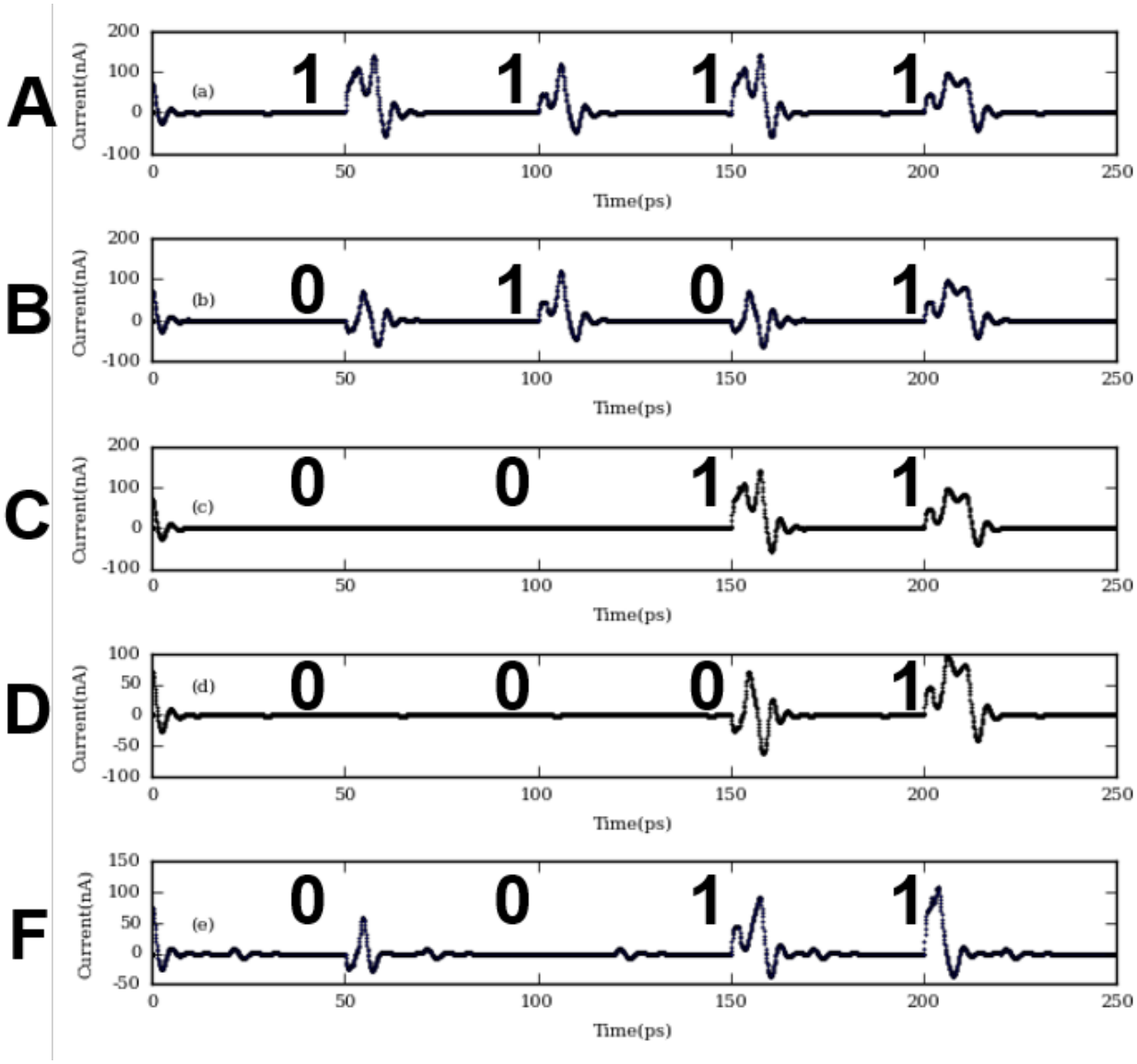


Figure 4.34: Simulation results of OR-AND gate. (a) Input A. (b) Input B. (c) Input C. (d) Input D. (e) Output F

4.6 Summary

Quantum phase-slip junctions provide an alternative way to implement logic circuits using superconductors that may have some advantages such as significant reduction in circuit complexity, supported by multiple ways to design logic circuits using voltage bias as opposed to current bias in JJ-based circuits, along with considerably lower power consumption compared to JJ based circuits. The building blocks of charge-based logic circuits have

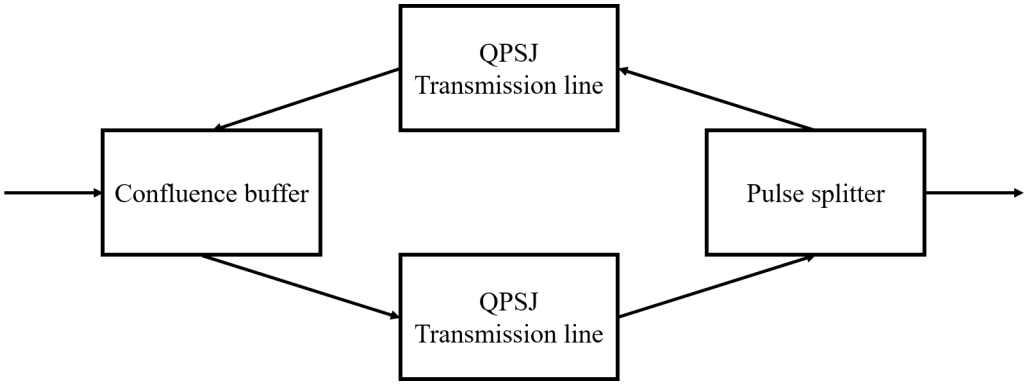


Figure 4.35: Block diagram of QPSJ based ring oscillator

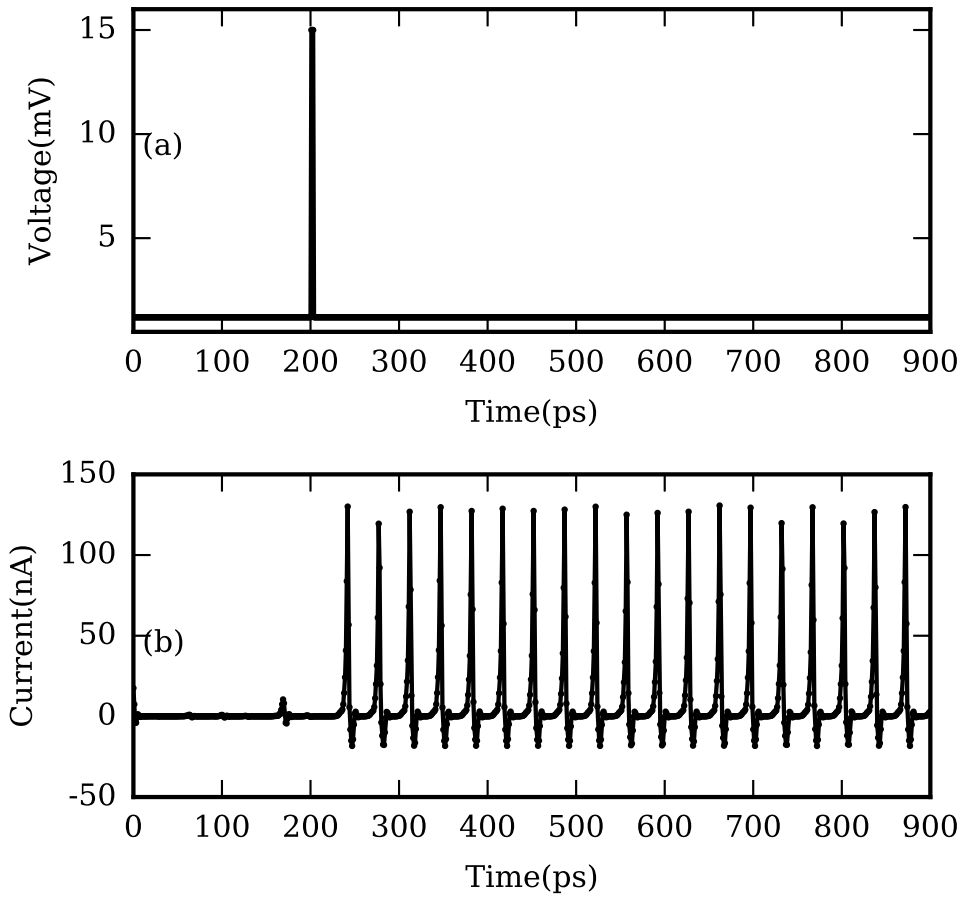


Figure 4.36: Simulation result of a ring oscillator

been demonstrated in simulations, along with examples of the developed logic gates using previously developed models to support these conclusions. However, there are several challenges to overcome, particularly in building and testing these junctions. These include

understanding the details of required materials and design principles required to control junction parameters to suit charge-based logic operation.

Chapter 5

Complementary quantum logic circuits using JJs and QPSJs

5.1 Introduction

In this chapter, we explore a new set of circuits, that incorporate both single-flux-quantum and quantized charge-based complementary quantum logic (CQL) circuits [105]. Therefore, the basic circuits comprise of circuits that convert single-flux quantum voltage pulses to quantized charge pulses and vice versa to simplify logic and integration operations of individual flux and charge based logic circuits. Additionally, CQL includes fan-out circuits that enable single flux input to several charge outputs, or a single-flux input to a charge and a flux output. Control gate circuit allows controlled switching operation in the form of a charge input controlling flux output. The operation of these circuits is demonstrated in simulations using WRSPICE. An XOR gate implementation is presented as an example to illustrate the operation of these circuits. The developed complementary quantum logic circuits show promise for higher power efficiency and simpler design in the form of fewer junctions for a given logic implementation, leading to the possibility of higher integration density.

5.2 Interface Circuits Between SFQ and Charge-based Logic Circuits

Complementary quantum logic circuits comprise of both the SFQ pulses encoded in a superconducting loop formed by two JJs and an inductor, as well as the quantized charge pulses encoded on a charge island formed by two QPSJs and a capacitor, as their basic building blocks. The following circuits employ these blocks and the corresponding signals generated, in achieving various operations that are essential in a digital logic family.

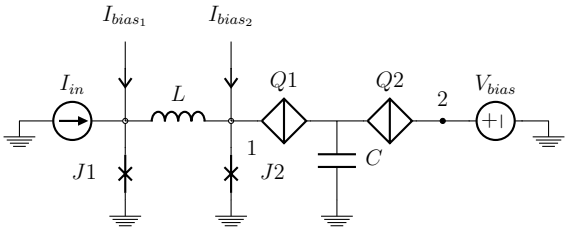


Figure 5.1: SFQ voltage pulse to quantized charge current pulse conversion circuit designed with an SFQ cell and a QPSJ charge island cell. $I_C(J1) = I_C(J2)$, $V_C(Q1) = V_C(Q2)$. DC bias $V_{bias} = 1.4V_C$. $I_{bias_1} = I_{bias_2} = 0.7I_C$.

5.2.1 Flux to Charge Conversion Circuit

The cells corresponding to SFQ loop and charge island can be used in a single circuit to realize flux to charge conversion. The resulting circuit is shown in Figure 5.1. The two identical JJs in the circuit are biased with currents that are 70% of their critical currents I_C and the two identical QPSJs are biased using a DC source V_{bias} with a value of 1.4 x critical voltage V_C of the junction. An input pulse current drives junction $J1$ to its resistive state generating a voltage pulse corresponding to a flux quantum in the loop formed by $J1$, L and $J2$, that subsequently switches $J2$. The critical voltage of the QPSJs are chosen such that the voltage pulse corresponding to flux quantum at $J2$ can sufficiently drive the QPSJ from its Coulomb blockade state to the conducting state, thereby generating a current pulse of constant area $2e$ at the output. Simulation results of this circuit showing input current pulse, voltage from SFQ loop and the output current pulse from $Q2$ are shown in Figure 5.2.

5.2.2 Charge to Flux Conversion Circuit

The reciprocal circuit of flux to charge conversion circuit shown in Figure 5.1 can be used for charge to flux conversion. The circuit schematic that can achieve such operation is shown in Figure 5.3, with the parameters identical to the circuit in Figure 5.1. The simulation results are shown in Figure 5.4. We note that the shape of the SFQ pulse output presented in Figure 5.4(c) is different from the shape of the SFQ pulse observed in Figure 5.2(b), but with equal areas (under the curve), each corresponding to single flux quantum. The difference in

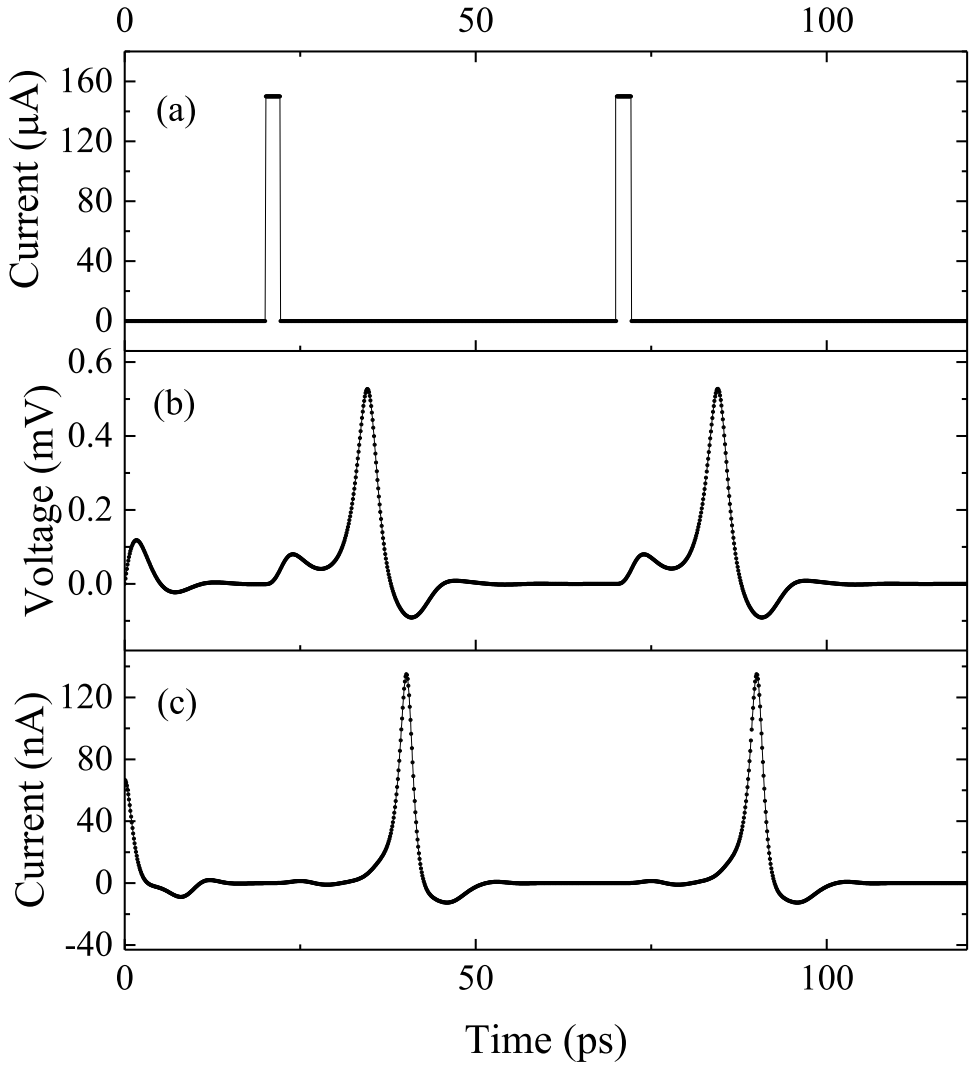


Figure 5.2: Simulation results of flux to charge conversion circuit shown in Figure 5.1. $I_C(J1, J2) = 100\mu$A, $V_C(Q1, Q2) = 0.7$mV, $L = 10.4$pH, $C = 0.23$pF. $V_{bias} = 1$mV. Magnitude of pulse input $I_{in} = 150\mu$A. (a) Input current pulses to $J1$ from I_{in}. (b) SFQ pulse output from SFQ loop formed by $J1$, $J2$ and L measured at node 1 of Figure 5.1. (c) Quantized charge output from the charge island formed by $Q1$, $Q2$ and C measured at node 2 of Figure 5.1.

shape occurs due to the differences in the current pulses (magnitude and duration) applied to the junctions $J1$ in each circuit. This also explains the different SFQ pulse shapes that will be shown in the various other circuits discussed in this chapter. Furthermore, the current pulse output from the charge island corresponding to quantized charge of $2e$ is not sufficient to switch large JJs of critical current of 100μA. Therefore, an input pulse of higher voltage

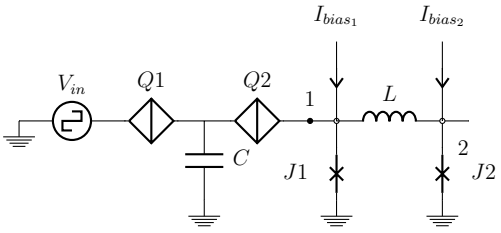


Figure 5.3: Quantized charge current pulse to SFQ voltage pulse conversion circuit designed with an SFQ cell and a QPSJ charge island cell. $I_C(J1) = I_C(J2)$, $V_C(Q1) = V_C(Q2)$. $I_{bias_1} = I_{bias_2} = 0.7I_C$.

amplitude is used to generate a charge pulse corresponding to ∼1000 Cooper pairs, which is sufficient to induce an SFQ pulse at the output for circuit components with the specified parameters. Preliminary simulation results show that, in order to generate a single SFQ pulse output with only a single Cooper pair pulse input, a JJ with a considerably smaller critical current (i.e. up to a few micro-amperes) and a QPSJ with a larger critical voltage (i.e. several hundred milli-volts) are necessary. Practical realization of similar circuits may be challenging with existing technologies, but may be possible with the development of suitable devices or circuits (i.e., with QPSJ-based current amplification). We note that circuits such as these can assist with moving information forward in digital circuits.

5.3 Fan-out Circuits

Fan-out circuit schematic is useful to drive several gates with charge/flux input connected to a flux/charge outputs. Conversion from flux to charge and vice versa enables using a single input to drive several outputs without decrease in the pulse amplitudes. Furthermore, it is possible to split the input to either charge or flux output in the same circuit. These two operations are demonstrated in the circuits below.

5.3.1 SFQ Input Splitter to Multiple Quantized Charge Outputs

The circuit shown in Figure 5.5 can be used to split an SFQ pulse input to three quantized charge outputs. This operation can be extended to a higher number outputs

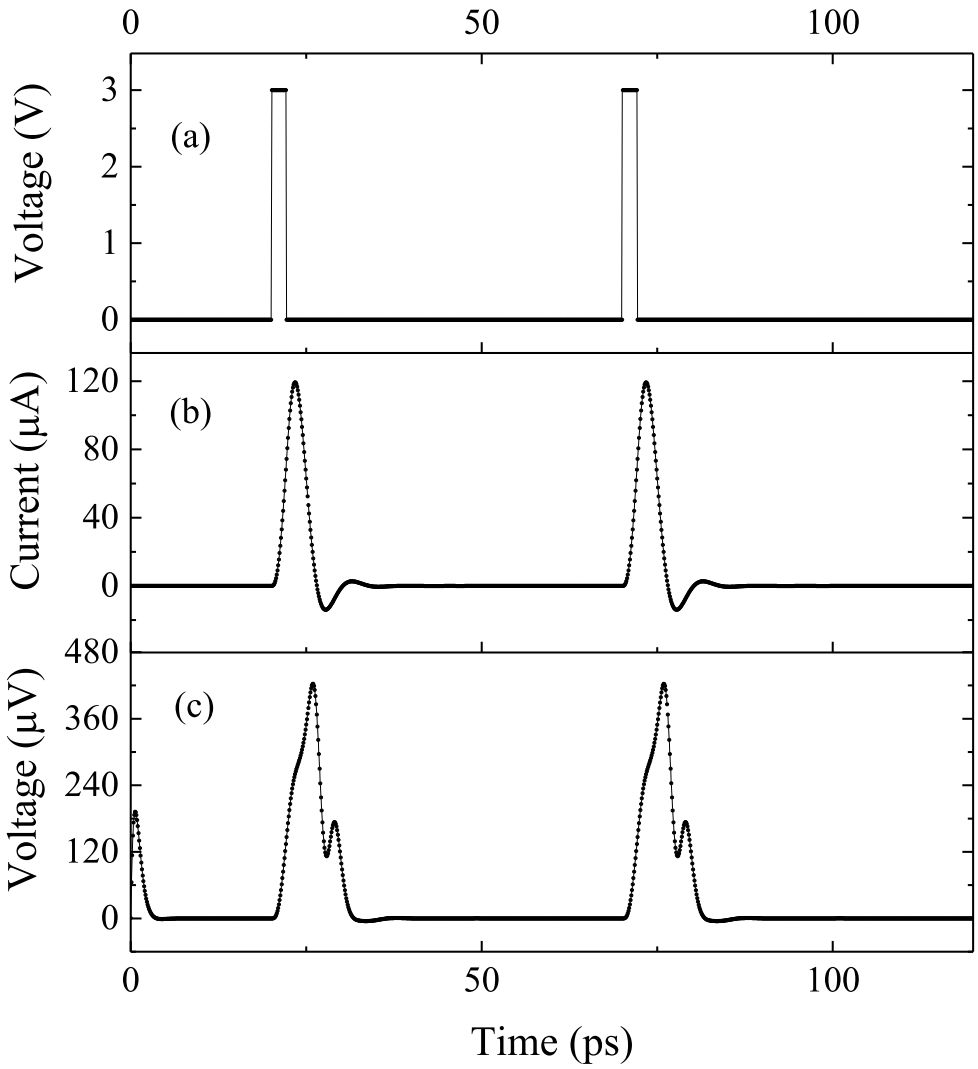


Figure 5.4: Simulation results of charge to flux conversion circuit shown in Figure 5.3. $I_C(J1, J2) = 100\mu$A, $V_C(Q1, Q2) = 0.7$mV, $L = 10.4$pH, $C = 0.23$pF. Magnitude of pulse input $V_{in} = 2.8$V. (a) Voltage pulse input to $Q1$ with high voltage amplitude from V_{in}. (b) Current pulse output from charge island formed by $Q1$, $Q2$ and C measured at node 1 of Figure 5.3. (c) Flux output from the SFQ loop formed by $J1$, $J2$ and L measured at node 2 of Figure 5.3.

by including more charge islands at the output of SFQ loop. Furthermore, there are no restrictions on the junction parameters irrespective of the number of outputs when the islands are biased with sufficient voltage. This is because the voltage drop at node 1 of Figure 5.5 due to leakage current through connected charge islands is negligible. The simulation results of the circuit shown in Figure 5.5 are shown in Figure 5.6. The reciprocal circuit operation,

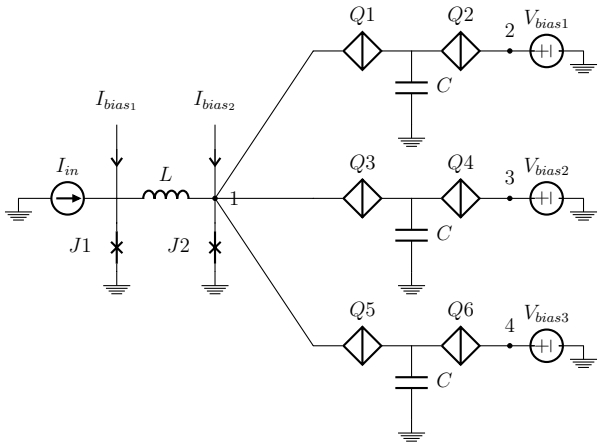


Figure 5.5: A single SFQ input to three quantized charge outputs with loop and island circuit parameters identical to that of Figure 5.1. $I_C(J1) = I_C(J2)$, $V_C(Q1) = V_C(Q2) = V_C(Q3) = V_C(Q4) = V_C(Q5) = V_C(Q6)$. DC bias $V_{bias1} = V_{bias2} = V_{bias3} = 1.4V_C$. $I_{bias_1} = I_{bias_2} = 0.7I_C$.

i.e. from charge input to several flux outputs is possible provided the critical currents of JJs are significantly lower (i.e. on the order of a few micro-amperes). Practical realization may be challenging with present technologies, as mentioned in Section II.B., without internally amplifying the charge input.

5.3.2 SFQ Input Splitter to SFQ and Charge Quantum Output Splitter

The circuit shown in Figure 5.7 can be used to split a single SFQ pulse input to an SFQ pulse output and a quantized charge pulse output. Simulations results illustrating this operation are shown in Figure 5.8.

5.4 Switching and Logic Circuits for CQL Family

5.4.1 Control gate

The signal flow to the output of the conversion circuits can be controlled using a signal input through a QPSJ similar to control/buffer circuit from [96] resulting in a similar operation. An example control circuit is shown in Figure 5.9. The JJs $J1, J2$, QPSJs $Q2, Q3$,

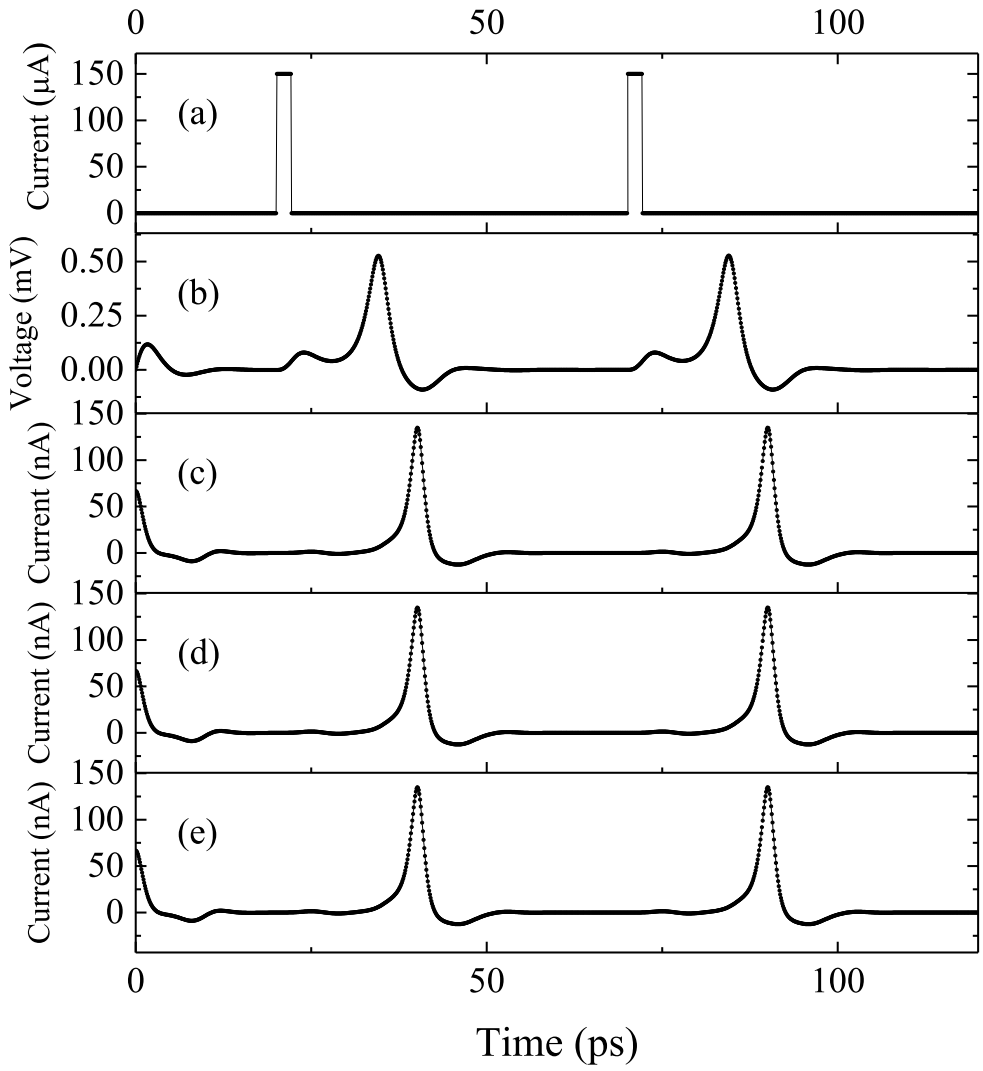


Figure 5.6: Simulation results of fan-out circuit shown in Figure 5.5. $I_C(J1, J2) = 100\mu$A, $V_C(Q1, Q2, Q3, Q4, Q5, Q6) = 1$mV, $L = 10.4$pH, $C = 0.23$pF. $V_{bias1} = V_{bias2} = V_{bias3} = 0.7$mV. (a) Current input to the SFQ loop formed by $J1$, $J2$ and L from I_{in}. (b) SFQ voltage pulse output from the loop formed by $J1$, $J2$ and L measured at node 1 of Figure 5.5. (c) Output at the charge island formed by $Q1$, $Q2$ and C measured at node 2 of Figure 5.9. (d) Output at the charge island formed by $Q3$, $Q4$ and C measured at node 3 of Figure 5.9. (e) Output at the charge island formed by $Q5$, $Q6$ and C measured at node 4 of Figure 5.9.

along with the inductor L and capacitor C together form the flux to charge conversion circuit shown in Figure 5.1. An additional QPSJ $Q1$ is included along with a step input for switch operation. The critical voltage of $Q1$ is lower than that of $Q2$ and $Q3$, with all other

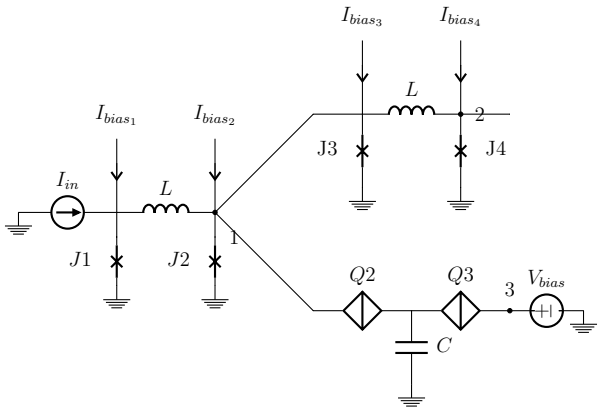


Figure 5.7: A fan-out circuit with single SFQ pulse input with two outputs corresponding to SFQ pulse and quantized charge pulse respectively. $I_C(J1) = I_C(J2) = I_C(J3) = I_C(J4)$, $V_C(Q1) = V_C(Q2)$. DC bias $V_{bias1} = 1.4V_C$. $I_{bias_1} = I_{bias_2} = I_{bias_3} = I_{bias_4} = 0.7I_C$.

parameters used in the circuit identical to that of Figure 5.1. When the input V_{in} is high, the SFQ pulse from $J2$ switches junction $Q1$ before junction $Q2$, resulting in no current pulse at the output. When the input V_{in} is low, the SFQ pulse from $J2$ switches $Q2$, resulting in flux to charge conversion. Simulation results illustrating this operation are shown in Figure 5.10. Similar operation can be implemented with charge to flux conversion circuit.

5.4.2 XOR Gate

A two input XOR gate can be implemented using two flux to charge conversion circuits combined with control gates in parallel. Four inputs are applied to the SFQ cells at junctions $J1$ and $J3$, and at the junctions $Q1$ and $Q4$. The input 1 at junction $J1$ and the input at $Q4$ are high at the same time, and the input 2 at $J3$ and the input at $Q1$ are high at the same time. This is illustrated in the circuit shown in Figure 5.11, and the corresponding simulation results are shown in Figure 5.12. During practical implementation, same input signals can be used in these cases with appropriate charge/flux conversion circuits. When both the inputs are '1', QPSJs $Q1$ and $Q4$ are switched, therefore the signals generated in both SFQ cells do not travel into the QPSJ charge islands. This results in the output '0'. When only one of the inputs is '1', the SFQ pulse generated in the JJ corresponding to that input is converted to quantized charge at the corresponding island, generating the output

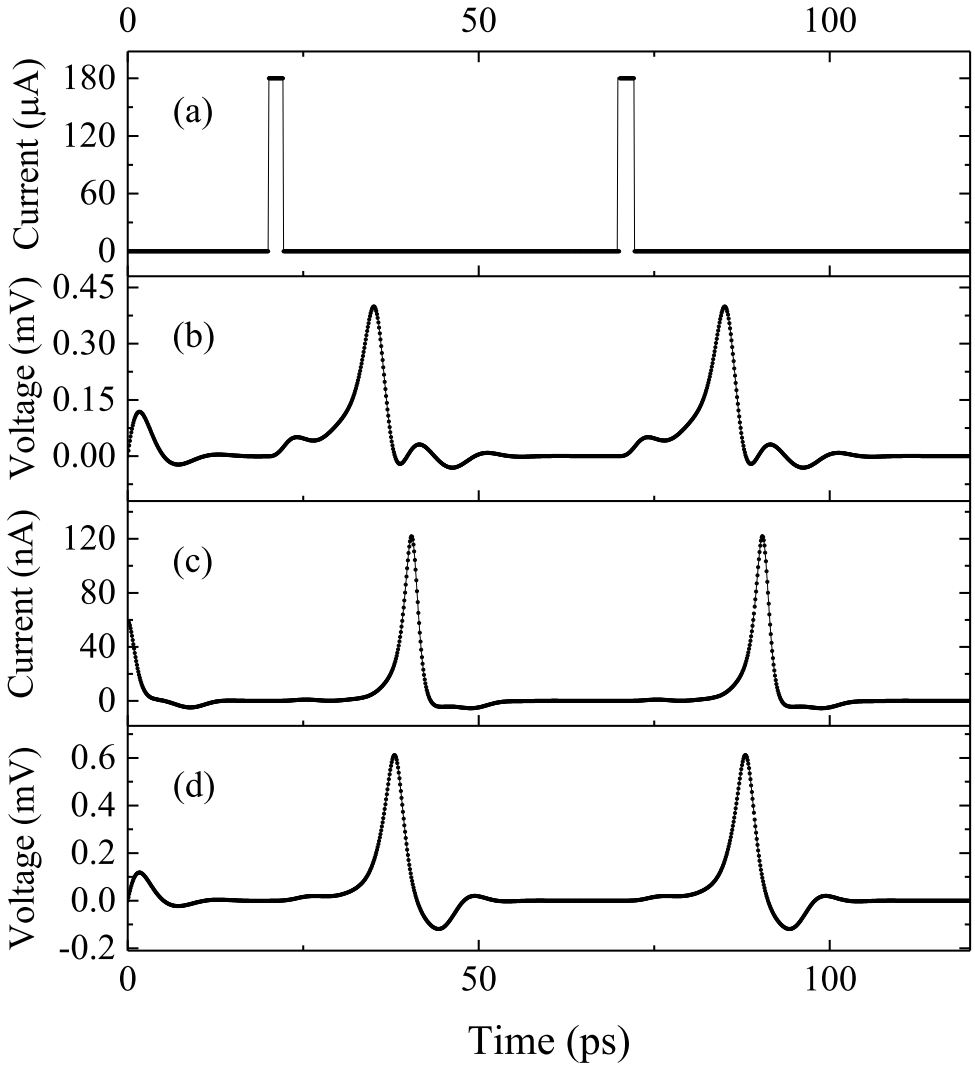


Figure 5.8: Simulation results of fan-out circuit shown in Figure 5.7. $I_C(J1, J2, J3, J4) = 100\mu$A, $V_C(Q1, Q2) = 0.7$mV, $L = 10.4$pH, $C = 0.23$pF. $V_{bias1} = 1$mV. (a) Current input to the SFQ loop formed by $J1$, $J2$ and L from I_{in}. (b) SFQ voltage pulse output from the loop formed by $J1$, $J2$ and L measured at node 1 of Figure 5.7. (c) Output at the charge island formed by $Q1$, $Q2$ and C measured at node 2 of Figure 5.7. (d) Output at the SFQ loop formed by $J3$, $J4$ and L measured at node 3 of Figure 5.7.

'1'. The output is '0' when both the inputs are '0', as none of the junctions are switched, resulting in no SFQ pulses.

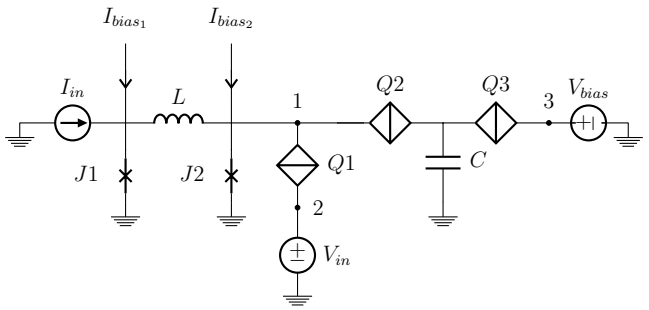


Figure 5.9: Control circuit formed by including an additional QPSJ $Q1$ at the output of SFQ loop with a pulse voltage input. $I_C(J1) = I_C(J2)$, $V_C(Q2) = V_C(Q3) > V_C(Q1)$. DC bias $V_{bias} = 1.4V_C$. $I_{bias_1} = I_{bias_2} = 0.7I_C$.

5.5 Discussion

CQL circuits provide an a new way to perform digital logic operations in superconducting electronics that are predominantly based on JJs alone, by utilizing QPSJs, with some potential advantages. The charge islands formed by QPSJs can generate quantized charge pulses that are similar to SFQ pulses, but the switching energy of QPSJs to generate a current pulse is estimated to be order of 1-5 zJ. This is considerably smaller than that of currently available JJ technologies which dissipate energy in the order of several aJ. Using JJs and QPSJs together enables convenient fan-out to multiple outputs without a loss of output signal amplitude, in addition to requiring fewer junctions to implement a logic operation compared to JJ-based circuits.

Although CQL circuits may provide significant advantages, challenges exist in practical realization of these circuits, pertaining to the material and design of QPSJs for controlled generation of quantum-phase slips in nano-wires, along with a possible need for lower operating temperatures (perhaps below 1 K). Other potential issues exist such as interference of charge noise with the charge on islands. The extent of these issues and possible solutions may only be evident after sufficient investigation through experiments.

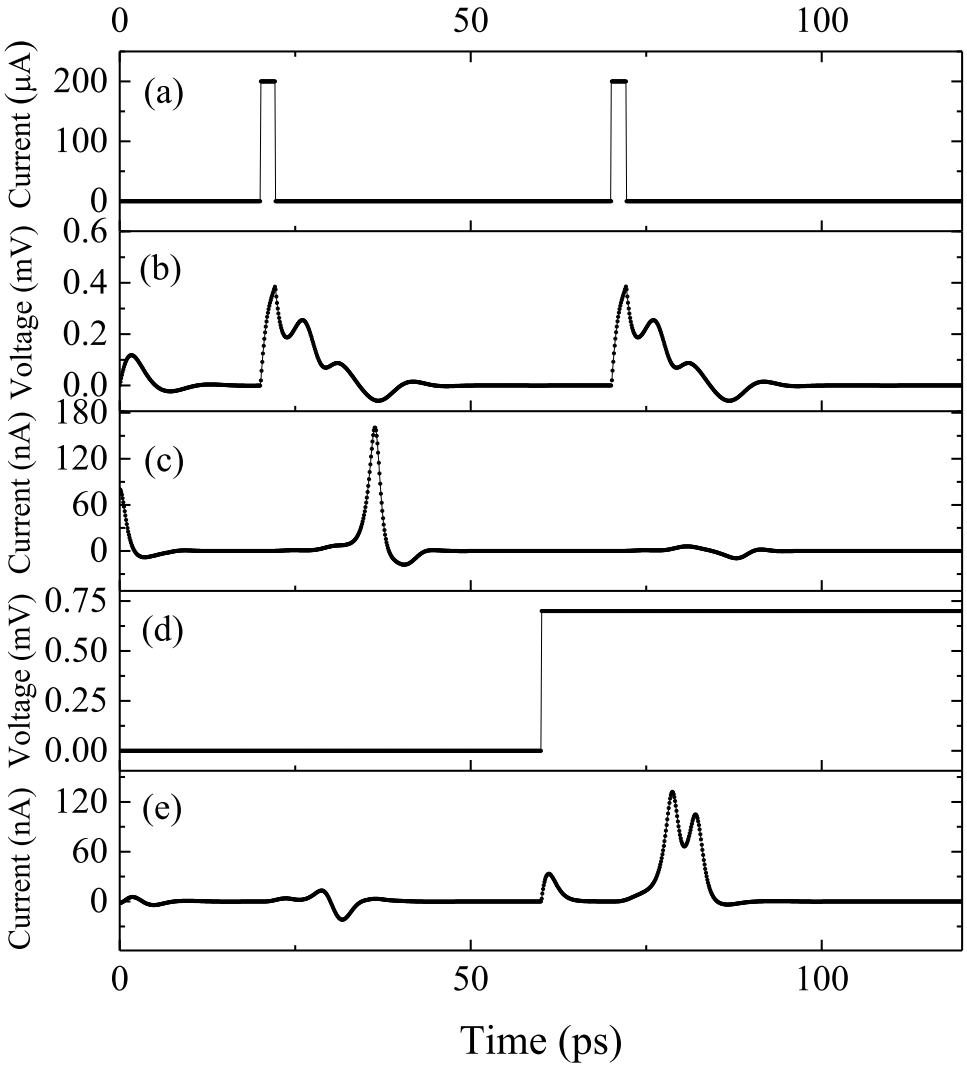


Figure 5.10: Simulation results of the control circuit shown in Figure 5.9. $I_C(J1, J2) = 100\mu$A, $V_C(Q2, Q3) = 1$mV, $V_C(Q1) = 0.5$mV, $L = 10.4$pH, $C = 0.23$pF. $V_{bias} = 1$mV. Magnitude of pulse input $I_{in} = 200$nA. (a) Current input to the SFQ loop formed by $J1$, $J2$ and L from I_{in}. (b) SFQ voltage pulse output from the loop formed by $J1$, $J2$ and L measured at node 1 of Figure 5.9. (c) Output at the charge island formed by $Q2$, $Q3$ and C measured at node 3 of Figure 5.9. (d) Voltage input V_{in} that controls the output current. (e) Current pulse through the QPSJ $Q1$ when V_{in} is high measured at node 2 of Figure 5.9.

5.6 Summary

A new family of circuits is introduced that combines the SFQ operation of JJs and quantized charge operation of QPSJ based circuits to perform digital logic. These circuits provide an alternative way to perform logic operations that may significantly simplify the

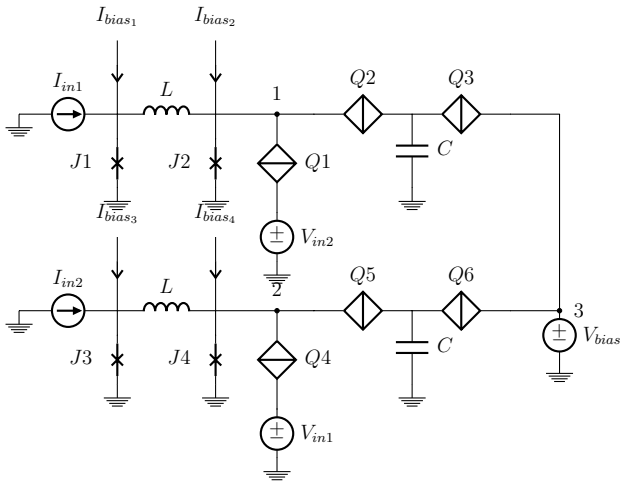


Figure 5.11: XOR gate operation achieved by introducing additional QPSJs $Q1$ and $Q4$ at the output of SFQ loops, with a pulse voltage input.

design when compared to JJ-based logic families, therefore may improve flexibility when these circuits are scaled to peta and exa-scale computers. Flux to charge conversion circuits and vice versa are presented that can be interfacing circuits between JJ and QPSJ based logic circuits. Logic operations such as an inverter and fan-out to multiple outputs are demonstrated as examples to illustrate the applications of these logic circuits. However, substantial developments in technology are required for physical realization of single QPSJs that exhibit these properties, as well as in testing the circuits discussed in this chapter.

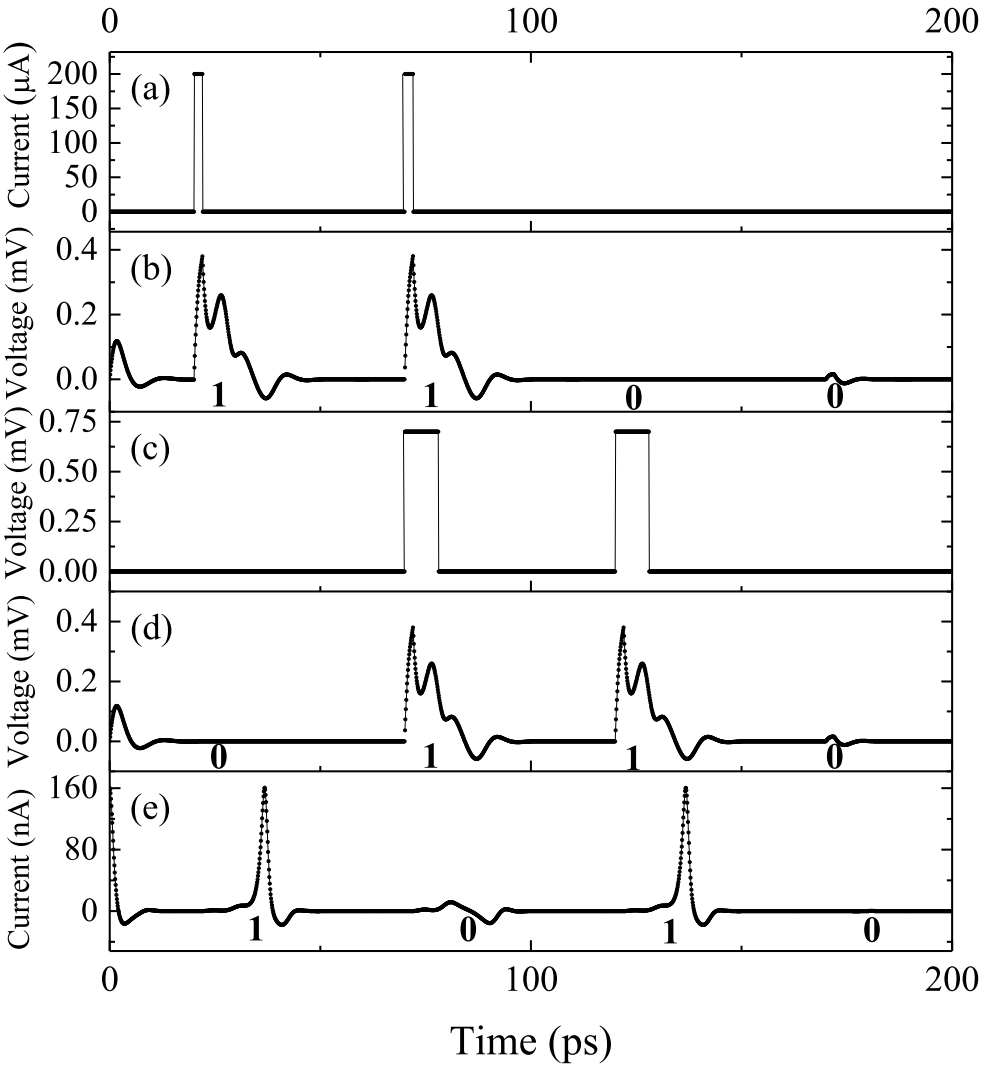


Figure 5.12: Simulation results of XOR gate shown in Figure 5.9. (a) Input current pulses I_{in1} to generate SFQ pulses in loop $J1$, L and $J2$. (b) Input 1 of XOR gate from SFQ loop $J1$, L and $J2$ measured at node 1 of Figure 5.11. (c) Input voltage pulse from V_{in2} to generate quantized charge pulses at $Q1$. (d) Input 2 of XOR gate from SFQ loop $J3$, L and $J4$ measured at node 2 of Figure 5.11. (e) Output of XOR gate as quantized charge current pulses from $Q3$ and $Q6$ measured at node 3 of Figure 5.11.

Chapter 6

Adiabatic quantum charge parametron circuits using JJs and QPSJs

6.1 Introduction

Quantum flux parametron [106], a Josephson junction (JJ) analog to the original parametron circuit [107] has been shown to perform logic operations with energy consumption on the order of thermal energy (k_BT), when operated adiabatically [4]. In this chapter, a parametron circuit has been developed using quantum phase-slip junctions (QPSJs) that has two degenerate ground states that are used as the two switching states of the binary logic system '0' and '1'. Here, a QPSJ-based parametron circuit is demonstrated in simulation, exhibiting operation that is a dual-operation of an adiabatic quantum flux parametron based on JJs. The circuit design is explained, along with useful parameters to operate it adiabatically. Potential energy calculations for this circuit show energy consumption on the order of k_BT at a temperature of 2 K, when appropriate circuit parameters are used. This is followed by circuit simulation results of various logic circuits that enable universal logic implementation. Comparison to quantum flux parametron shows possible faster circuit operation and lower energy consumption when charge parametron is used, therefore highlighting potential advantages.

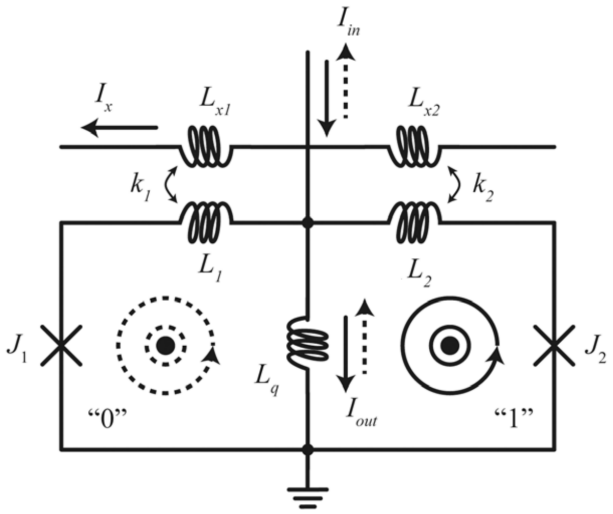
6.2 Quantum Charge Parametron Circuit

Figure 6.1 shows two different circuits that are duals to each other based on charge-flux duality. Figure 6.1(a) is the quantum flux parametron circuit used for adiabatic operation in [4] using JJs. Figure 6.1(b) is the dual circuit based on QPSJ. The T-junction formed

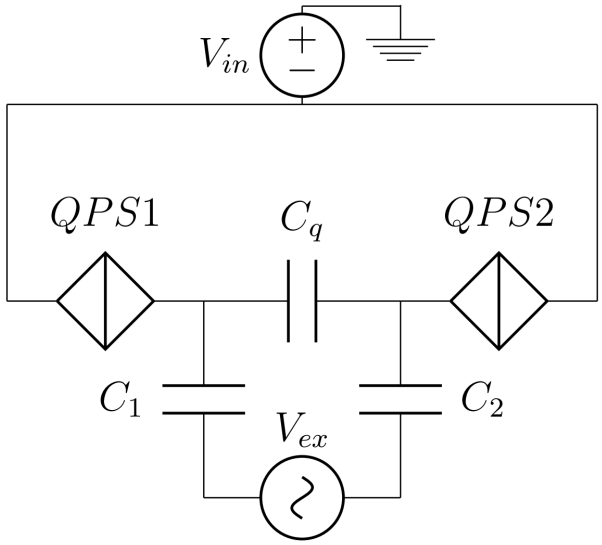
by inductors L_1, L_2 and L_q is replaced by the dual π-junction formed by capacitors C_1, C_2 and C_q. Similar to the excitation current source is coupled to inductors L_1 and L_2 in flux parametron, excitation voltage source is coupled to capacitors C_1 and C_2. The loops trapping flux formed by J_1, L_1, L_q and J_2, L_2, L_q are replaced by the islands trapping charge formed by QPS_1, C_1, C_q and QPS_2, C_2, C_q. Finally, the input current signal (I_{in}) parallel to both the loops is replaced by the input voltage signal (V_{in}) in series to both the islands. In the JJ parametron circuit, the excitation source is responsible in switching either of the JJs and creating a flux in loop. The JJ that is being switched depends on the polarity of the input signal. The input signal is typically very small i.e. of the order of $0.1I_c$, while the output current is higher than I_c (where I_c is the critical current of both the identical junctions). Similar to this circuit operation, the excitation source in charge parametron is responsible for generating charge tunneling on to either of the charge islands on C_1 and C_2, while the input voltage signal polarity determines the current direction. The two logic bits 0 and 1 in both the circuits is determined by the output current direction. In JJ parametron, the output current is the current through the inductor L_q, while in QPSJ parametron, the output current is the current in the loop formed by QPS_1, QPS_2 and C_q. It can be shown that, in both the circuits, it is possible to choose the parameters such as inductances/capacitances, excitation source magnitudes and frequencies, such that the switching between these logic states consumes energy less than the thermal energy limit k_BT at the operating temperature. This adiabatic operation enables reversible computing, therefore theoretically reducing the energy consumption for computing operation to zero, and is explained quantitatively for QPSJ charge parametron in the following sections.

6.3 Switching Energy of the Charge Parametron Circuit

In order to ensure that the circuit shown in Figure 6.1 has switching energy less than that of the thermal energy at the operating temperature, the circuit parameters must be tuned appropriately to establish two degenerate ground states, and during the switching, the energy



(a) Quantum flux parametron circuit with JJs [4]



(b) Quantum charge parametron with QPSJs

Figure 6.1: (a) Quantum flux parametron circuit with JJs [4] and (b) quantum charge parametron with QPSJs.

barrier between them is lowered to zero. This is possible by calculating the potential energy of the circuit and understanding the tunable parameters to tune the switching energy. A simplified potential energy of the QPSJ charge parametron is given by Equations 6.1 and 6.2. In these equations, the capacitors C_1 and C_2 of Figure 6.1(b) are considered as short. This simplification allows illustration of adiabatic operation. The complete circuit analysis will be shown in later circuits.

$$U_{QCP} = E_S[\frac{(q_{out} - q_{in})^2}{\beta_L} - 2cos(q_{out})cos(q_{ex})] \tag{6.1}$$

where,

$$\beta_L = 2C_q V_C(\frac{2\pi}{2e}) \tag{6.2}$$

q_{out} is the normalized output charge, q_{in} is the normalized input charge and q_{ex} is the normalized excitation charge and Es is the phase-slip energy. Therefore, the parameters that determine the adiabatic mode of circuit operation are the load capacitance C_q and the excitation and input charge magnitude. The potential energy normalized to the phase-slip energy can be plotted as a function of β_L and q_{ex}. In Figure 6.2, the potential energy as a function of normalized output charge is shown. It is shown that, a double potential well is formed corresponding to the two current directions, i.e. the two logic states of the circuit. The barrier between the potential wells determines the cost of switching from one logic state to another. The circuit is in either of the two lowest energy stable states while no switching is performed.

With the appropriate choice of C_q to make the parameter $\beta_L = 1$, the energy barrier can be brought down to zero enabling adiabatic switching. This is illustrated in Figure 6.3, where potential energy as a function of excitation and parameter β_L is shown.

Switching between logic states depends on the polarity of input voltage. The potential energy with input voltage is shown in Figure 6.4. A very small input voltage (of the order of $0.1V_C$, where V_C is the critical voltage of either of QPSJs) is necessary to perform switching operation. The input voltage creates an energy difference in both the logic states such that the lower energy state becomes more stable.

The energy dissipation and speed of operation of the circuit for both JJ and QPSJ based parametrons are compared. It can be shown that, for adiabatic operation, QPSJ parametron can be operated at higher operating speeds. Furthermore, QPSJ parametron consumes lower

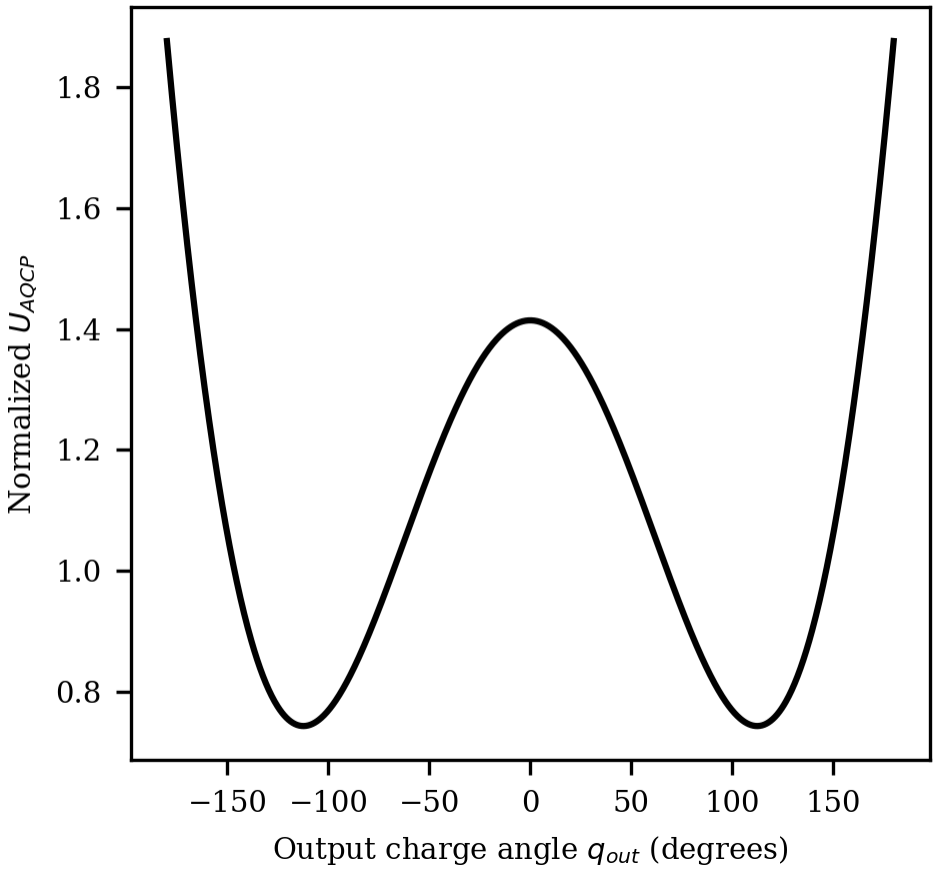


Figure 6.2: Potential energy of QPSJ charge parametron plot as a function of normalized output charge.

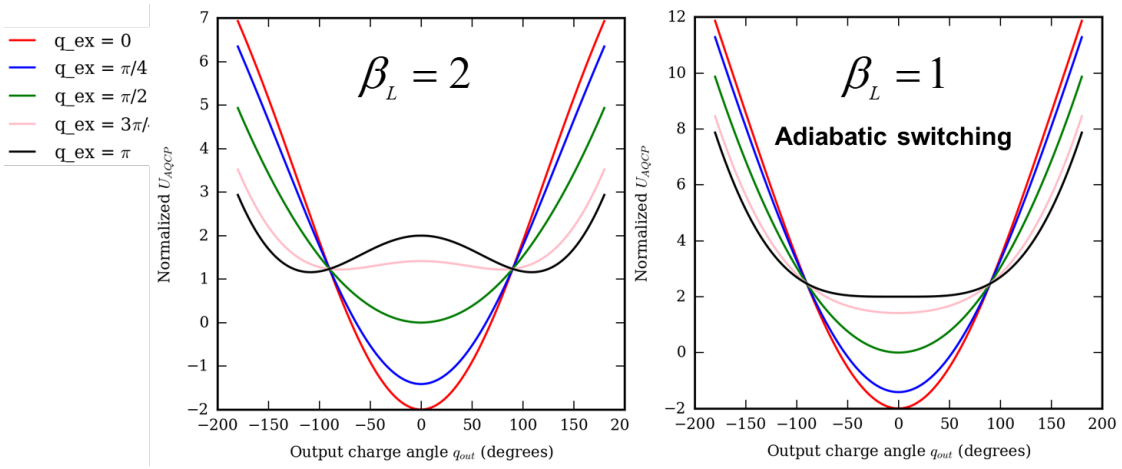


Figure 6.3: Potential energy of QPSJ charge parametron as a function of parameter β_L and normalized excitation charge illustrating adiabatic switching.

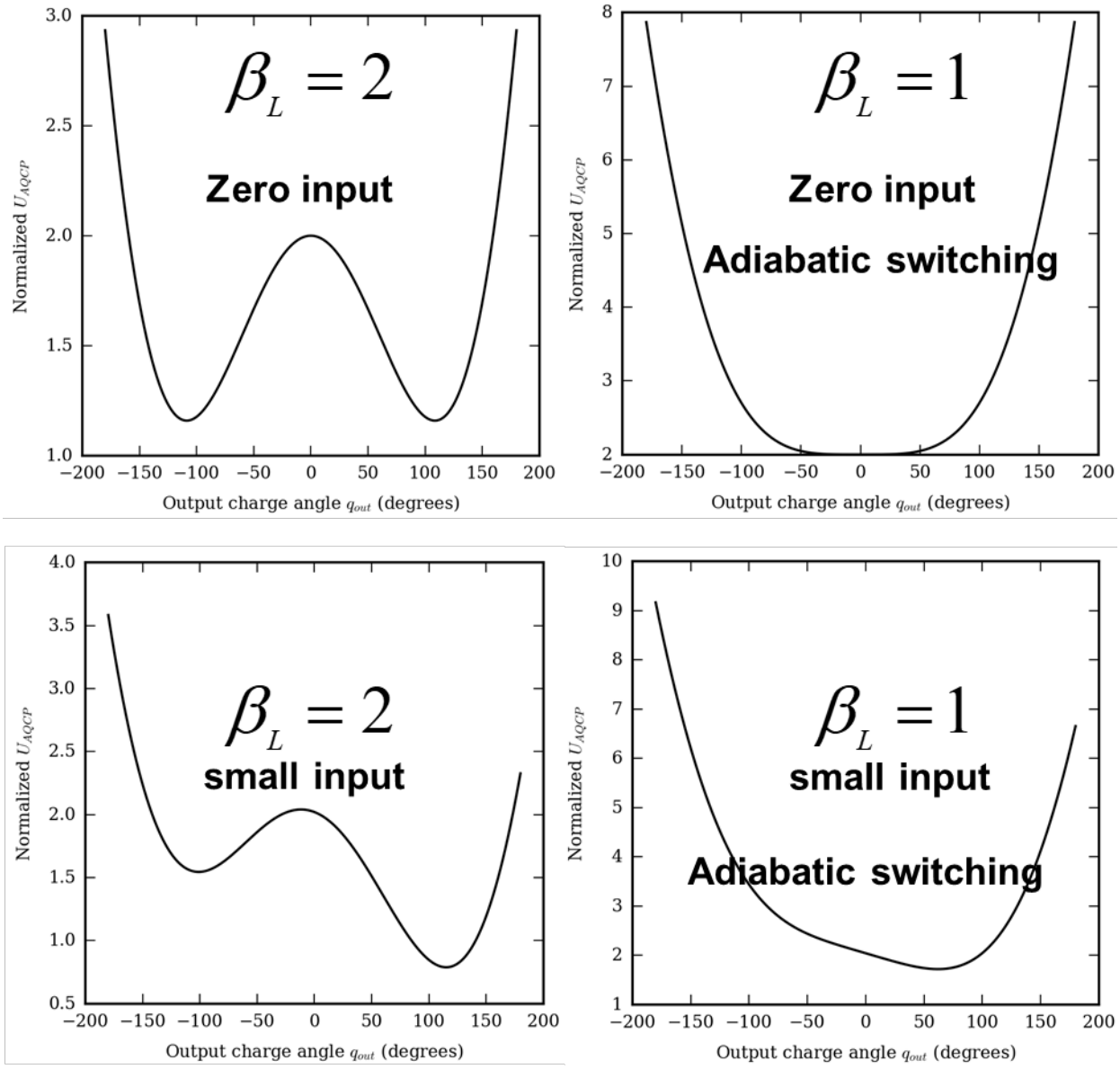


Figure 6.4: Potential energy of QPSJ charge parametron illustrating the effects of input voltage.

energy compared to JJ parametron. The comparison shown in Figure 6.5 is for the smallest junction sizes reported.

When the capacitors C_1 and C_2 are included in the potential energy equation, as parameters that can be chosen to obtain adiabatic operation, the potential energy equation is given by Equation 6.3.

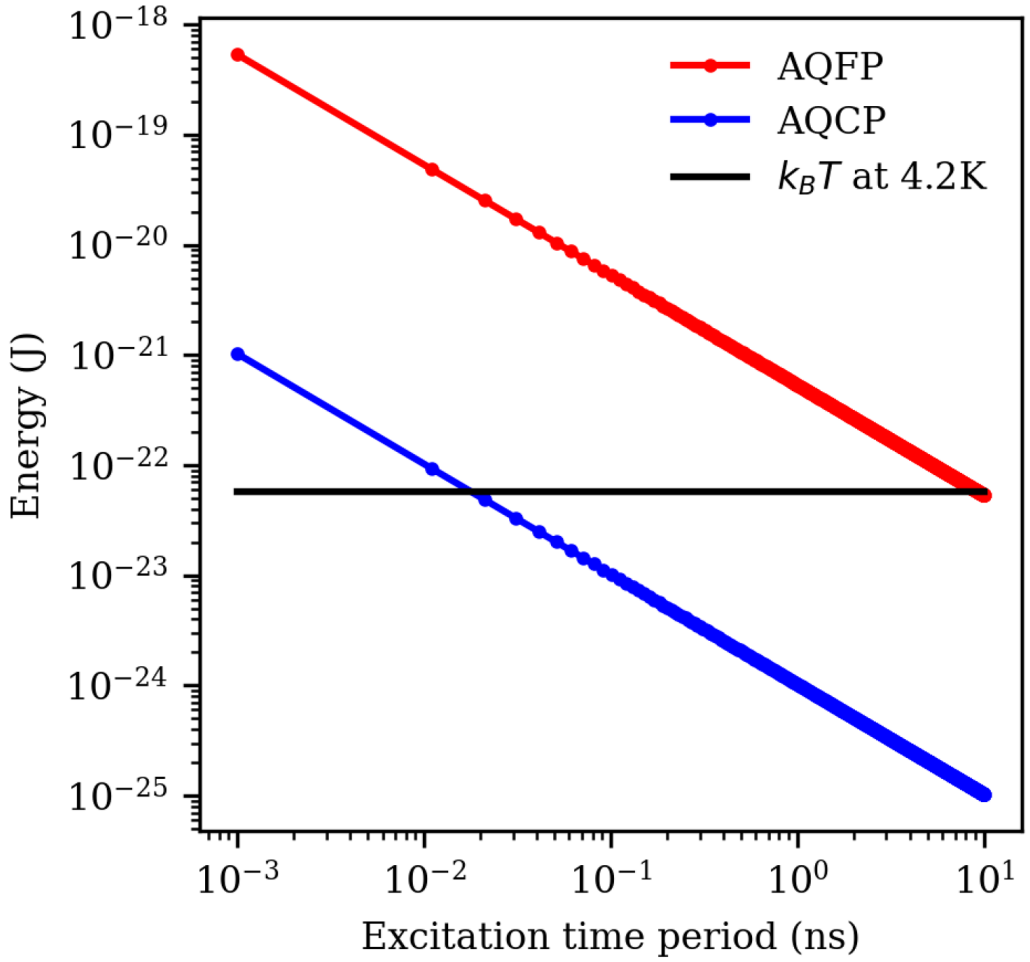


Figure 6.5: Energy consumption versus operating speed comparison of JJ and QPSJ based parametrons. Thermal energy at 4.2 K is shown. The operation below thermal energy is for adiabatic switching.

$$U_{QCP} = E_S[\frac{(q_{ex} - q_-)^2}{\beta_L} + \frac{(q_{in} - q_+)^2}{\beta_L + 2\beta_q} - 2cos(q_-)cos(q_+)] \tag{6.3}$$

where,

$$\beta_L = 2C_1V_C(\frac{2\pi}{2e}) \tag{6.4}$$

and,

$$\beta_q = 2C_qV_C(\frac{2\pi}{2e}) \tag{6.5}$$

$$q_+ = \frac{q_1 + q_2}{2} \tag{6.6}$$

$$q_- = \frac{q_1 - q_2}{2} \tag{6.7}$$

6.4 Circuit Designs and Simulations

The circuit shown in Figure 6.1(b) is simulated with the following parameters. QPS_1, QPS_2: V_C: 400 μV, R_n: 1 kΩ, L: 10 nH. C_1, C_2: 0.228 fF, C_q: 0.5 fF, V_{in}: 200 μV, V_{ex}: 200 μV magnitude, 250 ps period. The simulation results of the circuit is shown in Figure 6.6. Input (+1) implies V_{in}: +200 μV and input (-1) implies V_{in}: -200 μV. Input is DC in this simulation. When input is (+1), the corresponding output current is positive. The current pulses are only seen during positive cycle of excitation, with zero current when excitation is negative. When the input is (-1), the output current is negative. This cell can be configured to form an inverse majority logic gate. Majority logic gate is a reversible gate, therefore satisfying conditions suitable for reversible computing. These conditions include logical and physical reciprocity, i.e. the input logic state can be achieved when the output is injected into the input/output of an identical inverse majority gate.

Figure 6.6: Simulation results of a QPSJ charge parametron cell shown in Figure 6.1.

The majority gate schematic is shown in Figure 6.7. It is identical to the basic QPSJ charge parametron but has three voltage input signals in series.

NAND and NOR operation of inverse majority gate simulations are shown in Figure 6.8 below. Tables 6.1 and 6.2 show the truth tables for the operation.

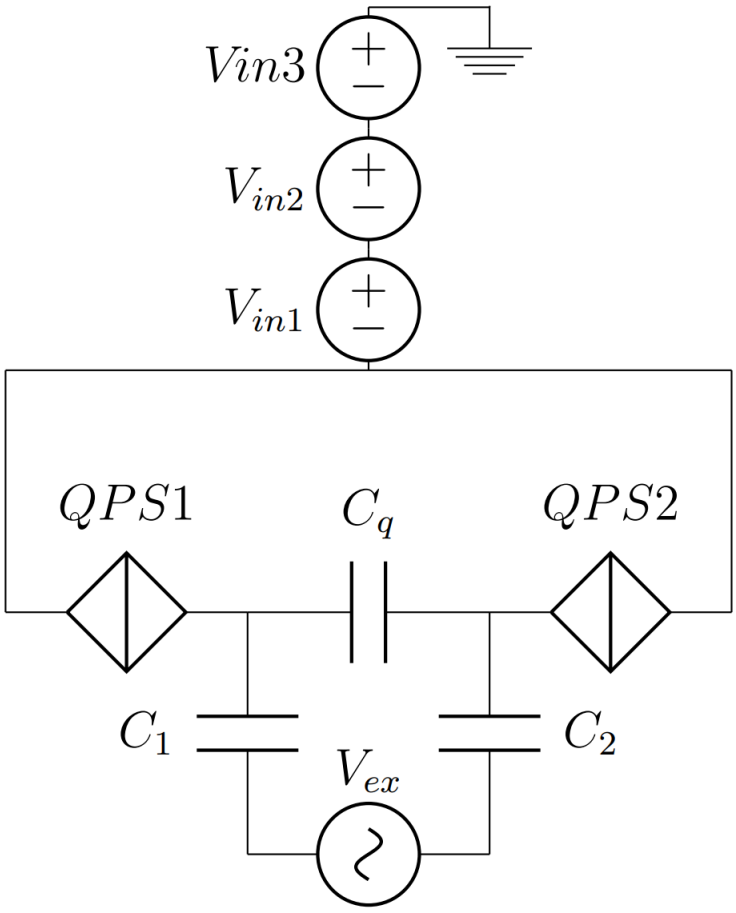


Figure 6.7: 3-input inverse majority gate using QPSJ charge parametron circuit.

In1	In2	In3	Out
1	1	1	-1
1	-1	1	-1
-1	1	1	-1
-1	-1	1	1

In1	In2	In3	Out
1	1	-1	-1
1	-1	-1	1
-1	1	-1	1
-1	-1	-1	1

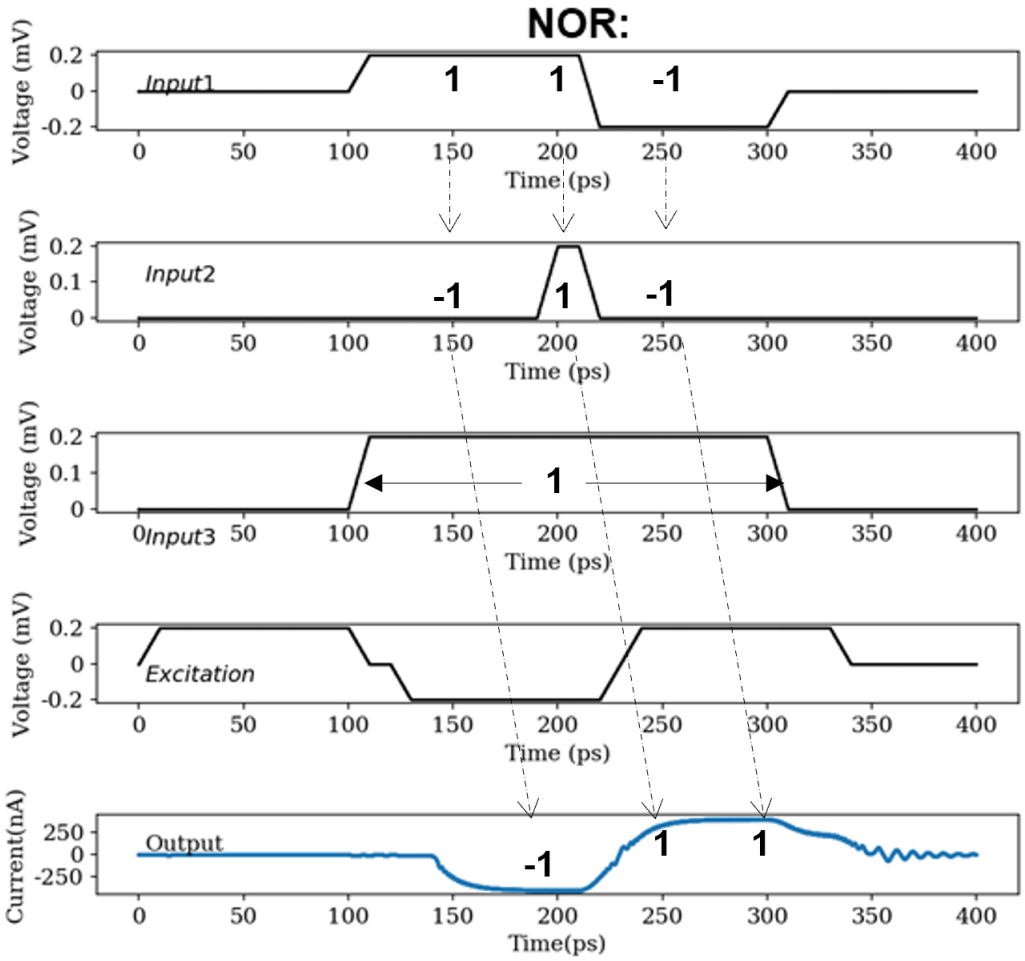


Figure 6.8: NOR operation using inverse majority gate according to tables 1 and 2.

6.5 Switching Energy of the Parametron Circuit

The future work mainly includes optimizing the circuit operation by tuning the circuit parameters to achieve adiabatic mode of operation. This involves tuning the parameters $beta_L$ and β_q of equations 6.4 and 6.5 respectively. For adiabatic operation of the charge parametron circuit, the switching energy must be below the thermal energy k_BT, i.e. $4x10^{-23}$ J. The bit energy of the current circuit can be estimated from simulations as shown in Figure 6.10 below. A single cycle of the excitation voltage and current are integrated, and the energy is calculated below:

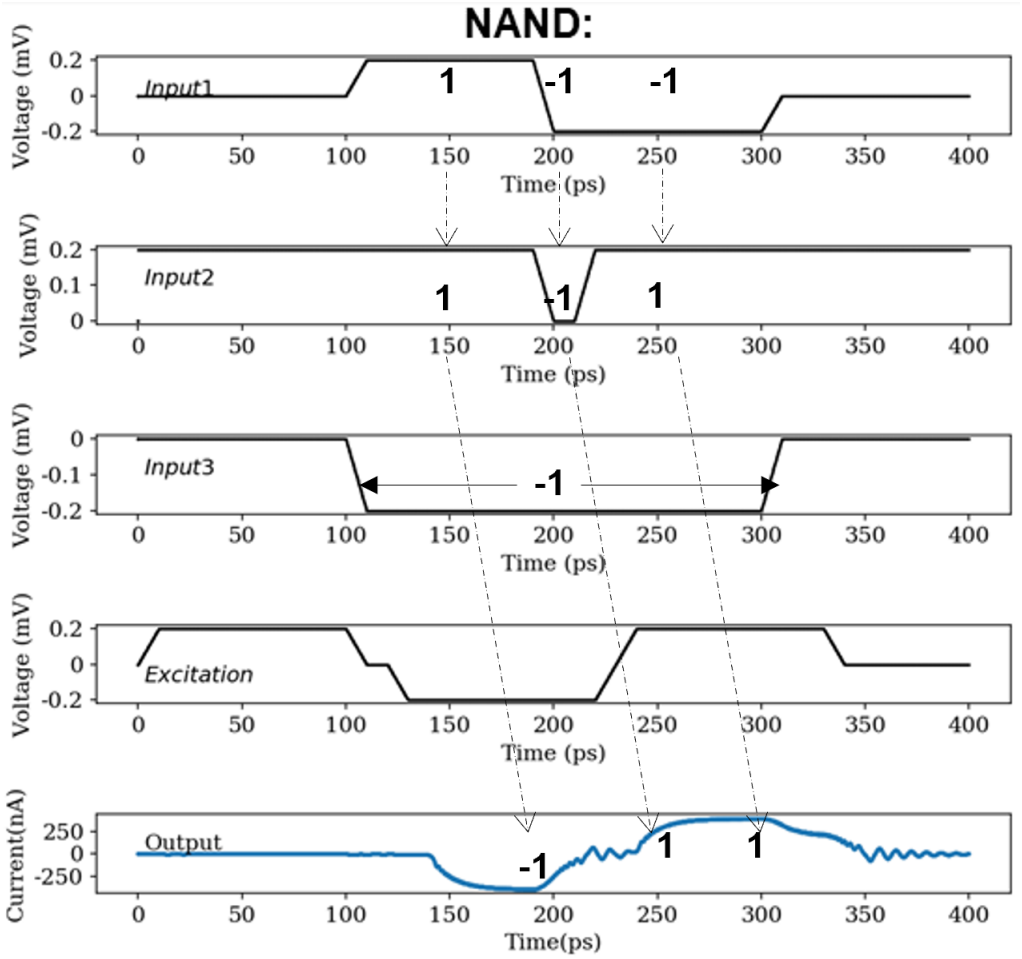


Figure 6.9: NOR operation using inverse majority gate according to tables 1 and 2.

$$E_{QCP} = \frac{1.99x10^{-14})(3.67x10^{-17})}{100x10^{-12}} = 7.34x10^{-21} per\, bit \tag{6.8}$$

The calculated energy per bit is for the clock at a frequency of 10 GHz, without any optimization to achieve adiabatic operation. The switching energy will be further reduced by tuning junction parameters, the Beta parameters and clock speed. Furthermore, this report outlines the operation of a single cell of charge parametron circuit family and its corresponding logic circuits. Therefore, it is necessary to demonstrate circuit operation of several single cells together, to show that this technology is scalable. Future work involves identifying suitable circuit schematics to couple several charge parametron circuits and logic gates to show that the output from a single cell can be used to drive the adjacent cell.

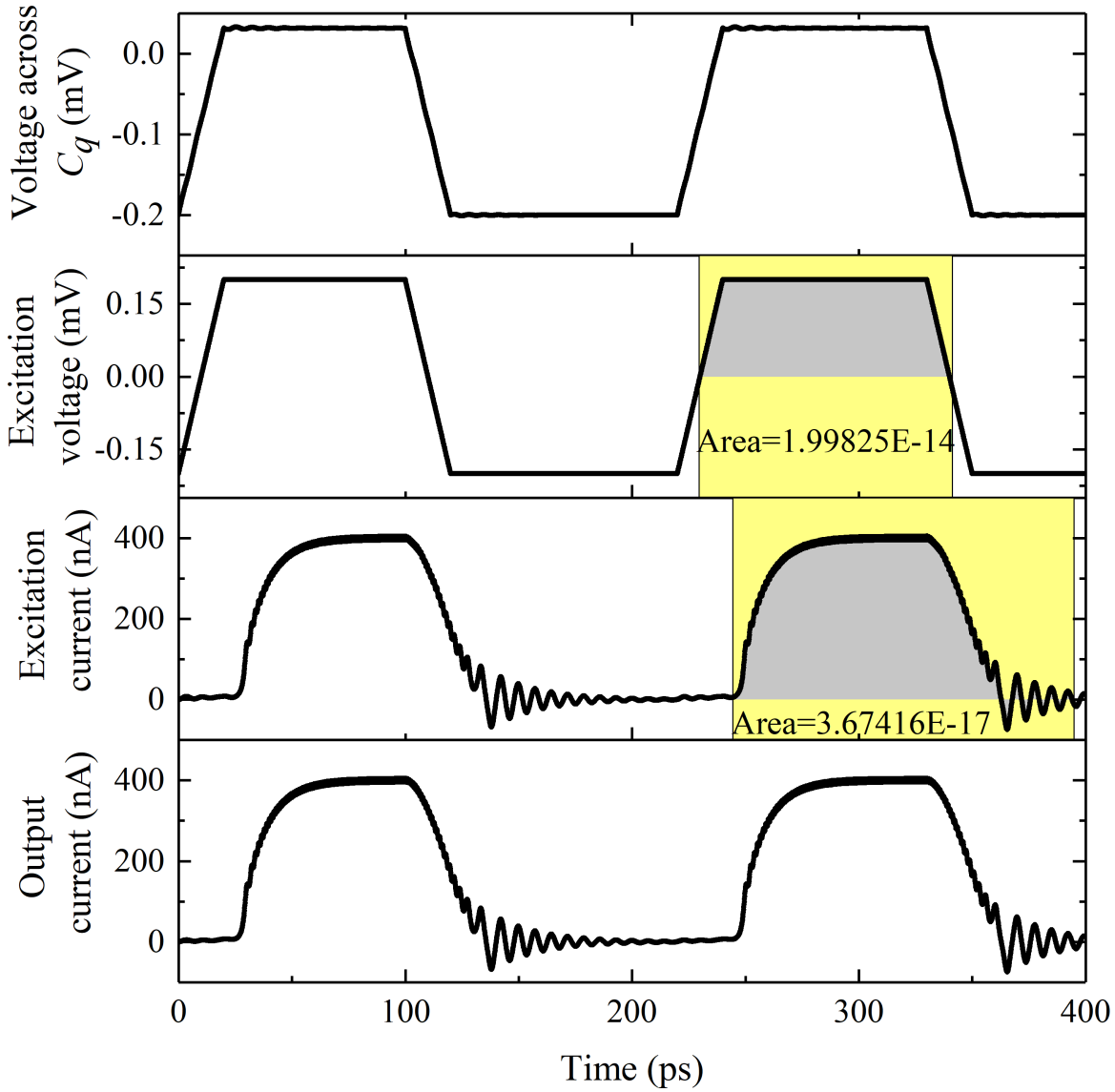


Figure 6.10: Area under the curve for voltage and current wave-forms corresponding to single switching cycle used to calculate energy per bit.

Chapter 7

Design and material composition of QPSJs

7.1 Introduction

In this chapter, the design and material composition of QPSJs that are suitable to fabricate the logic circuits discussed in this dissertation are estimated based on the phase-slip energy physical model presented by Mooij et. al [5]. The critical voltage of the Coulomb blockade across the QPSJ is dependent on the maximum phase-slip energy of the nano-wire. The device parameters such as critical voltage, normal resistance and the geometrical inductance can be extracted from the conditions laid out by [5] that maximize the probability of quantum phase-slips across the nano-wire. In the following sections, these conditions are used to estimate suitable materials for QPSJs as well as their design parameters such as the nano-wire length, width and thickness, along with the measurement temperature. Furthermore, the switching energy and the switching delay for the chosen design and material parameters are estimated. The programs used to calculate these estimations are provided in the appendix.

7.2 Design and Material Composition Estimations for QPSJs

The quantum phase-slip energy of a QPSJ based on the compact circuit model presented in chapter 2 is given by Equation 7.1 below. The energy of the phase-slip depends on the phase, where maximum phase-slip energy is given by E_s. This is the energy barrier for the flux to tunnel across the nano-wire generating a phase-slip center, and suppresses the superconductivity.

$$E = E_s(1 - cos(q)) \tag{7.1}$$

where normalized charge q is given by,

$$q = \frac{2\pi}{2e}, 0 < q < 2\pi, n \in Z \tag{7.2}$$

The maximum phase-slip energy E_s is given by Equation 7.3 according to [5]. It is a function of material parameters such as critical temperature T_c, coherence length ξ and normal resistance per coherence length R_ξ.

$$E_s = a\frac{A}{\xi}k_B T_c \frac{R_q}{R_\xi} exp(-b\frac{R_q}{R_\xi}) \tag{7.3}$$

In this model, the constants a and b are unknown and are assumed to be material dependent. k_B is the Boltzmann constant, R_q is the quantum resistance $\frac{h}{4e^2} = 6.45k\Omega$, A is the length of the wire and

$$R_\xi = \frac{\xi R_n}{A} \tag{7.4}$$

R_n is the normal resistance. Another energy scale of interest with respect to the quantum phase-slips is the inductive energy of the nano-wire. The inductive energy of the nano-wire can be calculated as shown below according to [5].

$$E_L = \frac{{\Phi_0}^2}{2L} = 17.4\frac{R_q}{R_n}k_B T_c \tag{7.5}$$

For the probability of the quantum phase-slips to be highest in a nano-wire, the conditions in Equation 7.6 [5] and Equation 7.8 must be satisfied.

$$0.1 \leq \alpha_c \leq 1 \tag{7.6}$$

where

$$\alpha_c = \frac{E_s}{E_L} \tag{7.7}$$

$$E_s \gg k_B T \tag{7.8}$$

In these various conditions, the constraints can be related to physical dimensions of the nano-wire such as length l, area of cross-section (related to width w and thickness t) and the material parameters such as critical temperature T_c, coherence length ξ and resistivity ρ.

Examples of designs of InOx and NbN are shown in Figures 7.1 and 7.3 and the corresponding switching energy and switching delay for $InOx$ are shown in Figures 7.4 and 7.5. Figure 7.6 shows a comparison between the phase-slip energy for a junction of nominal physical dimensions and the thermal energy as a function of temperature. Since phase-slip energy is not directly dependent on temperature, a single value for each material is shown. Another energy scale is added to this plot that represents $100 * k_B T$. This is a suggested energy scale chosen such that the noise level when measuring phase-slip properties are minimal and therefore may not significantly distort the tunneling phenomenon. Similar energy differences between Josephson energies and thermal energies are used for JJs. Furthermore, temperature also affects the $I_C R_N$ product in JJs. The switching speed of a junction is directly proportional to its $I_C R_N$ product. Similarly, in case of QPSJs, the switching speed is proportional to critical voltage V_C. This separation factor between thermal energy and phase-slip energy ensures a high switching speed for QPSJs. However, this is only an estimate and not a necessary condition to observe phase-slips.

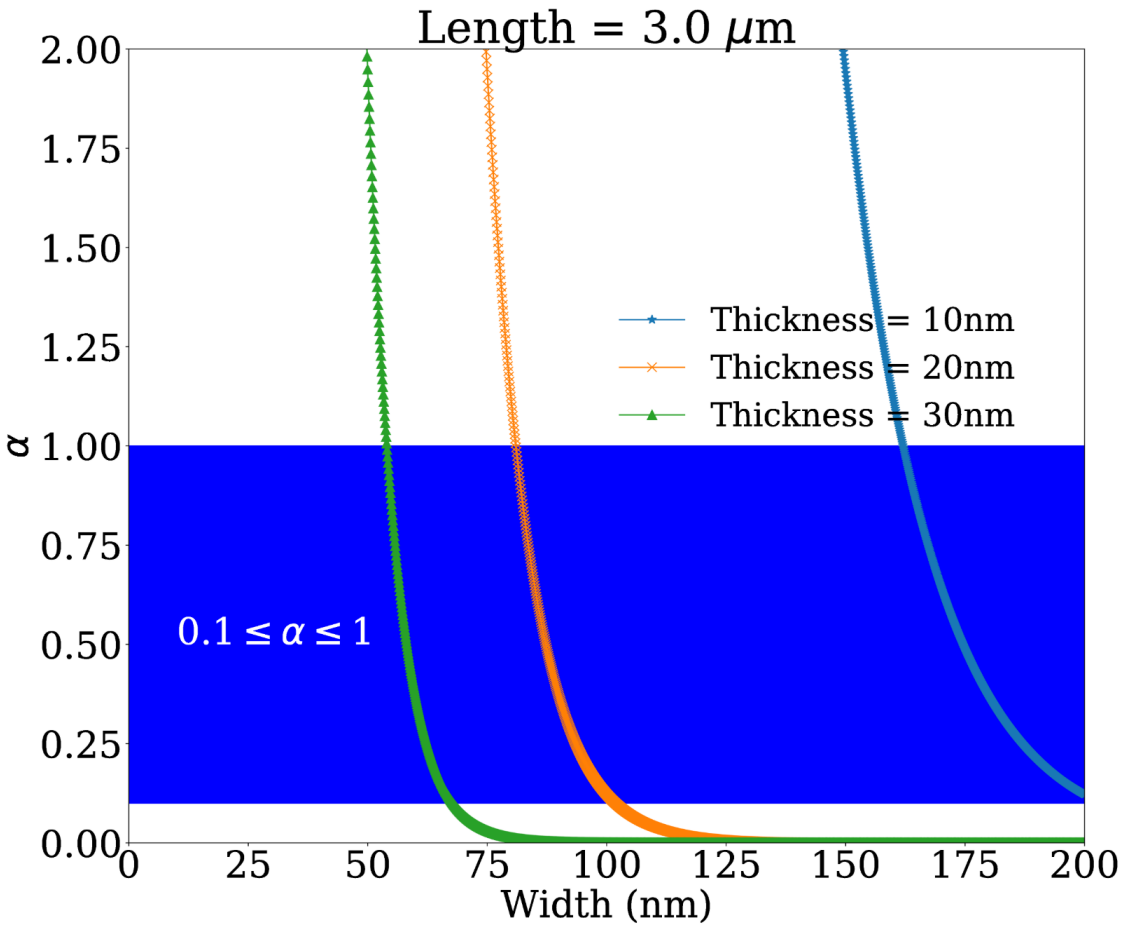


Figure 7.1: Design parameter evaluation for $InOx$. Shaded region shows design parameter combinations satisfying condition for forming a QPSJ.

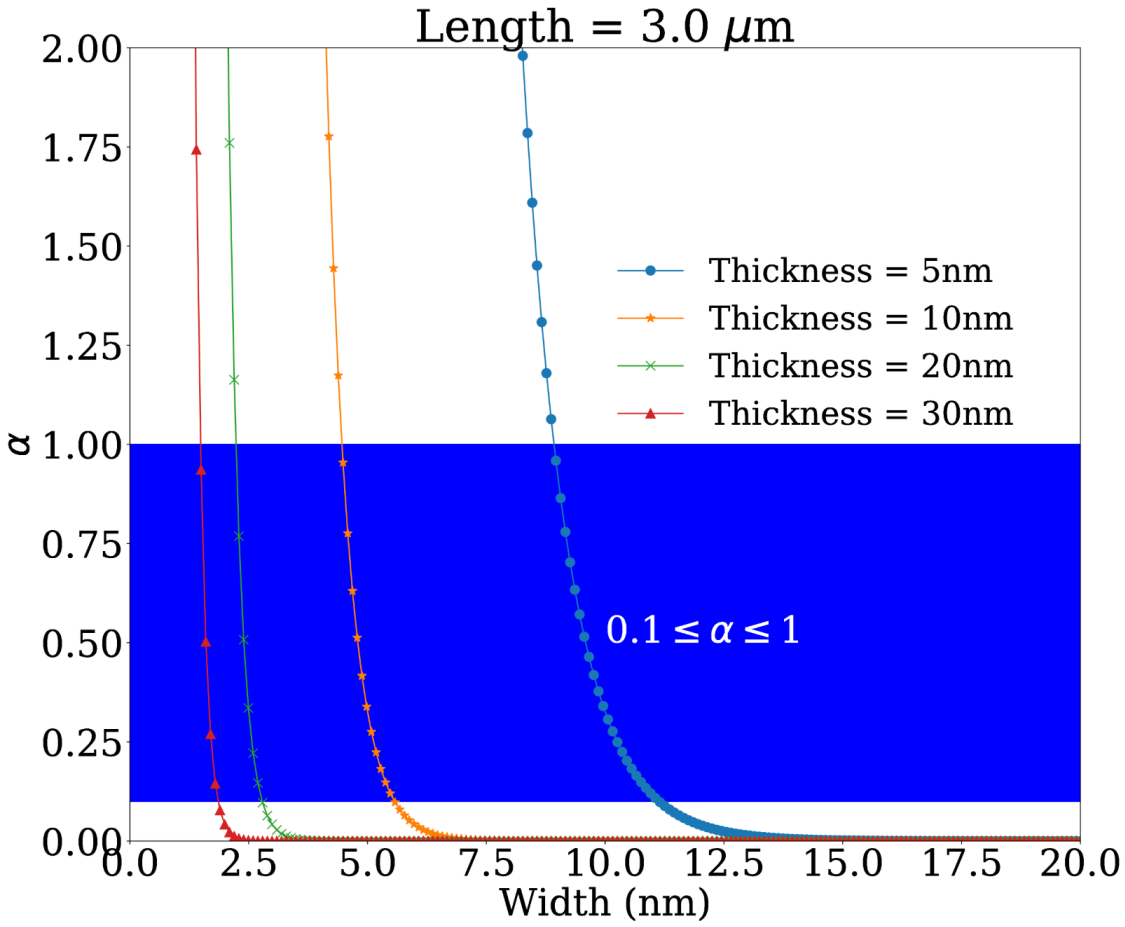


Figure 7.2: Design parameter evaluation for NbN. Shaded region shows design parameter combinations satisfying condition for forming a QPSJ.

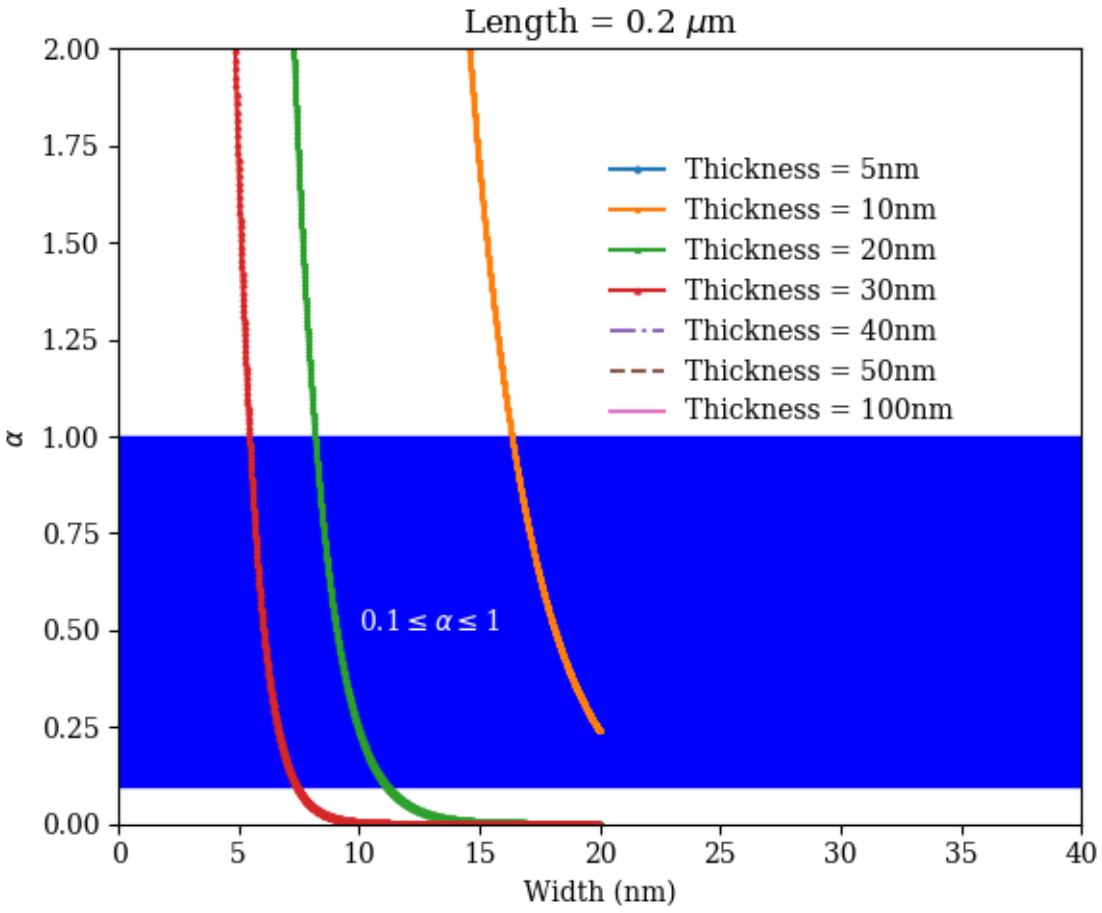


Figure 7.3: Design parameter evaluation for $NbTiN$. Shaded region shows design parameter combinations satisfying condition for forming a QPSJ.

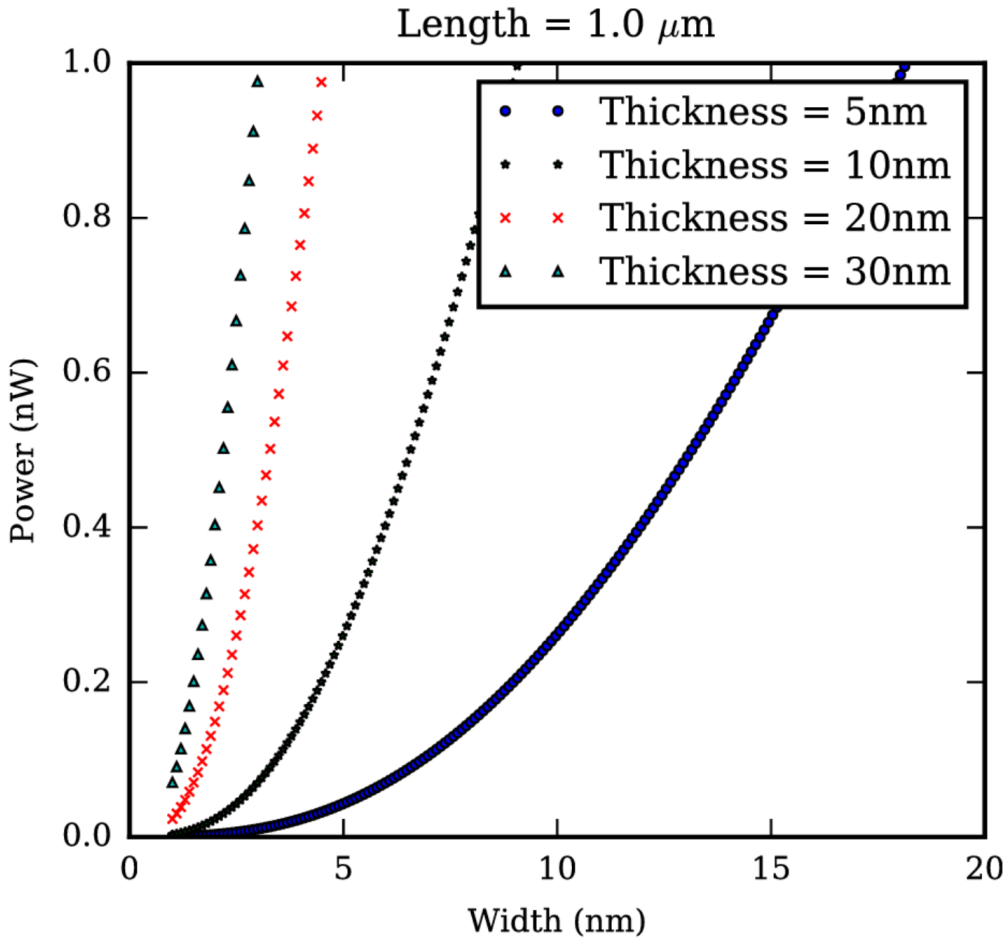


Figure 7.4: Power dissipated per switching event in an InOx QPSJ calculated based on a model by Mooij et al. [5] for a nano-wire of length 1 μm.

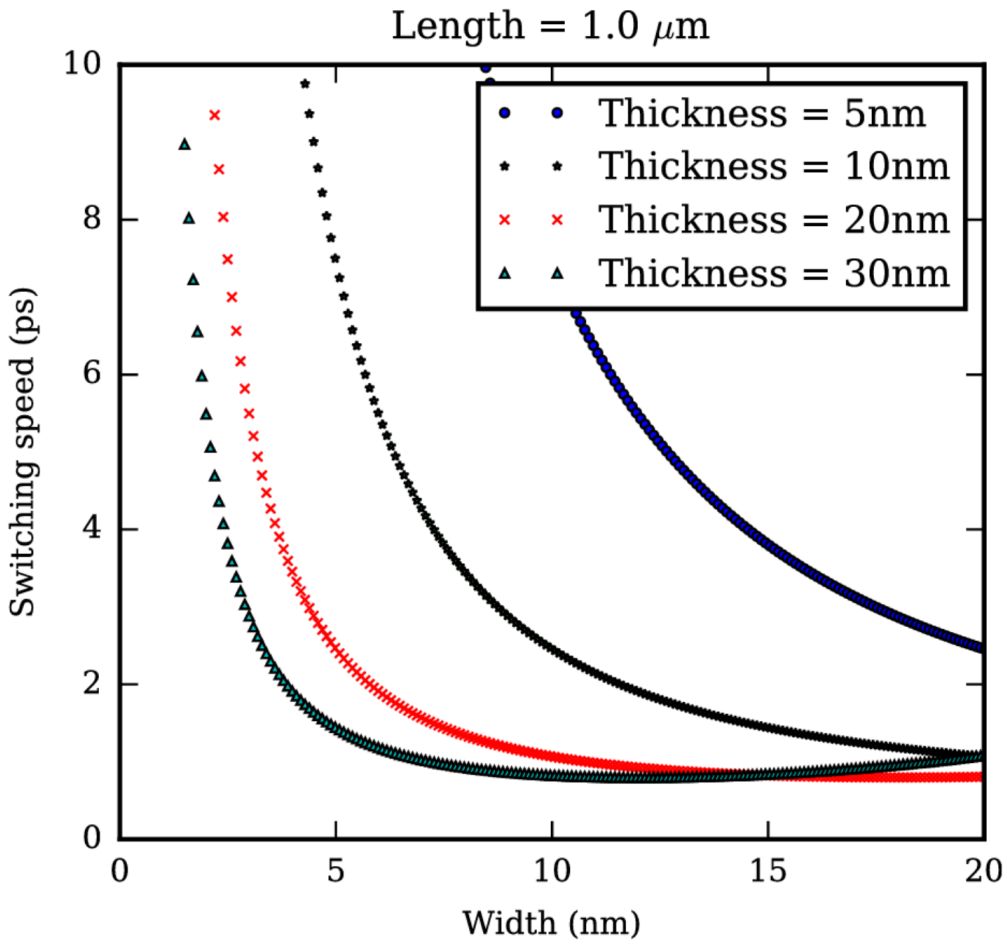


Figure 7.5: Switching speed in an InOx QPSJ calculated based on the model by Mooij et al. [5] for a nano-wire of length 1 μm.

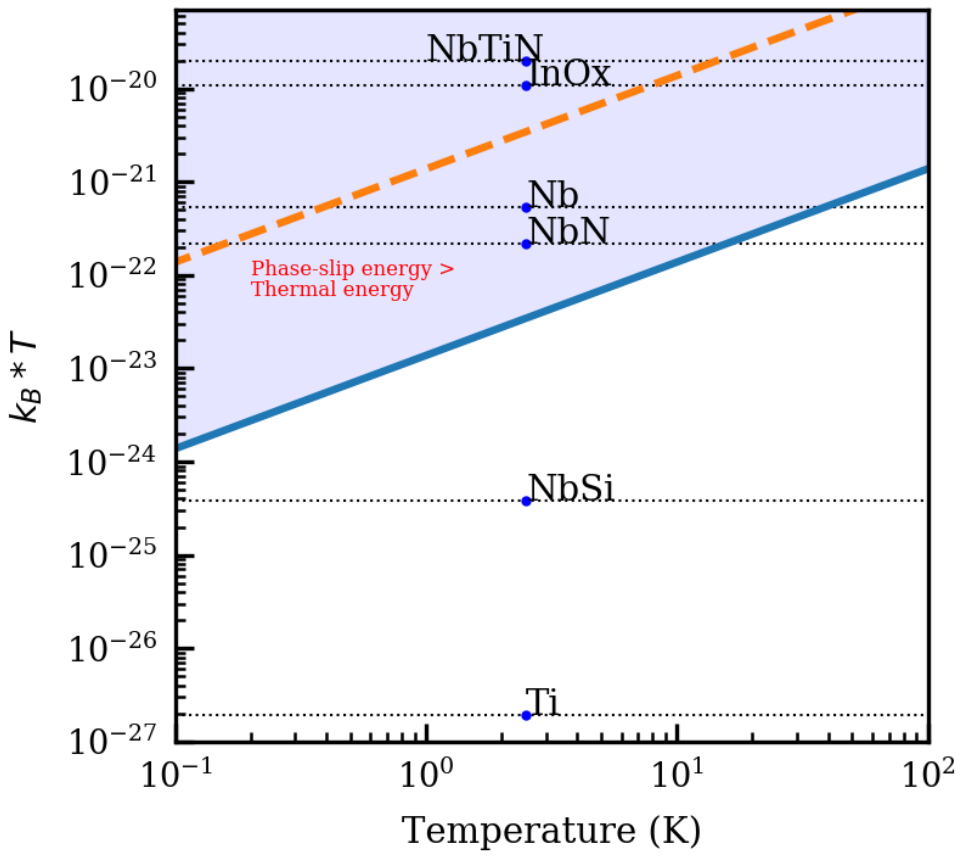


Figure 7.6: Phase-slip energy in various materials compared to thermal energy (k_BT) as a function of temperature. This plot can be used to estimate measurement temperatures for QPSJs in different materials. The dotted red line is the recommended phase-slip energy (two orders above thermal energy) line as a function of measurement temperature.

Chapter 8

Conclusion

8.1 Potential Advantages of QPSJ-based Logic Circuits

Superconducting computing presents advantages compared to CMOS based computing in terms of speed and power dissipation [27]. Currently, superconducting computing is exclusively based on JJs. Our estimations show that the reduction in power dissipation, and associated reduced energy per operation, can be even more significant for QPSJ-based circuits, for the cases of peta and exa-scale computing, while maintaining or improving speed over JJ-based circuits. According to the equations in [6], the power dissipation versus delay per switching event for varying junction geometries can be calculated and is shown in Figure 8.1. Similarly, the switching energy versus delay per switching event of JJs and QPSJs are compared in Figure 8.2. The energy per switching event for a typical QPSJ with parameters from [73] can be calculated as $E_{swqpsj} = (2e)(V_C) = 2(1.6{*}10^{-19}C)(0.7{*}10^{-3}V) = 2.24zJ$, while the energy per switching event for a typical JJ with a critical current of 100 μA is $E_{swjj} = (\Phi_0)(I_C) = (2.067 * 10^{-15}Wb)(100 * 10^{-6}A) = 0.21aJ$. A comparison of phase-slip energy (i.e. the energy barrier at the nano-wire during flux tunneling calculated using the model by Mooij et. al [5]) for various materials of interest and thermal energy versus temperature is shown in Figure 7.6. At a given measurement temperature, phase-slip energy must be at least two orders of magnitude higher than thermal energy for quantum tunneling of flux instead of thermal activation. Therefore, InOx, NbN and, perhaps NbTiN are materials of interest for QPSJs. Although Nb appears to have high phase-slip energy, the kinetic inductance of the material is low, making it difficult to observe quantum phase-slips.

It is important to note that these are estimates based on simulation and a primary goal of future efforts should be to explore and refine these estimates by building and testing relevant devices and circuits.

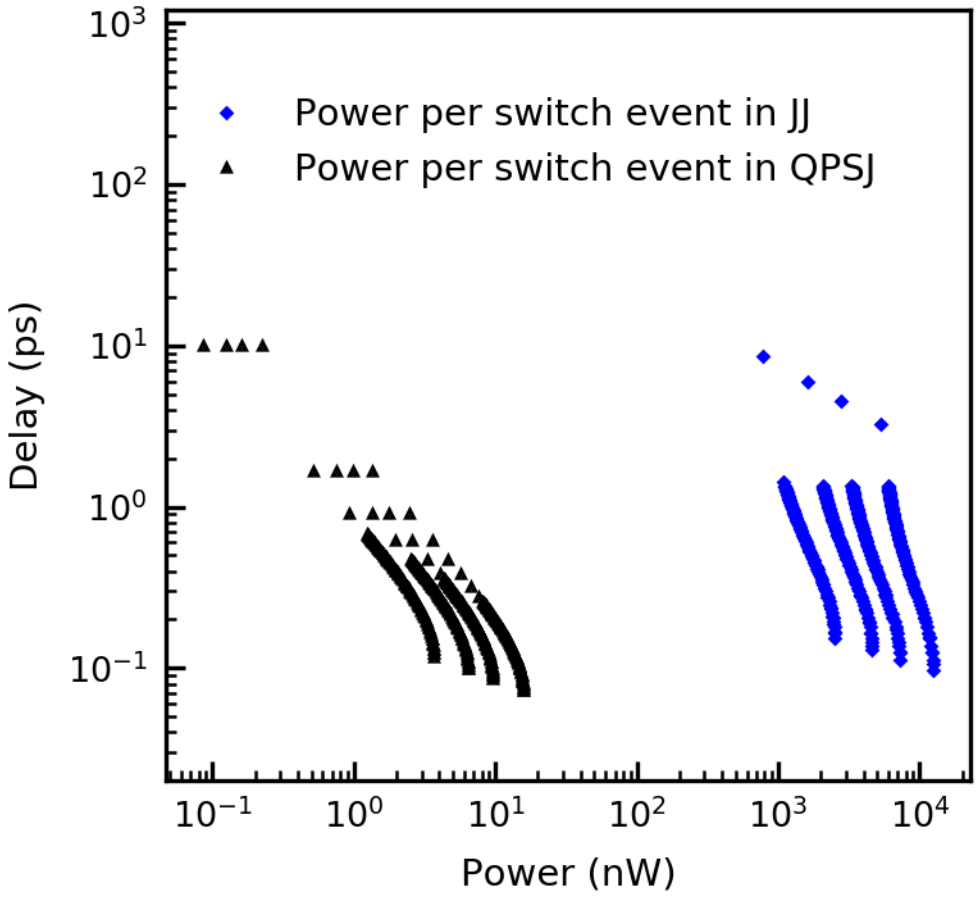


Figure 8.1: Delay versus power comparison of JJs in SFQ circuits and QPSJs in charge-based logic circuits, calculated according to [6] (Chapter 6). The different curves for QPSJ are for different nano-wire widths and lengths. The different curves for JJ are for different junction areas and critical current densities.

Promising potential advantages of QPSJ-based superconducting electronics:

- QPSJ based circuits are voltage-biased compared to current-biasing in JJ based circuits. This shows promise to reduce circuit complexity in large-scale integration.

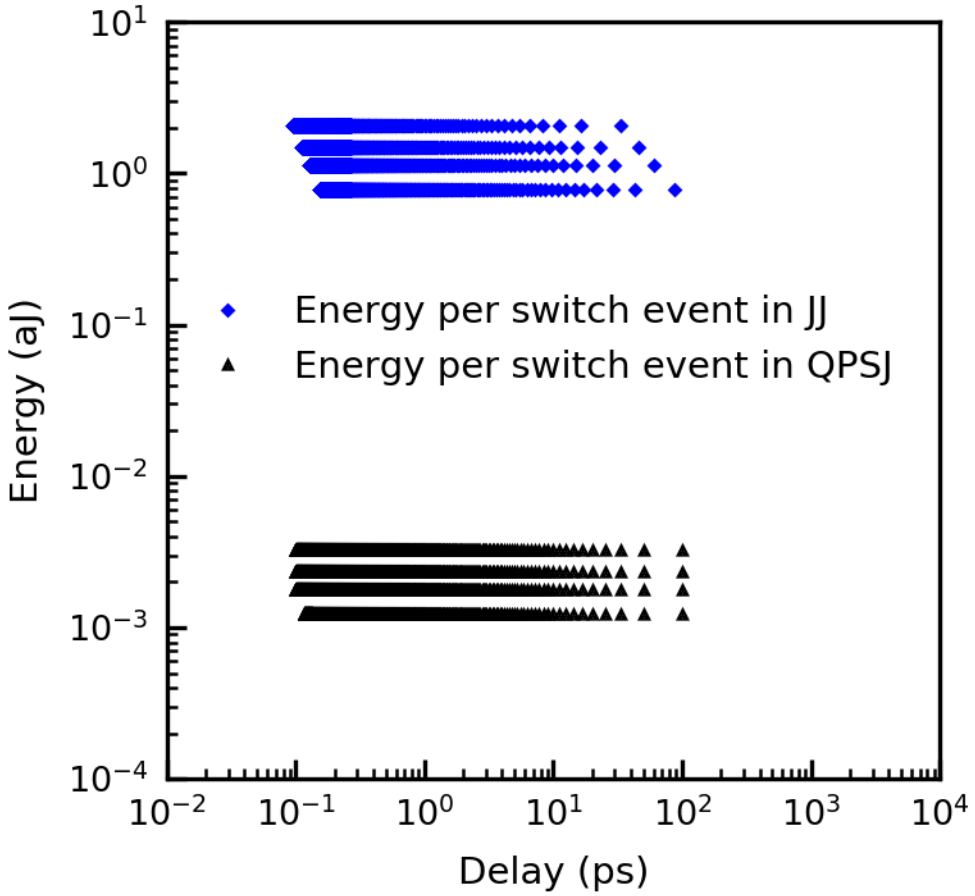


Figure 8.2: Switching energy versus delay comparison of JJs in SFQ circuits and QPSJs in charge-based logic circuits, calculated according to [6] (Chapter 6). The different curves for QPSJ are for different nano-wire widths and lengths. The different curves for JJ are for different junction areas and critical current densities.

- It is challenging to scale existing JJs to junction sizes of a few nanometers, because as critical current of JJs get smaller, larger inductances, and therefore larger logic cells, are needed for SFQ loops. Furthermore, superconducting loops that can store flux quantum occupy a substantial area. QPSJs use nano-wires with cross-sectional dimensions of 10s of nanometers and with charge storage possible in an area of a few 10s of square nanometers. A single logic cell (i.e. a charge island) of charge-based logic will be less than 500 nm long and less than 50 nm wide (for two QPSJs in series with

a capacitor at their node), whereas a single SFQ logic cell is a loop made of two JJs and an inductor with an area of a few square micrometers.

- Estimations show an advantage in power dissipation in QPSJs of approximately 2 orders of magnitude, or even higher for the QPSJs in adiabatic circuits, compared to JJs in each switching event, along with low or negligible static power dissipation while maintaining operation speed.

Nevertheless, implementation of circuits based on QPSJs also presents potential challenges and risks, the extent of which are yet to be explored in detail and will be explored in future efforts. These include:

- Observing quantum phase-slips in nano-wires, and controlling them, is challenging; particularly because of lack of sufficient experimental research.

- QPSJs may need to be operated at temperatures below that required for JJs, possibly because of thermal noise; thereby introducing the need for additional cooling. If this is true, and how much lower, are questions that must be answered before implementing QPSJ-based circuits at a higher level.

- Due to the nature of charge-based logic being implemented using a small number of electrons per logic bit (2e), charge noise may have significant effects. The extent of this issue is yet unknown and needs more exploration to determine the impact and development of possible solutions.

Some of the aspects of QPSJs are similar to previous or existing technologies, such as single-electron transistors (SETs) [108], superconducting nano-wire single photon detectors (SNSPDs) [109], microwave kinetic inductance detectors (MKIDs) [110] and nTrons [111], with respect to physical attributes such as tunnel barriers (in the case of SETs) and nano-wire device geometry, as in SNSPDs, MKIDs and nTrons. There are some similarities, but

also some significant differences between QPSJ-based circuits and each of these other devices or technologies. The important difference arises from the tunnel barrier that forms in QPSJ-based structures, which is inherent to the physics of the quantum phase-slip phenomenon, as opposed to materially-, optically- or thermally- defined (or induced) barriers in SETs, SNSPDs and nTrons. For the case of SETs, the similarity exists in quantized charge (electron) tunneling through a barrier, which is the phenomenon that was proposed for use in digital logic applications [108]. The basis of operation of QPSJs in logic circuits relies on a Cooper pair (or multiple pairs) tunneling through a quantum phase-slip-defined barrier, which is not materially defined (i.e., not defined as a barrier material), along a superconductor nano-wire. This can be contrasted with the operation of SETs where the tunneling barrier is physically defined (as a barrier material between semiconducting, or in some case superconducting, regions) for a single-electron to tunnel during a switching event. Furthermore, SETs are three terminal devices that require regenerating charge on the islands through a gate voltage, in contrast to the two-terminal logic cell defined for QPSJ-based logic circuits. Since the information-carrying particle in QPSJ-based circuits is a non-scattering Cooper pair, this is expected to allow regenerative action similar to JJ-based circuits relying on flux generation and propagation (for example in a Josephson transmission line, JTL). QPSJ-based logic circuits are estimated to be up to two orders of magnitude faster while allowing a decrease in power dissipation by two orders of magnitude, compared to SETs [108]. SNSPDs are devices with a barrier induced in the nano-wire by an external optical excitation, and therefore are suitable for applications in imaging and optical sensing. Achieving digital logic operations using SNSPDs may require significant additional hardware (although there is interest in their use in optical transducers for quantum computing applications [109]). nTrons are another set of three-terminal superconducting devices proposed as alternative to JJ-based structures for several applications including classical computing [110]. While they are achieved using thermally activated barriers, the switching operation is based on limiting or re-routing current due to the activated barriers and are therefore

not analogous to JJ-based operation. The currents through the devices are not limited to quantized charge tunneling, and lead to several orders of magnitude higher switching energy [111] as compared to the estimates provided for QPSJ switching. In summary, QPSJs in our proposed circuit applications are primarily viewed as dual devices to JJs, where flux tunnels across the nano-wire (superconducting barrier), similar to charge tunneling across a non-superconducting barrier in JJs. QPSJ-based logic circuits can be thought of as being quite similar or complementary to JJ-based logic circuits, while providing several advantages over or enhancing circuit performance when used in conjunction with them.

8.2 Future Work

One of the main areas of need, to advance QPSJ technology to a useful point, is to develop suitable and reproducible processes to fabricate nano-wires that have controlled quantum phase-slips at temperatures of 4 K or higher. Superconducting compounds such as NbN, NbTiN and InOx must be explored for nano-wires for the reasons described in the previous sections. Nano-wires of different sizes and configurations must be fabricated and tested. Phase slips have been observed at temperatures above the sub-K regime [112], though the initial logic circuits most likely require testing down into the several 100s of mK to provide a suitable temperature range over which to observe and control the phase slips while also connecting the device performance and behavior to controllable fabrication processes, materials and device geometry. Once reproducible QPSJs are realized, next steps must involve fabricating simple circuits. Circuits, such as a single charge island, formed by two QPSJs and a parasitic capacitor, with an island at the node formed by these devices, will be fabricated and characterized. Initial testing of these circuits will be similar to DC characterization of single QPSJs, to determine the presence of quantized charge on islands. The technology will then be suitable to demonstrate operations of complex circuits using QPSJs. These will include driver/receiver circuits and charge transmission lines with different lengths (i.e., numbers of gates), formed by a series of charge island circuits, which can

be tested with clocks of different frequencies to verify quantized charge pulse propagation and explore energy/power dissipation. Future directions involve design, fabrication, demonstration and detailed exploration of the operation and performance of the different types of digital and neuromorphic circuits [113, 114]. These must also include addressing certain engineering challenges such as charge noise, need for amplification, etc., through designing, fabricating and testing additional suitable circuits and test structures.

8.3 Conclusion

Quantum phase-slip junctions and the related circuit families discussed here offer a promising new form of superconducting electronics, which has been predominantly based on Josephson junctions. Our work thus far has shown some of the appealing aspects of QPSJ-based systems, such as energy efficiency and operating speed, with several possible additional advantages over those based on JJs. This project has been internally funded up to this point, which is why our work has mainly been in simulation with limited dabbling in the experimental work (preliminary materials deposition and simple test device designs). External funding is expected to significantly impact progress, particularly in practical implementation of QPSJs and related circuits, because it will allow our team (including graduate students) to focus on exploring and tackling the experimental challenges. Although this chapter describes several circuit families, the initial steps will be to work towards practical realization of QPSJ devices, along with suitable test structures and, perhaps, simple logic cells to provide insight into the accuracy of our initial simulation-based work. The progress in designing digital and neuromorphic circuits was described to motivate the exploration of QPSJs suitable for superconducting electronics aimed at advanced information processing and computing technologies. Success in these initial steps will provide a path to justify the exploration of larger circuits leading to superconducting computing using the various circuit families introduced.

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Appendices

Appendix A

The device parameters used for QPSJs in circuit simulations are based on calculations using a phase-slip energy model presented by Mooij et. al. [5] as detailed in Chapter 7 of this dissertation. In this section, the python programs developed to calculate the physical parameters that can be used for evaluation of circuit parameters are presented. The program for estimation of QPSJ physical parameters for a given material are shown below: ————————————————————————————————- //

Name: QPSJ parameters //

Purpose: Estimation of range of QPSJ physical parameters for experimental phase-slip observation //

Author: Uday Goteti //

Created: 04/03/2016 //

Last edited: 01/23/2018 //

————————————————————————————————- //

```
from numpy import * //
from math import *//
import matplotlib.pyplot as plt //
from matplotlib.widgets import * //
def kbt(t)://
kb = 1.38064852e-23 Boltzmann's constant//
kbt = kb*t//
return kbt//
def Rcl(cl, l, Rn): //
Rcl = cl*Rn/l //
return Rcl //
def Es(cl, l, t, Rn): //
a,b for NbN //
a = 0.52 //
b = 0.1 //
a = 0.21 //
b = 0.115 //
a,b for InOx //
a = 1.5 //
b = 1.2 //
new a and b for qps transistor //
a = 0.18 //
b = 0.16 //
Rq = 6.45e3 //
Rc = Rcl(cl, l, Rn) //
```

```
kb = kbt(t) //
Es = a*(l/cl)*kb*(Rq/Rc)*exp(-b*(Rq/Rc)) //
return Es //
def El(Rn, t): //
kb = kbt(t) //
Rq = 6.45e3 //
El = 17.4*(Rq/Rn)*kb //
return El //
def Alpha(cl, l, t, Rn): //
Ea = Es(cl, l, t, Rn) //
Eb = El(Rn, t) //
Alpha = Ea/Eb //
return Alpha //
def NbN(): //
NbN = dict(t = 16.00, Tc of NbN in K //
cl = 5e-9, Coherence length of NbN in m //
Rho = 62e-8) NbN resistivity in Ohm-m at 20K //
return NbN //
def NbTiN(): //
NbTiN = dict(t = 18.00, Tc of NbN in K //
cl = 4.26e-9, Coherence length of NbN in m //
Rho = 100e-8) NbN resistivity in Ohm-m at 20K //
return NbTiN //
def NbSi(): //
NbSi = dict(t = 3.10, Tc of NbSi in K //
cl = 15e-9, Coherence length of NbSi in m //
Rho = 150e-8) NbSi resistivity in Ohm-m at 20K //
return NbSi //
def InOx(): //
InOx = dict(t = 2.7, Tc of InOx in K //
cl = 10e-9, Coherence length of InOx in m //
Rho = 14e-5) InOx resistivity in Ohm-m at 20K?? (not
sure if it is 20K) //
return InOx //
def Nb(): //
Nb = dict(t = 9.25, Tc of Nb in K //
cl = 38e-9, Coherence length of Nb in m //
Rho = 50e-9) Nb resistivity in Ohm-m at 20K?? (not sure about this value) //
return Nb //
def Ti(): //
Ti = dict(t = 0.3, Tc of Ti in K //
cl = 2.7e-6, Coherence length of Ti in m //
Rho = 1e-6) Ti resistivity in Ohm-m at 20K //
return Ti //
def TaN(): //
```

TaN = dict(t = 3.9, Tc of TaN in K //
cl = 6e-9, Coherence length of TaN in m //
Rho = 38e-5) TaN resistivity in Ohm-m at 20K?? (not
sure if it is 20K) //
return TaN //
def plot(ls, i): //
d = NbSi() //
d = NbN() //
d = InOx() //
d = Nb() //
d = Ti() //
d = TaN() //
t = d['t'] //
cl = d['cl'] //
Rho = d['Rho'] //
l = ls //
ws = linspace(1e-10, 200e-10, 2000) nano-wire width in m //
d = [5e-9, 10e-9, 20e-9, 30e-9, 40e-9, 50e-9, 100e-9] nano-wire thickness in m //
Rns = ws.copy() //
ala = ws.copy() //
alb = ws.copy() //
alc = ws.copy() //
ald = ws.copy() //
ale = ws.copy() //
alf = ws.copy() //
alg = ws.copy() //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(l/(w*d[0])) //
a = Rns[idx] //
print "
ala[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(l/(w*d[1])) //
alb[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(l/(w*d[2])) //
alc[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(l/(w*d[3])) //
ald[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(1/(w*d[4])) //
ale[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(1/(w*d[5])) //

alf[idx] = Alpha(cl, l, t, Rns[idx]) //
for idx, w in enumerate(ws): //
Rns[idx] = Rho*(1/(w*d[6])) //
alg[idx] = Alpha(cl, l, t, Rns[idx]) //
font = 'family' : 'serif', //
'weight' : 'normal', //
'size' : 40 Fixed font parameters for the plot
- latex - change if necessary //
plt.figure(i,figsize=(18,15),facecolor='w', edgecolor='k') //
plt.plot((1e9)*ws, ala, '-o', label = 'Thickness = 5nm', ms=10) //
plt.plot((1e9)*ws, alb, '-*', label = 'Thickness = 10nm', ms=10) //
plt.plot((1e9)*ws, alc, '-x', label = 'Thickness = 20nm', ms=10) //
plt.plot((1e9)*ws, ald, '-',label='Thickness=30nm',ms=10)//
plt.plot((1e9)*ws, ale, '-.', label = 'Thickness = 40nm') //
plt.plot((1e9)*ws, alf, '–', label = 'Thickness = 50nm') //
plt.plot((1e9)*ws, alg, '-,', label = 'Thickness = 100nm') //
plt.ylabel(r'α') //
plt.xlabel('Width (nm)') //
plt.title('Length =
plt.axhspan(0.1, 1, color = 'blue', alpha = 0.1) //
plt.text(10, 0.5, r'0.1$\leq \alpha \leq$1', color='white') //
plt.xlim([0,12]) //
plt.ylim([0,2]) //
plt.rc('font', **font) //
plt.legend(frameon = False, loc = (0.5,0.5), prop='size':35) //
plt.tight$_l ayout$()//
def Energies$_p lots$() : //
d$_N bsi = NbSi$()//
d$_N bn = NbN$()//
d$_I nox = InOx$()//
d$_N b = Nb$()//
d$_T i = Ti$()//
d$_T aN = TaN$()//
d$_N bTiN = NbTiN$()//
t$_N bsi = d_N bsi['t']$//
cl$_N bsi = d_N bsi['cl']$//
Rho$_N bsi = d_N bsi['Rho']$//
Rn$_N bsi = Rho_N bsi * (1e16)$//
t$_N bn = d_N bn['t']$//
cl$_N bn = d_N bn['cl']$//
Rho$_N bn = d_N bn['Rho']$//
Rn$_N bn = Rho_N bn * (3e-6)/((5e-9)*(10e-9))$//
t$_N bTiN = d_N bTiN['t']$//
cl$_N bTiN = d_N bTiN['cl']$//
Rho$_N bTiN = d_N bTiN['Rho']$//

$\mathrm{Rn}_N bTiN = Rho_N bTiN * (3e-6)/((5e-9)*(10e-9))//$
$\mathrm{t}_I nox = d_I nox['t']//$
$\mathrm{cl}_I nox = d_I nox['cl']//$
$\mathrm{Rho}_I nox = d_I nox['Rho']//$
$\mathrm{Rn}_I nox = Rho_I nox * (3e-6)/((70e-9)*(20e-9))//$
$\mathrm{t}_N b = d_N b['t']//$
$\mathrm{cl}_N b = d_N b['cl']//$
$\mathrm{Rho}_N b = d_N b['Rho']//$
$\mathrm{Rn}_N b = Rho_N b * (4e-6)/((2e-9)*(10e-9))//$
$\mathrm{t}_T i = d_T i['t']//$
$\mathrm{cl}_T i = d_T i['cl']//$
$\mathrm{Rho}_T i = d_T i['Rho']//$
$\mathrm{Rn}_t i = Rho_T i * (1e-6)/((1e-9)*(1e-9))//$
$\mathrm{t}_T aN = d_T aN['t']//$
$\mathrm{cl}_T aN = d_T aN['cl']//$
$\mathrm{Rho}_T aN = d_T aN['Rho']//$
$\mathrm{Rn}_T aN = Rho_T aN * (3e-6)/((20e-9)*(5e-9))//$
$\mathrm{Es}_N bsi = Es(cl_N bsi, 3e-6, t_N bsi, Rn_N bsi)//$
$\mathrm{Es}_N bN = Es(cl_N bn, 3e-6, t_N bn, Rn_N bn)//$
$\mathrm{Es}_I nox = Es(cl_I nox, 2e-6, t_I nox, Rn_I nox)//$
$\mathrm{Es}_N b = Es(cl_N b, 4e-6, t_N b, Rn_N b)//$
$\mathrm{Es}_T i = Es(cl_T i, 1e-6, t_T i, Rn_t i)//$
$\mathrm{Es}_T aN = Es(cl_T aN, 2e-6, t_T aN, Rn_T aN)//$
$\mathrm{Es}_N bTiN = Es(cl_N bTiN, 2e-6, t_N bTiN, Rn_N bTiN)//$
t = linspace(0, 100, 10000) //
Eb = kbt(t) //
plt.figure(11, figsize=(2.9, 2.6), // dpi=300,facecolor='w',
edgecolor='k') //
plt.plot(t, Eb) //
plt.plot(t, Eb*100, linestyle='dashed') //
plt.yscale('log') //
plt.xscale('log') //
$\mathrm{plt.plot}(2.5, \mathrm{Es}_N bsi, 'bo', markersize = 1)//$
$\mathrm{plt.text}(2.5, \mathrm{Es}_N bsi, r'NbSi', fontsize = 7)//$
$\mathrm{plt.hlines}(\mathrm{Es}_N bsi, 0.1, 100, colors = 'k', linestyles = 'dotted', lw = 0.5)//$
$\mathrm{plt.plot}(2.5, \mathrm{Es}_N bN, 'bo', markersize = 1)//$
$\mathrm{plt.text}(2.5, \mathrm{Es}_N bN, r'NbN', fontsize = 7)//$
$\mathrm{plt.hlines}(\mathrm{Es}_N bN, 0.1, 100, colors = 'k', linestyles = 'dotted', lw = 0.5)//$
$\mathrm{plt.plot}(2.5, \mathrm{Es}_I nox, 'bo', markersize = 1)//$
$\mathrm{plt.text}(2.5, \mathrm{Es}_I nox, r'InOx', fontsize = 7)//$
$\mathrm{plt.hlines}(\mathrm{Es}_I nox, 0.1, 100, colors = 'k', linestyles = 'dotted', lw = 0.5)//$
$\mathrm{plt.plot}(2.5, \mathrm{Es}_N b, 'bo', markersize = 1)//$
$\mathrm{plt.text}(2.5, \mathrm{Es}_N b, r'Nb', fontsize = 7)//$
$\mathrm{plt.hlines}(\mathrm{Es}_N b, 0.1, 100, colors = 'k', linestyles = 'dotted', lw = 0.5)//$
$\mathrm{plt.plot}(2.5, \mathrm{Es}_T i, 'bo', markersize = 1)//$

plt.text(2.5, $\mathrm{Es}_T i, r'Ti', fontsize = 7)$//
plt.hlines($\mathrm{Es}_T i, 0.1, 100, colors =' k', linestyles =' dotted', lw = 0.5)$//
plt.plot(1, $\mathrm{Es}_T aN,' bo')$//
plt.text(0.4, $\mathrm{Es}_T aN, r'TaN', fontsize = 25)$//
plt.plot(2.5, $\mathrm{Es}_N bTiN,' bo', markersize = 1)$//
plt.text(1, $\mathrm{Es}_N bTiN, r'NbTiN', fontsize = 7)$//
plt.hlines($\mathrm{Es}_N bTiN, 0.1, 100, colors =' k', linestyles =' dotted', lw = 0.5)$//
plt.ylabel('$k_B * T$', fontsize = 7) //
plt.xlabel('Temperature (K)', fontsize = 7) //
plt.tick$_p arams(labelsize = 6.5, direction =' in', which =' both')$//
plt.fill$_b etween(t, Eb, 7e - 20, color =' blue', alpha = 0.1)$//
plt.text(0.2, 1e-22, r'Phase-slip energy ¿ ', color='red', fontsize=4) //
plt.text(0.2, 0.6e-22, r'Thermal energy', color='red', fontsize=4) //
plt.ylim([1e-27,7e-20]) //
plt.xlim([0.1,100]) //
plt.tight$_l ayout()$//
def main(): //
ls = [0.5e-6, 1e-6, 2e-6, 3e-6, 4e-6, 5e-6] nano-wire length in m //
for idx, l in enumerate(ls): //
plot(l, idx) //
Energies$_p lots()$//
if $_n ame_{==" m ain_{"}:}$//
main() //
plt.show() //

Appendix B

The program below can be used to calculate the power and energy versus delay for QPSJ and JJ based circuits, examples of which are shown in Chapter 8 of this dissertation:

Name: QPSJ switching times and power-delay

Purpose: Calculation of switching times and power of QPSJ as a function of junction dimensions

Author: Uday Goteti

Created: 06/06/2016

Last edited: 01/23/2017

```
from numpy import *
from math import *
import matplotlib.pyplot as plt
from matplotlib.widgets import *
from QPSJ_parametersimport*
import xlwt
font = 'family' : 'Arial',
'weight' : 'normal',
'size' : 22
book1 = xlwt.Workbook(encoding="utf-8")
sheet1 = book1.add_sheet("Sheet1")
book2 = xlwt.Workbook(encoding="utf-8")
sheet2 = book2.add_sheet("Sheet1")
def rql(a,b):
phi0 = 2.067833758e-15
Ic = b*1e-6
C = 26.939e-15
R = a
Lk = phi0/(2*pi*Ic*R)
t1 = R*C
t2 = Lk/R
t = max(t1, t2)
P = 2*(Ic*Ic)*R
P = (0.7*Ic)*phi0*(1/(t1+t2))
return t, P
def sfq(a,b):
phi0 = 2.067833758e-15
Ic = b*1e-6
```

```
C = 26.939e-15
R = a
Lk = phi0/(2*pi*Ic*R) (added R as a normalizing factor)
Lk = phi0/(2*pi*Ic) Without normalizing factor R - more accurate?
t1 = R*C
t2 = Lk/R
t = max(t1, t2)
P = 2*(Ic*Ic)*R + (Ic*Ic)*(10)
P = (0.7*Ic)*phi0*(1/(t1+t2)) + (0.7*Ic*0.7*Ic)*(10)
return t, P
def qps(a,b):
Vc = b*1e-5
q0 = 3.20435324e-19
R = a*1e3
L = 1e-9
Ck = q0/(2*pi*Vc)
t1 = L/R
t2 = R*Ck
t = max(t1, t2)
P = 2*(Vc*Vc)/R
P = (0.7*Vc)*q0*(1/(t1+t2))
return t, P
def Vc(cl, l, t, Rn):
q0 = 3.20435324e-19
Vc = (2*pi/q0)*Es(cl, l, t, Rn)
return Vc
def Power(l, w, dp):
d = NbSi()
d = NbN()
d = InOx()
d = Nb()
d = Ti()
t = d['t']
cl = d['cl']
Rho = d['Rho']
Rn = Rho*(l/(w*dp))
P = 2*(Vc(cl, l, t, Rn)*Vc(cl, l, t, Rn))/Rn
return P
def Speed(l, w, dp):
q0 = 3.20435324e-19
d = NbSi()
d = NbN()
d = InOx()
d = Nb()
d = Ti()
```

```
L = 1e-9
t = d['t']
cl = d['cl']
Rho = d['Rho']
Rn = Rho*(l/(w*dp))
Ck = q0/(2*pi*Vc(cl, l, t, Rn))
t1 = L/Rn
t2 = Rn*Ck
s = max(t1, t2)
return s
def Psweep(ls, i):
font = 'family' : 'Arial',
'weight' : 'normal',
'size' : 3.25
ls = [5e-7, 1e-6, 2e-6, 3e-6, 4e-6, 5e-6, 6e-6] nano-wire length in m
l = ls
ws = linspace(1e-9, 200e-9, 2000) nano-wire width in m
d = [5e-9, 10e-9, 20e-9, 30e-9, 40e-9, 50e-9, 100e-9] nano-wire thickness in m
Psa = ws.copy()
Psb = ws.copy()
Psc = ws.copy()
Psd = ws.copy()
Pse = ws.copy()
Psf = ws.copy()
Psg = ws.copy()
for idx, w in enumerate(ws):
Psa[idx] = Power(l, w, d[0])
for idx, w in enumerate(ws):
Psb[idx] = Power(l, w, d[1])
for idx, w in enumerate(ws):
Psc[idx] = Power(l, w, d[2])
for idx, w in enumerate(ws):
Psd[idx] = Power(l, w, d[3])
for idx, w in enumerate(ws):
Pse[idx] = Power(l, w, d[4])
for idx, w in enumerate(ws):
Psf[idx] = Power(l, w, d[5])
for idx, w in enumerate(ws):
Psg[idx] = Power(l, w, d[6])
plt.figure(num=i, figsize=(1.4, 1.3), dpi=600, facecolor='w', edgecolor='k')
plt.plot((1e9)*ws, (1e9)*Psa, 'ok', label = 'Thickness = 5nm', markersize = 0.05, fillstyle
= 'full')
plt.plot((1e9)*ws, (1e9)*Psb, '¡r', label = 'Thickness = 10nm', markersize = 0.05, fill-
style = 'full')
```

plt.plot((1e9)*ws, (1e9)*Psc, '¿b', label = 'Thickness = 20nm', markersize = 0.05, fillstyle = 'full')

plt.plot((1e9)*ws, (1e9)*Psd, '$^{g\prime}$, $label =\prime Thickness = 30nm\prime, markersize = 0.05, fillstyle =\prime full\prime$)

plt.plot((1e9)*ws, (1e6)*Pse, 'ok', label = 'Thickness = 40nm', ms = 5)

plt.plot((1e9)*ws, (1e6)*Psf, '–', label = 'Thickness = 50nm', ms = 0.5)

plt.plot((1e9)*ws, (1e6)*Psg, '-,', label = 'Thickness = 100nm', ms = 0.5)

plt.ylabel('Power (nW)')

plt.xlabel('Width (nm)')

plt.title('Length =

plt.rc('font', **font)

plt.legend(frameon=False, loc = (0.475,0.075), fontsize=3.25)

plt.tick$_p arams(labelsize = 3.25, direction =\prime in\prime, which =\prime both\prime)$

plt.axhspan(0.1, 1, color = 'blue', alpha = 0.1)

plt.text(15, 0.5, r'0.1$\leq \alpha \leq$1', fontsize = 25)

plt.xlim([0,20])

plt.ylim([0,1])

plt.tight$_l ayout()$

plt.legend()

i=0

while(i ¡ 2000):

sheet1.write(i, 0, (1e9)*ws[i])

sheet1.write(i, 1, (1e9)*Psa[i])

sheet1.write(i, 2, (1e9)*Psb[i])

sheet1.write(i, 3, (1e9)*Psc[i])

sheet1.write(i, 4, (1e9)*Psd[i])

i+=1

book1.save("Powers.xls")

def Ssweep(ls, i):

font = 'family' : 'Arial',

'weight' : 'normal',

'size' : 3.25

ls = [5e-7, 1e-6, 2e-6, 3e-6, 4e-6, 5e-6, 6e-6] nano-wire length in m

l = ls

ws = linspace(1e-9, 200e-9, 2000) nano-wire width in m

d = [5e-9, 10e-9, 20e-9, 30e-9, 40e-9, 50e-9, 100e-9] nano-wire thickness in m

Ssa = ws.copy()

Ssb = ws.copy()

Ssc = ws.copy()

Ssd = ws.copy()

Sse = ws.copy()

Ssf = ws.copy()

Ssg = ws.copy()

ls = 1e-6

for idx, w in enumerate(ws):

Ssa[idx] = Speed(l, w, d[0])
for idx, w in enumerate(ws):
Ssb[idx] = Speed(l, w, d[1])
for idx, w in enumerate(ws):
Ssc[idx] = Speed(l, w, d[2])
for idx, w in enumerate(ws):
Ssd[idx] = Speed(l, w, d[3])
for idx, w in enumerate(ws):
Sse[idx] = Speed(l, w, d[4])
for idx, w in enumerate(ws):
Ssf[idx] = Speed(l, w, d[5])
for idx, w in enumerate(ws):
Ssg[idx] = Speed(l, w, d[6])
fig, ax = plt.subplots(num=i, figsize=(1.4, 1.3), dpi=600, facecolor='w', edgecolor='k')
ax.plot((1e9)*ws, (1e12)*Ssa, 'ok', label = 'Thickness = 5nm', markersize = 0.05, fillstyle = 'full')
ax.plot((1e9)*ws, (1e12)*Ssb, '¡r', label = 'Thickness = 10nm', markersize = 0.05, fillstyle = 'full')
ax.plot((1e9)*ws, (1e12)*Ssc, '¿b', label = 'Thickness = 20nm', markersize = 0.05, fillstyle = 'full')
ax.plot((1e9)*ws, (1e12)*Ssd, '$^{g\prime}$, $label =\prime Thickness = 30nm\prime, markersize = 0.05, fillstyle =\prime full\prime$)
plt.plot((1e9)*ws, (1e6)*Pse, '-.', label = 'Thickness = 40nm', ms = 0.5)
plt.plot((1e9)*ws, (1e6)*Psf, '–', label = 'Thickness = 50nm', ms = 0.5)
plt.plot((1e9)*ws, (1e6)*Psg, '-,', label = 'Thickness = 100nm', ms = 0.5)
plt.ylabel('Switching speed (ps)')
plt.xlabel('Width (nm)')
plt.title('Length =
plt.rc('font', **font)
plt.legend(frameon=False, loc = (0.475,0.675), fontsize=3.25)
plt.tick$_p arams(labelsize = 3.25, direction =\prime in\prime, which =\prime both\prime)$
plt.axhspan(0.1, 1, color = 'blue', alpha = 0.1)
plt.text(15, 0.5, r'0.1$\leq \alpha \leq$1', fontsize = 25)
plt.xlim([0,25])
plt.ylim([0,12])
plt.tight$_l ayout()$
plt.legend()
return Ssa, Ssb, Ssc, Ssd, Sse, Ssf, Ssg
i=0
while(i ¡ 2000):
sheet2.write(i, 0, (1e9)*ws[i])
sheet2.write(i, 1, (1e9)*Ssa[i])
sheet2.write(i, 2, (1e9)*Ssb[i])
sheet2.write(i, 3, (1e9)*Ssc[i])
sheet2.write(i, 4, (1e9)*Ssd[i])

i+=1
book2.save("Speeds.xls")
def main():
al = linspace(0.1, 50, 100)
bl = linspace(35, 150, 10)
$t1_rql = al.copy()$
$P1_rql = al.copy()$
$t1_sfq = al.copy()$
$P1_sfq = al.copy()$
$t1_qps = al.copy()$
$P1_qps = al.copy()$
$t2_rql = al.copy()$
$P2_rql = al.copy()$
$t2_sfq = al.copy()$
$P2_sfq = al.copy()$
$t2_qps = al.copy()$
$P2_qps = al.copy()$
$t3_rql = al.copy()$
$P3_rql = al.copy()$
$t3_sfq = al.copy()$
$P3_sfq = al.copy()$
$t3_qps = al.copy()$
$P3_qps = al.copy()$
$t4_rql = al.copy()$
$P4_rql = al.copy()$
$t4_sfq = al.copy()$
$P4_sfq = al.copy()$
$t4_qps = al.copy()$
$P4_qps = al.copy()$
font = 'family' : 'Arial',
'weight' : 'normal',
'size' : 12
for idx, a in enumerate(al):
$t1_rql[idx], P1_rql[idx] = rql(a, 380)$
$t1_sfq[idx], P1_sfq[idx] = sfq(a, 380)$
$t1_qps[idx], P1_qps[idx] = qps(a, 380)$
$t2_rql[idx], P2_rql[idx] = rql(a, 550)$
$t2_sfq[idx], P2_sfq[idx] = sfq(a, 550)$
$t2_qps[idx], P2_qps[idx] = qps(a, 550)$
$t3_rql[idx], P3_rql[idx] = rql(a, 720)$
$t3_sfq[idx], P3_sfq[idx] = sfq(a, 720)$
$t3_qps[idx], P3_qps[idx] = qps(a, 720)$
$t4_rql[idx], P4_rql[idx] = rql(a, 1000)$
$t4_sfq[idx], P4_sfq[idx] = sfq(a, 1000)$
$t4_qps[idx], P4_qps[idx] = qps(a, 1000)$

fig, ax = plt.subplots(num=10, figsize=(2.8, 2.6), dpi=300, facecolor='w', edgecolor='k')
ax.plot((1e9)*P1$_s fq$, (1e12)*$t1_s fq$,$' bD'$, $label =' \ Powerperswitcheventin JJ'$, $ms = 1, lw =$
1)
ax.plot((1e9)*P1$_r ql$, $(1e12) * t1_r ql$,$' -ro'$, $label =' \ RQL'$, $ms = 5$)
ax.plot((1e9)*P1$_q ps$, $(1e12) * t1_q ps$,$' k'^{,label=' Powerperswitcheventin QPSJ',ms=1,lw=1)}$
ax.plot((1e9)*P2$_r ql$, $(1e12) * t2_r ql$,$' -ro'$, $ms = 5$)
ax.plot((1e9)*P2$_q ps$, $(1e12) * t2_q ps$,$' k'^{,ms=1,lw=1)}$
ax.plot((1e9)*P2$_s fq$, $(1e12) * t2_s fq$,$' bD'$, $ms = 1, lw = 1$)
ax.plot((1e9)*P3$_r ql$, $(1e12) * t3_r ql$,$' -ro'$, $ms = 5$)
ax.plot((1e9)*P3$_q ps$, $(1e12) * t3_q ps$,$' k'^{,ms=1,lw=1)}$
ax.plot((1e9)*P3$_s fq$, $(1e12) * t3_s fq$,$' bD'$, $ms = 1, lw = 1$)
ax.plot((1e9)*P4$_r ql$, $(1e12) * t4_r ql$,$' -ro'$, $ms = 5$)
ax.plot((1e9)*P4$_q ps$, $(1e12) * t4_q ps$,$' k'^{,ms=1,lw=1)}$
ax.plot((1e9)*P4$_s fq$, $(1e12) * t4_s fq$,$' bD'$, $ms = 1, lw = 1$)
plt.tick$_p arams(labelsize = 6.5, direction =' \ in', which =' \ both')$
plt.xlabel('Power (nW)', fontsize=7)
plt.ylabel('Delay (ps)', fontsize=7) plt.rc('font', **font)
plt.yscale('log')
plt.xscale('log')
plt.xlim([0.02,20])
plt.ylim([0.02,1200])
plt.legend(frameon=False, loc = (0.01,0.75), fontsize=7)
plt.tight$_l ayout()$
ax.tick$_p arams(direction =' \ in', length = 6, width = 2, colors =' \ black')$
ls = [2e-6]
[5e-7, 1e-6, 2e-6, 3e-6]
, 4e-6, 5e-6, 6e-6] nano-wire length in m
for idx, l in enumerate(ls):
Psweep(l, idx)
for idx, l in enumerate(ls):
Ssweep(l, idx+2)
if$_{name_{==''_{main_{''}:}}}$
main()
plt.show()

Appendix C

The programs below are used to estimate the energy dissipation in adiabatic quantum charge parametron circuits detailed in Chapter 6 of this dissertation. The various plots that describe the adiabatic switching are calculated using the python programs below:

Name: Adiabatic quantum charge parametron

Purpose: Calculate switching energy of AQCP to aid developing adiabatic operation by adding parameters

Author: Uday Goteti

Created: 05/01/2017

Last edited: 05/01/2017

```
from numpy import *
from math import *
import matplotlib.pyplot as plt
from matplotlib.widgets import *
def Uaqcp(q_out, q_ex) :
Es = 1 Normalized (set to 1) - can be made a variable later
B_L = 1Effectofthisparameterisyettobeinvestigatedforadiabaticoperation
q_in = 0inputiszero
U = Es*(((q_out - q_in) * (q_out - q_in))/B_L - 2 * cos(q_out) * cos(q_ex))
return U
def main():
font = 'family' : 'serif',
'weight' : 'normal',
'size' : 7
q_outs = linspace(-pi, pi, 1000)
q_ex = [0, pi/4, pi/2, 3 * pi/4, pi]
Ua = q_outs.copy()
Ub = q_outs.copy()
Uc = q_outs.copy()
Ud = q_outs.copy()
Ue = q_outs.copy()
for idx, q_outinenumerate(q_outs) :
Ua[idx] = Uaqcp(q_out, q_ex[0])
for idx, q_outinenumerate(q_outs) :
Ub[idx] = Uaqcp(q_out, q_ex[1])
for idx, q_outinenumerate(q_outs) :
Uc[idx] = Uaqcp(q_out, q_ex[2])
```

```
for idx, q_outinenumerate(q_outs) :
Ud[idx] = Uaqcp(q_out, q_ex[3])
for idx, q_outinenumerate(q_outs) :
Ue[idx] = Uaqcp(q_out, q_ex[4])
plt.figure(num=1, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
plt.plot(q_outs * (180/pi), Ua,' red', label =' q_ex = 0', ms = 1)
plt.plot(q_outs * (180/pi), Ub,' blue', label =' q_ex =π/4', ms = 1)
plt.plot(q_outs * (180/pi), Uc,' green', label =' q_ex =π/2', ms = 1)
plt.plot(q_outs * (180/pi), Ud,' black', label =' q_ex = 3π/4', ms = 1)
plt.plot(q_outs * (180/pi), Ue,' black', label =' q_ex =π', ms = 1)
plt.ylabel('Normalized U_AQCP')
plt.xlabel('Output charge angle q_out (degrees)')
plt.rc('font', **font)
plt.legend(frameon=False)
plt.tight_layout()
if _name_=="_main_":
main()
plt.show()
```

Appendix D

Calculate switching energy of AQCP to aid developing adiabatic operation by adding parameters - with 2 control parameters //

———————————————————————————————————————- ———

Name: Adiabatic quantum charge parametron - modified circuit

Purpose: Calculate switching energy of AQCP to aid developing adiabatic operation by adding parameters - with 2 control parameters

Author: Uday Goteti

Created: 11/06/2017

Last edited: 11/06/2017

———————————————————————————————————————-

from numpy import * //

from math import * //

import matplotlib.pyplot as plt //

from matplotlib.widgets import * //

def Uaqcp(qp,q,q_ex, B_L, B_q) : //

Es = 1 Normalized (set to 1) - can be made a variable later //

$B_L = 3Effectofthisparameterisyettobeinvestigatedforadiabaticoperation$

$q_in = 3inputiszero$

$B_q = 1$

qp = (q1 + q2)/2 (q1 + q2)/2 - may need to modify later

$q_= (q1 - q2)/2(q1 - q2)/2 - mayneedtomodifylater$

U = Es*(((q$_e$x−$q_)$*(q_ex−$q_)$)/B_L+((q_in−qp)*(q_in−qp))/(B_L+2∗B_q)−2∗$cos(q_)$∗$cos(qp)$)

return U

def beta$_p arам(q_ex)$: $font = 'family' :' serif'$,

'weight' : 'normal',

'size' : 7

$B_Ls = linspace(0.001, 10, 10)$

$B_qs = linspace(0.001, 20, 10)$

qp = 1

$q_=1$

U = [[0 for x in range(1000)] for y in range(1000)]

for idx, $B_Linenumerate(B_Ls)$:

for idy, $B_qinenumerate(B_qs)$:

U[idx][idy] = Uaqcp(qp,q,q_ex, B_L, B_q)

return U, B_Ls, B_qs

def main():

font = 'family' : 'serif',

'weight' : 'normal',
'size' : 7
$\mathrm{B}_L s = linspace(0.001, 10, 10)$
$\mathrm{B}_q s = linspace(0.001, 20, 10)$
$\mathrm{B}_L = 20$
$\mathrm{B}_q = 10$
qp = 1
$\mathrm{q}_{=}1$
qps = linspace(-4, 4,1000)
$\mathrm{q}_s = linspace(-4, 4, 1000)$
$\mathrm{q}_e x = [0, pi/4, pi/2, 3 * pi/4, pi, 5 * pi/4, 3 * pi/2, 7 * pi/4, 2 * pi]$
$\mathrm{q}_e x = [0]$
Ua = [[0 for x in range(1000)] for y in range(1000)]
Ub = [[0 for x in range(1000)] for y in range(1000)]
Uc = [[0 for x in range(1000)] for y in range(1000)]
Ud = [[0 for x in range(1000)] for y in range(1000)]
Ue = [[0 for x in range(1000)] for y in range(1000)]
Uf = [[0 for x in range(1000)] for y in range(1000)]
Ug = [[0 for x in range(1000)] for y in range(1000)]
Uh = [[0 for x in range(1000)] for y in range(1000)]
Ub = a.copy()
Uc = a.copy()
Ud = q.$copy()$
Ue = q.$copy()$
for idx, qp in enumerate(qps):
for idy, $\mathrm{q}_i nenumerate(q_s)$:
Ua[idx][idy] = Uaqcp(qp,q,$q_e x[0], B_L, B_q$)
Ub[idx][idy] = Uaqcp(qp,q,$q_e x[1], B_L, B_q$)
Uc[idx][idy] = Uaqcp(qp,q,$q_e x[2], B_L, B_q$)
Ud[idx][idy] = Uaqcp(qp,q,$q_e x[3], B_L, B_q$)
Ue[idx][idy] = Uaqcp(qp,q,$q_e x[4], B_L, B_q$)
Uf[idx][idy] = Uaqcp(qp,q,$q_e x[5], B_L, B_q$)
Ug[idx][idy] = Uaqcp(qp,q,$q_e x[6], B_L, B_q$)
Uh[idx][idy] = Uaqcp(qp,q,$q_e x[7], B_L, B_q$)
for idx, $\mathrm{q}_o utinenumerate(q_o uts)$:
Uc[idx] = Uaqcp($\mathrm{q}_o ut, q_e x[2]$)
for idx, $\mathrm{q}_o utinenumerate(q_o uts)$:
Ud[idx] = Uaqcp($\mathrm{q}_o ut, q_e x[3]$)
for idx, $\mathrm{q}_o utinenumerate(q_o uts)$:
Ue[idx] = Uaqcp($\mathrm{q}_o ut, q_e x[4]$)
plt.figure(num=1, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
meshgrid(B_L, B_q)
CS = plt.contourf(qps, $\mathrm{q}_s, Ua, 10, origin =' lower')' red', label =' q_e x = 0', ms = 1$)
plt.colorbar(CS)
plt.figure(num=2, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')

CS2 = plt.contourf(qps, $q_s, Ub, 10, origin =' lower'$)
plt.colorbar(CS2)
plt.figure(num=3, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS3 = plt.contourf(qps, $q_s, Uc, 1000, origin =' lower'$)
plt.colorbar(CS3)
plt.figure(num=4, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS4 = plt.contourf(qps, $q_s, Ud, 1000, origin =' lower'$)
plt.colorbar(CS4)
plt.figure(num=5, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS5 = plt.contourf(qps, $q_s, Ue, 10, origin =' lower'$)
plt.colorbar(CS5)
plt.figure(num=6, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS6 = plt.contourf(qps, $q_s, Uf, 10, origin =' lower'$)
plt.colorbar(CS6)
plt.figure(num=7, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS7 = plt.contourf(qps, $q_s, Ug, 10, origin =' lower'$)
plt.colorbar(CS7)
plt.figure(num=8, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS8 = plt.contourf(qps, $q_s, Uh, 10, origin =' lower'$)
plt.plot($q_o uts * (180/pi), Ub,' blue', label =' q_e x = \pi/4$', ms = 1)
plt.plot($q_o uts * (180/pi), Uc,' green', label =' q_e x = \pi/2$', ms
= 1)
plt.plot($q_o uts * (180/pi), Ud,' black', label =' q_e x = 3\pi/4$', ms = 1)
plt.plot($q_o uts * (180/pi), Ue,' black', label =' q_e x = \pi$', ms = 1)
plt.colorbar(CS8)
plt.ylabel('q+ = (q1+q2)/2')
plt.xlabel('q- = (q1-q2)/2')
plt.clabel(CS, 'Normalized potential energy (E/Es)')
plt.rc('font', **font)
plt.legend(frameon=False)
plt.$tight_l ayout()$
def main():
$q_e xs = [0, pi/4, pi/2, 3 * pi/4, pi, 5 * pi/4, 3 * pi/2, 7 * pi/4, 2 * pi]$
for idx, $q_e xinenumerate(q_e xs)$:
U, $B_L s, B_q s = beta_p aram(q_e x)$
plt.figure(num=idx, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
CS = plt.contourf($B_L s, B_q s, U, origin =' lower'$)
if $_n ame_{==" _m ain_"}:$
main()
plt.show()

Appendix E

The program below is an extension of the previous program to allow calculation of energy dissipation per adiabatic switching related to physical dimensions and material of the QPSJ.

Name: QPSJ switching times and power-delay

Purpose: Calculation of switching times and power of QPSJ as a function of junction dimensions

Author: Uday Goteti

Created: 06/26/2017

Last edited: 06/26/2017

```
from numpy import *
from math import *
import matplotlib.pyplot as plt
from matplotlib.widgets import *
from QPSJ_parametersimport*
def Taqfp():
phi0 = 2.067833758e-15
IcRn = 1.6e-3
Taqfp = phi0/(IcRn)
return Taqfp
def Eaqfp(a,b,Taqfp):
phi0 = 2.067833758e-15
Ic = a*1e-6
Trf = b*1e-9
Tsw = Taqfp
Eaqfp = 2*Ic*phi0*(Tsw/Trf)
return Eaqfp
def Taqcp(c,d):
q0 = 3.20435324e-19
Vc = c*1e-3
Rn = d*1e3
Taqcp = q0*Rn/Vc
return Taqcp
def Eaqcp(b,c,Taqcp):
q0 = 3.20435324e-19
Vc = c*1e-3
Tsw = Taqcp
```

```
Trf = b*1e-9
Eaqcp = 2*q0*Vc*(Tsw/Trf)
return Eaqcp
def main():
font = 'family' : 'serif',
'weight' : 'normal',
'size' : 7
Trf = linspace(0.001,10,1000)
Ics = [100,200,300,400,5000]
Vcs = [0.2,0.4,0.6,0.8,1]
Rns = [0.5,1,2,5,10]
Tj = Taqfp()
Tq = Taqcp(Vcs[1],Rns[4])
Ej = Trf.copy()
Eq1 = Trf.copy()
Eq2 = Trf.copy()
Eq3 = Trf.copy()
Eq4 = Trf.copy()
Eq5 = Trf.copy()
Eb1 = Trf.copy()
Eb2 = Trf.copy()
for idx, T in enumerate(Trf):
Ej[idx] = Eaqfp(Ics[0],T,Tj)
Eq1[idx] = Eaqcp(T,Vcs[0],Tq)
Eq2[idx] = Eaqcp(T,Vcs[1],Tq)
Eq3[idx] = Eaqcp(T,Vcs[2],Tq)
Eq4[idx] = Eaqcp(T,Vcs[3],Tq)
Eq5[idx] = Eaqcp(T,Vcs[4],Tq)
Eb1[idx] = kbt(4.2)
Eb2[idx] = kbt(0.1)
plt.figure(num=1, figsize=(3.3, 3.1), dpi=300, facecolor='w', edgecolor='k')
plt.plot(Trf, Ej, '-o', label = 'AQFP', ms = 3)
plt.plot(Trf, Eq1, '-o', label = 'Vc=0.2mV', ms = 3)
plt.plot(Trf, Eq2, '-*', label = 'Vc=0.4mV', ms = 3)
plt.plot(Trf, Eq3, '-d', label = 'Vc=0.6mV', ms = 3)
plt.plot(Trf, Eq4, '-D', label = 'Vc=0.8mV', ms = 3)
plt.plot(Trf, Eq5, '-x', label = 'Vc=1mV', ms = 3)
plt.plot(Trf,Eb1, 'r-', label = 'Kb*T at 4.2K')
plt.plot(Trf,Eb2, 'b-', label = 'Kb*T at 2K')
plt.ylabel('Energy(J)')
plt.xlabel('Excitation time(ns)')
plt.title('Length =
plt.yscale('log')
plt.xscale('log')
plt.rc('font', **font)
```

```
plt.legend(frameon=False)
plt.title('Rn = 10kΩ')
plt.tight_layout()
if __name__=="__main__":
main()
plt.show()
```