The Effects of Aging on Doped Lead-Free Solder under Thermal Shock and Thermal Cycling

by

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Abstract

In this experiment, the thermal shock performance of various doped Pb-free solder pastes on Ball Grid Array (BGA) packages and resistors were observed in order to determine their reliability. This investigation is based on evaluating the potential substitutes to replace the SAC305 solder paste which has deleterious effects in long term isothermal aging conditions. The effects of doping SAC305 solder balls with small amounts of Bismuth (Bi), Indium (In), Manganese (Mn), Nickel (Ni), and Antimony (Sb) either directly or via the solder paste used for assembly have been studied. Packages used for testing were SMR 2512, QFN's, 6mm BGA, 15mm BGA, 31mm BGA, and 35mm BGA. The test results have led to a downselection of optimum material combinations that offer a potential solution to the well-known material degradation of SAC305 solder alloys with aging. The test conditions had two different time/temperature periods: After assembly (No aging) and an accelerated aging condition of 6 months at 125°C. Each test board was temperature shocked 3000 times (−40°C to 125°C) with a 15-minute thermal profile (5-minute dwell time and 2.5-minute transition time). The electrical continuity of solder interconnect was examined during the tests. The failure analysis shows recrystallized-assisted crack nucleation in the solder joints. Solder materials that showed higher thermal shock reliability and reduced degradation in characteristic lifetime after aging compared with SAC305 were chosen for the next phase of the test which is Phase II.

Phase II considers the long term aging effects of Pb-free solders with higher thermal shock reliability. Isothermal aging at 75°C for 6, 12, and 24 months were used. The board substrate for Phase II was Megtron6. The test vehicles were comprised of surface mount resistors, 5mm, 6mm, 13mm, 15mm, 17mm, 31mm, 35mm, and 45mm BGA packages. The assemblies were subjected

to thermal cycles of -40°C to +125°C with a 120-minute thermal profile with a 15-minute dwell time and 45-minute transition time. Solder pastes have lower degradation as measured by characteristic lifetime after 24 months of aging at 75°C compared with Sn-3Ag-0.5Cu (SAC305) and tin-lead (SnPb) solder pastes [1]. A high level of degradation was seen for the SAC305 solder paste throughout the test from Phase I. Failure analysis indicated that crack propagation occurred at the top and bottom of the solder joint. The only material from Phase II to outperform the materials in TC-Phase I (SAC305 and SnPb) for the 24-month aged group was Sn-4Ag-0.5Cu-0.05Ni solder paste which exhibited a much lower degradation rate (17%). According to these results, Sn-4Ag-0.5Cu-0.05Ni solder paste performed best across all BGA design. The materials performed much differently when used with the 2512 resistors. Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni pastes were the top performing materials for the 2512 resistors but performed poorly for BGA components. Sn-4Ag-0.5Cu-0.05Ni proved to be the worst material for 2512 resistors.

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List of Abbreviations

AOI	Automated Optical Inspection
BGA	Ball Grid Array
BSE	Back-Scattered Electron
CABGA	Chip Array Ball Grid Array
CDF	Cumulative Distribution Function
CTE	Coefficient of Thermal Expansion
CVBGA	Very thin Chip Array Ball Grid Array
DNP	Distance to Neutral Point
DFR	Decreasing Failure Rate
EDX	Energy Dispersive X-ray spectroscopy
ENIG	Electroless Nickel Immersion Gold
ENEPIG	Electroless Nickel Electroless Palladium Immersion Gold
FEA	Finite Element Analysis
FR	Flame Retardant
GPIB	General Purpose Interface Board
HASL	Hot Air Solder Leveling
ICT	In-Circuit Testing
IMC	Intermetallic Compound
ImAg	Immersion Silver
ImSn	Immersion Tin

LLTS	Liquid to Liquid Thermal Shock
MTTF	Mean Time to Failure
OSP	Organic Solderability Preservative
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PDF	Probability Density Function
PLCC	Plastic-Leaded Chip Carrier
QFN	Quad-Flat No leads
SAC	Tin (Sn) – Silver (Ag) – Copper (Cu)
SBGA	Super Ball Grid Array
SEM	Scanning Electron Microscope
SMR	Surface Mount Resistor
SnPb	Tin – Lead
TAB	Tape Automatic Bonding
TAL	Time above Liquidus
TC-SJR	Thermal Cycling – Solder Joint Reliability
TV	Test Vehicle
UTS	Ultimate Tensile Strength

List of Symbols

Ag	Silver
Bi	Bismuth
Cu	Copper
Co	Cobalt
Fe	Iron
In	Indium
Mn	Manganese
Ni	Nickel
Pb	Lead
Sb	Antimony
Sn	Tin
SAC305	96.5%Sn-3.0%Ag-0.5%Cu solder

Chapter 1 Introduction to Electronic Packaging

1.1 Electronic Packaging

Electronics is an enormous and ubiquitous industry in the world. It is highly instrumental in the development of science, technology, manufacturing and overall economy of participating countries [2]. After the development of the Integrated Circuit (IC), industries developed proclivity towards miniaturization of electronic devices that are used in our everyday lives [3]. Examples include the transformation from earlier versions of computers that operated on transistors to handheld devices such as smartphones and wearable electronics. The electronic products are primarily utilized to process different types of information. The processing of information can solely be achieved by a system comprised of semiconductors that are interconnected, powered, cooled, and protected by packaging [2]. The term "packaging" is often misunderstood by engineers where they associate packaging with product shipment. Electronic packaging refers to "installation and connection of many electronic and electro-mechanical components in an enclosure which protects the system from the environment and provides access for maintenance" [4]. Electronic packaging provides four major functions consisting of [4]:

1. Electrical signal interconnection
2. Mechanical and environmental protection
3. Power distribution
4. Heat dissipation

Figure 1.1 illustrates different levels of electronic packaging. The initial stage of electronic packaging includes dicing of a silicon wafer into a chip and then fabricating the diced chip using photolithographic techniques. The chip embodies electronic devices such as resistors, transistors, etc. with organized interconnections constituting an Integrated Circuit (IC) that performs desired electrical function [4].

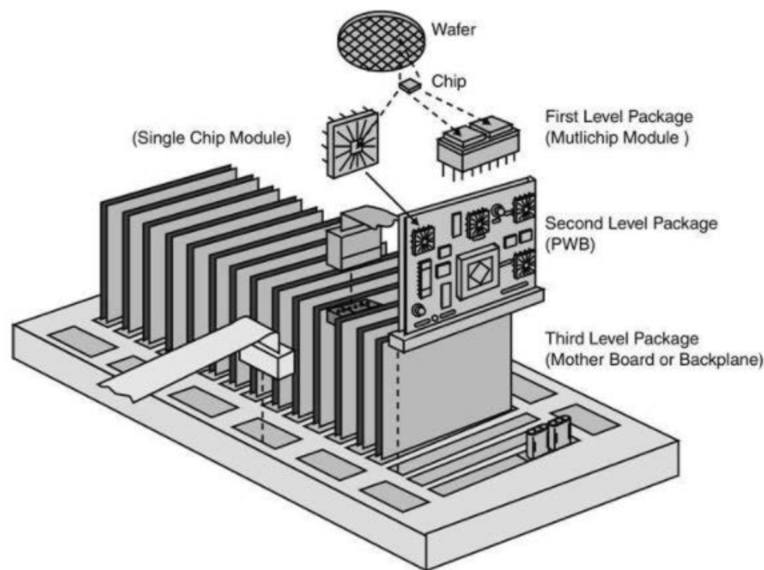


Figure 1.1 Levels of packaging in electronic system [5]

After testing, the chip is accommodated in a chip carrier, and wire bonding or solder balls are used to form electrical connection between the chip and the carrier. The chip carrier indicates the First-Level package as shown in the above figure, and the electrical connection to the chip carrier is the First-Level of interconnect. The Second-Level package mentioned in the figure refers to placement of several chip carriers on a substrate (Printed Circuit Board) and interconnecting together through wire traces on the board is the Second-Level of interconnect. The Third-Level

package includes insertion of edge connectors on circuit board into a motherboard that permits communication from one circuit board to another [4].

1.2 Chip Carriers

The primary function of the chip carrier (IC package) is to safeguard the chip from mechanical stress, environment (humidity and pollution) and electrostatic discharge during handling. Additionally, it acts as a mechanical interface for testing, burn-in and electrical interconnection through pins, leads or pads which serve as a foundation for solder joints. The chip carrier must comply with all device performance requirements such as electrical, thermal, quality, reliability and cost objectives. The chip carriers appear in variety of lead arrangements and mounting types that are classified into families defined by method of mounting to boards. They are Through Hole Mount (THM) and Surface Mount (SM) [2], [4]. There are different packages that falls under those families as shown in Figure 1.2.

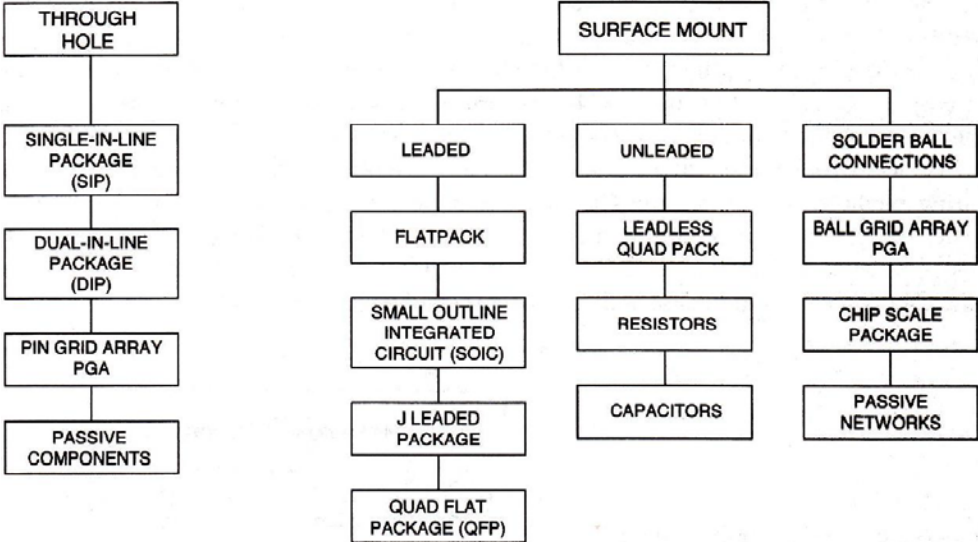


Figure 1.2 Chip carrier package design [4]

1.2.1 Through Hole Mount Package

Through Hole Mount (THM) refers to the mounting type where the leads on the chip carrier are inserted into the holes drilled in the Printed Circuit Board (PCB). The illustration of Through Hole Mount is shown below.

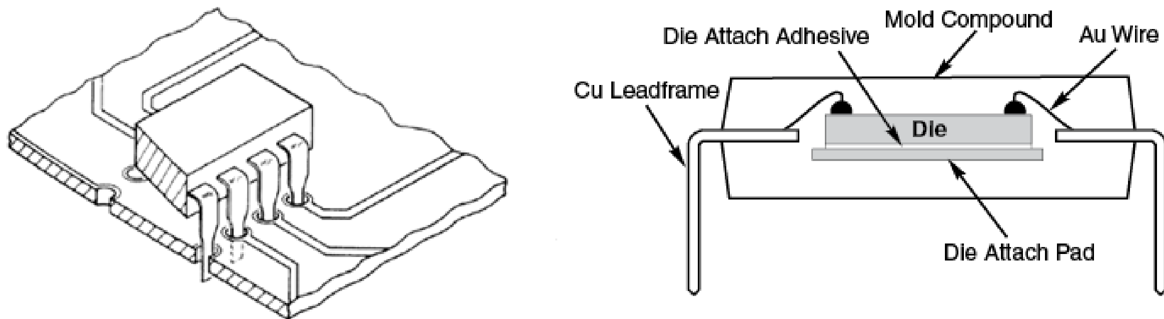


Figure 1.3 Through Hole chip carrier mounted on board (left) [4], Cross-section view of Through Hole chip carrier (right) [6]

The chip (die) is connected through tape wire bonding to the lead that are extended from the package as shown in Figure 1.3. The extended leads are embedded into the board through plated-through-hole. Then the leads are cut out at the back side of a board after they are clinched onto the board. The clinched lead can hold the package before the wave soldering process. The mechanical and electrical connections between the chip carrier and the board are formed via solder joints created after soldering. Also, this chip carrier can be inserted onto a breadboard for electrical testing.

Through Hole chip carriers consist of different packages such as Dual-In-Line Package (DIP), Single-In-Line Package (SIP), and Pin Grid Array (PGA) as shown in Figure 1.4. The DIP as seen in Figure 1.4a embodies two rows of pins with a lead pitch of 2.54 mm (100 mil) along the longer side of the rectangular package and row spacing of 7.62 mm. It is generally used for

microprocessor, microcontrollers, digital, and analog circuits. The DIPs are available in a variety of sizes depending on the usage and I/O ranging from 8 to 64.

The SIP shown in Figure 1.4b is identical to the DIP except it consists of a single row of pins with a lead pitch similar to standard DIP. The SIP is used to enclose chips with a lower I/O count. The variation of SIP includes Zigzag in-line package (ZIP) as shown in Figure 1.4c. The pins are narrow and staggered to reduce lead pitch to 1.27mm (50mil).

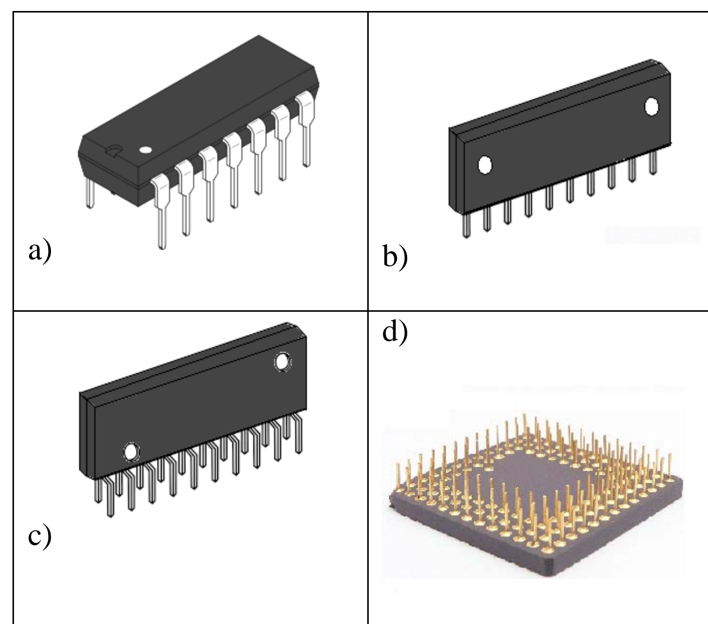


Figure 1.4 a) Dual In-line Package [7], b) Single In-Line Package [8], c) Zigzag In-Line Package [9], d) Pin Grid Array [10]

The advantage of using DIPs include lower cost of implementation and reduced engineering effort [11]. The disadvantage of DIPs is poor area efficiency because the lead pins have a pitch size of 2.54 mm and are only deployed on both sides of the package. Second, for the I/O count greater than 64, this package is not a wise option as the standard I/O count of DIPs is limited to 64. This package requires the solder pad's outside diameter of 1.27 mm (50 mil) to be drilled on PCB. Since the lead pitch is about 2.54 mm (100 mil), the pads leaves about 50 mil for

the wiring channel between pins which is an issue to provide more than three wiring traces per channel. The third disadvantage of using DIPs is poor wirability [4].

Another THM Chip Carrier known as a Pin Grid Array (PGA) as shown in Figure 1.4d serves as a better alternative to the DIP since it can be used for higher I/O count or requirement of lower thermal resistance. The body of chip carrier is fabricated from organic material, Bismaleimide Triazine (BT), or ceramic (multilayer alumina) depending on sealing requirement. The pin diameters are 0.51 to 0.64 mm (20 to 25 mil). The advantages of using a PGA package are higher I/O count and they can be designed to couple directly with heat frame through heatsink. The disadvantages include higher production cost for multilayered ceramic due to its limited supply and higher cost of production for PCB because it demands drilling and plating a large number of holes for pin [4].

1.2.2 Surface Mount Packages

The electronics industries implemented Surface Mount (SM) packages during 1980s in order to accomplish higher board density and better electrical performance. The demand for SM packages exceeded that of THM packages in 1990s. Surface Mount Technology (SMT) refers to an attachment of the chip carrier on the copper pad coated with solder paste and the solder interconnect is created through Reflow soldering. This technology eliminates the need for through hole per lead thereby reducing the vias (plating holes) and board layers. This technology also allows the components to be placed on both sides of the board that can increase the space for additional components. The SM packages can be used for higher pin counts where leads are used on all four sides of the package. There are different types of SM packages depending on the type

of leads used for I/O from the chip carrier. They include leaded package, leadless package, and Ball Grid Array (BGA) package.

1.2.2.1 Leaded Package

The common leaded packages that are available are J lead packages and Gull wing packages as seen in Figure 1.5. The J lead packages fold the lead into a small pocket under the package mitigating lead deformation while shipping and handling. The J lead package can be positioned on the board, bond them with solder paste, and create solder joints after subjecting the boards to IR or vapor phase reflow soldering [4]. The J lead with pocket protecting lead and solder joint connection can be seen in Figure 1.5b.

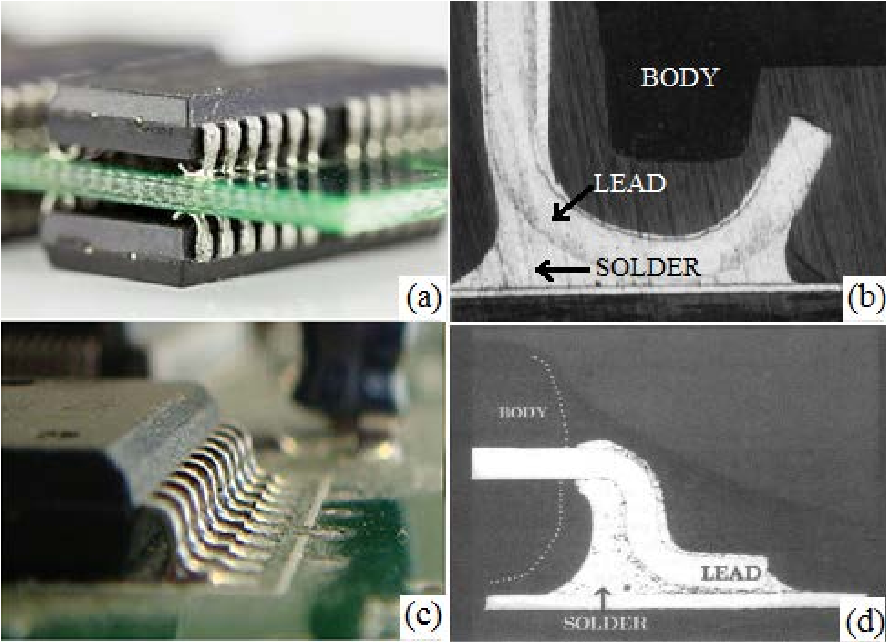


Figure 1.5 a) J lead package [12], b) Cross-section of J lead package [4], c) Gull wing package (right) [13], Cross-section of gull wing package [4]

The only available pitch size for J lead is 1.27 mm (50 mil). It can only be used up to 84 pins. Another leaded package is Gull Wing package as shown in Figure 1.5c, where the leads bend down and out, is used for lower and higher pin count packages. The lead pitch varies between 0.5 mm to 1.27 mm (20 mil to 50 mil). Figure 1.6 shows different families of leaded packages.

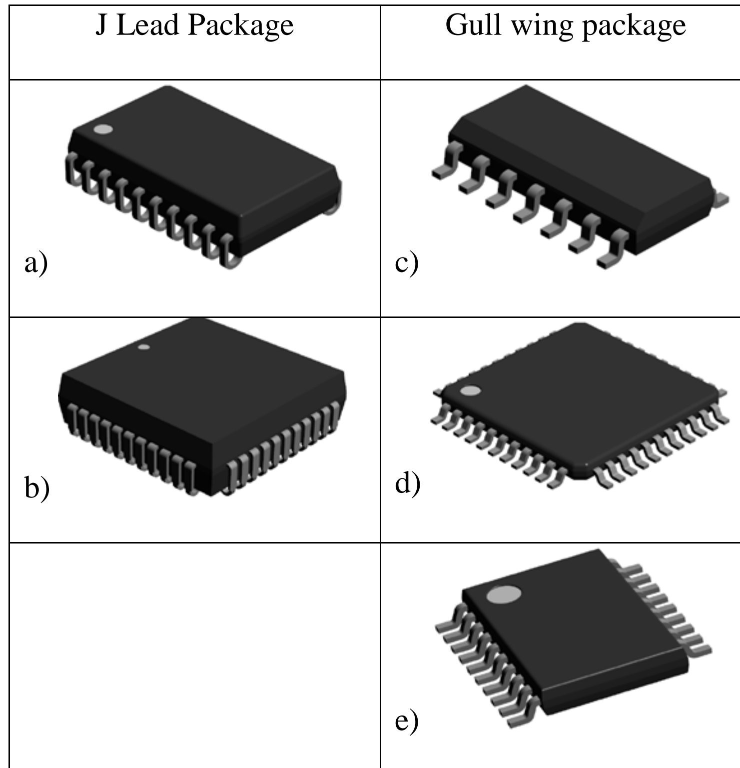


Figure 1.6 a) Small Outline J Lead (SOJ), b) Quad Flat J Lead package, c) Small Outline Integrated Circuit (SOIC), d) Quad Flat Lead package, e) Thin Small Outline Package (TSOP) [14]

Small Outline J Lead (SOJ) is a typical J lead package which has lead on both sides of the package. The Quad Flat J Lead package is also known as Plastic Leaded Chip Carrier (PLCC). Quad Flat Lead package incorporates lead on all four sides. It is not possible to have higher lead pins in bigger packages due to difficulty in maintaining flatness of package to ensure all leads are in contact with the solder pad. Small Outline Integrated Circuit (SOIC) shown in Figure 1.6c have

gull wing leads on both sides of the package. The Thin Small Outline Package in Figure 1.6e is a smaller and lighter package that is commonly used in portable electronics.

The advantages of using a gull wing package include their compatibility with almost any reflow soldering process, their good ability to self-align during reflow, and their compatibility towards finer pitch packages. The disadvantages are difficulty in solder joint inspection compared with J Lead, fragility, and susceptibility to lead coplanarity and lead bending. The shipping and handling are better with J lead package. J lead packages have a higher profile than gull wing packages which is a disadvantage for packages with lower profile [15].

1.2.2.2 Leadless Package

Leads in leaded packages are fragile and can be deformed during shipping and handling. This issue has been eradicated by replacement of leads with metallized pads fixed on the chip package. These metallized pads have a pitch size of 1.27 mm (50 mil) which makes it an area-efficient package.

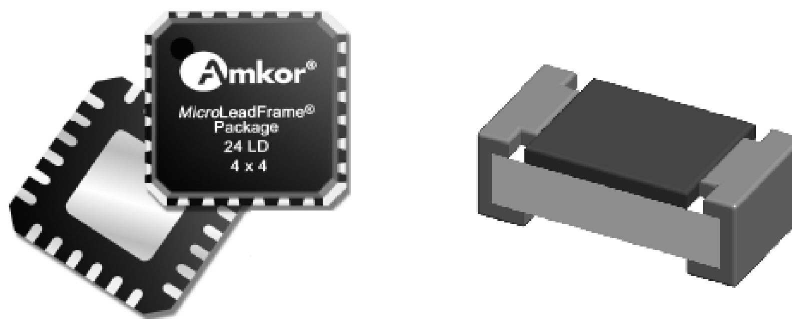


Figure 1.7 Leadless packages a) Quad Flat No lead package (left) [16], b) Surface Mount Resistor (right) [14]

The metallized pads under the package are placed directly on the copper pad coated with solder paste on PCB before reflow. The common leadless packages are Quad Flat No lead (QFN) and Surface Mount Resistors (SMR). The typical QFN package used is Micro Lead Frame (MLF), as shown in Figure 1.7a, and its cross-section is shown in Figure 1.8a.

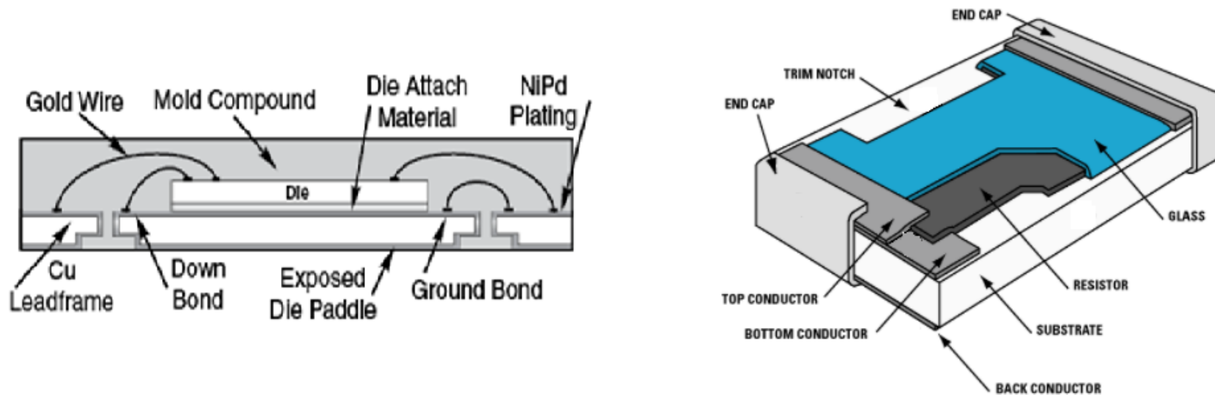


Figure 1.8 Cross-section view of leadless packages a) Micro Lead Frame (MLF) package [16], b) Surface Mount Resistor (SMR) [17]

The exposed thermal pad (die paddle) on the bottom enhances the thermal and mechanical properties of the package. Also, the pad efficiently conducts heat to the PCB and provides a stable ground through down bonds and electrical connections through the conductive die attach material. The advantage of this package include small size and weight as well as excellent thermal and mechanical properties [18]. For the QFN package, the height of the solder paste starts at a few mils and the solder paste slumps during reflow soldering; the height of the package is quite low. Due to its low height, it can be a disadvantage for larger packages, as cleaning the flux residue between PCB and the package gets difficult [4], [15].

1.2.2.3 Ball Grid Array Package

The Ball Grid Array (BGA) is similar to the PGA package except it has solder balls instead of leads underneath the package as shown in Figure 1.9. The connection between the chip carrier and the board is through the solder balls underneath the package. The BGA solder balls can have a pitch size lesser than that of leadless and leaded packages, making it a better advantage. The diameter of the solder ball differs from 0.5 mm to 0.89 mm (20 mil to 35 mil). The pitch sizes available for BGA are 0.8 mm (32 mil), 1 mm (40 mil), 1.27 mm (52 mil), and finer pitches.

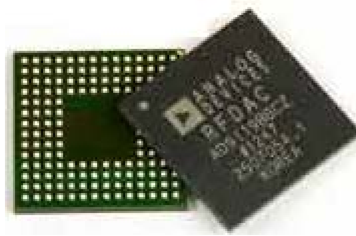


Figure 1.9 Top and bottom view of BGA package

There are a variety of BGA packages where the die for all types is connected to its substrate by Tape Automatic Bonding (TAB) or connected through flip chip direct attachment, as shown in Figure 1.10.

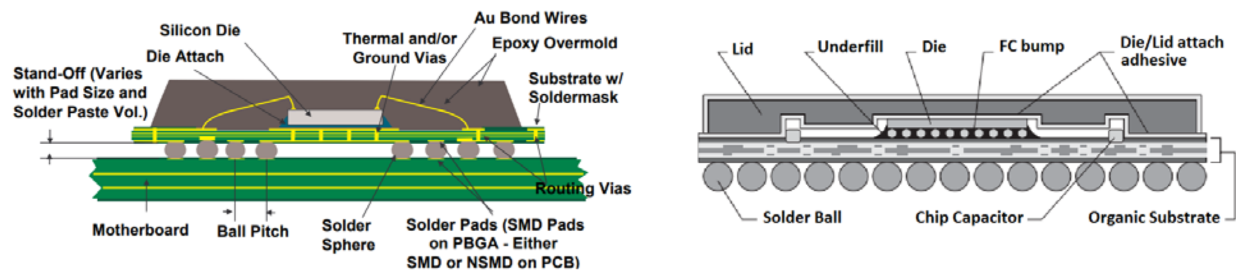


Figure 1.10 Cross-section view of a) PBGA (left), b) Flip chip BGA (right)

In PBGA packages, the gold wires are used in TAB for connecting die to a wiring pad on the package substrate. The wiring connections are made using vias to carry signals from one layer to another in the substrate. The connection between the PBGA package and the board substrate is formed through solder balls during reflow soldering. The number of I/O in PBGA packages varies depending on the pitch and package dimension.

For Flip Chip BGA shown in Figure 1.10, the conductive bump is placed on the die surface. Then it is flipped and placed face down, so the interconnection is formed between the die and package through the conductive bump. The advantages of BGA package include

- Smaller size, lower in weight and cost
- Higher I/O capability than leaded and leadless packages
- Enhanced heat dissipation

The manufacturing advantages of BGA are

- Lower coplanarity issues
- Ability to self-align during reflow
- Reduced solder bridging during paste printing
- Mitigation of handling issues compared with leaded package
- Higher yield after assembly

There are disadvantages of using BGA packages. It is not feasible to rework individual solder joints after assembly. It is also difficult to inspect the solder balls under the package. The rigidity of package and solder balls are likely to increase the failure during thermal cycling [4].

1.3 Substrate for Electronics Assemblies

The PCB, also known as Printed Wiring Board (PWB), is an essential foundation of an electronic circuit. It is the primary element in mechanical design of an electronic system. The substrate is a base material which is a non-conductive layer that can add mechanical strength to PCB. The substrate is etched and laminated with copper sheets. Different types of PCB are Single-layer PCB, Double-layer PCB, and Multilayer PCB, as seen in Figure 1.11. Single-layer PCB consists of a single layer of the copper layer where components can be placed.

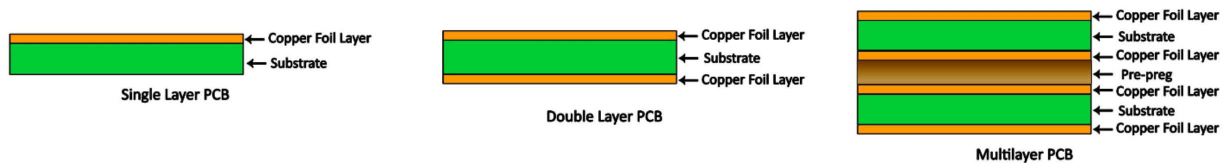


Figure 1.11 Types of PCB [19]

Double-layer PCB has a copper layer on both sides, and it is used in complex circuits for higher circuit density and routing efficiency. The interconnection of copper layer between both the sides can be achieved by drilling and plating holes known as vias as shown in Figure 1.12.

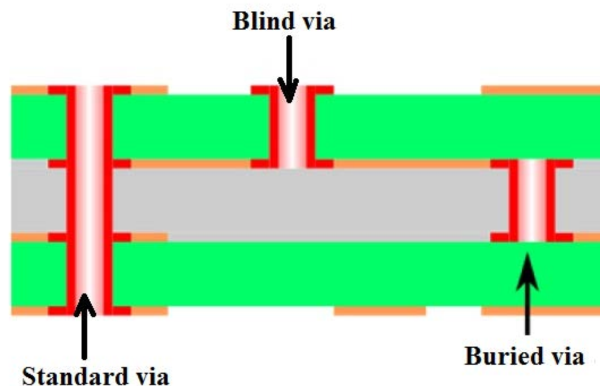


Figure 1.12 Types of vias

Multilayer PCB consists of three or more copper layers, including an external "pads only" layer. For high-density circuits, the number of layers can extend up to 50. These boards are fabricated by laminating the single or double-sided, pre-etched, patterned sheets of laminate together using partially cured resin known as prepreg [2]. For higher density circuits, techniques such as buried and blind vias are used, as shown in Figure 1.12. Buried vias are used for the interconnection between inner layers of copper without the necessity of drilling through the entire board thickness. The connection between the outer layer and the successive buried layer on one side can be achieved through blind vias.

The PCB has the following functions

- Serves as a mounting surface for packages to be placed
- Acts as the base for solder pads to create a mechanical connection between package and board
- Provides wiring channels to facilitate package-to-package connections
- Test bed at specific points on the board where probing can be performed to check the component functionality
- Provides a platform for marking surface (fiducial) to assist accurate component placement during the assembly process

1.3.1 Substrate Material

The most commonly used substrate in the single, double, and multilayer PCB is glass epoxy substrates. The substrate is the composite material comprising of epoxy as resin and glass fiber as the base material. The glass fiber provides structural stability, and the resin imparts ductility. FR-4 is one of the most standard glass epoxy substrates that are used today. FR laminates designated

as Flame Retardant has the property of self-extinguishing if a component shorts and causes fire. The properties of FR-4 can be seen in Table 1.1. The glass transition temperature (T_g) is defined as the temperature in which the polymer transforms from a hard, brittle condition to a rubber state[15]. For the FR-4 substrate, the glass transition temperature is 170°C, and it can vary between 120°C to 180°C depending on the resin composition. The maximum recommended operating temperature for this substrate is 130°C. The linear coefficient of thermal expansion (CTE) is about 13ppm/°C, which is one of the most important physical property in choosing the substrates. The CTE can differ depending on laminate material, number of copper layers, wiring density and operating environment. The CTE of the board substrate must match with that of the package substrate to improve assembly reliability [15].

Table 1.1 Properties of FR-4 Substrate [20]

Property	Values	Unit
Glass Transition Temperature (Tg)	170	°C
Decomposition Temperature (Td)	300	°C
CTE, z-axis (Pre Tg)	60	ppm/°C
CTE, z-axis (Post Tg)	250	ppm/°C
CTE, x-axis, y-axis (Pre Tg)	13	ppm/°C
CTE, x-axis, y-axis (Post Tg)	14	ppm/°C
Thermal Conductivity	0.3-0.4	W/mK
Tensile Strength (Lengthwise direction)	62950	$lb/inch^3$
Tensile Strength (Crosswise direction)	47680	$lb/inch^3$
Flexural Strength (Lengthwise direction)	93700	$lb/inch^3$
Flexural Strength (Crosswise direction)	78200	$lb/inch^3$
Youngs Modulus (Grain direction)	3684	ksi
Youngs Modulus (Fill direction)	3116	ksi
Flammability	V-0	Rating
Moisture Absorption	0.2	%
Maximum Operating Temperature	130	°C

1.3.2 Solder Mask

The copper traces on the substrate can be oxidized and must be protected. Solder bridging can also occur between closely spaced solder pads during assembly which is known as inadvertent solder connection between the copper pads. Solder mask is applied to the copper traces to avoid this. The solder mask is a thin layer of a polymer coating applied over portions of board that cannot not be soldered during assembly. It protects the board from moisture and surface contamination during operating life. It is also used to control the placement of solder during the automated soldering process. Solder mask can be applied by screening or film lamination. Acrylic or epoxy polymer are the common materials used in solder mask [1,3,14].

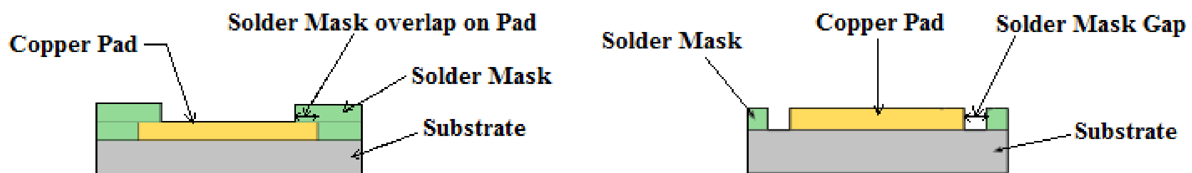


Figure 1.13 Cross-section view of a) Solder Mask Defined (left), b) Non-Solder Mask Defined (right)

There are two kinds of solder mask based on the design that is Solder Mask Defined (SMD) and Non-Solder Mask Defined (NSMD) as shown in Figure 1.13. In SMD, the solder mask is defined by exposing a specific area of the copper pad, as shown in the above figure. SMD pads are used on component substrates. The overlapping solder mask in SMD avoids copper pad from lifting off of PCB during thermo-mechanical stress. The opening in mask develops a medium for each solder balls on BGA to align on the pad during the reflow soldering process. For NSMD, there is no contact between the solder mask and the copper pad, leaving a gap between them. This

pad is a standard on PCB substrate. The thermo-mechanical fatigue resistance is higher for NSMD pad due to low-stress concentration based on the solder pad interface geometry [2], [15].

1.3.3 Surface Finish

Solder mask cannot be used on areas of copper traces where electrical contact is needed instead surface finish is applied on exposed copper pads. Surface finish protects the copper pad from oxidation and corrosion. It can also be used as a test point or area for solder wetting. Surface finish is also known as surface coating. The cross-section view of a PCB with a surface finish on the copper pad can be seen in Figure 1.14. Surface finish can also increase solderability of solder paste on copper pads by mixing its outer layer during reflow soldering [4], [15].

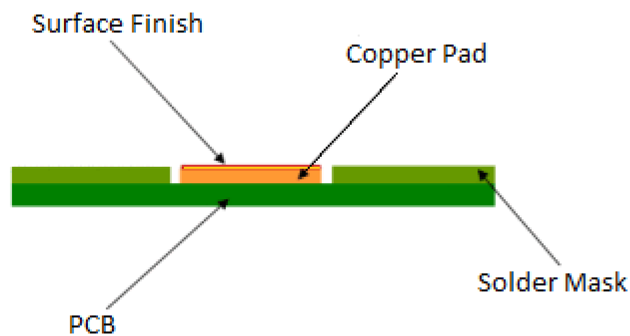


Figure 1.14 Cross-section view of PCB with surface finish

There are various types of surface finishes depending on the method of coating

- Hot Air Solder Leveling (HASL): HASL used to be a dominant surface finish for PCB utilizing tin-lead solders. It is a physical deposition process using molten solder into which board is dipped to apply coatings. The PCB is then taken out of the molten solder, and it is passed through pressurized hot air knives to remove excess molten solder and to level the solder on the copper pad. The coating is dense, good adhesion and low cost. The

disadvantage is that the nonuniformity of coating can cause solderability problems. During hot air leveling, boards are subjected to thermal shock-inducing board warpage and paste printing issues.

- Organic Solderability Preservative (OSP): OSP is an anti-tarnish coating with water-based organic compound over a copper surface on PCB to impede oxidation. The solderability is higher than HASL. The advantage is that it is low in cost and environment-friendly as it can be used with lead-free solders. It provides a flat surface. The disadvantage is lower shelf life, and it can degrade at a higher temperature causing oxidation.
- Immersion Silver (ImAg): It is a thin layer of silver about 0.15-0.3μm deposited on the copper pad. The cost of deposition is higher, but the throughput is higher than the OSP. It has good solderability due to the presence of silver and easy to probe during In-circuit Testing (ICT). It can cause microvoids resulting in early failure during thermal cycling. The exposed silver can be tarnished when it is in the field for more extended time arising in poor board quality. It is also prone to creep corrosion when exposed to airborne sulfur [21].
- Immersion Tin (ImSn): It is used in a backplane system connected by press-fit pin configuration. It is low in cost, an excellent finish for ICT, and provides a flat surface where fine pitch packages can be placed. ImSn demands complicated plating process with a bath containing stannous halide and thiourea. It is difficult for wave soldering after assembly. This surface finish forms a thin layer of SnCu (Tin Copper) intermetallic when exposed to elevated temperature. Solderability and tin whisker formation are a concern when aged for a longer time [21].

- Electroless Nickel Immersion Gold (ENIG): It consists of a thin layer of gold above a thick layer of Nickel (Ni) on the copper pad. It is easier to assemble finer pitch due to its excellent flatness. It does not tarnish or oxide due to dissolution of gold into the solder. It is highly robust during assembly. It has better shelf life and solderability. The presence of nickel makes it a barrier for copper diffusion during wave solder and rework. The issues associated with this surface finish is the high cost, gold plating process, which may result in black pad defect when uncontrolled.
- Electroless Nickel Electroless Palladium Immersion Gold (ENEPIG): Compared with ENIG, ENEPIG consists of a layer of electroless palladium over nickel layer on the copper pad. The purpose of palladium is to prevent black pad defect. It forms a superior solder joint with lead-free solders. The shelf life for ENEPIG is 12 months. It is expensive and unwise for drop and shock applications [21].

1.4 Solder Interconnection

Soldering is a process of joining metals by heating the base material to below solidus temperature and applying the filler metal with liquidus temperature not exceeding 450°C (840°F). The filler metal is melted, joined together, and solidified to form a secure connection [22]. The solidus temperature is defined as the maximum temperature at which the material remains in a completely solid state. The liquidus temperature is a minimum temperature at which material is completely in a liquid state. Applications of soldering include plating, plumbing, and electrical connections [4]. For electronics applications, the connection between leads or terminations and PCB is established through solder paste during reflow soldering. Solder paste is applied to the PCB through screening, stenciling, or dispensing. Solder paste is a “homogeneous and kinetically stable

mixture of solder alloy, powder, flux, and vehicle capable of forming metallurgical bonds at soldering conditions that can be adapted to automated production in making reliable and consistent joints" [2]. Solder pastes are depicted as fusible alloys of elements such as Tin (Sn), Lead (Pb), Silver (Ag), Copper (Cu), Bismuth (Bi), Antimony (Sb), Indium (In), and Cadmium (Cd) with liquidus temperature below 450°C. Constituents of the solder paste are shown in Figure 1.15.

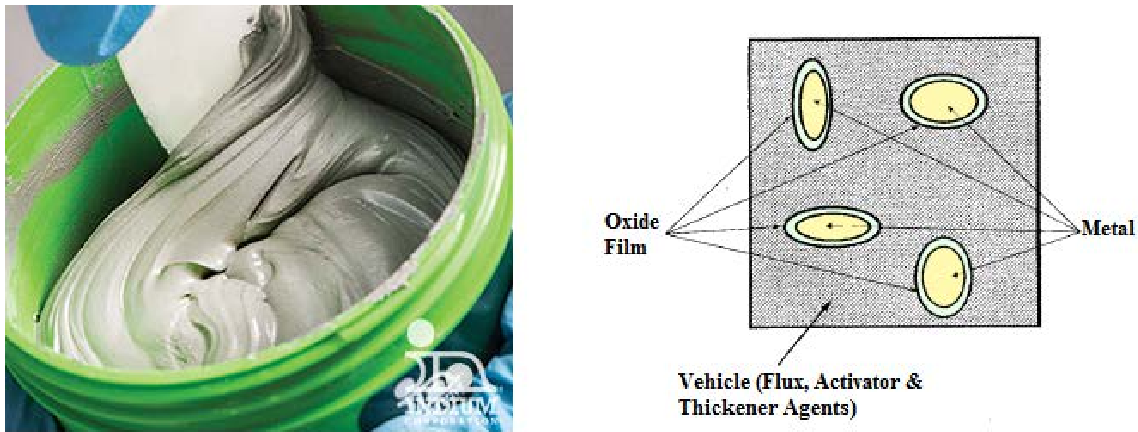


Figure 1.15 a) Solder paste (left), b) Constituents of solder paste (right) [15]

The process of producing solder materials involves rapid cooling of molten solder of suitable composition on a rotating wheel to form fine solder materials. An inert environment is essential for solder material manufacturing to take place to minimize oxidation. Solder pastes have the same composition when compared to solder bars but cost more than solder bars due to stringent quality tests, the addition of solvents, flux, and the added scrap in manufacturing the solder powder to the required shape and size. The factors which should be controlled to get the desired properties are metal composition, metal content, particle size and shape, flux activators and wetting action, solvent and void formation [15].

The solder connection between leads or terminations and PCB is created through the melting of solder pastes during reflow soldering. A metallurgical bond between the copper pad on

PCB and the solder joints is formed through a layer of Intermetallic Compound (IMC). The IMC layer thickness has to be contained due to its brittle nature. The selection of alloys are based on the following criteria [2]:

- Melting temperature range of alloy with respect to service temperature
- Mechanical properties of alloy with respect to service life
- Wettability on specific substrates
- Eutectic versus non-eutectic compositions
- Service compatibility in terms of environment

1.4.1 Tin-Lead solder

The most popular choice of solder alloy has been Tin-Lead (SnPb) solder. It has been used by Romans in aqueducts for more than 2000 years [23]. Among the SnPb solder alloys, the most popular alloy for electronic industries is a combination of 63%Sn and 37%Pb by weight [4], [15]. The reason behind this selection is that this alloy is eutectic meaning this alloy has a specific temperature at which entire alloy completely melts when increasing above that temperature and solidifies when below that temperature. The melting point of eutectic 63%Sn-37%Pb alloy is 183°C. The phase diagram of binary alloy Sn-Pb is shown below in Figure 1.16.

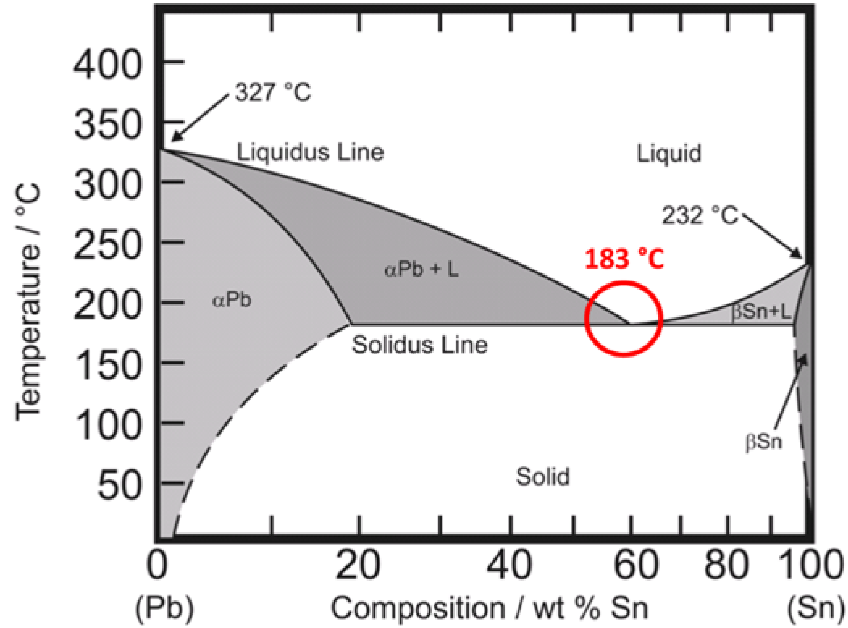


Figure 1.16 Phase diagram of Tin-Lead (SnPb) solder alloy [24]

The eutectic SnPb alloy is easier to work compared with non-eutectic alloys which have a pasty range. The pasty range is a range of temperatures in which the alloy is partially solid and liquid. For example, 60%Sn-40%Pb alloy have the pasty range between 183°C and 188°C where the alloy becomes a liquid state at 188°C. The alloys with pasty range are not recommended when it comes to surface mount assembly. The 63%Sn-37%Pb alloy has the lowest melting temperature of about 183°C whereas Sn and Pb element each have 232°C and 327°C. The eutectic 63%Sn-37%Pb alloy has significant advantages over other tin-lead alloys [4], [15], [22] that are

- Eutectic composition with a unique melting temperature
- Low cost
- Good wetting
- Fair fatigue resistant
- Strong joint above or below room temperature

- Higher electrical conductivity
- Provides excellent electrical, thermal, and mechanical performance in electronic packaging

1.4.2 Lead-Free solder

Though SnPb solders are commonly used in electronic industries, there are environmental concerns associated with the usage of lead. Lead is not a problem when contained in electronic product. After the usage of the product, it ends up in the landfill where lead may leach out of the product and then gets accumulated into drinking water pipes. Lead has an adverse effect on human health, causing neurological, reproductive and physical development disorder. Lead poisoning is detrimental to young children resulting in damaged neurological development [15], [25].

The legislations were considered restricting lead in the United States during the early 1990s, considering the effects of lead. The roadmap on the commercialization of lead-free solders was developed by the Japan Institute of Electronics Industry Development Association (JEIDA) committee in 2000. In the United States, the IPC association proposed the roadmap emphasizing on lead-free solder research and development during the year 2000 [26]. The European Commission proposed two legislations on 2008 - Directive on Waste of Electrical and Electronic Equipment (WEEE) and a Directive on the Restriction of the Use of Certain Hazardous Substances (RoHS) in Electrical and Electronic Equipment. Directive on WEEE required member states to set up a recycling center for WEEE where consumers can send it for no charge at the end of service life. Directives on RoHS were focused on the transition to lead-free electronics in 2008 [27].

After legislations were proposed, the electronics industry was seeking to find the potential solder alloy to replace the conventional tin-lead solder known as lead-free solders. Various factors were considered in choosing lead-free solder alloy:

- Environment-friendly
- Good wetting
- Melting temperature similar to eutectic tin-lead
- Smaller pasty range temperature in the phase diagram
- Similar physical properties as eutectic tin-lead
- Longer shelf life

There were no lead-free solder alloys that would serve as a drop-in replacement of eutectic tin-lead. Depending on the usage application, there were commercially available lead-free solder alloys. Studies were conducted to choose appropriate alloys for specific applications. In the end, industries chose Tin-Silver-Copper (Sn-Ag-Cu) abbreviated as SAC alloy.

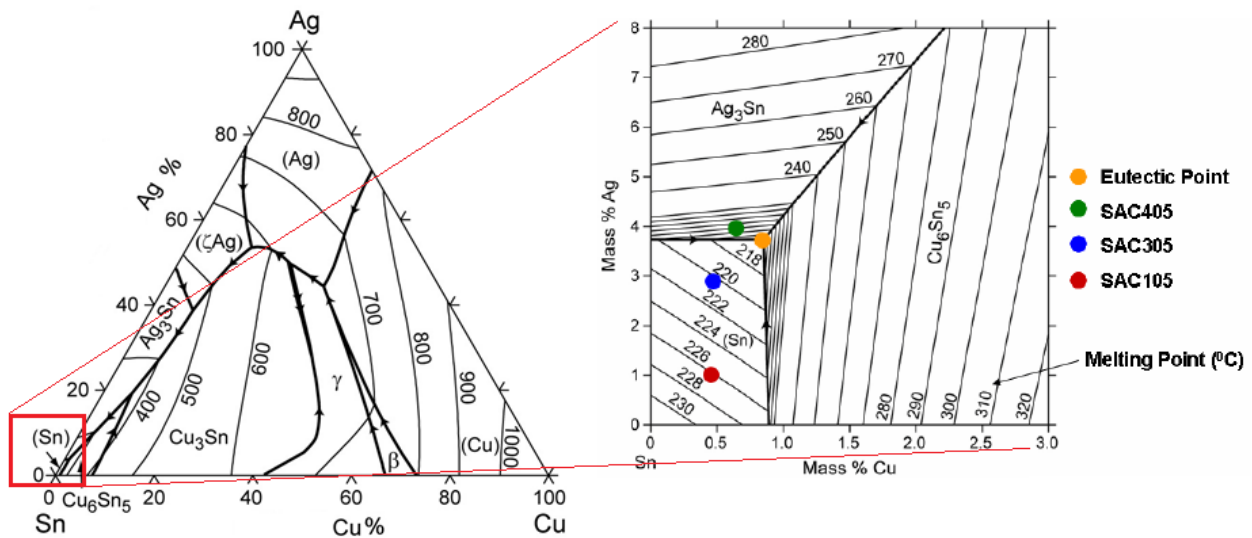


Figure 1.17 Ternary Sn-Ag-Cu alloy phase diagram

The phase diagram of ternary Sn-Ag-Cu alloy is shown above in Figure 1.17. The survey was conducted by Soldertec, and it is shown that 70% of industries preferred SAC based alloys,

as shown in Figure 1.18 (left). From the SAC alloys, the industries chose between 3-4% content of silver and between 0.5-1% of copper, as shown in Figure 1.18 (right) [28].

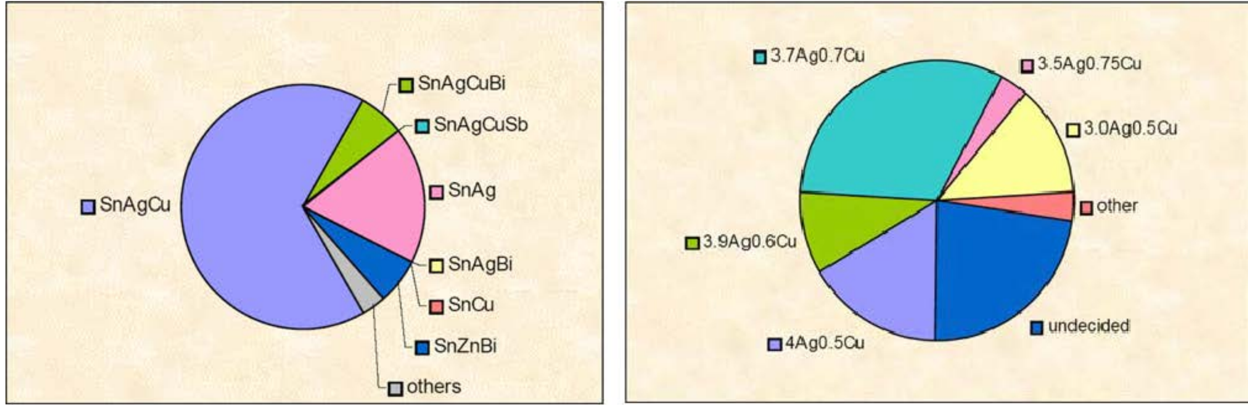


Figure 1.18 Market share of lead-free solders (left), Market share of SAC alloys (right) [28]

The describing of SAC based alloys are given below [4], [15]:

- 99.3Sn-0.7Cu: It is a low-cost alloy due to the absence of silver, which is used in high-temperature applications such as automobile. It does not contain lead and silver. The melting temperature is 227°C. This alloy has shown better low cycle fatigue life than eutectic SnPb [29], but it is prone to tin whiskers.
- 96.5Sn-3.5Ag: This alloy is eutectic. It has a higher strength than SnPb and good wetting on the copper pads. The melting temperature is slightly lower than 99.3Sn-0.7Cu, which is 221°C and also it is expensive compared to 99.3Sn-0.7Cu.
- 96.5Sn-3Ag-0.5Cu (SAC305): This was recommended by JEITA and is very popular in US electronic industries. The melting temperature is 217°C that is higher than SnPb solder and lower than lead-free solders mentioned above. It has good mechanical and solderability properties. This alloy is not suitable for mechanical applications.

- 98.5Sn-1Ag-0.5Cu (SAC105): It is cheaper compared with SAC305 due to reduced silver content. This alloy has better mechanical drop/shock resistance than SAC305 [30]. It is suitable for portable electronic applications.
- 95.5Sn-3.8Ag-0.7Cu (SAC387): This alloy has similar characteristics as SAC305 with slightly higher silver concentration.
- 95.5Sn-3.9Ag-0.6Cu (SAC396): This alloy was recommended by US National Electronics Manufacturing Initiative (NEMI).

The lead-free alloys with different elements such as Indium (In), Bismuth (Bi), Antimony (Sb), Gold (Au), and Zinc (Zn) added to Sn solder were proposed with the hope of improvement in the mechanical properties of the solder. They include [4], [15]:

- 48Sn-52In: It has a eutectic temperature of 118°C. It has a lower melting point where its application does not require high temperature. Indium is resistant to oxidation but can corrode in a humid environment. The constraint in using this alloy is the cost of indium element, which is expensive compared to silver.
- 42Sn-58Bi: This alloy's eutectic temperature is 138°C. The presence of bismuth can lower the melting point. Bismuth also provides greater joint strength. This alloy cannot be used in pad coated with lead which results in decreased thermal cycle fatigue. The constraint in using this alloy is the limited availability of bismuth.
- 95Sn-5Sb: It is applicable in high-temperature applications due to its melting temperature in the range of 232-240°C, which is relatively higher than tin-lead and SAC alloys. The antimony increases mechanical strength and hardness to the solder joint. Toxic nature of antimony and poor wetting are the issues in using this alloy.

- 80Sn-20Au: It is used to bond die to the chip carrier. It has the highest melting temperature of about 280°C. It is expensive.
- 91Sn-9Zn: The eutectic temperature of this alloy is about 199°C. It is used to solder aluminum to remove the oxides. It is prone to corrosion.

1.5 Surface Mount Technology Assembly Process

Surface Mount Technology (SMT) refers to the attachment of packages on the copper pad coated with solder paste, and the solder interconnection is created through reflow soldering. The general SMT assembly process is shown in Figure 1.19 below.

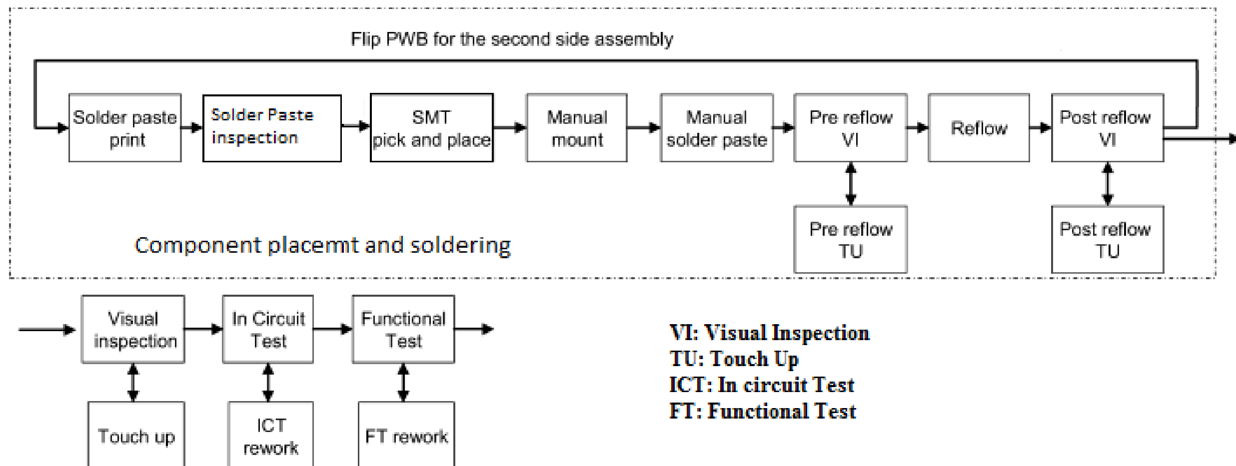


Figure 1.19 SMT assembly process [31]

SMT assembly consists of the following steps.

1. Solder paste printing: The initial step in SMT assembly is the solder paste printing. Solder paste is first applied to all the copper pads on PCB through a stencil. A stencil comprises of a thin metal sheet made of stainless steel with apertures or holes cut into it that matches the component pattern on PCB. The purpose behind stencil printing is to deposit the solder

paste accurately on copper pads. Solder paste between package terminals and PCB have to be at an acceptable level to meet the electrical and mechanical performances. The standard stencil printing method used is squeegee blade printing, as shown in Figure 1.20 below.

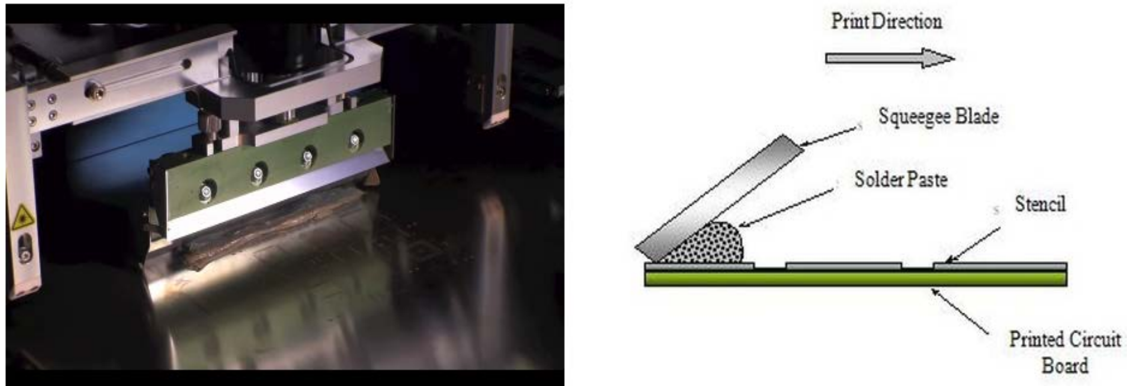


Figure 1.20 Squeegee blade printing process (left), cross-section representation of squeegee blade printing (right) [32]

A squeegee blade is a tool to print the solder paste across onto the PCB with an applied force. The printing direction is back and forth. Squeegee blade is usually made of metal or polyurethane. Critical factors for an effective printing process include squeegee speed, squeegee pressure, stencil cleaning, stencil separation speed, PCB support, printing stroke, inspection, storage, and handling.

After printing, the paste printing quality is inspected. The 2-D inspection is carried out to examine the paste area, and 3-D inspection is used to check its volume. The 2-D inspection example is shown below, indicating inadequate printing.

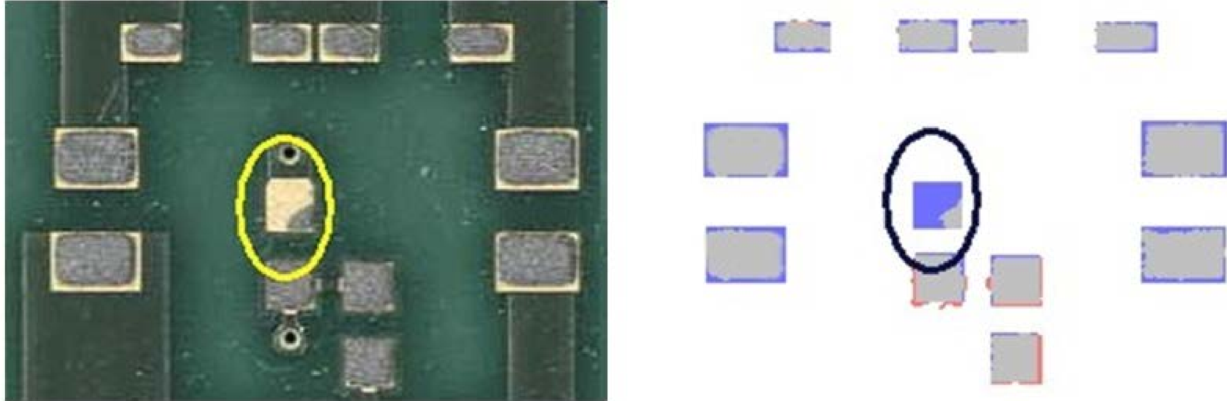


Figure 1.21 Fault identification using 2-D inspection

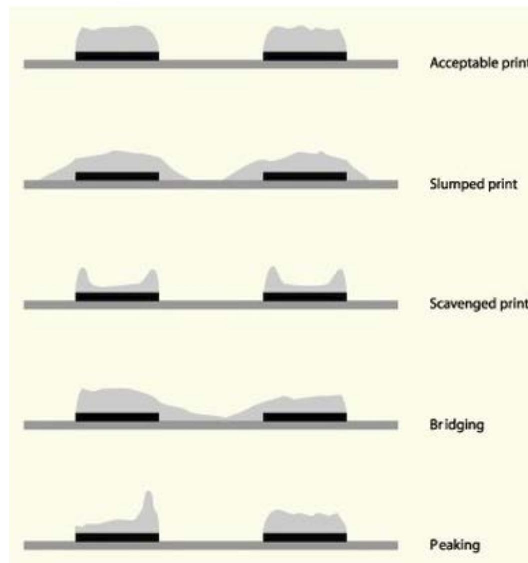


Figure 1.22 Different types of print

Figure 1.22 shows the different possible print that can occur. If one of the critical factors mentioned above regarding the squeegee is not taken care, it can either result in slumped print, scavenged print, bridging or peaking.

2. Component pick and place: After the print quality is passed, then the components are placed on the PCB is performed using a pick and place machine. The components are aligned according to design land pattern of PCB such that solder termination of package

rests on the solder paste. The component placement is facilitated through the visual makings on the board known as fiducial, as shown in Figure 1.23.

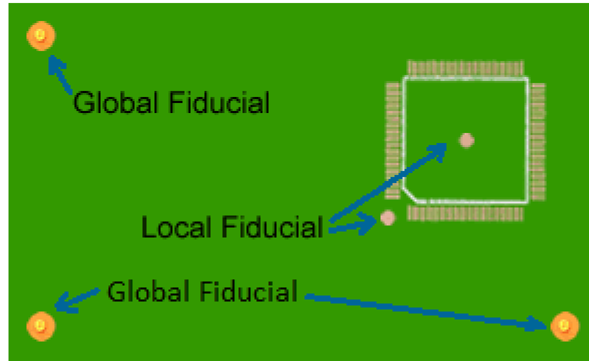


Figure 1.23. Types of fiducial

There are two types of fiducial – Global and Local fiducial. Global fiducial aids in setting the coordinate system for PCB and local fiducial is used for accurate placement of fine pitch components. For global fiducial, any three corners can be used. For local fiducial, it can either be at center of the package or corner of the package. There are different types of component placement machines depending on board size, placement speed and precision, component types and its feeders, optical alignment, and inspection effectiveness [15].

3. Reflow Soldering: After components are mounted on the PCB, the PCB is placed in the reflow oven where strong metallurgical bond is formed between the package termination and the copper pad on PCB. Reflow oven can be of two different types that are Infrared and Convection oven. Figure 1.24 shows schematics of the convection oven, which consists of different zones set at different temperatures. The PCB is moved on the conveyor belt, and it is subjected to time-temperature profile before forming a joint.

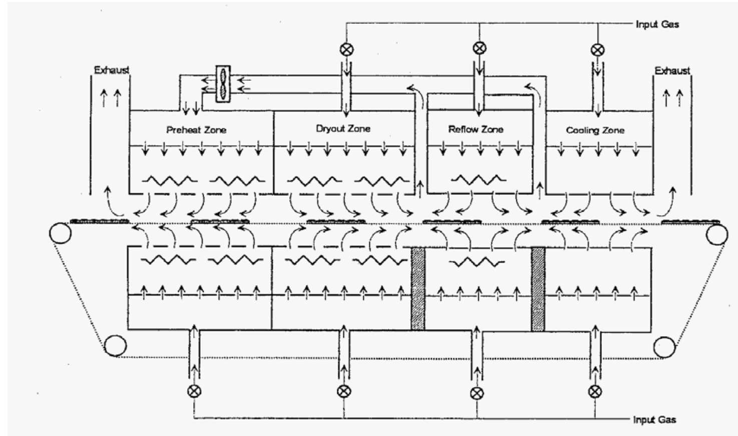


Figure 1.24 Convectional reflow oven (left), schematic representation of reflow oven in different zones (right) [15]

Reflow profile consists of four stages, known as zones, as shown in the above figure. They are:

a. Preheat zone: Initially PCB is heated to a target temperature at a rate, not more than 3°C/sec. The solvent in the solder paste is outgassed in this stage. If the temperature is heated quickly, the components can crack.

b. Soak zone: After the preheating stage is complete, the solder paste volatile is removed, and the flux is activated. This zone lasts for 60 to 120 seconds. After this zone is complete, the entire PCB's thermal equilibrium is reached before reflow.

c. Reflow zone: This zone is also known as "Time above Liquidus (TAL)" where the oven temperature is above the melting point of solder paste to transform into liquid. The TAL is set between 30 to 60 seconds for proper wetting to take place. The higher reflow temperature has to be monitored closely such that it can cause damage in components.

d. Cooling zone: This zone allows the solidification of solder joints after reflow zone. The allowable cooling rate must not exceed 4°C/seconds.

4. Inspection: After the reflow soldering process, X-ray inspection or Automated Optical Inspection (AOI) is performed to ensure there are no defects in solder joints. AOI checks for component presence, polarity, solder presence, and solder shorts. X-ray can be used to detect solder voids and internal component damage. The example of different inspections is shown below in Figure 1.25.

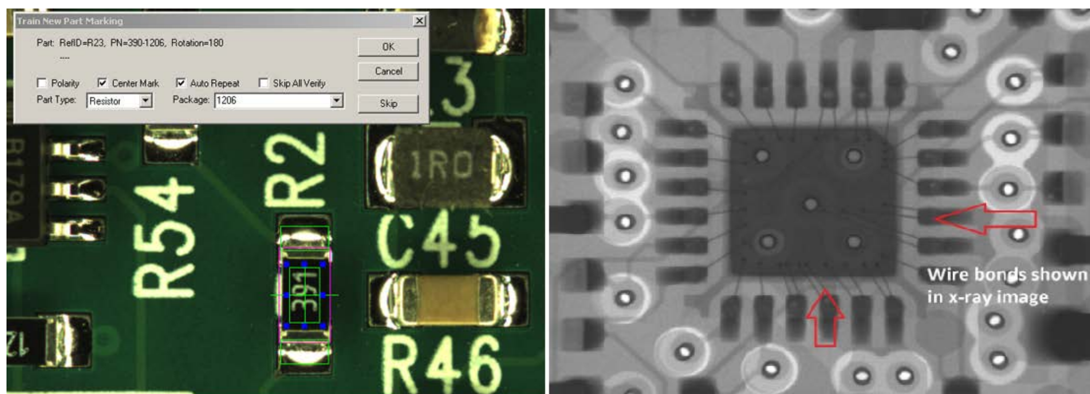


Figure 1.25 AOI (left), X-ray imaging (right) [33]

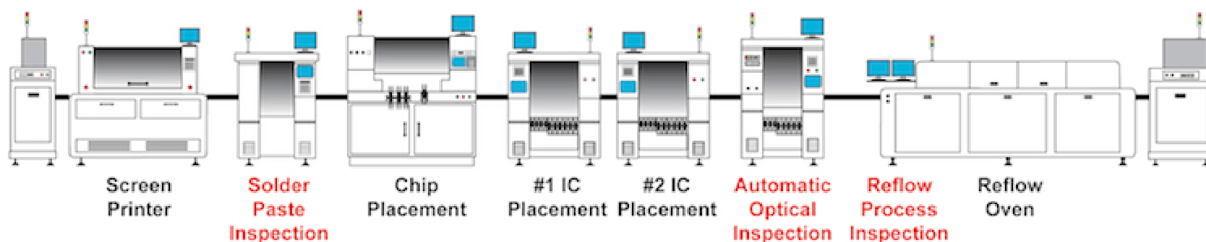


Figure 1.26 Overview of SMT assembly process [34]

The overview of a typical SMT Assembly is shown in Figure 1.26. After the assembly and inspection are complete, the mechanical or thermal tests are conducted to determine the solder joint reliability.

1.6 Reliability testing

After the SMT assembly, it is vital to determine the lifetime and reliability of each package. The BGA packages were used to replace the Plastic Quad Flat Packages for electronics applications in future. Several new packaging technologies were introduced. The availability of reliability data is limited, which decreased its widespread usage because of the complexity of the Flip chip, PGA, QFP, and CSP reliability compared with PLCC reliability. The failure process has to be accelerated to reduce testing time, its cost, and to determine physical and mathematical models for assessing the test results [35]. Standard Acceleration Life Test includes

- Accelerated Temperature Cycling (ATC): It is used to analyze the reliability performance of different packages. It can also be used to detect latent process defects in the first few cycles and fatigue (wear out) failure distribution for a given device and environment. The testing is performed in cycle time between two temperature extremes compared to normal operating temperature.
- Thermal Shock: It consists of two types: Air to air thermal shock and Liquid to Liquid Thermal Shock testing (LLTS). In air to air thermal shock, it comprises an air chamber in which specimen is alternatively exposed to hot and cold air. In LLTS, specimens are placed in a chamber consisting of a hot and cold liquid bath. It is alternatively immersed in both the bath with different temperature extremes using basket transfer mechanism. The only

difference between thermal shock and thermal cycling is that thermal shock is the exposure in a sudden change in temperature compared with thermal cycling.

- Drop: It uses a machine to generate free fall on specimens. It is designed to evaluate the mechanical shock resistance of the specimen. This test is crucial for Pb-free solder research in portable electronics applications.
- Vibration: This test is designed to evaluate components for usage in electrical equipment to endure moderate to harsh vibration as a result of transportation and field. It is also used to test electronic packages used in automobile and military.

Chapter 2 Literature Review

2.1 Solder joint reliability

As mentioned earlier in Section 1.1, electronics industries are miniaturizing the devices with the purpose of higher component density and real-estate, improved mechanical performance and lower SMT assembly cost. Even after achieving those factors, the reliability of devices is a concern. The reliability is defined as the ability of a device or system to perform its function in a specified time [36].

The reliability of SMT Assembly is examined based on wafer level reliability, board level reliability and package reliability corresponding to interconnection hierarchy. Mohd [37] specified board level reliability as interconnect reliability testing, which is used to assess the quality and reliability of solder interconnections after mounting packages on the PCB. Matin [38] mentioned that solder joint subjected to thermo-mechanical fatigue during field usage such as power cycling, temperature cycling, drop, shock or vibration resulting in solder joint failure and causing the whole device to fail. It is not possible to isolate the effect of a thermal and mechanical load on solder materials subjected to real thermo-mechanical loading condition. The two effects must be studied separately. Li [39] indicated the mismatch in CTE between dissimilar materials as a source of deformation and thermo-mechanical stress resulting in cracks in solder joints. Zhang [40], [41] and Sanders [1] investigated the crack propagation in the solder joint either through the bulk solder or along the intermetallic layer located at the solder joint/component interface and solder joint/copper pad on the PCB substrate. Zhang [39,40], Hai [42], Sanders [1], and Shen [43] analyzed the long term isothermal aging effect at elevated temperatures on the experimental lifetime of packages. Basit [44] generated 3-Dimensional Finite Element Analysis (FEA) models

to simulate the thermal cycling and aging of BGA solder joints. The FEA showed a good correlation between the experimental result and the simulated result. Table 2.1 shows the design parameters of BGA packages and its effect on fatigue life.

Table 2.1 Design parameters and its effect on fatigue life [45]

Design Parameter	Fatigue Life Improved by	Magnitude of Effect
Size of Silicon Die	Smaller is better	Large
Package Standoff	Higher is better	Large
SMD vs. NSMD Pads	NSMD is better	Large
Interposer Thickness	Thicker is better	Large
PCB Thickness	Thinner is better	Large
Mold Compound CTE	Higher is better	Large
Thickness of Silicon Die	Thinner is better	Small
Mold Compound Thickness	Thinner is better	Small
Mold Compound Modulus	Lower is better	Small

2.2 Properties important to solder joint reliability

The melting temperature of a solder material is one of the critical factors from a reliability perspective. The higher the melting temperature of a solder, the more it is resistive towards a failure mechanism known as creep. Depending on the application, the lower melting temperature is also used. The other properties essential to solder reliability include [4], [15], [46]:

- Coefficient of Thermal Expansion (CTE)
- Voiding percentage
- Grain growth
- Intermetallic formation
- Initial microstructure
- Mechanical properties
- Failure modes
- Thermal cycling performance
- Corrosion and oxidation resistance

2.3 Failure modes

The typical failure mode in flip chip is shown below in Figure 2.1.

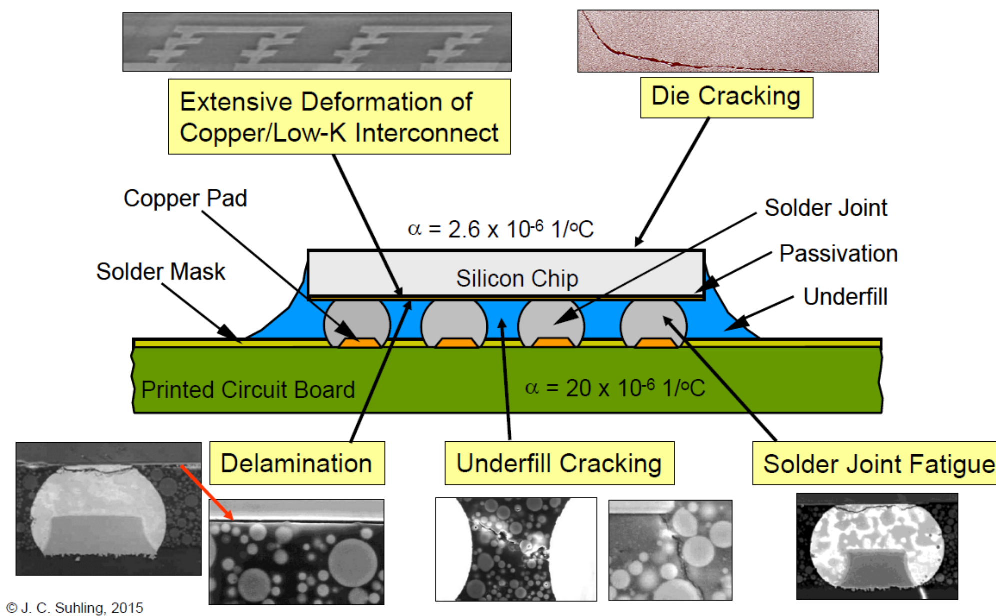


Figure 2.1 Typical failure modes in flip chip [48]

The assembly type is Flip chip On Board (FOB). The flip chip is attached to the substrate through solder balls. The underfill adhesive, made of epoxy with glass filler particles, is used to fill between the chip and board to minimize the CTE difference between the chip and PCB substrate. The underfill also reduces the strain on the solder joint interconnections, resulting in improved fatigue [48].

The typical failure modes in packages consist of [47]:

- Die cracking
- Solder joint fatigue
- Underfill/Encapsulant cracking
- Wire bond failure
- Delamination at the interposer substrate

In the case of conventional packages, the cracking through mold compound and flip chip interconnection failure are a significant problem [48].

2.4 Characteristic solder joint failure

The reason behind the electrical failure of electronic components is due to failure in solder connection during usage. Generally, the brittle failure occurs at the earlier stage compared with ductile failure that takes longer to occur. In the solder joint, two common failure modes that occur for BGA packages that are crack through the bulk solder and along the IMC boundary layer, as shown in Figure 2.2.

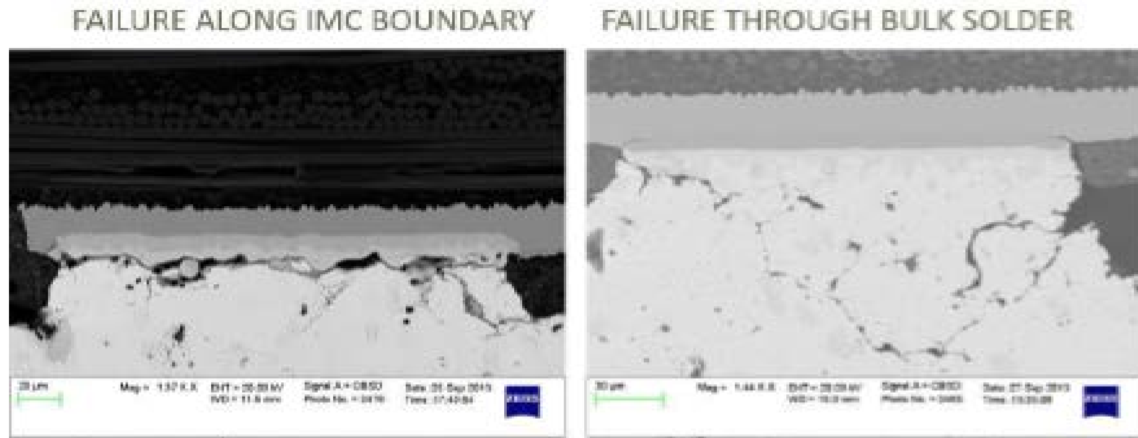


Figure 2.2 Solder joint failure mode for BGA packages [45]

The crack initiation generally occurs at top corner of the solder joint closer to the IMC layer. Crack can propagate along the IMC layer, boundaries of IMC inclusion, or bulk solder. Crack along the IMC layer indicates lower reliability and failure along the bulk solder is favored from a reliability aspect [49]–[51].

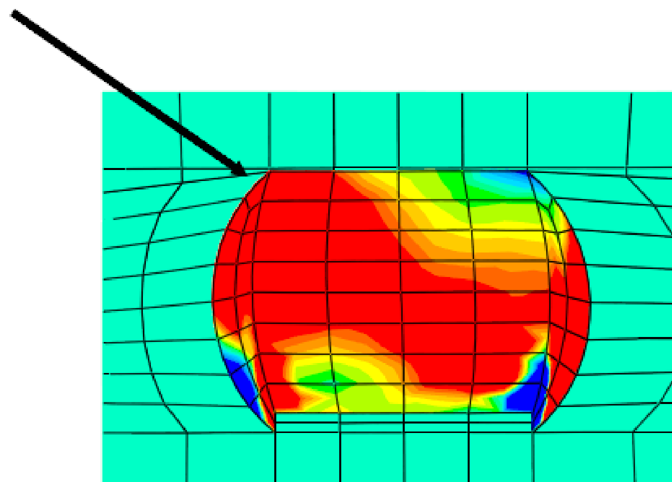


Figure 2.3 FEA model: Induced stress maximized at the upper corner of the joint [47]

Based on FEA model, the von mises stress distribution illustrated that the highest stress concentration in an individual solder joint from BGA package occurs at the corner located at the

top and bottom region, as shown in Figure 2.3. For the Non-Solder Mask Defined (NSMD) pads on the substrate, the highest stress concentration is located at the opposite side of the solder joint under component Under Bump Metallization (UBM) [49], [51]. That is the point where crack initiation occurs.

Lau [52] mentioned the reason behind the solder joint failure and other interconnection is due to its exposure to various environmental stresses in the field. They include [52]:

- Temperature
- Voltage
- Humidity
- Mechanical shock (Drop)
- Current density (Electromigration)
- Corrosion
- Vibration
- Mechanical bending and twisting

The prevalent types of failures in the field are overstress (Overload) failure and fatigue failure. Overstress failure happens when applied stress on the solder joint is greater than its capacity. Fatigue failure occurs during cyclic loading when the solder joint reaches the plastic state. After the solder joint attained the plastic state, crack initiates and then propagates, resulting in failure.

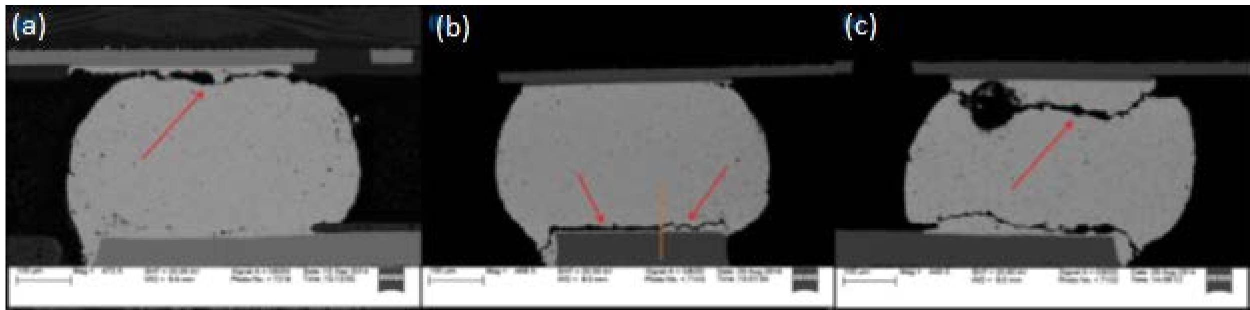


Figure 2.4 Types of failure modes in BGA packages [1]

The typical fatigue failure mode can be seen in Figure 2.4a, where crack propagates along with the IMC layer at the component side. In Figure 2.4b, the crack before the orange vertical line indicates the brittle failure and crack at the right of the same line illustrates ductile failure. Failure due to possible recrystallization is shown in Figure 2.4c.

2.4.1 Fatigue

The importance of fatigue is apparent, where at least half of all mechanical failures in engineering materials are caused due to fatigue [53]. The failures in electronic components are associated with solder joint fatigue failure. The fatigue is caused due to mismatch in CTE between package and board substrate under cyclic loading. There are two components of fatigue failures that are crack initiation and crack propagation [54]. Failures can also occur under repetitive loading below the yield stress. A fatigue crack is formed when the material attains plastic deformation during cyclic straining. Under plastic deformation, an irreversible dislocation occurs leading to persistent slip bands (PSB), intrusion, and extrusion in surface grain. Due to continuous straining, microcrack can develop within intrusion or extrusion within PSB and under higher stress crack propagates. Figure 2.5 shows an illustration of the crack initiation process.

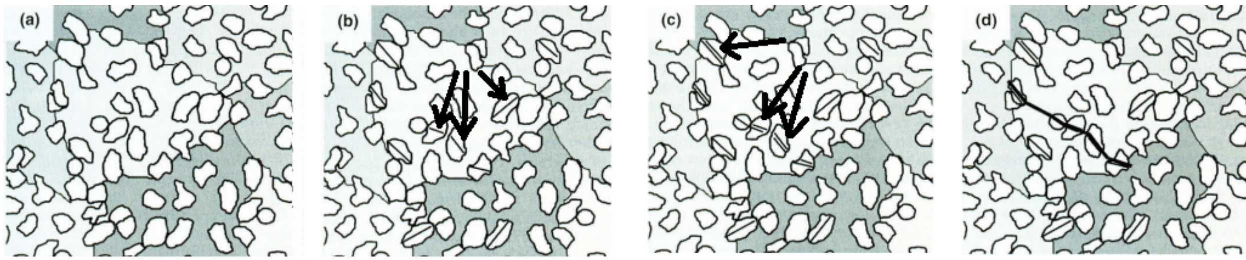


Figure 2.5 a) Initial microstructure before load, b) Slip accumulation in grain, (c) Slip band crack within certain grain and slip accumulation in neighboring grains, (d) Formation of crack within microstructure [55]

The process of fatigue crack occurs in three stages. They consist of [56]:

- Stage 1: Crack initiation and transient growth. Crack is formed in high-stress concentrated region. It occurs at the sample surface. High cyclic stress causes slip band formation leading to the creation of intrusion and extrusion surface. The intrusion surface is where microcrack is originated.
- Stage 2: Steady-state crack growth. Crack propagates through plastic deformation and fracture of the crack tip under repeated stress cycling.
- Stage 3: Interaction and saturation. The small crack is grown to a point where it meets the other crack forming a complete crack propagation, ultimately causing failure.

The fatigue mechanism of solder joints was investigated by Matin [38]. He also detected the presence of PSB in solder joints facilitating the fatigue mechanism. The fatigue mechanism in solder joints is caused due to three factors: thermal mismatch between copper pad and solder, intrinsic thermal mismatch caused by Sn anisotropy and mechanical constraints posed by the copper pad on solder [38].

2.4.2 Creep properties

Creep refers to the time-dependent strain plastic deformation under constant stress [57]. One of the dominant failure modes in the solder joint due to its higher homologous temperature (T_h) is creep deformation [58]. The homologous temperature is defined as the ratio of material's temperature to its melting temperature (T_m) expressed in Kelvin [59].

$$T_h = \frac{T}{T_m} \quad \text{Eq. 2.1}$$

When the homologous temperature is higher than $0.5T_m$, then creep deformation generally occurs in materials [59]. The solder materials undergo creep deformation even at room temperatures due to their lower melting temperature. At room temperature, the T_h for eutectic SnPb solder and SAC solders are $0.65T_m$ and $0.6T_m$. They both are greater than $0.5T_m$ capable enough of generating rapid creep deformation. The creep testing is performed by applying tensile stress (constant load) on a sample and measuring the strain with respect to time [60]. Figure 2.6 shows the creep curve, which consists of three stages of creep after the initial strain.

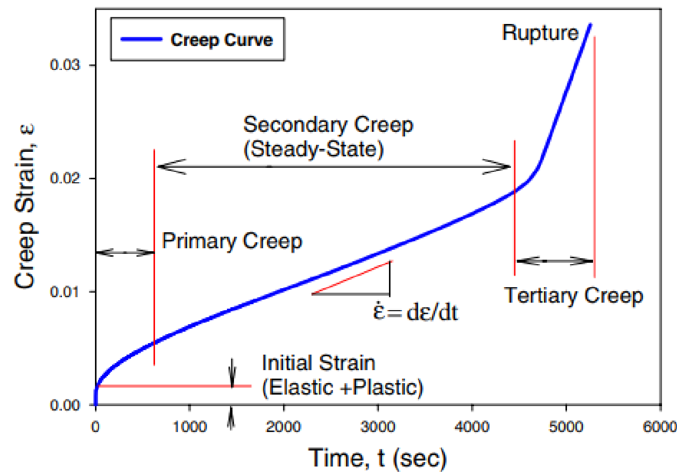


Figure 2.6 Creep curve [28]

- Primary creep (Transient creep): The strain rate is high at the beginning and decreases over time due to strain hardening, which can restrict deformation.
- Secondary creep (Steady-state creep): The plastic deformation takes place at this stage when the T_h is higher than $0.5T_m$. The strain rate is constant due to the strain hardening that reduces deformation speed. The recovery and recrystallization (softening) increase the creep rate. In the secondary creep stage, there is a balance between strain hardening and recovery.
- Tertiary creep: This stage occurs when recovery overtakes strain hardening mechanism. The strain rate increases over time, leading to necking or micro-cracking, causing failure (rupture).

2.4.3 Tensile properties

The tensile properties are depicted by the stress-strain curve shown in Figure 2.7. The stress-strain curve contains two regions: the elastic region and the plastic region. In the elastic region, the stress follows a linear relationship with strain following Hooke's law, as shown in the below equation.

$$\sigma = E\varepsilon \qquad \text{Eq. 2.2}$$

where σ is the stress, E is Young's modulus of elasticity and ε is the strain. The Young's modulus, generally known as the static modulus, is calculated using slope from the stress-strain curve. In the elastic region, when the load is removed, the material goes back to its original shape. When higher load is applied to a sample that exceeds the elastic limit, the plastic deformation occurs which is irreversible.

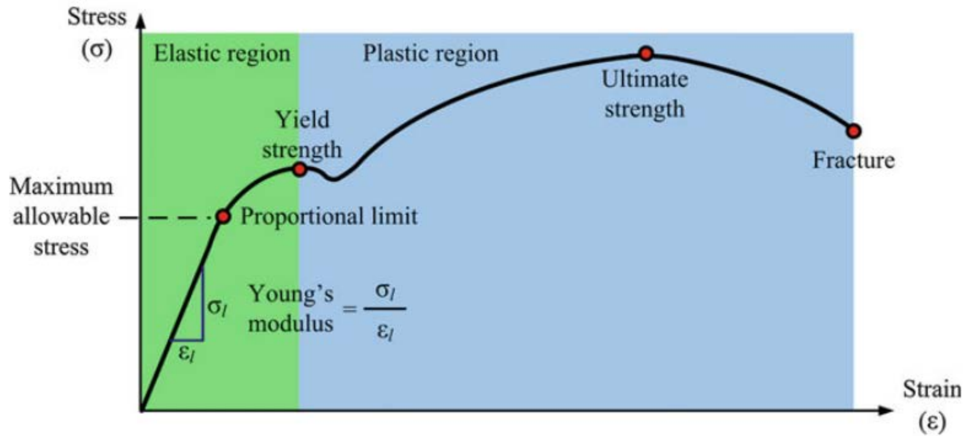


Figure 2.7 Stress-strain curve [61]

In the plastic region, the sample elongates and decreases in diameter. Yield strength (YS) is defined as the stress at which plastic deformation begins to occur in the sample. When the load is removed at a point above YS, then the stress-strain curve is parallel to initial Young's modulus. The Ultimate Tensile Strength (UTS) is defined as the maximum stress that the material can endure before failure under loading. The necking occurs between the UTS until fracture.

2.4.4 Coefficient of Thermal Expansion

During a normal operating cycle, the electronic packages are subjected to thermally induced stress due to temperature changes, power cycling and other stresses. The package failure is caused due to mismatch in CTE between PCB substrate and package, generating thermal fatigue and shear strain, resulting in package failure. The linear CTE is expressed as the linear expansion of material per unit change in temperature. The linear CTE is given by:

$$\frac{\Delta L}{L} = \alpha_L \Delta T \qquad \text{Eq. 2.3}$$

where α_L is the linear CTE, L is the original length, ΔL is the change in length, and ΔT is the change in temperature.

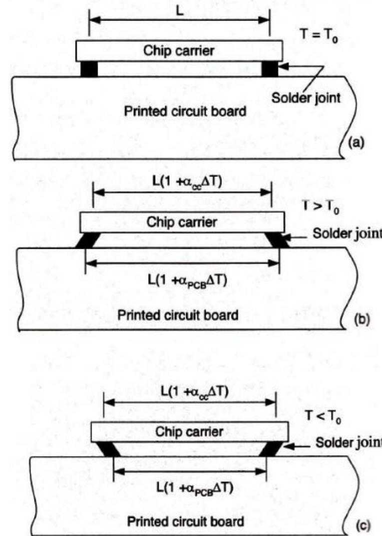


Figure 2.8 Illustration of solder joint deformation due to thermal strain, a) No strain-induced, b) Shear strain due to increase in temperature, c) Shear strain due to decrease in temperature [4]

Suhling [4] presented an analytical model known as Distance to Neutral Point (DNP) relation to understanding the solder joint fatigue failure caused due to thermally induced shear strain. The DNP is a 2-D model with package mounted on the PCB connected through solder joints. DNP is the distance between the center of a solder joint at the package outer edge and center of the package. Figure 2.8 shows the illustration of thermally induced shear strain in solder joints. At the temperature T_0, no stress is induced, as seen in Figure 2.8a. Generally, CTE of the substrate is higher than CTE of the package. When there is an increase in temperature, the PCB expands more than package and contracts when the temperature is decreased, as shown in Figure 2.8b and Figure 2.8c. Due to the expansion and contraction, the shear strain is induced in the solder joint. The shear strain, γ, is calculated from DNP as follows:

$$\gamma = \frac{L*(\alpha_{PCB} - \alpha_{CC})*\Delta T}{2*h} \quad \text{Eq. 2.4}$$

where L is length of the package, h is height of the solder joint, ΔT is change in temperature, α_{PCB} and α_{CC} are the CTE of PCB substrate and chip carrier (package). The shear strain increases linearly with an increase in package length, greater CTE mismatch, and change in temperature. It decreases with an increase in height of the solder joint. The package reliability can be enhanced by increasing height of the solder joint and reducing CTE mismatch between PCB and package.

2.4.5 Intermetallic Compound

The solder connection between solder balls and PCB is created through the melting of solder pastes during reflow soldering. A metallurgical bond between the copper pad on PCB and the solder joints is formed through a layer of Intermetallic Compound (IMC). The IMC layer thickness has to be contained due to its brittle nature. The IMC layer grows throughout the lifetime of the solder joint. It is formed through surface metallization through molten solder. During reflow, the solder begins to melt, and tin from solder paste is dissolved on to the copper present on the substrate through wetting. The IMC growth persists as long as the temperature is above the melting temperature of alloy [62]. The IMC layer is highly brittle compared with other portions of the solder joint, and it facilitates the crack propagation along with that layer. Thicker IMC can cause early failures. Depending on the surface finish and solder paste composition, different types of IMCs can be formed [63].

2.4.5.1 Ag_3Sn IMC

The Ag_3Sn IMC is formed due to reaction between Sn and Ag present in SAC based solder materials [28]. Sidhu [64] showed different morphologies of Ag_3Sn in Sn-Ag solder paste, as shown in Figure 2.9. The Ag_3Sn IMC would be spherical in shape for water-cooled samples, and it appears to be needle-like structure in furnace-cooled sample. The cooling rate determined the Ag_3Sn IMC size and morphology.

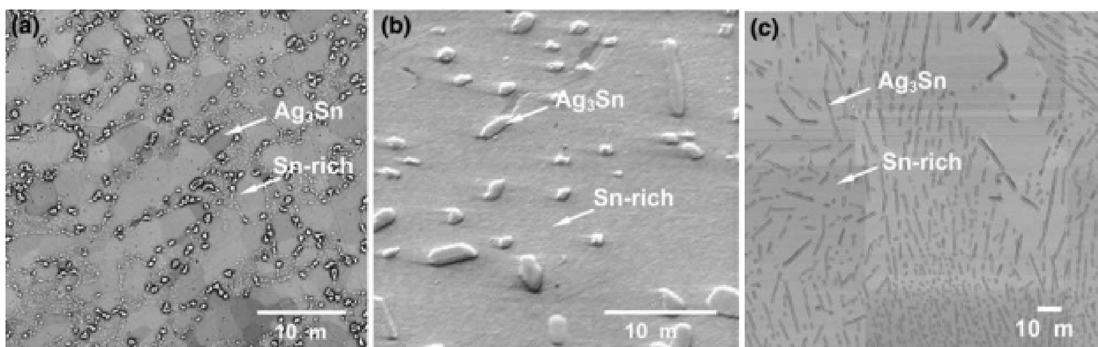


Figure 2.9 Different morphologies of Ag_3Sn IMC (a) Water-cooled, (b) Water-cooled aged, and (c) Furnace-cooled solder microstructures [64]

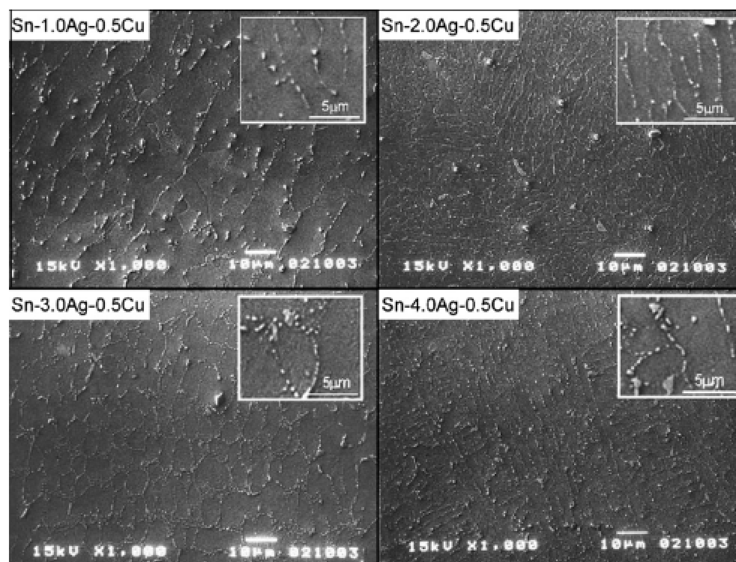


Figure 2.10 Initial microstructures of SAC alloys [65]

Kariya [65] revealed the initial microstructures of SAC alloys with Ag content varying from 1 to 4%, as shown in Figure 2.10. All four alloys consist of Ag_3Sn and Cu_6Sn_5 IMC particles in the β-Sn matrix. The SAC105 has a larger Sn grain and interparticle space of IMCs that are coarse compared with other alloys. The SAC205 alloy has a cell-like Sn grain and finer IMC particles. The IMC particles in SAC305 appear to be like a network structure. The β-Sn grain and IMC particles are finer than other alloys. With an increase in Ag content, the interparticle space and grain size decreases, enhancing the mechanical strength of the solder joint. Coyle [66] and Kittidacha [67] indicated that the higher the Ag content, the better thermal fatigue resistance it is due to its population of Ag_3Sn particles. But the trend is opposite for drop shock performance as demonstrated by Kittidacha [67], where lower Ag performs better due to the presence of higher Sn having lower young's modulus and lower yield strength.

2.4.5.2 Cu-Sn IMC

The primary Cu-Sn IMC is Cu_6Sn_5 that is formed due to reaction between Sn in solder and copper pad. The Cu_6Sn_5 IMC is commonly found when OSP surface finish is used. The initial morphology of Cu_6Sn_5 IMC can be seen in Figure 2.11. Depending on the cooling rate, the IMC morphologies are different, as mentioned by Deng [68]. The water and air-cooled samples exhibit a thin and planar structure, as shown in Figure 2.11a and Figure 2.11b. In the case of furnace-cooled, where cooling rate is the lowest, the thicker η phase with scalloped morphology was observed, as shown in Figure 2.11c.

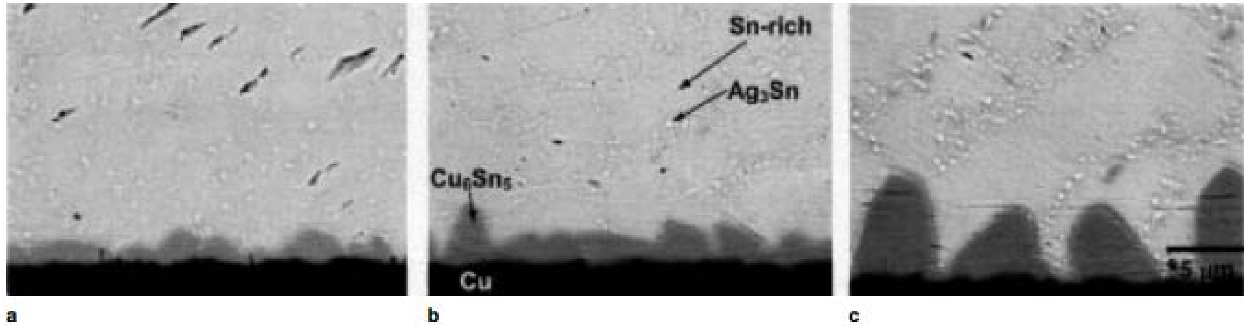


Figure 2.11 Initial morphology of Cu_6Sn_5 IMC a) Water-quenched, b) Air-cooled, c) Furnace-cooled [68]

Roubaud [69] and Tu [70] conducted an experiment and demonstrated that when samples are aged at elevated temperatures, another IMC layer known as Cu_3Sn is formed between Cu pad and Cu_6Sn_5 layer. The IMC interface at Cu pad/solder after 32 days of aging at 150°C is shown in Figure 2.12, where OSP surface finish was used. The Cu_3Sn layer was noticeable after aging at a higher temperature. The IMC growth was modeled using parabolic growth kinetics [71]:

$$w = w_o + D\sqrt{t} \quad \text{Eq. 2.5}$$

where w is the thickness of IMC, w_o is the initial thickness of IMC layer, D is the diffusion coefficient, and t is time.

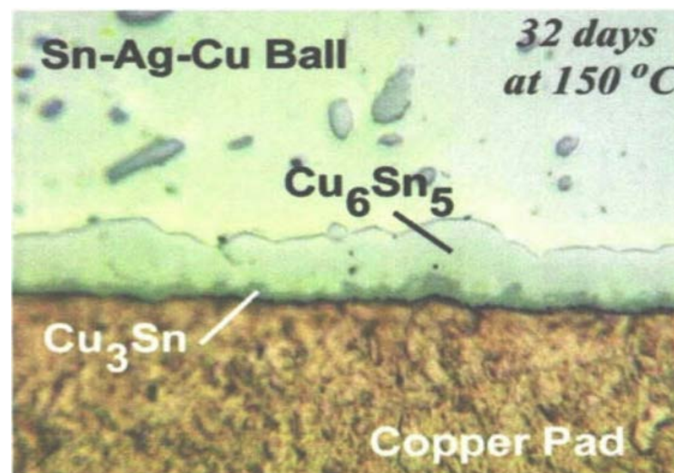


Figure 2.12 IMC interface at the Cu pad/Solder ball [69]

A similar observation was seen by Deng [68] where Cu_3Sn layer growth is apparent after aging for a longer time, as shown in Figure 2.13. Chung [72] indicated that the dominant mechanism for growth of Cu_3Sn and Cu_6Sn_5 layers are grain boundary and phase boundary diffusion.

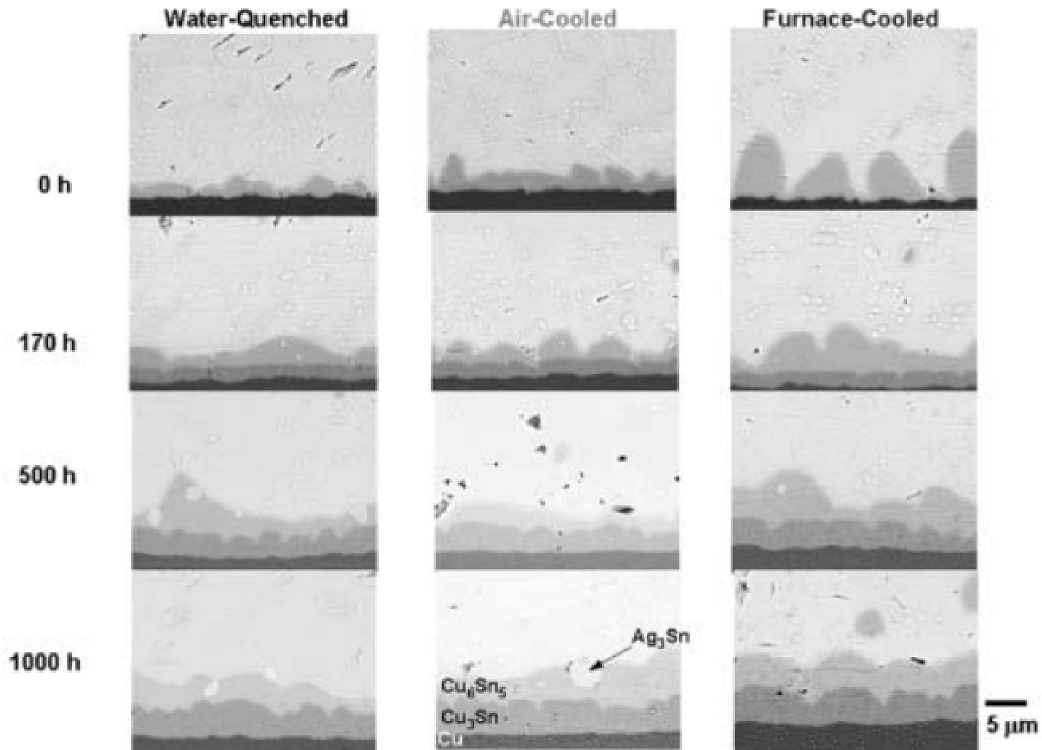


Figure 2.13 IMC morphology development during aging at 140°C [68]

2.4.5.3 Cu-Ni-Sn IMC

This IMC is usually found when ENIG or ENIPEG surface finishes are used. It can be found on OSP coating when SAC alloy is doped with Ni. Che [73] performed an experiment where ENIG and OSP surface finish were used with Sn-3.8Ag-0.7Cu solder paste. He investigated the IMC growth up to 500 hours of testing at 125°C. The IMC interface where OSP surface finish was

used has shown similar morphology, as seen in previous studies [68][69]. The IMC morphologies using ENIG surface finish aged at different times are shown in Figure 2.14.

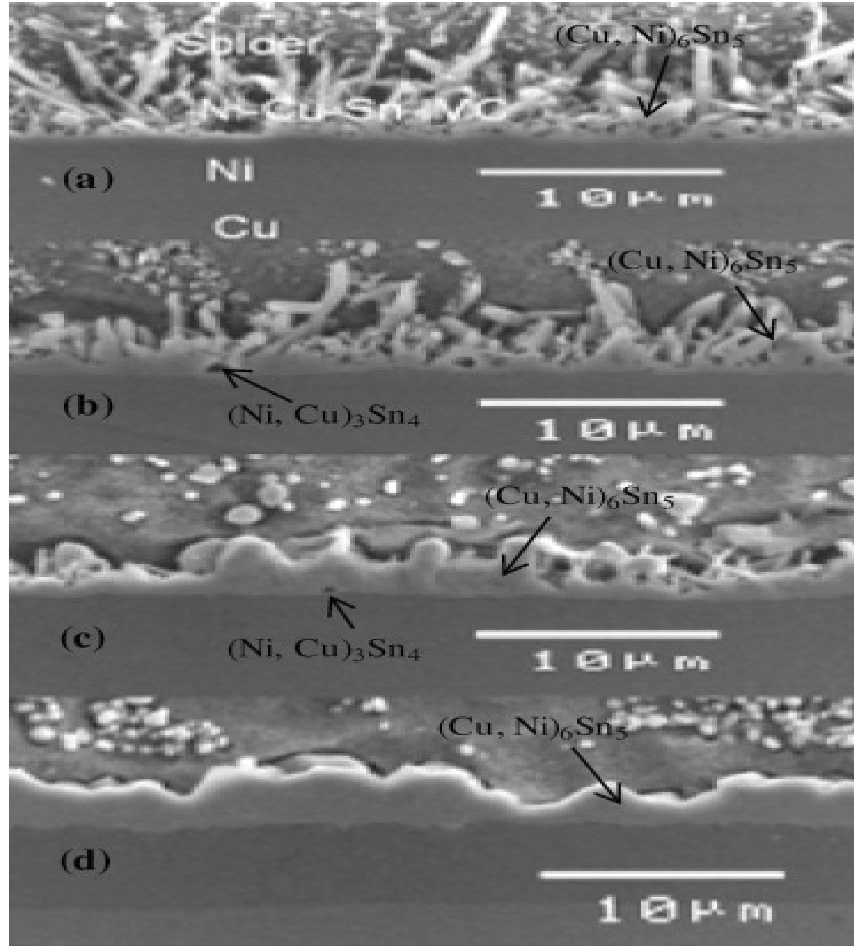


Figure 2.14 Microstructure change of the IMC layer at solder/ENIG interface under different aging times, (a) 0 h, (b) 120 h, (c) 260 h and (d) 500 h. [73]

After reflow, a needle-like layer of (Cu, Ni)$_6$Sn$_5$ is formed at the Ni pad interface. This IMC formation is typical when the solder is made of more than 0.5% by weight of Cu. After isothermal aging, (Ni, Cu)$_3$Sn$_4$ layer is formed between (Cu, Ni)$_6$Sn$_5$ and Ni pad interface. The transformation from needle-like structures to planar structures were seen after a longer period of aging. The (Ni, Cu)$_3$Sn$_4$ layer is immersed into planar IMC and disappears after further aging. A

similar pattern was observed by Berthou [74]. The growth rate of $(Cu, Ni)_6Sn_5$ IMC layer is lower compared with Cu_6Sn_5 due to the presence of Ni, which acts as the diffusion barrier.

2.4.6 Recrystallization

The electronic products fail either due to the external environmental factors, thermal or mechanical load. Though thermos-mechanical loads are not the primary factors of failure, the change in solder's microstructure caused due to recrystallization during loading can affect the solder joint reliability. The change in microstructure can alter the mechanical properties of the solder joint. Xu [75] discovered the occurrence of dynamic recrystallization phenomenon in SAC solder joints. The microstructural evolution reported by Xu is shown in Figure 2.15.

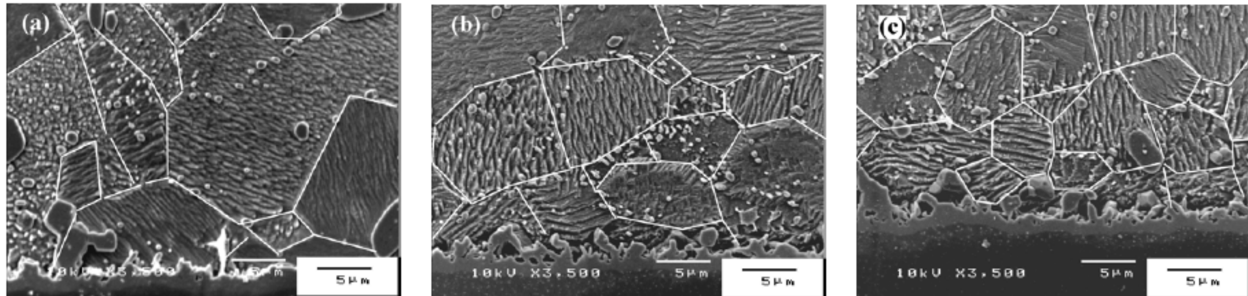


Figure 2.15 Dynamic recrystallization of Sn-rich during thermal cycling a) As reflowed, b) After 500 thermal cycles, c) After 1500 thermal cycles [75]

The grain size measurement was taken at each stage. After reflow, the initial average grain size was about 20μm. After 500 cycles, it reduced to 13μm and was further decreased to 5-8μm after 1500 cycles. The reduction in grain size increased the number of grains and grain boundary area. The change in grain size during thermal cycling indicated the occurrence of dynamic recrystallization. Sundelin [76] studied the recrystallization behavior in Chip Scale Package and resistors. Sundelin indicated that recrystallization nucleates in the region where strain is

concentrated. Recrystallization enabled propagation of the inter-granular crack. Berthou [74] proposed the evolution of SAC solder joint microstructure in thermo-mechanical fatigue which can be seen in Figure 2.16.

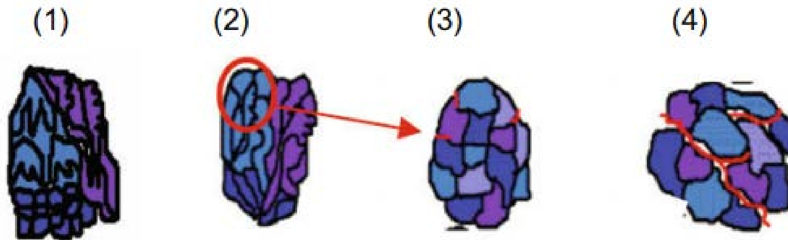


Figure 2.16 Recrystallization phenomenon [74]

In step (1) from Figure 2.16, the dendrite structures (β-Sn) are fine and regular with the same crystallographic orientation, which can be seen in polarized light microscopy. In this case, the solder joints consist of few crystallographically independent dendrite groups where one group represents one Sn macro-grain. The number of Sn macro-grain varies from 1 to 6 on average after reflow. In step (2), the number of Sn macro-grain increases and the dendritic structure is rougher. The recrystallization of Sn macro-grain occurs in a zone of higher strain accumulation, as shown in the red circle in step (2) from the above figure. The recrystallization is a division of part of Sn macro-grain into Sn of smaller size. The crack initiation occurs in step (3) along the Sn grain boundaries. In step (4), the crack propagates through the recrystallized zone along the Sn grain boundary until the electrical opening of solder joint [74]. Mattila [77] observed the onset of microstructural changes at about 750 to 1000 thermal cycles near corner regions of the solder joint, as seen in Figure 2.17. The plastic deformation is the highest in the corner of the joint.

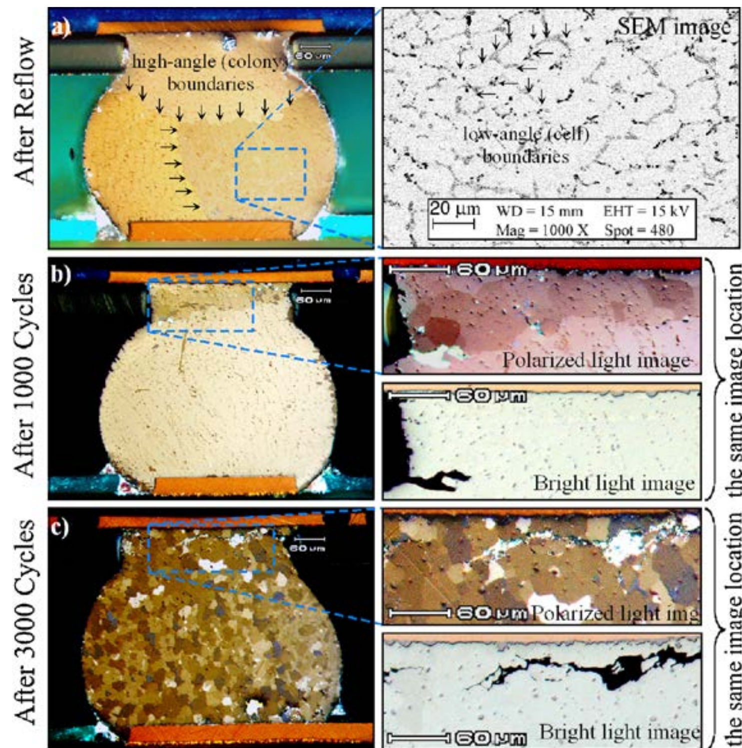


Figure 2.17 Microstructural evolution of SAC alloy by recrystallization a) As reflowed, b) After 1000 thermal cycles, c) After 3000 thermal cycles [77]

After plastic deformation, the internal energy is stored in solder joints in the form of lattice defects (Dislocation). The increased internal energy acts as a driving force for competitive restoration process: Recovery and Recrystallization. The recovery process does not create notable change in microstructure, but microstructural change is apparent during the recrystallization process. The recovery process of SAC alloy causes depletion of stored energy due to high stacking fault energy of Sn. During dynamic loading, the onset of recrystallization occurs where strain hardening is more effective than recovery. After microstructural changes caused due to recrystallization, the crack propagates through bulk solder. Due to the microstructural evolution of SAC solders, one can correlate the field reliability and accelerated test reliability. By studying the

recovery and recrystallization phenomenon, lifetime prediction model incorporating the microstructural evolution effect can be developed, thereby reducing reliability testing [77].

2.5 Statistical Analysis of Failure Data

The time to failure data is collected, and it is fitted into a particular distribution function. The parametric method is used to analyze the data, and the following steps are used [36]:

- Plotting failure data
- Identifying the distribution of failure data
- Fitting the data using candidate distribution
- Obtain information on failure data using fitted distribution

The Probability Density Function (PDF), f(t), is used to plot the failure data as a function of time. The Cumulative Distribution Function (CDF) is defined as the percentage of failure as a function of time denoted as F(t). The CDF is also known as Unreliability, Q(t).

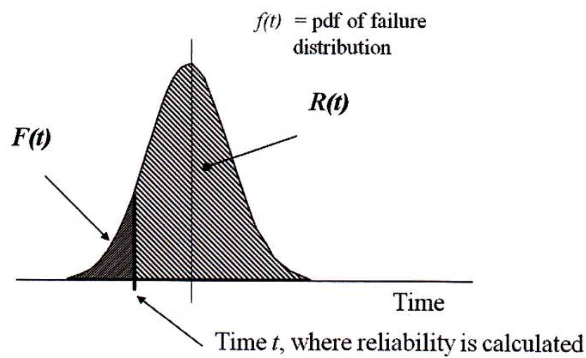


Figure 2.18 PDF and its relation to reliability function [78]

The reliability function, R(t), is defined as the percentage of survivors as a function of time, and it is calculated by R(t) = 1 – F(t). The relationship between these functions is expressed in

Figure 2.18. Another parameter used in reliability analysis is failure rate (Hazard function). It can be calculated by dividing the PDF by reliability function. Each component or products have a different failure rate. The Bathtub curve is shown in Figure 2.19 demonstrates different failure rates as a function of time.

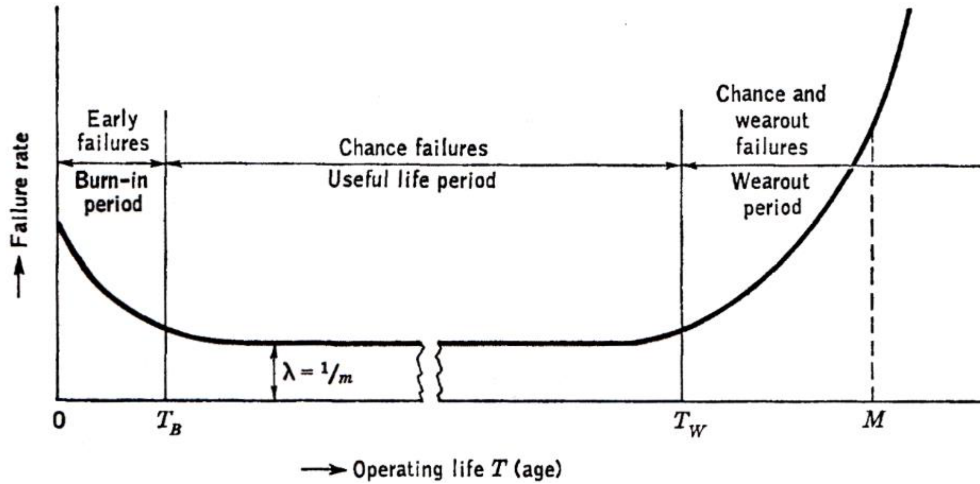


Figure 2.19 Bathtub curve [79]

The early failures until T_B shown in the above figure is caused to infant mortality. The reason behind early failures is caused to defects during the manufacturing process. The failure rate is highest in the beginning and decreases over time. The curve follows the Decreasing Failure Rate (DFR). Burn-in is performed in order to eliminate the weak products for reliability enhancement over time. In the next section, the failure rate is constant where failures are caused randomly or catastrophically. This section depicts the useful life of the product. The failure rate is the lowest in this section. In the next section, the failure rate increases over time due to aging, wear out, or fatigue failure [36], [79], [80]. The distribution to useful life that follows constant failure rate is exponential distribution. The PDF of an exponential distribution is,

$$f(t) = \lambda e^{-\lambda t}, t > 0 \qquad \text{Eq. 2.6}$$

where λ is the rate parameter. The exponential distribution follows memoryless property meaning the time to failure does not depend on how it lasted. Most of the reliability engineers commonly fit the failure data using weibull distribution. The PDF of weibull distribution is,

$$f(t) = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}}, t \geq \gamma \qquad \text{Eq. 2.7}$$

The characteristic lifetime (η) is the cycles at which 63.2% of the population is expected to fail. The shape (β) classifies the different failure modes. The location parameter (γ) is known as the minimum guaranteed lifetime. The above PDF is generally 3-parameter weibull distribution where β, η and γ are estimated. For the 3-parameter weibull, the characteristics lifetime is calculated as ($\eta + \gamma$). The reliability function, R(t) of 3-parameter weibull is described as

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt \qquad \text{Eq. 2.8}$$

$$R(t) = 1 - \int_0^t \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1} e^{-\left(\frac{t-\gamma}{\eta}\right)^{\beta}} dt, t \geq \gamma$$

$$R(t) = e^{-(\frac{t-\gamma}{\eta})^{\beta}}, t \geq \gamma \qquad \text{Eq. 2.9}$$

The hazard function is calculated by dividing PDF by reliability function,

$$h(t) = \frac{f(t)}{R(t)} = \frac{\beta}{\eta}\left(\frac{t-\gamma}{\eta}\right)^{\beta-1}, t \geq \gamma \qquad \text{Eq. 2.10}$$

The Mean Time to Failure (MTTF) is calculated by integrating Eq. 2.10 from 0 to infinity,

$$MTTF = \int_0^\infty R(t)dt = \int_0^\infty e^{-(\frac{t-\gamma}{\eta})^{\beta}} dt, t \geq \gamma$$

$$MTTF = \gamma + \eta * \Gamma(1 + \frac{1}{\beta}) \qquad \text{Eq. 2.11}$$

The above equations only apply for 3-parameter weibull distribution. For the 2-parameter weibull distribution, the distribution starts from 0 ($t > 0$) as opposed to γ. The PDF f(t), R(t), h(t) and MTTF for 2-parameter are derived by substituting γ=0 in Eq 2.7, 2.9, 2.10 and 2.11, we get

$$f(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1} e^{-\left(\frac{t}{\eta}\right)^{\beta}}, t \geq 0 \qquad \text{Eq. 2.12}$$

$$R(t) = e^{-(\frac{t}{\eta})^{\beta}}, t \geq 0 \qquad \text{Eq. 2.13}$$

$$h(t) = \frac{\beta}{\eta}\left(\frac{t}{\eta}\right)^{\beta-1}, t \geq 0 \qquad \text{Eq. 2.14}$$

$$MTTF = \eta * \Gamma(1 + \frac{1}{\beta}) \qquad \text{Eq. 2.15}$$

Another reliability metric used by reliability engineers is BX%. It is defined as the time at which X% of components fail. For example, some engineers use B10 life meaning time at which 10% of the population have failed.

The failure data points are plotted in weibull probability paper, and least square regression is used to fit the data points in a straight line. The CDF of 2-parameter weibull is given by

$$F(t) = 1 - e^{-(\frac{t}{\eta})^{\beta}}, t \geq 0 \qquad \text{Eq. 2.16}$$

$$1 - F(t) = e^{-(\frac{t}{\eta})^{\beta}}$$

Taking natural logarithm on both sides, we get

$$\ln\big(1 - F(t)\big) = -\left(\frac{t}{\eta}\right)^{\beta}$$

$$-\ln\big(1 - F(t)\big) = \left(\frac{t}{\eta}\right)^{\beta}$$

Taking natural logarithm again on both sides, we get

$$\ln\left(-\ln\left(1-\mathrm{F(t)}\right)\right) = \beta \ln\left(\frac{t}{\eta}\right)$$

$$\ln\left(\ln\left(\frac{1}{1-\mathrm{F(t)}}\right)\right) = \beta \ln(\mathrm{t}) - \beta \ln(\eta) \qquad \text{Eq. 2.17}$$

The above equation is of the form y = mx + c where y-axis in weibull graph is the term in the left side equation, and x-axis is ln(t) from the equation on the right side. The slope β and characteristic lifetime η are obtained from the weibull graph. Softwares like Reliasoft Weibull++, Minitab, and Weibull Smith can plot the weibull graphs and compute the parameters. The example of weibull graphs can be seen in Figure 2.20.

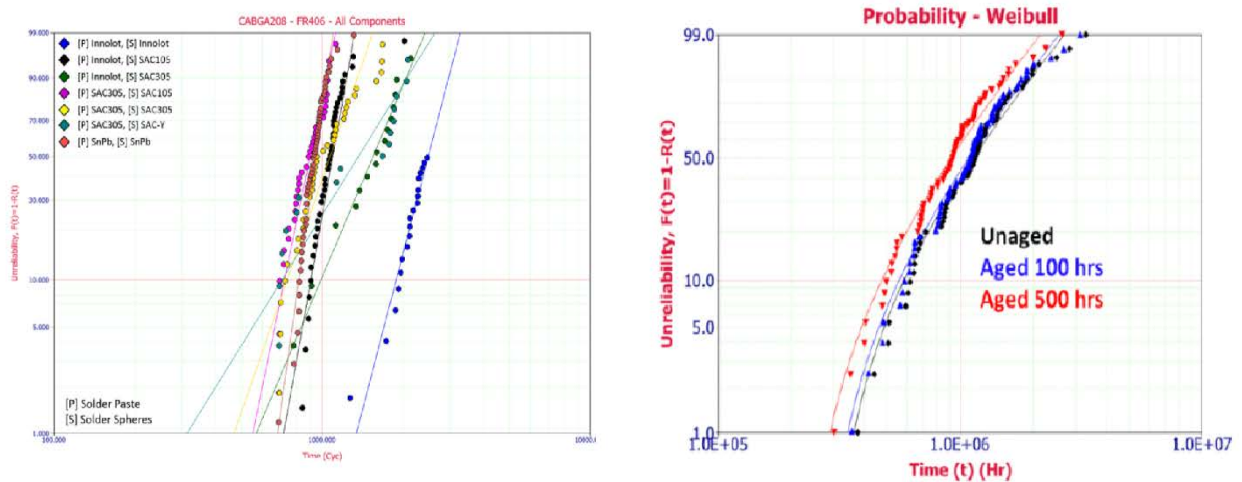


Figure 2.20 a) 2-parameter weibull graph (left) [81], b) 3-parameter weibull graph (right) [82]

2.6 Effect of Isothermal aging on solder joints

When the lead-free solder joints in electronic assemblies are isothermally aged and/or thermal cycling environment, there appears to be constant change in its microstructure, mechanical response, and failure mechanism [28]. These changes during aging effect on the solder reliability

resulting in degradation of its mechanical properties. The aging effects are aggravated at higher temperatures used thermal cycling tests. Even at room temperatures, there is a significant variation in microstructures and mechanical properties.

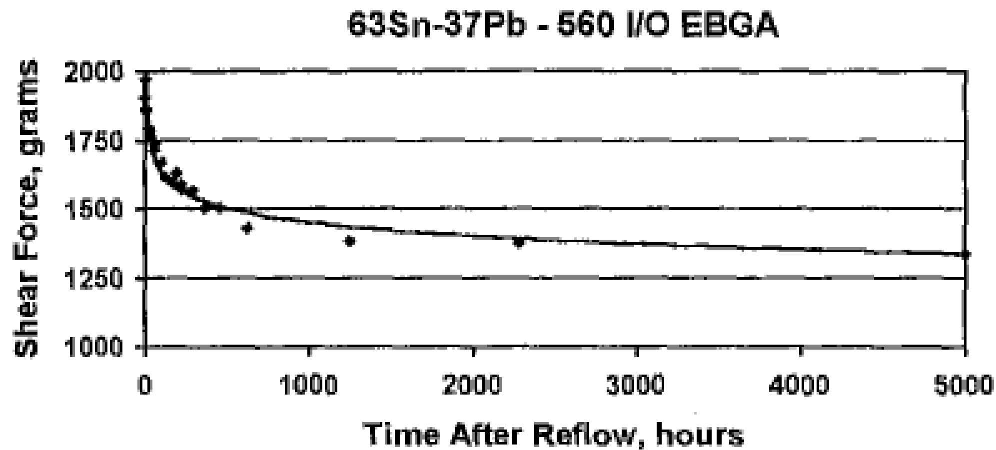


Figure 2.21 Decrease in shear force as a function of aging time after reflow for eutectic Sn-Pb solder balls [83]

Coyle [83] demonstrated the effect of aging on shear strength for eutectic SnPb solder balls. He found that after an initial 240 hours of aging at room temperature after reflow, there is approximately 20% reduction in shear force and microhardness, as shown in Figure 2.21. The change in microstructures was correlated with a reduction in shear strength and microhardness. Lee [84] conducted shear testing of eutectic SnPb solder ball from the PBGA package. He concluded that after 3 days of aging at room temperature, there is a 10% drop in shear strength, as indicated in Figure 2.22.

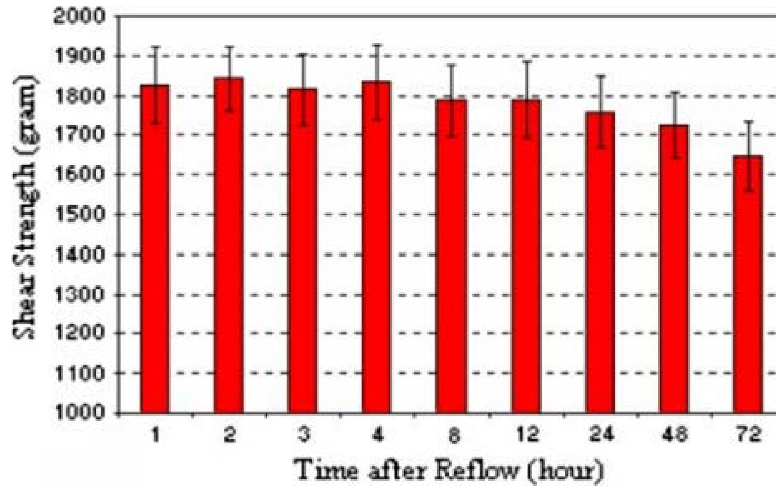


Figure 2.22 Decrease in shear strength as a function of aging time (3 days) after reflow for eutectic Sn-Pb solder balls [84]

Ma [85] did creep testing on SAC305, SAC405, and SnPb alloys that were aged at room temperature and elevated temperature (125°C). The creep rate of three alloys as a function of room temperature aging is shown in Figure 2.23a. The SAC alloys have better creep resistance compared with SnPb when aged at room temperature.

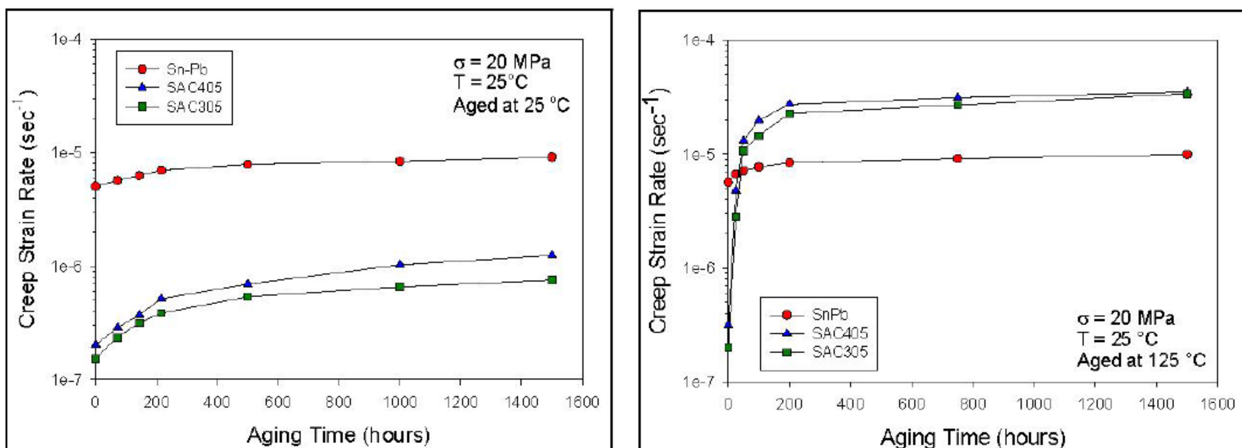


Figure 2.23 a) Comparison of SnPb and SAC creep rate for aging at room temperature (25°C), b) Comparison of SnPb and SAC creep rate for aging at elevated temperature (125°C) [85]

When aged at 125°C, the creep resistance of SAC alloys appear to be higher than SnPb until 50 hours, as shown in Figure 2.23b. After the crossover point, the creep rate of SAC alloys is higher than SnPb. Ma [86] investigated the impact of aging on thermal cycling of SAC alloys using different packages and aging temperature (100°C and 150°C).

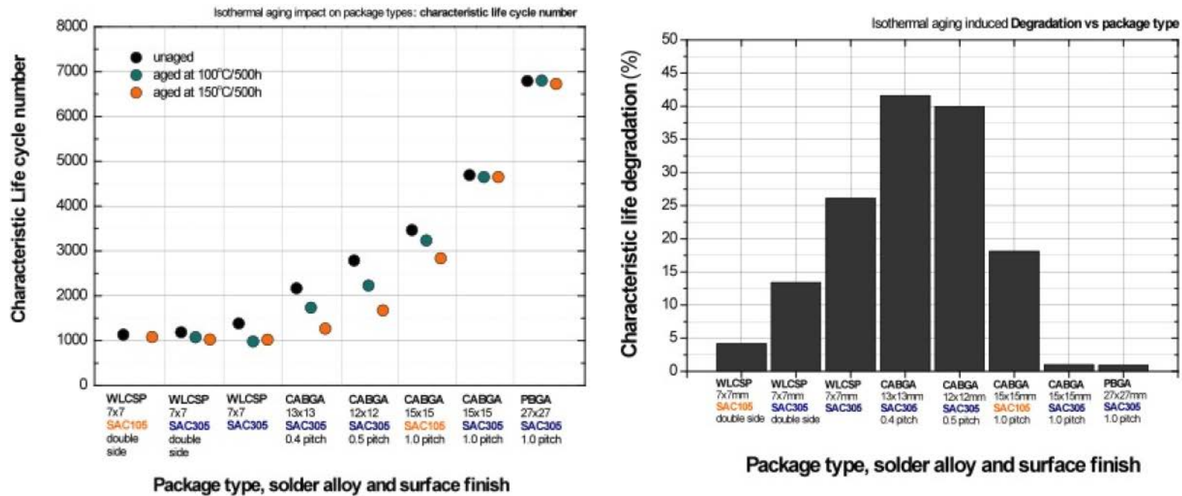


Figure 2.24 a) Characteristic lifetime of various packages before and after isothermal aging (left), b) Characteristic lifetime degradation of various packages before and after isothermal aging (right) [86]

The results shown above in Figure 2.24 illustrates that impact of aging on thermal cycling reliability is highly dependent on package type, pitch size, and solder alloys. The higher stress package resulted in a higher impact on aging and package with lower stress showed minimal aging effect. Ma [87] analyzed the aging effect on dynamic shock testing of lead-free alloys using Flip Chip BGA (FCBGA) package. The FCBGAs with different PCB materials (Phenolic and Non-phenolic) were aged at 100°C and 150°C for 500 hours and 1000 hours. He found that between 20 to 35% degradation in shock performance when aged at higher temperatures, as shown in Figure 2.25.

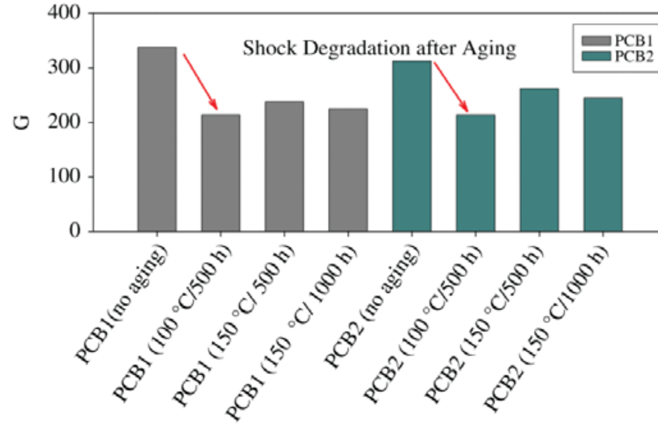


Figure 2.25 Effect of aging on shock performance on different PCB materials [87]

Zhang [88] conducted thermal cycling reliability of fine pitch packages with SAC105, SAC305, and SnPb solder alloys that were aged for 6 months (25°C, 55°C, 85°C and 125°C). Also, the comparison between ImSn, ImAg, and SnPb surface finish was performed. He found that the BGA package's characteristic lifetime degraded nearly 53% after aging at elevated temperatures. The deterioration of SAC alloys appears to be the highest compared with SnPb alloy that was tested, as shown in Figure 2.26.

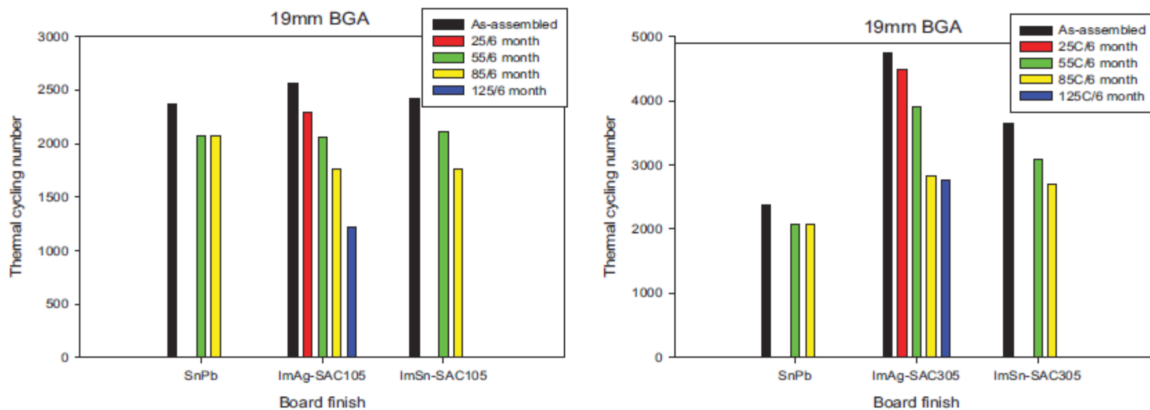


Figure 2.26 Characteristic lifetime summary of 19mm BGA with different surface finishes before and after aging: a) SAC105 and SnPb solder ball (left), b) SAC305 and SnPb solder ball (right) [88]

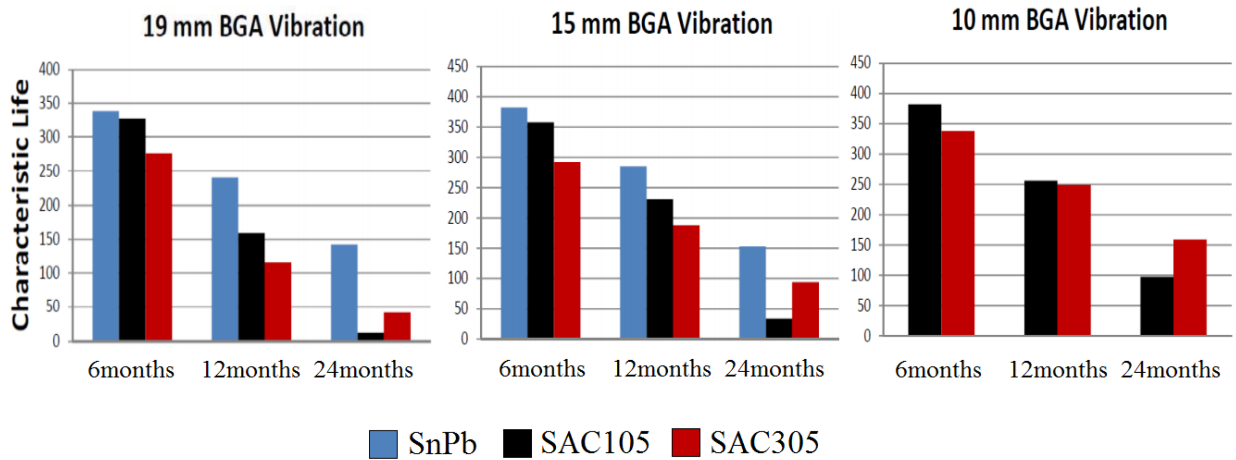


Figure 2.27 Vibration summary various BGA package aged at 55°C for the different aging times [89]

Namo [89] analyzed the effect of aging on the vibration of SnPb, SAC105 and SAC305 alloys at 55°C for 6 months, 12 months, and 24 months. The findings are shown in Figure 2.27, where he concluded that vibration performance is poorer after aging for a longer time.

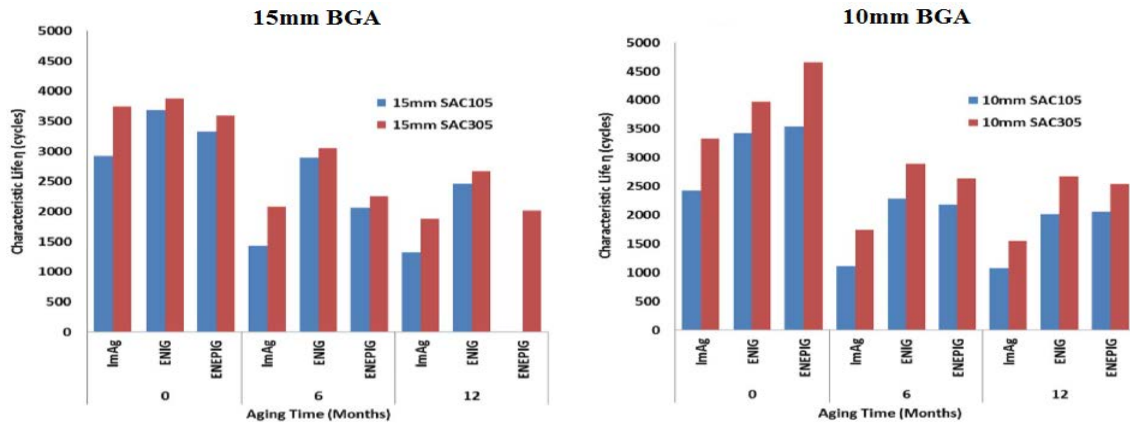


Figure 2.28 Characteristic lifetime summary of BGAs with different surface finishes before and after aging at 125°C: a) 15mm BGA (left), b) 10mm BGA (right) [42], [43]

Hai [42] and Shen [43] evaluated the long term aging effect of SAC alloys with ImAg, ENIG, and ENIPEG surface finish by conducting a thermal cycling test. They found that SAC

alloys built with ENIG and ENIPEG surface finish performed better than SAC alloys with ImAg surface finish, and these surface finishes appear to be a solution for long term reliability.

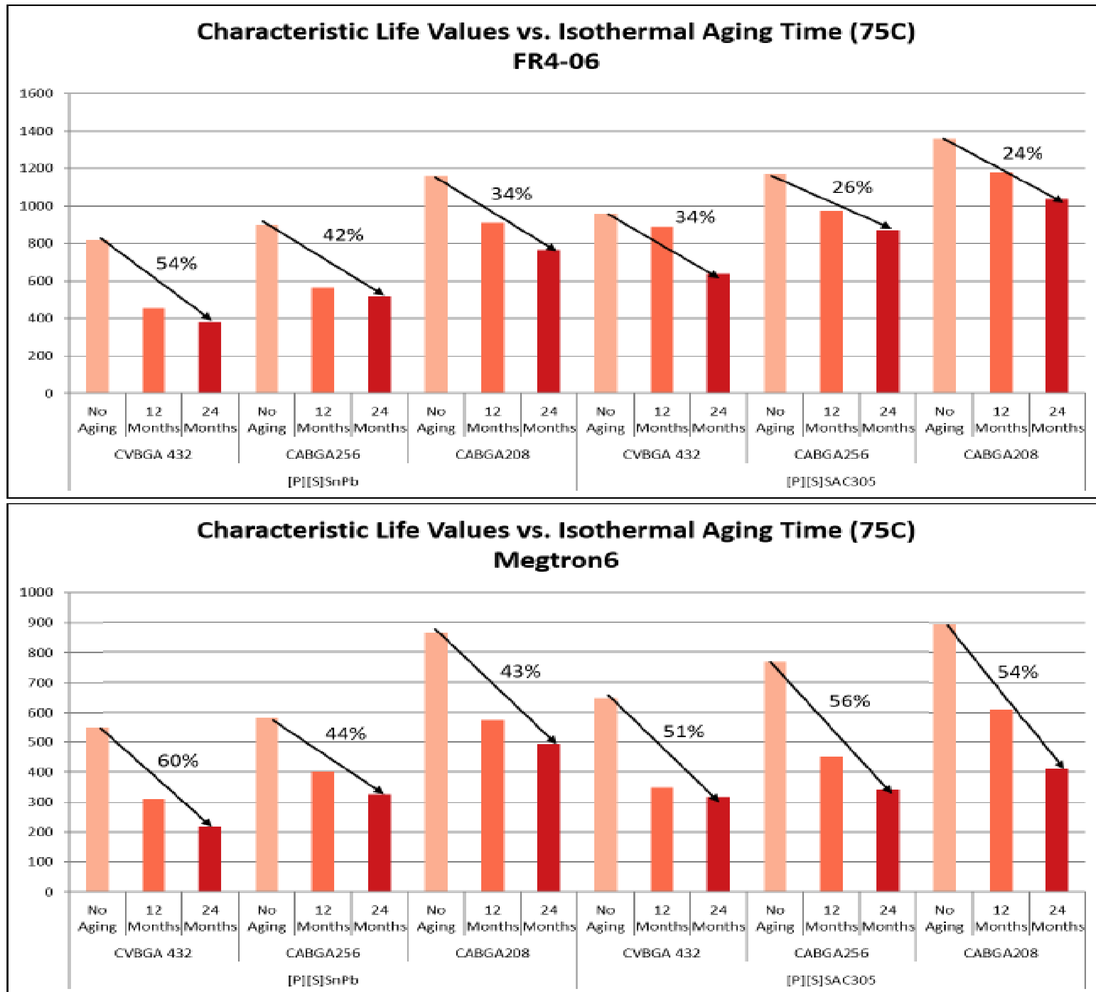


Figure 2.29 Characteristic lifetime summary of various BGAs with different board substrate before and after aging at 75°C: a) FR-406 (Top), b) Megtron6 (Bottom) [1]

Sanders [1] investigated the long term aging effect of packages on different board substrates. He found that Megtron6 deteriorates higher than FR-406 after 24 months of aging at 75°C. Zhou [90] performed long term reliability of SAC105, SAC305, and SnPb alloys. He concluded that the BGA characteristics lifetime reduced by nearly 63% after 24 months of aging

at elevated temperatures. The Finite Element Analysis (FEA) on the aging effect of solders were constructed by Motalab [91]. The revised Anand viscoplastic stress-strain relation was established based on the material parameters that changed after aging. Motalab deduced that the FEA model had shown deterioration in the package lifetime upon comparing it with experimental results done by Zhang [88].

2.7 Solder Doping

Several research papers indicated significant degradation of characteristics lifetime and mechanical properties of solder joint when aged at room temperature and elevated temperature for a longer time [1], [28], [40]–[44], [83]–[94]. One of the most critical factors that contributed towards the solder joint failure was the Cu_3Sn intermetallic growth. One effective method for dealing with the resulting package life reductions is to micro-alloy (or “dope”) the existing SAC formulations with elements such as Bismuth (Bi), Antimony (Sb), Indium (In), Nickel (Ni), Zinc (Zn), Iron (Fe), Manganese (Mn) and Cobalt (Co) to control their aging properties [95], [96]. The use of a composition-tailored solder paste is significantly advantageous from a manufacturing standpoint. The mechanical properties and the failure behavior of lead-free solder joints vary for different doped SAC alloys. These dopants can affect the Cu_3Sn intermetallic layer, thereby reducing its growth after aging [97]–[101].

Anderson [102] measured the shear strength of SAC, SAC-Fe, and SAC-Co alloys after aging at 150°C for 100 hours and 1000 hours. He found that brittle failure was observed at the IMC interface for SAC alloy, and ductile failure was seen for SAC-Fe and SAC-Co alloys. The IMC thickness of Cu_3Sn and the total IMC (Cu_3Sn + Cu_6Sn_5) thickness was plotted as a function of aging time, as shown in Figure 2.30.

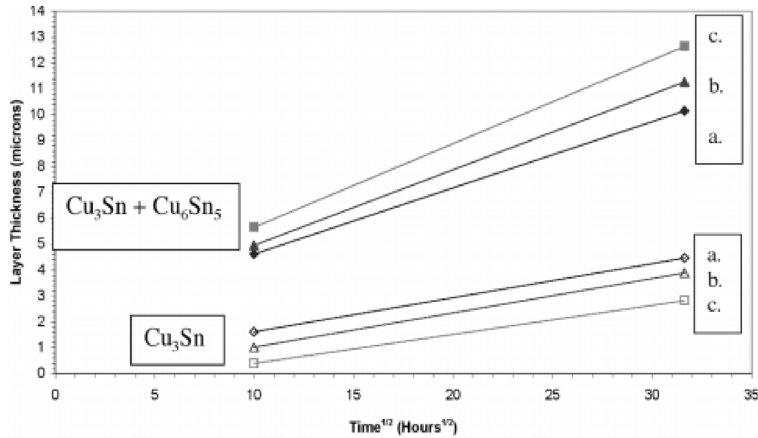


Figure 2.30 Comparison of the Cu3Sn and total IMC thickness measurements as a function of aging at 150°C for solder joints made from (a) Sn-3.7Ag-0.9Cu, (b) Sn-3.7Ag-0.7Cu-0.2Fe, and (c) Sn-3.7Ag-0.6Cu-0.3Co [102]

The SAC-Co alloy has shown reduced Cu_3Sn thickness followed by SAC-Fe alloy after aging for 1000 hours at 150°C. Anderson [103] demonstrated that there are elements beyond Co and Fe, for doping with SAC alloy, that is effective in void coalescence and embrittlement after aging. Such elements include Ni, Mn, and Zn. These elements have potential in reduction of Cu_3Sn layer, thereby reducing the overall IMC thickness.

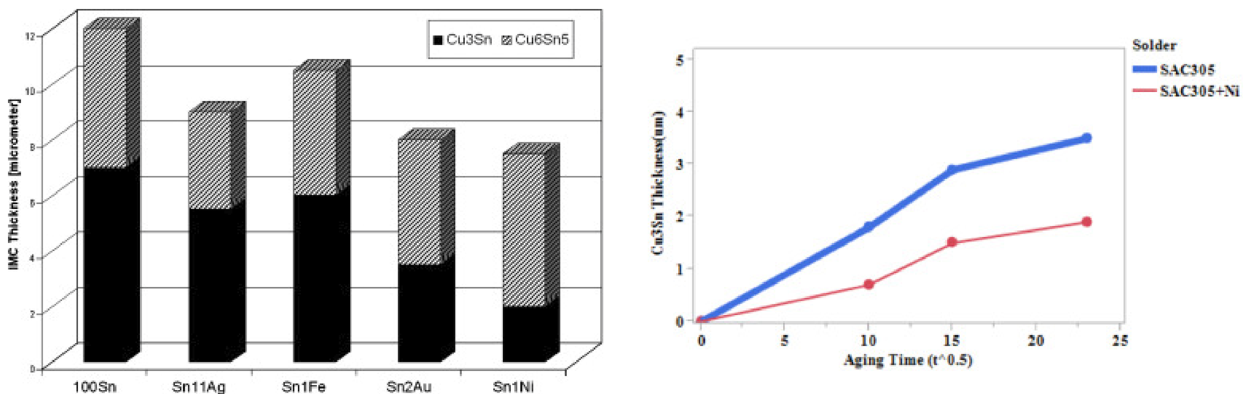


Figure 2.31 a) IMC thickness after annealing at 150°C for 2560 hours (Left) [104], b) Effect of Ni on Cu_3Sn intermetallic growth (Right) [99]

Laurila [104] studied the interfacial reaction of elements such as Ni, Au, Ag, and Fe with Sn-rich solder. The aging effect was analyzed with respect to the interfacial reaction. The IMC thickness after aging for 2560 hours at 150°C was measured at the Cu/solder interface, as shown in Figure 2.31a. The Sn doped with Ni has demonstrated a decrease in IMC growth after aging followed by Au but have a weaker effect. Henshall [99] indicated that the SAC doped with Ni could suppress the Cu_3Sn formation during aging compared with SAC305 alloy, as shown in Figure 2.31b. Wang [105] mentioned that by increasing the Ni element as small as 0.01% by weight, the Cu_3Sn growth is inhibited, as shown in Figure 2.32.

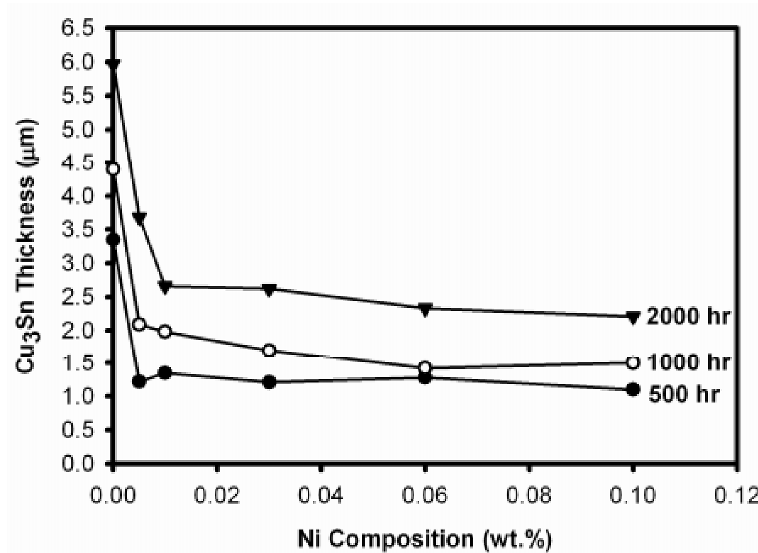


Figure 2.32 The thickness of each Cu3Sn layer plotted as a function of Ni content in Sn2.5Ag0.8Cu solder after aging at 160°C [105]

In the above figure, the SAC alloy with 0.1% Ni when aged at 160°C for a long time have shown lower IMC layer compared to SAC alloys with lower Ni. Watanabe [106] concluded that the reason behind the suppression of Cu_3Sn IMC upon SAC doped Ni alloy is the formation of $(Cu, Ni)_6Sn_5$ layer at the interface between the solder and Cu substrate. That layer acts as a barrier

to the growth of Cu_3Sn IMC layer. Yang [107] also indicated the same and also added that the more Ni is added, the thicker $(Cu, Ni)_6Sn_5$ layer it gets and the thinner Cu_3Sn IMC layer. Ni increases the strength of IMC, thereby reducing brittle failure and an increase in shear or pull strength. Jiang [108] concluded that the addition of Ni and Zn towards SAC alloy could reduce overall IMC growth ($Cu_3Sn + Cu_6Sn_5$). Also, the interfacial failure after the addition of Zn and Ni can be reduced after multiple reflow and aging.

Cheng [109] and Anderson [110] mentioned the addition of Co and Ni in SAC alloys results in refinement of β-Sn grain microstructure, undercooling suppression, and improvement in shear strength. Gao [111] studied the interfacial reaction of SAC, SAC-Ni, and SAC-Co with a copper substrate and analyzed the aging effect. He concluded Co and Ni have a higher affinity with Sn compared with Copper. The $(Cu, Ni)_6Sn_5$ and $(Cu, Co)_6Sn_5$ IMC layers were formed at the interface before aging that inhibited the diffusion of Cu_3Sn growth.

Another element known as bismuth is added to SAC solder, which is known to decrease the melting temperature of the solder. After aging, it can improve the strength of solder through precipitation hardening while suppressing the formation of Ag_3Sn IMC in bulk solder [112]–[114]. Addition of Bi to low Ag SAC solder can improve drop performance of SAC solder due to its effect on interfacial IMC though it can strengthen solder matrix [113]. The Bi addition can also result in a linear increase in Ultimate Tensile Strength (UTS) [101]. Liu [115] found that after aging, segregation of Bi can occur making the IMC more brittle though it reduces IMC growth. Ahmed [100] compared the mechanical behavior of SAC+Bi and SAC105 after aging at 100°C for 3 months. He found that SAC+Bi have shown improvement in mechanical properties and are highly resistant to aging-induced degradation.

Doping antimony with SAC solder can improve mechanical properties of solder joints, but toxicity is a significant concern [96]. The interfacial reaction analysis between Sb and SAC alloy after aging were conducted by Chen [116]. The reaction between Sb and SAC results in the formation of $Ag_3(Sn, Sb)$ in the β-Sn matrix and Cu_6Sn_5. Antimony can increase the activation energy, thereby reducing the diffusion rate and excessive IMC growth.

Another element indium is used as a doping element to lower the melting temperature. Kannachai [117] measured the effect of aging on microhardness and microstructure of SAC doped In. He found significant deterioration in microhardness over aging time and an increase in average grain size with higher Indium content. With higher In content, the mechanical strength is weaker due to its softness.

Chapter 3 Research Agenda

Due to the deleterious aging effect of SAC305 solder paste, solder paste vendors proposed different kinds of solder materials with the hope of replacing SAC305 solder paste. Electronic manufacturers must find solder materials for improvement in product reliability. Solder materials mentioned in Section 4.2 have the potential of replacing the SAC305 solder alloy. The agenda for this research is followed in a specific procedure:

Step 1: Execute liquid to liquid thermal shock testing on 9 different Pb-free alloys and compare two different aging groups - as assembled (No aging) and 6 months of isothermally aged boards at 125°C (solder downselect test)

Step 2: Perform failure analysis on solder joints and measure the Intermetallic thickness

Step 3: Downselect the solder materials that outperformed conventional SAC305 tested in liquid to liquid thermal shock testing

Step 4: Conduct accelerated Thermal Cycling Testing (TC-SJR Phase II) on downselected solder materials from the previous test

Step 5: Perform the comparison of materials between as assembled (No aging), 6 months of isothermal aging at 75°C, 12 months of isothermal aging at 75°C, and 24 months of isothermal aging at 75°C

Step 6: Perform failure analysis on solder joints and measure the Intermetallic thickness

The solder material for harsh environment electronics or high-speed supercomputer applications can be chosen based on the recommendation at the end of step 6.

Chapter 4 Solder downselect test

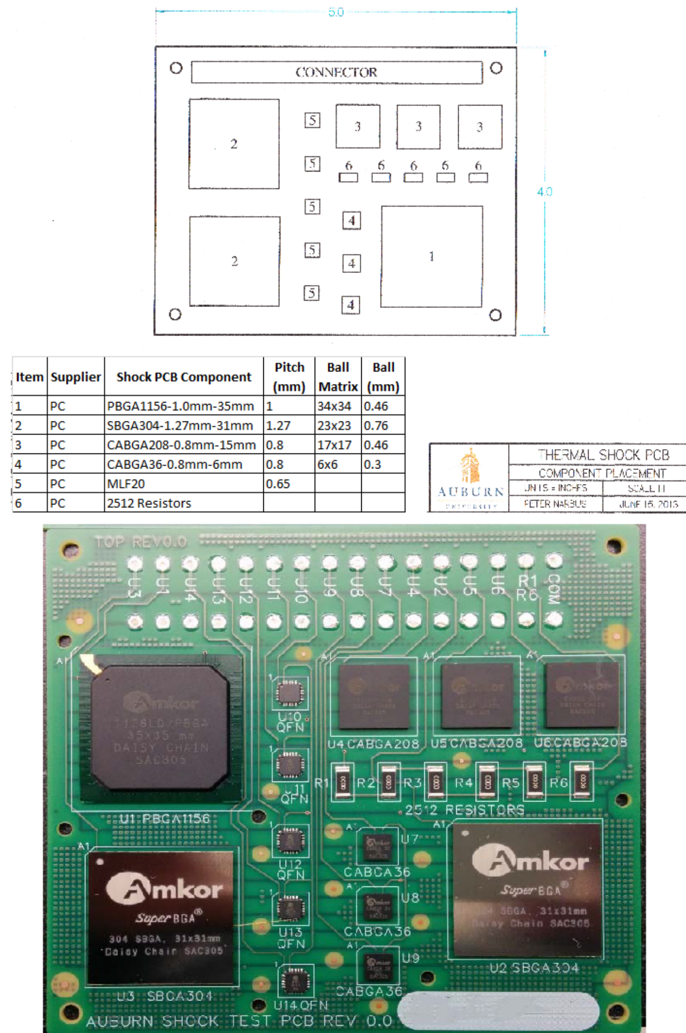
4.1 Purpose of Experiment

Previous researches indicated significant reduction in mechanical properties and characteristics lifetime of solder joint after aging at a longer duration. One method for dealing with the observed package life reduction is to microalloy (or “dope”) existing SAC formulations with elements such as Bi, Sb, In, Ni, Mn, and Co to improve the solder aging performance [95], [96]. This is an active, ongoing effort by solder paste manufacturers looking for performance improvement through the consultation of available multicomponent phase diagrams followed by new alloy synthesis and fatigue testing. Additional metals are also added by picking elements from the same column of the periodic table using intuition, luck, and empirical trials. This work is complicated by different and often conflicting solder property changes as small metal percentages are added to the base SAC305 alloy. Typically, only a fraction of 1 at% is necessary to yield significant changes in microstructure and resulting mechanical and physical properties of the solder alloy [118].

The mechanical properties and the failure behavior of Pb-free solder joints vary for different doped SAC alloys [97]–[101], [119], [120]. From the manufacturing standpoint, the use of composition tailored solder pastes offers significant advantages. This work provides a direct comparison between several solder pastes that were doped in order to reduce the aging effects of the resulting joints. The purpose of this project is to find a solder material to replace the SAC spheres and improve the package reliability. Liquid to liquid thermal shock test was conducted to evaluate solder joint reliability comparing after assembly and 6month aged materials.

4.2 Board Design and Assembly

The test vehicle was manufactured by TTM Technologies (Time-To-Market Interconnect Solutions), Chippewa Falls Division.



Item	Supplier	Shock PCB Component	Pitch (mm)	Ball Matrix	Ball (mm)
1	PC	PBGA1156-1.0mm-35mm	1	34x34	0.46
2	PC	SBGA304-1.27mm-31mm	1.27	23x23	0.76
3	PC	CABGA208-0.8mm-15mm	0.8	17x17	0.46
4	PC	CABGA36-0.8mm-6mm	0.8	6x6	0.3
5	PC	MLF20	0.65		
6	PC	2512 Resistors			

Figure 4.1 Thermal shock board design (top), assembled board (bottom)

The test boards used were standard 6-layer PCB's composed of copper vias, glass epoxy covered by a thin solder mask on both sides and an overlaid silkscreen for labeling. All the components mounted on the boards were chosen carefully to study their thermal shock reliability

with various doped solder pastes in both non-aged and aged conditions. Each of the test boards has a dimension of 107 x 127 mm, as seen in Figure 4.1.

The test vehicle had three 15mm BGA's (CABGA208), three 6mm BGA's (CABGA36), two 31mm BGA's (SBGA304), one 35mm BGA (PBGA1156), six 2512 resistors, and six QFN's. The surface finish material was OSP. The surface finish used on the BGA package was ENIG and the board substrate used was FR-406. The BGA package substrate was Bismaleimide Triazine (BT). The test vehicle was designed to accommodate different BGA packages to investigate the effects of solder paste and solder alloy. The test boards were built with different solder alloys, as shown in Table 4.1. The 2512 resistors and 5mm QFN packages with 0.65mm pitch were added to understand the effect of doped solder paste on conventional packages.

Table 4.1 Solder alloy composition

Solder Paste Manufacturers	Material Code	Solder Alloy Composition
Alpha	SAC305	96.5Sn-3Ag-0.5Cu
	Innolot	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
	Maxrel Plus	Sn-3.8Ag-0.8Cu-3Bi-x1-x2
Heraeus	HT1.02	95Sn-2.5Ag-0.5Cu-2In
Accurus	Ecolloy	96.62Sn-0.92Cu-2.46Bi
Henkel	90SCLF318AGS88.5	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni (Type 3)
Indium	8399Y	Sn-0.5Ag-1Cu-0.03Mn
	Material 2	SAC Doped Sb
Inventec	Ecorel Free 405Y-16	Sn-4Ag-0.5Cu-0.05Ni

The solder downselect test matrix with different solder combinations, and the number of packages used is shown in Table 4.2. The QFN's and 2512 resistors consist of 100% Sn solder termination. Some of the 15mm (CABGA 208) and 31mm (SBGA 304) package were doped with

matched solder alloy, which means the solder termination in package ball alloy is same as solder pastes. The SAC305 solder paste doped with SAC305 alloy is considered as a baseline. All the other BGA packages consist of SAC305 solder ball alloy which can be seen in the table below. The total number of packages for each paste/solder ball combination is shown in Table 4.2; half were tested after assembly and the other half after 6 months of isothermal aging at 125°C.

Table 4.2 Solder downselect test design matrix

Solder Paste	Solder Ball Alloy	Package					
		15mm BGA	31mm BGA	35mm BGA	6mm BGA	QFN	2512 Resistors
SAC305	SAC305	60	40	20	80	X	X
	Sn	X	X	X	X	100	120
	Sn-0.92Cu-2.46Bi	30	20	X	X	X	X
Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni	SAC305	90	60	30	120	X	X
	Sn	X	X	X	X	150	300
Sn-2.5Ag-0.5Cu-2In	SAC305	90	60	30	120	X	X
	Sn	X	X	X	X	150	300
	Matched	30	20	X	X	X	X
Sn-3.8Ag-0.8Cu-3Bi-x1-x2	SAC305	90	30	30	120	X	X
	Sn	X	X	X	X	150	300
	Matched	30	10	X	X	X	X
Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni	SAC305	90	60	30	120	X	X
	Sn	X	X	X	X	150	240
Sn-0.5Ag-1Cu-0.03Mn	SAC305	90	30	30	120	X	X
	Sn	X	X	X	X	150	240
Sn-4Ag-0.5Cu-0.05Ni	SAC305	30	X	10	40	X	X
	Sn	X	X	X	X	150	60
SAC Doped Sb	SAC305	90	30	30	120	X	X
	Sn	X	X	X	X	150	240

4.2.1 Board Assembly process

All the boards were assembled at the University of Alabama at Huntsville (UAH) Electronics Packaging Lab. An EFAB Electroform stencil was used for stencil printing, where the

thickness of 4 mil (0.004 in) and 6 mil (0.006 in) were used. The solder paste print machine used was an MPM UP2000 HiE, as seen in Figure 4.2.

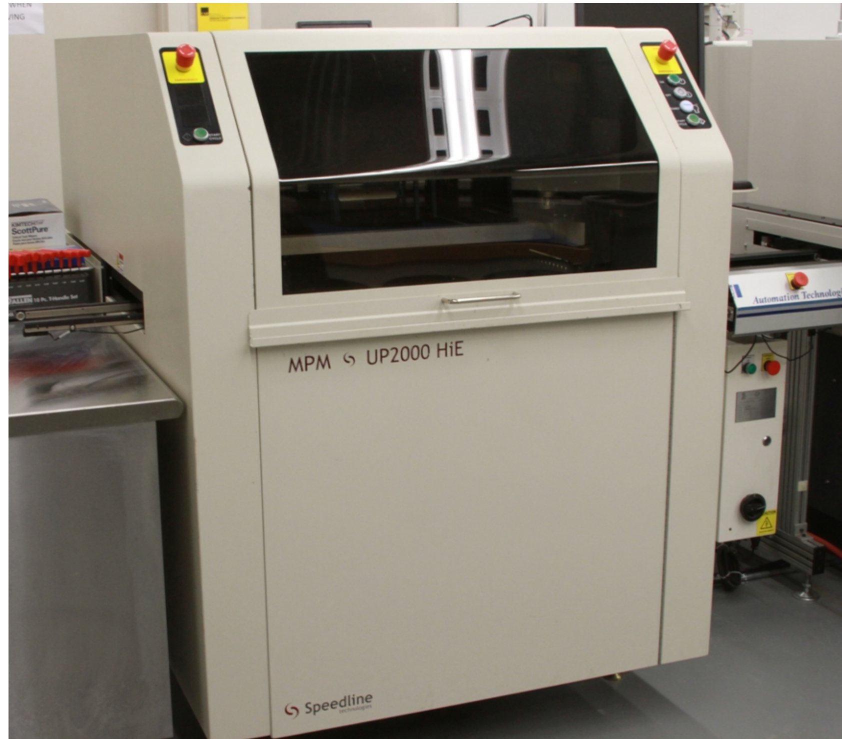


Figure 4.2 Solder paste print machine MPM UP2000 HiE

After solder paste is stencil printed on the PCB substrate, the assembly was inspected and verified by a 3D inspection process to check the area and the volume of the paste. The 3D inspection process machine used was Vision Master VM400 manufactured by ASC International, as shown in Figure 4.3. The VM400 is capable of making precise, 3-D measurements quickly and easily. To achieve high-resolution 3-D measurements, the VM400 uses sophisticated, proprietary image processing algorithms and a structured white light scheme. Height points are computed for every pixel in the field of view (FOV). The FOV consists of 640x480 (307,200) pixels. This gives the user a complete high-resolution 3-D profile of an object measured using VM400. The solder

paste height was measured on 32 pad locations for every 5th board to ensure the height falls under the acceptable range.

Figure 4.3. Vision Master 400

Figure 4.4. Assembleon MG-1 pick and place machine

Then the assembly is transferred to Assembleon MG-1 pick-and-place machine, shown in Figure 4.4, with a tray feeder to pick and place all the components. The machine has a pre-stored programmed algorithm to pick and place all test components onto the test vehicle correctly in order. The board was rechecked in case of skewed package placement.

The assembly for thermal shock boards was placed in 8-zone Vitrionic SMR800 reflow oven, as shown in Figure 4.5. The oven operates within a nitrogen gas environment. The reflow profile limits can be seen in Table 4.3. Low, Best and High are the three different reflow profiles that have been used. The values used in Low and High profile are shown under low limit and high limit in Table 4.3. The values for Best profile is set between low and high limit shown in Table 4.3. The thermal profiling used here is KIC 2000 Technology.

Figure 4.5. Vitrionic SMR800 reflow oven

Table 4.3. Reflow profile limits

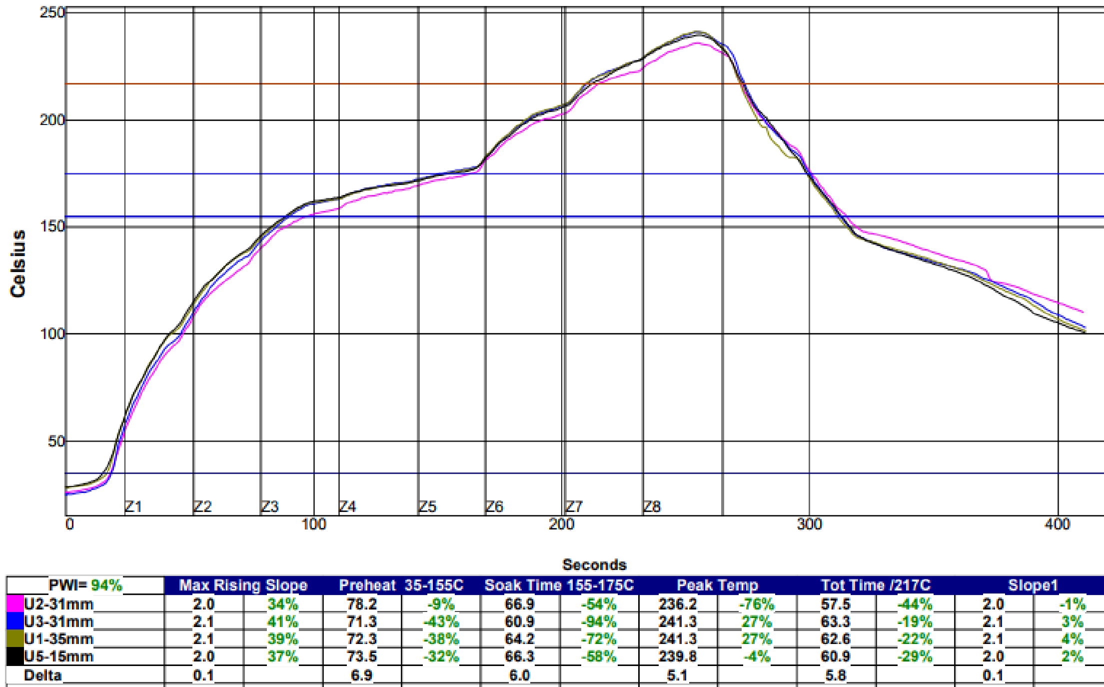
Statistics Name	Low Limit	High Limit
Maximum Rising Slope (°C/sec)	0	3
Preheat Time (seconds)	60	100
Soak Time (seconds)	60	90
Peak Temperature (°C)	235	245
Total Time Above Liquidus Temperature (seconds)	45	90
Cooling rate (°C/sec)	0	4

The preheat temperature was in the range of 35°C to 155°C. The soak temperature used was between 155°C to 175°C. The set point temperatures in different zones and conveyor speed for each profile are shown in Table 4.4.

Table 4.4. Reflow profile set point temperatures

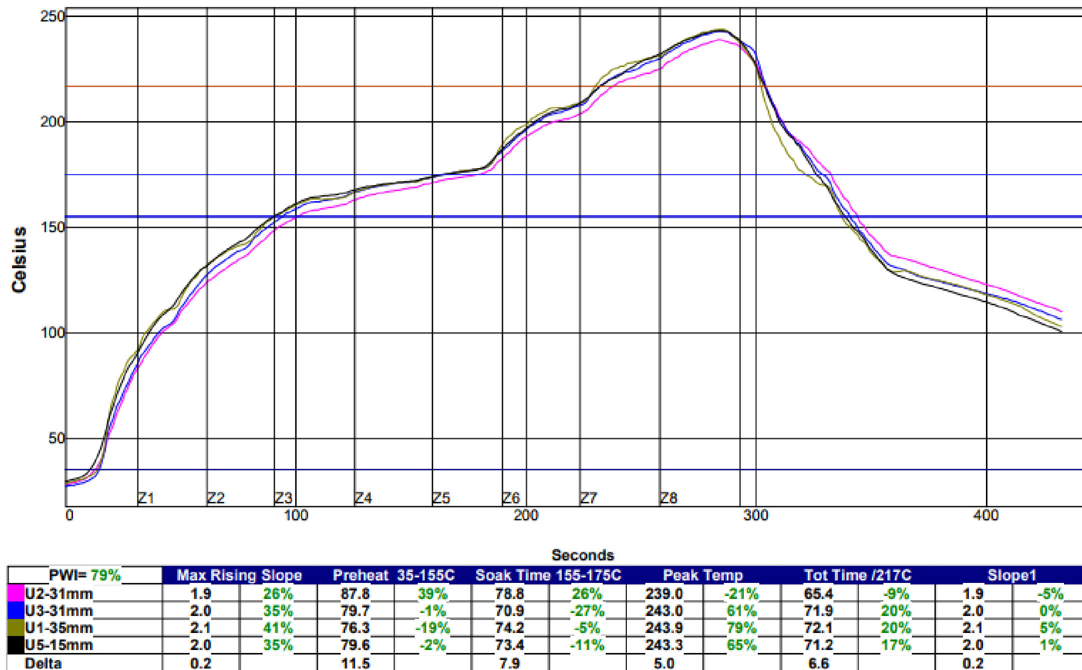
Profile	Conveyor speed (inch/min)	Zone Setpoint Temperature (°C)							
		1	2	3	4	5	6	7	8
Best	26	165	170	185	180	183	236	257	260
Low	29.6	165	175	190	180	180	240	260	260
High	23	160	170	180	180	180	240	255	255

The thermocouples were placed on different locations of the board to measure the temperature during 3 different reflow profile. The reflow profile has been determined through testing to make sure the solder joints have the best wetting and least board damage. The thermocouple readings for 8-zones in thermal shock test boards are shown in Figure 4.6 - Figure 4.8.



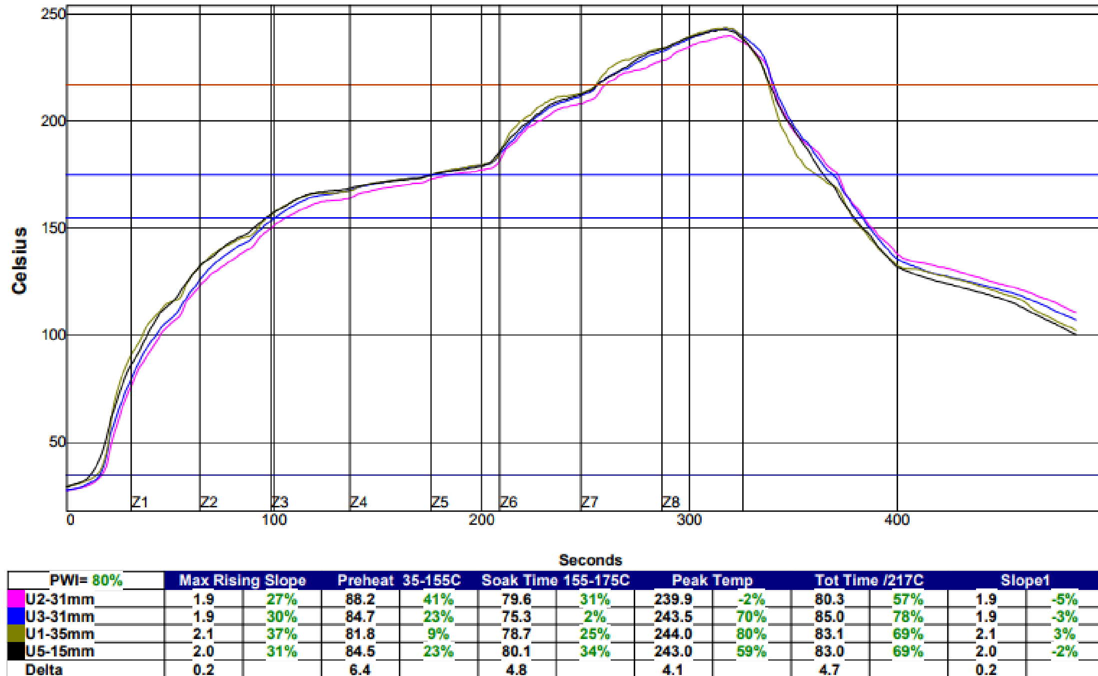
PWI= 94%	Max Rising Slope		Preheat 35-155C		Soak Time 155-175C		Peak Temp		Tot Time /217C		Slope1	
U2-31mm	2.0	34%	78.2	-9%	66.9	-54%	236.2	-76%	57.5	-44%	2.0	-1%
U3-31mm	2.1	41%	71.3	-43%	60.9	-94%	241.3	27%	63.3	-19%	2.1	3%
U1-35mm	2.1	39%	72.3	-38%	64.2	-72%	241.3	27%	62.6	-22%	2.1	4%
U5-15mm	2.0	37%	73.5	-32%	66.3	-58%	239.8	-4%	60.9	-29%	2.0	2%
Delta	0.1		6.9		6.0		5.1		5.8		0.1	

Figure 4.6. Thermal shock test reflow profile – Low



PWI= 79%	Max Rising Slope		Preheat 35-155C		Soak Time 155-175C		Peak Temp		Tot Time /217C		Slope1	
U2-31mm	1.9	26%	87.8	39%	78.8	26%	239.0	-21%	65.4	-9%	1.9	-5%
U3-31mm	2.0	35%	79.7	-1%	70.9	-27%	243.0	61%	71.9	20%	2.0	0%
U1-35mm	2.1	41%	76.3	-19%	74.2	-5%	243.9	79%	72.1	20%	2.1	5%
U5-15mm	2.0	35%	79.6	-2%	73.4	-11%	243.3	65%	71.2	17%	2.0	1%
Delta	0.2		11.5		7.9		5.0		6.6		0.2	

Figure 4.7. Thermal shock test reflow profile – Best



PWI= 80%	Max Rising Slope		Preheat 35-155C		Soak Time 155-175C		Peak Temp		Tot Time /217C		Slope1	
U2-31mm	1.9	27%	88.2	41%	79.6	31%	239.9	-2%	80.3	57%	1.9	-5%
U3-31mm	1.9	30%	84.7	23%	75.3	2%	243.5	70%	85.0	78%	1.9	-3%
U1-35mm	2.1	37%	81.8	9%	78.7	25%	244.0	80%	83.1	69%	2.1	3%
U5-15mm	2.0	31%	84.5	23%	80.1	34%	243.0	59%	83.0	69%	2.0	-2%
Delta	0.2		6.4		4.8		4.1		4.7		0.2	

Figure 4.8. Thermal shock test reflow profile – High

4.2.2 Board Inspection and Voiding Analysis

Quality assurance steps were taken. The resistance of each daisy-chained circuit component was checked by hand following reflow to eliminate them from inclusion in further testing. The yield was high.

Boards were also visually inspected, and x-ray analysis was used to determine typical solder-joint quality following reflow. X-ray voiding analysis indicated that build quality was found to be good.

Figure 4.9 and Figure 4.10 show representative voiding images for boards assembled with SAC305 solder paste and Innolot solder paste, respectively.

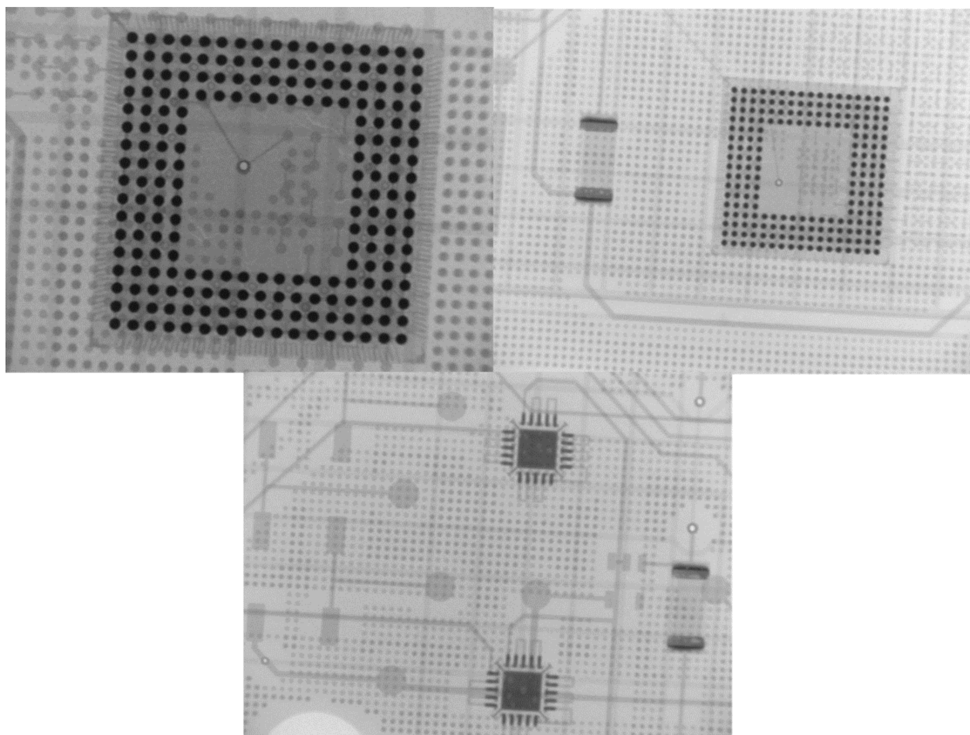


Figure 4.9. Representative X-ray inspection images for SAC305

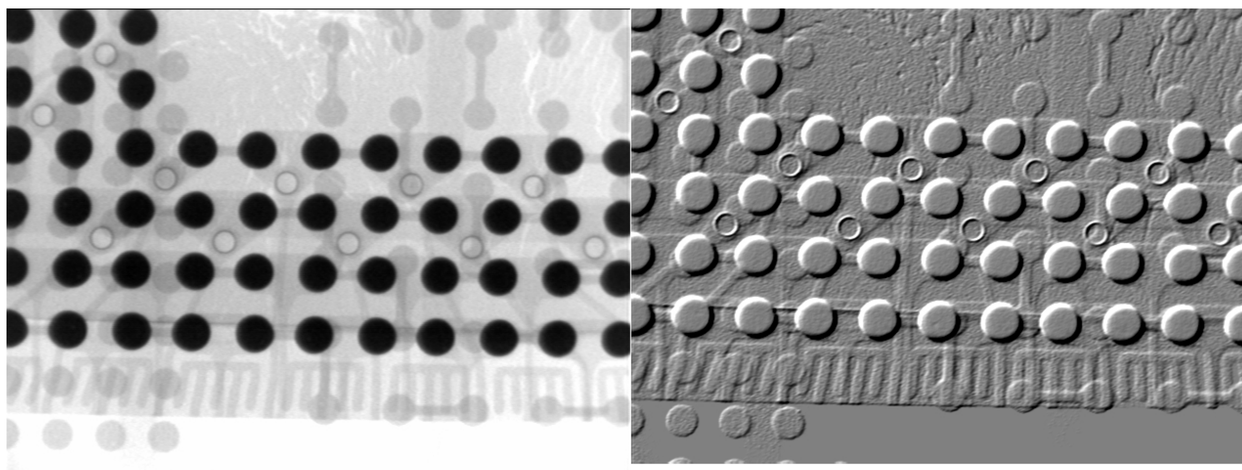


Figure 4.10. Representative X-ray inspection images for Innolot

4.3 Experimental Setup

4.3.1 Overview of Test Description

The boards were placed in Cincinnati Sub Zero Thermal Shock Bath (CSZ TSB) environmental chamber, as seen in Figure 4.11. They were exposed to the sudden extreme change in temperature from -40°C to +125°C. They were kept in a basket in which the transfer mechanism takes place. Since the boards are immersed in the liquid at extreme temperatures, it is subjected to higher thermal stress. The solder joint reliability was assessed under thermal shock condition.

Figure 4.11 Cincinnati Sub-Zero thermal shock bath chamber

4.3.2 Preliminary Test Setup

Galden D02TS fluid was filled on both the baths. The basket transfer mechanism was controlled by a Watlow F4 controller. First, the Watlow F4 controller was programmed based on the thermal profile requirement. Limit 97 controller was set up to measure the temperature of the

load. The High/Low limit temperature measured by the thermocouple was set using the Limit 97 controller. Limit 97 controller is used to display safety and limit messages created by the user to meet the requirements. Also, it provides safety assurance against instances where a high-temperature runaway condition could occur from a shorted input sensor or an output device that could fail in a closed position. The profile was executed without the actual boards. It is necessary to test the chamber first to ensure the smooth basket transfer and temperature of both the baths stays at the targeted temperature.

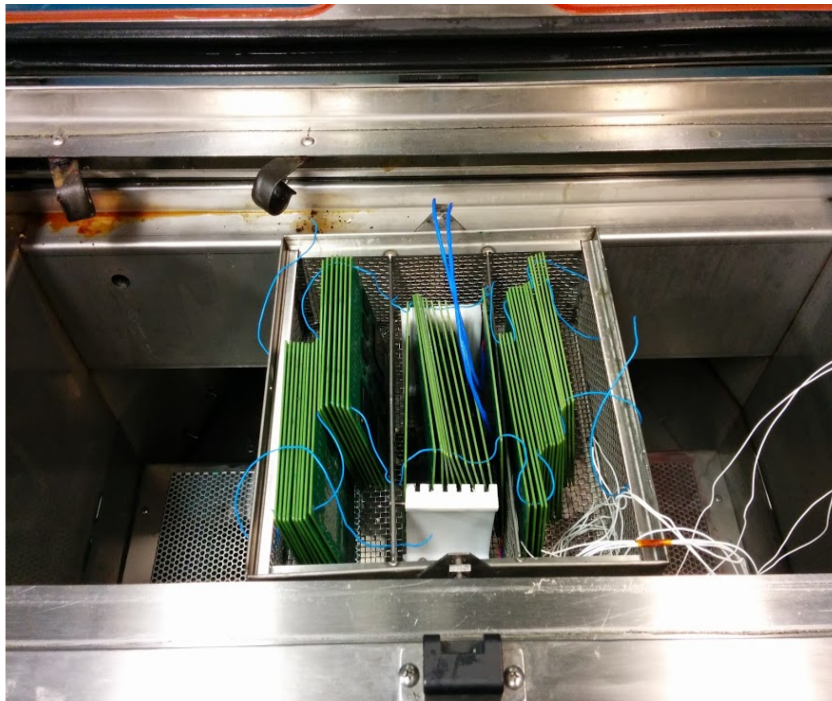


Figure 4.12. Thermal shock board setup

It is essential to check if the refrigerant compressor cools to -40°C. Then the boards were placed into the basket after the whole operation is smooth. Time to failure (cycles) for each component was measured after every 50 cycles. Fifty boards were tested at a time in the chamber, as seen in Figure 4.12. The boards assembled with different solder materials were subjected to a

liquid thermal shock test from -40°C to +125°C. The thermal shock consisted of 5-minute dwell time at each temperature extreme and 2.5-minute transition time. The test was stopped at 3000 cycles.

4.4 Result and Analysis

The package attributes for 15mm BGA (CABGA208) and 31mm BGA (SBGA304) are shown in Table 4.5. The material properties of packages and PCB used in liquid to liquid thermal shock are shown in Table 4.6 and Table 4.7. These material properties were collected from the literature [121], [122].

Table 4.5 Package Attributes for 15mm and 31mm BGA

Attribute	CABGA208	SBGA304
Package Size	15 x 15mm	31 x 31mm
Package Substrate	Bismaleimide Triazine (BT)	Bismaleimide Triazine (BT)
Package Type	Plastic	Metal capped
Package Thickness	1.0mm	1.25mm
Package Surface Finish	Electroless Nickel Immersion Gold (ENIG)	Electroless Nickel Immersion Gold (ENIG)
Die Size	12.7 x 12.7mm	10.8 x 10.8mm
Die Thickness	0.28mm	0.35mm
Solder Ball Count	208	304
Solder Ball Pitch	0.8mm	1.27mm
Solder Ball Metallurgy	SAC305/Matched	SAC305/Matched
Solder Ball Alignment	Perimeter	Perimeter
Solder Ball Diameter	0.36 ± 0.05mm	0.93mm
Solder Ball Height	0.30 ± 0.05mm	0.52mm

Table 4.6 Material properties of 15mm BGA [121] and 31mm BGA [122]

CABGA Package		
Material	Elastic Modulus (GPa)	CTE (ppm/°C) T (°C): -40 to 125
Copper Pad	129	16.3 x 10^{-6}
Silicon Die	152	2.5 x 10^{-6}
Die Adhesive	6.77	83.6 x 10^{-6}
Solder Mask	3.1	30.0 x 10^{-6}
Mold	23.52	10.0 x 10^{-6}
BT Substrate	17.89 (xy)	12.42 x 10^{-6} (xy)
	7.85 (z)	57 x 10^{-6} (z)

SBGA Package		
Material	Elastic Modulus (GPa)	CTE (ppm/°C) T (°C): 25 to 125
Copper Heat spreader	115.2	16.3 x 10^{-6}
Copper Ring	114.6	16.3 x 10^{-6}
Copper Pad	89.9	16.3 x 10^{-6}
Silicon Die	152	2.5 x 10^{-6}
Die Adhesive	1.2	83.6 x 10^{-6}
Solder Mask	6.8	30.0 x 10^{-6}
Mold	10.9	10.0 x 10^{-6}
BT Substrate	17.89 (xy)	12.42 x 10^{-6} (xy)
	7.85 (z)	57 x 10^{-6} (z)

Table 4.7 Material properties of FR-406 board substrate [121]

PCB Board		
Material	Elastic Modulus (GPa)	CTE (ppm/°C) T (°C): -40 to 125
FR-406	19.3 (xy) @-40℃	14.5 x 10^{-6} (xy)
	13.2 (xy) @125℃	
	8.48 (z) @25℃	67.2 x 10^{-6} (z)
	5.84 (z) @125℃	

A 2-parameter weibull (β, η) was used to analyze the reliability data for the 15mm BGA's, 31mm BGA's, and 2512 resistor packages. The shape (β) classifies the different failure modes. The characteristic lifetime denoted as η is a time in which 63.2% of the packages are expected to fail. There were no significant failures for 5mm BGA's, 35mm BGA's, and QFN's.

4.4.1 15mm BGA (CABGA 208)

The solder joint diameter after attach for 15mm BGA package was 0.55 mm and the height was 0.36 mm. Figure 4.13 shows the failure data for 15mm BGA package with various Pb-free solder pastes with SAC305 solder ball alloy after assembly (No aging) and thermal shock testing.

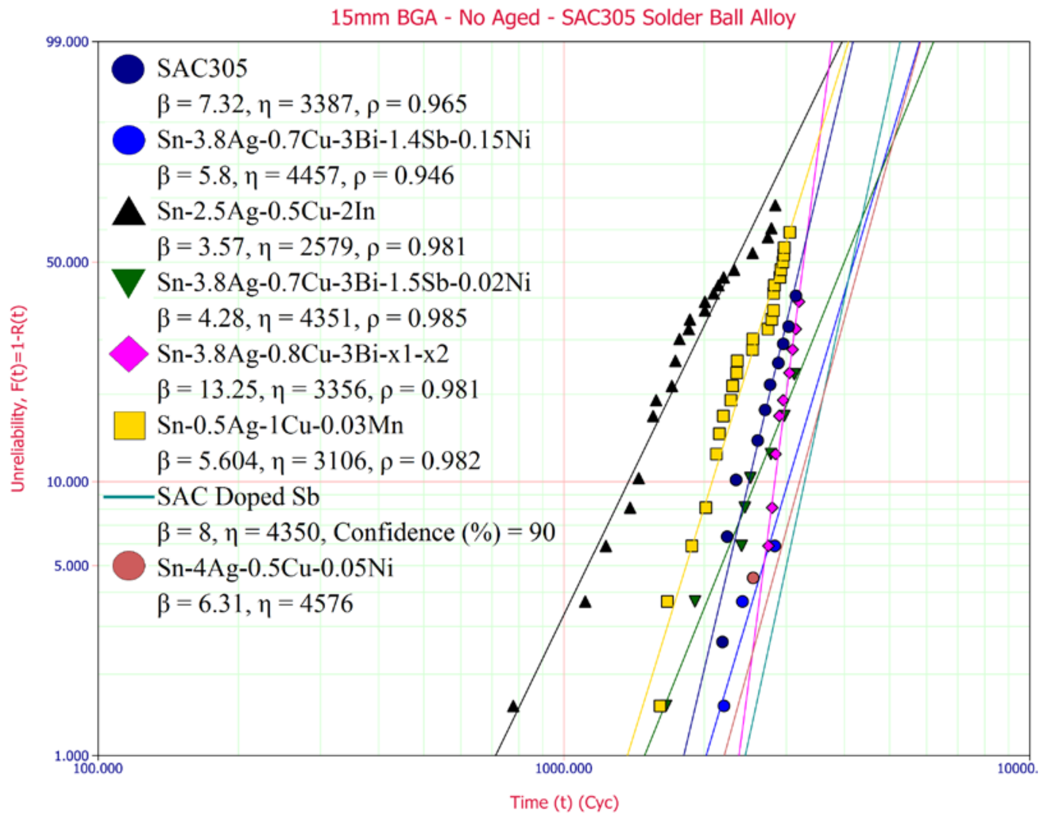


Figure 4.13 Weibull analysis for 15mm BGA with SAC305 solder ball alloy – As assembled

The solder pastes which performed substantially better than SAC305 solder paste and solder ball alloy were

- Sn-4Ag-0.5Cu-0.05Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni
- SAC doped Sb

No failures were seen for SAC doped Sb solder paste, and therefore 1-parameter weibull was used for estimation. The same given solder pastes after 6 months of aging at 125°C and thermal shock testing is shown in Figure 4.14.

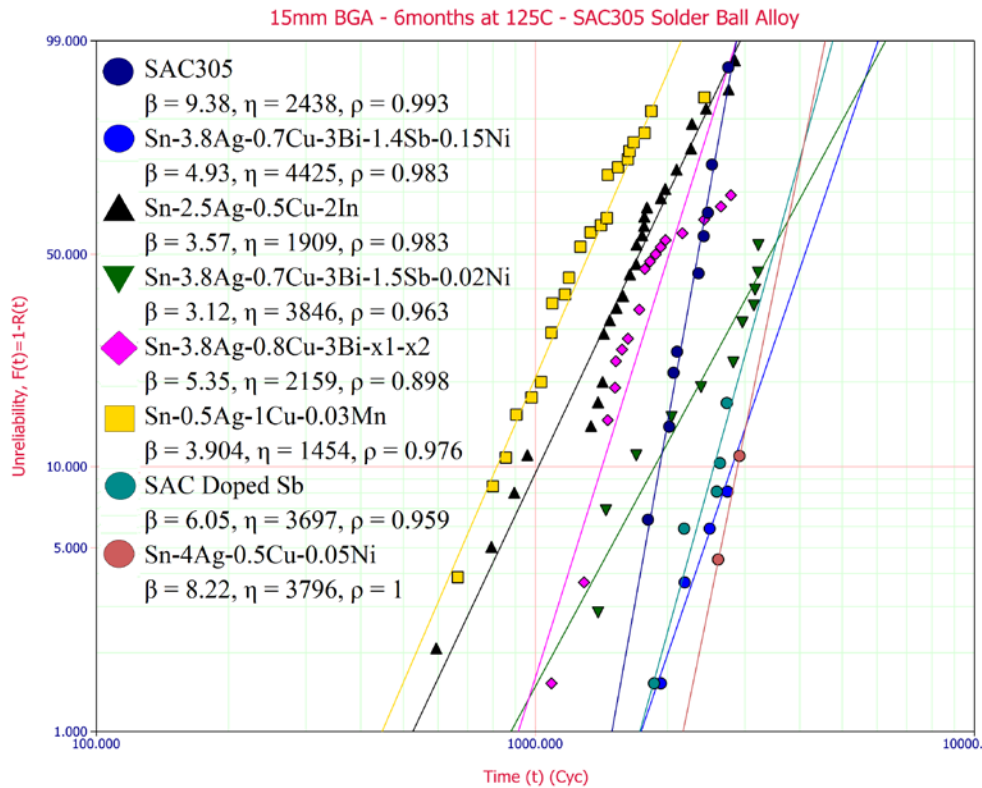


Figure 4.14 Weibull analysis for 15mm BGA with SAC305 solder ball alloy – 6 months at 125°C

After aging, the solder pastes with Bi, Ni, and Sb showed superior reliability compared with SAC305. The materials which performed better than SAC305 shows the following trend in the decreasing order of characteristics lifetime

- Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni
- Sn-4Ag-0.5Cu-0.05Ni
- SAC doped Sb

Figure 4.13 shows the failure data for 15mm BGA package with various Pb-free solder pastes with Matched solder ball alloy after assembly (No aging) and thermal shock testing.

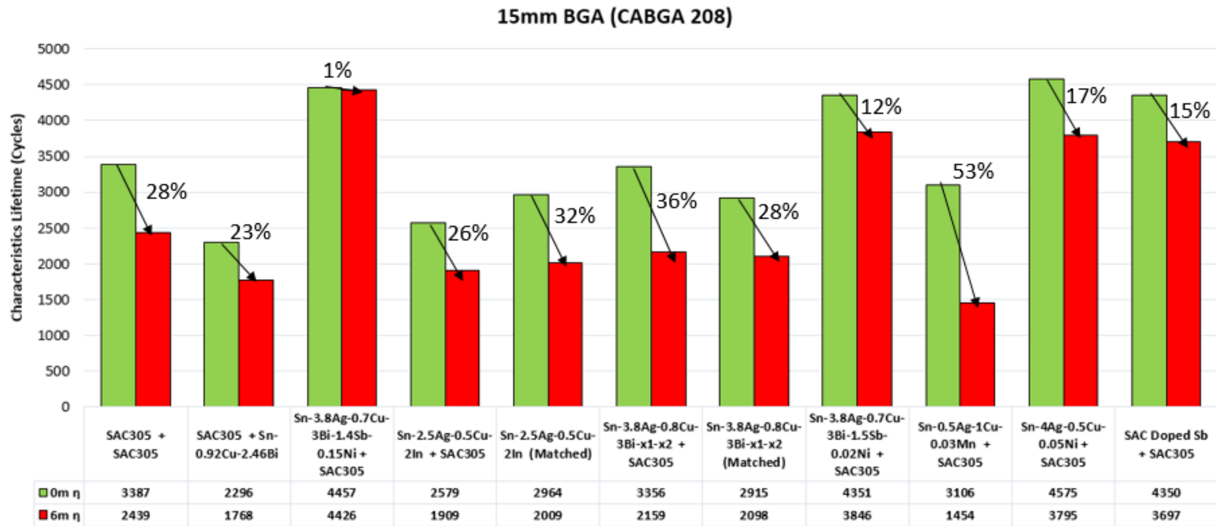


Figure 4.15 Characteristics lifetime summary of 15mm BGA packages

It is essential to analyze the effect of dopants after aging and therefore, the comparison of characteristics lifetime for the 15mm BGA package with characteristics lifetime degradation after aging is shown above in Figure 4.15. It can be seen that the addition of In towards SAC alloys did not show any improvement in characteristics lifetime compared with the baseline SAC305 paste after assembly and aging. But there is a difference in lifetime when the BGA is reballed with Sn-2Ag-0.5Cu-2In alloy and then mixed with the same paste, which appeared to be better than the SAC305 solder alloy.

Even though the Sn-0.92Cu-2.46Bi alloy ball on the BGA package mixed with SAC305 paste underperformed the baseline SAC305, the deterioration rate decreased with the addition of bismuth. The addition of bismuth in Sn-3.8Ag-0.8Cu-3Bi-x1-x2 solder paste and ball alloy did mitigate the effect of aging at 28% as opposed to 36% when mixed with SAC305 solder alloy.

The addition of manganese towards SAC alloy did not show any enhancement in the thermal shock resistance for Sn-0.5Ag-1Cu-0.03Mn solder paste and it has shown to be a poor combination.

Doping antimony to SAC alloy has improved the lifetime of the solder joints compared with the baseline SAC305. The addition of bismuth, antimony and nickel have proved to be useful in enhancing the mechanical strength of the solder material in Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni pastes. The higher percentage of Ag also showed superior reliability due to an increase in number of Ag_3Sn precipitate in Sn-4Ag-0.5Cu-0.05Ni solder.

The materials which showed reduced degradation of characteristics lifetime after aging and superior reliability compared with SAC305 are Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni, Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, Sn-4Ag-0.5Cu-0.05Ni, and SAC doped Sb solder pastes.

4.4.2 31mm BGA (SBGA 304)

Figure 4.16 shows failure data for the 31mm BGA package with various Pb-free solder pastes with the SAC305 solder ball alloy after assembly (No aging) and thermal shock testing.

The only solder pastes which performed better than SAC305 solder paste and solder ball alloy were

- Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni

Addition of Bi, Sb, and Ni to SAC solder paste appeared to improve the reliability after assembly which correlates with 15mm BGA package. SAC doped Sb which did well in 15mm BGA underperformed for 31mm BGA package compared with SAC305 solder pastes.

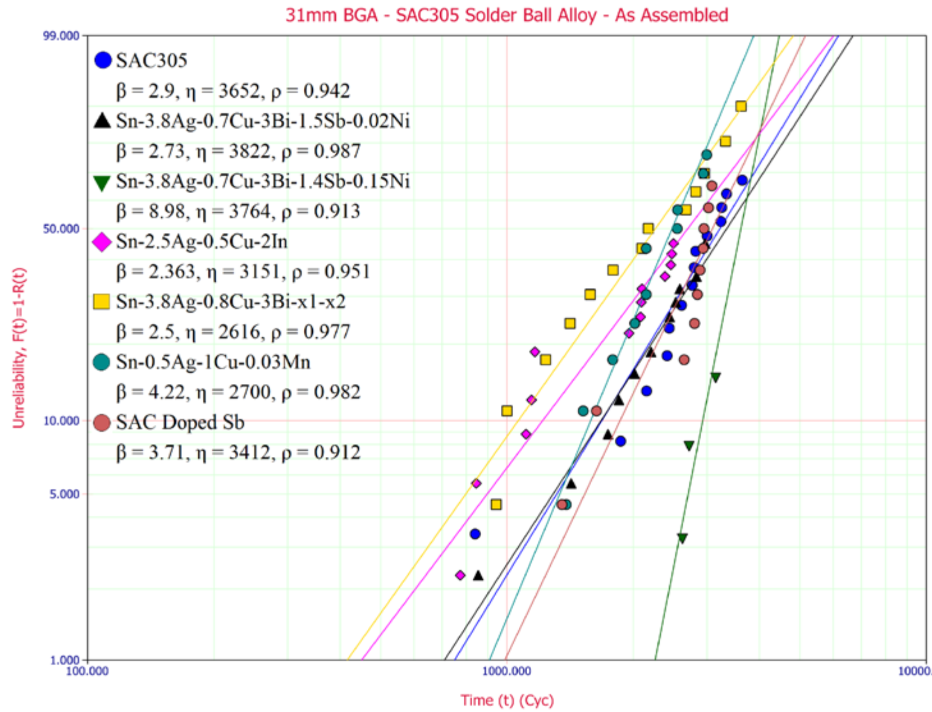


Figure 4.16 Weibull analysis for 31mm BGA with SAC305 solder ball alloy – As assembled

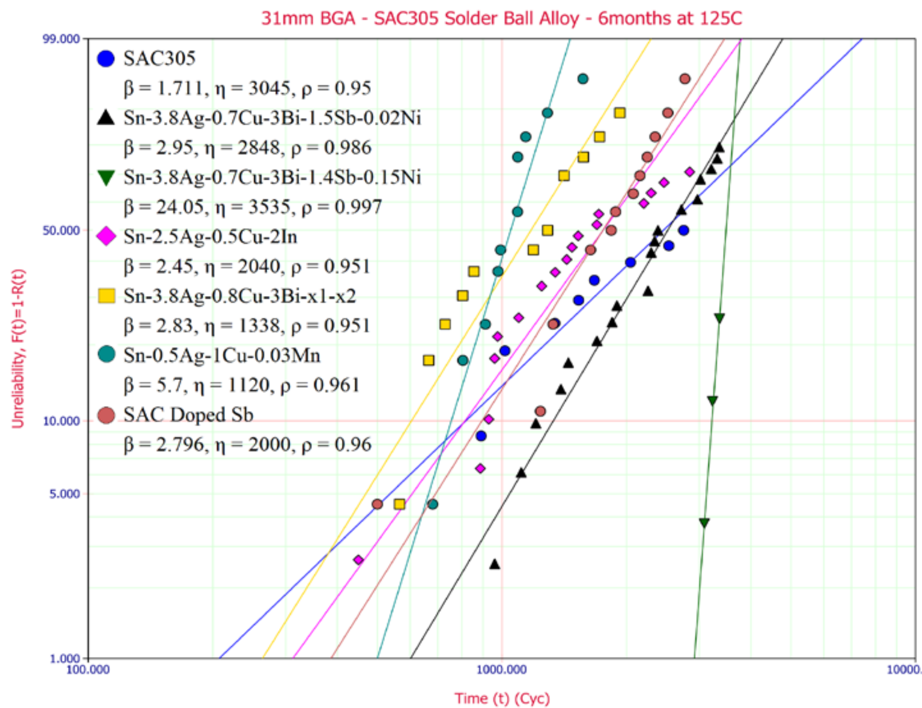


Figure 4.17 Weibull analysis for 31mm BGA with SAC305 solder ball alloy – 6 months at 125°C

The weibull graph for the solder pastes built using 31mm BGA package after aging and testing is shown in Figure 4.17. Only solder paste which outperformed was Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni which indicates increasing Ni content play a role in mitigating the aging and superior reliability.

Figure 4.18 shows failure data for the 31mm BGA package with various Pb-free solder pastes with Matched solder ball alloy after assembly (No aging) and thermal shock testing. It is shown that none of the solder pastes, when doped with same ball alloy, have proven to be better than SAC305 solder paste and solder ball alloy. After aging and testing shown in Figure 4.19 indicate a similar trend.

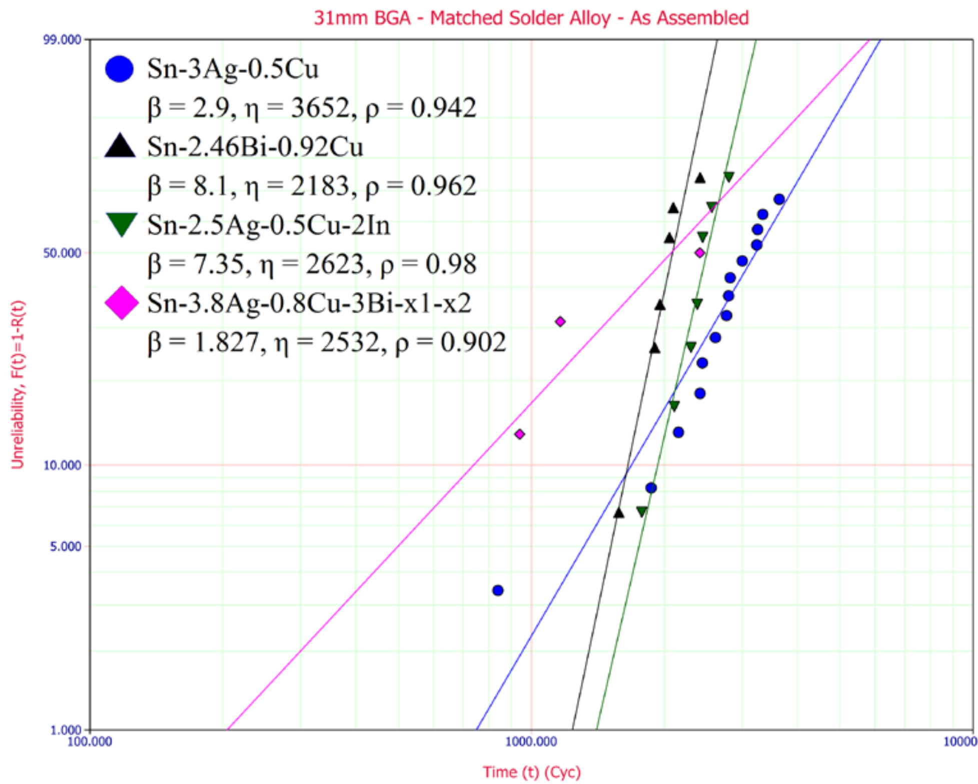


Figure 4.18 Weibull analysis for 31mm BGA with Matched solder ball alloy – As assembled

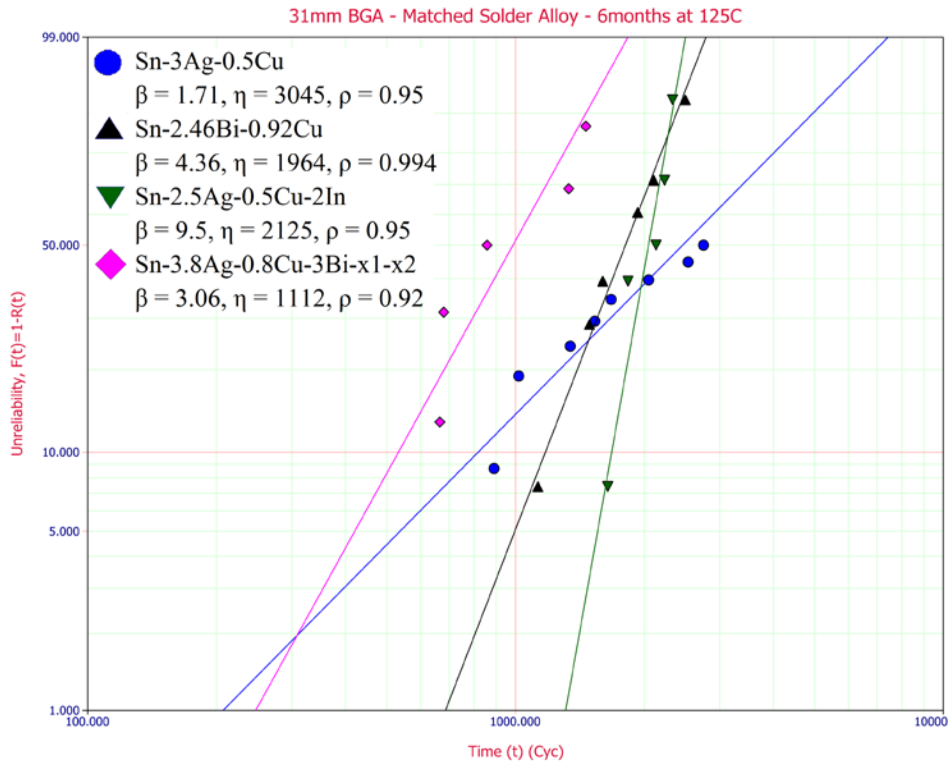
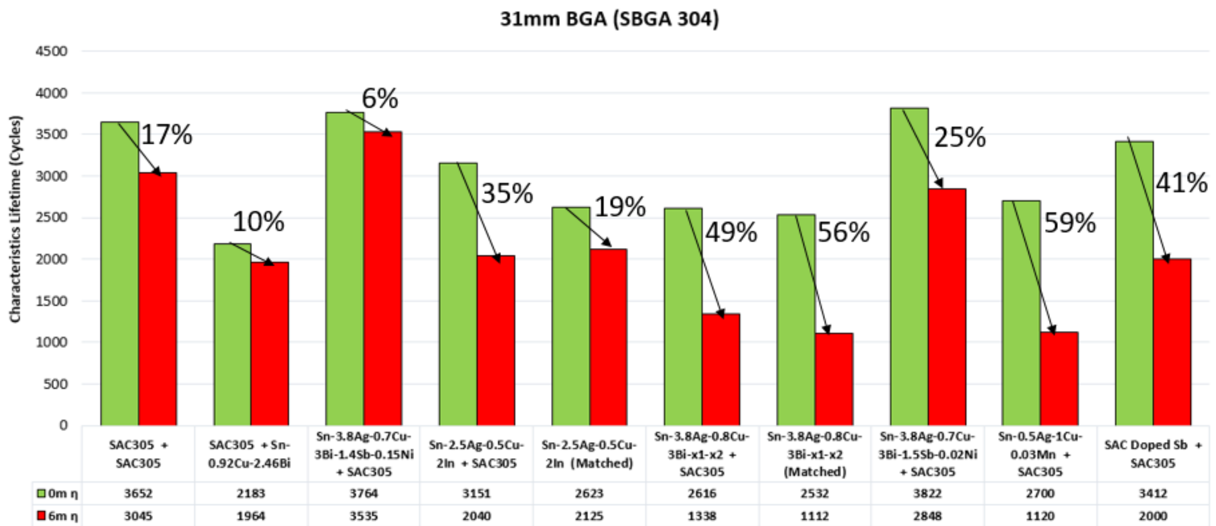


Figure 4.19 Weibull analysis for 31mm BGA with Matched solder ball alloy – 6 months at 125°C



	SAC305 + SAC305	SAC305 + Sn-0.92Cu-2.46Bi	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni + SAC305	Sn-2.5Ag-0.5Cu-2In + SAC305	Sn-2.5Ag-0.5Cu-2In (Matched)	Sn-3.8Ag-0.8Cu-3Bi-x1-x2 + SAC305	Sn-3.8Ag-0.8Cu-3Bi-x1-x2 (Matched)	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni + SAC305	Sn-0.5Ag-1Cu-0.03Mn + SAC305	SAC Doped Sb + SAC305
0m η	3652	2183	3764	3151	2623	2616	2532	3822	2700	3412
6m η	3045	1964	3535	2040	2125	1338	1112	2848	1120	2000

Figure 4.20 Characteristics lifetime summary of 31mm BGA packages

The characteristics lifetime summary of 31mm BGA is shown in Figure 4.20. The solder paste with least degradation and enhanced reliability compared with SAC305 solder paste was Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste with SAC305 ball alloy. Doping the solder ball alloy with the same material as the solder paste didn't look promising.

4.4.3 2512 resistors

The 2512 resistor is a passive component which consists of 100% Sn solder termination. Figure 4.21 shows the failure data for 2512 resistors with various lead-free solder pastes with Sn alloy after assembly (No aging) and thermal shock testing.

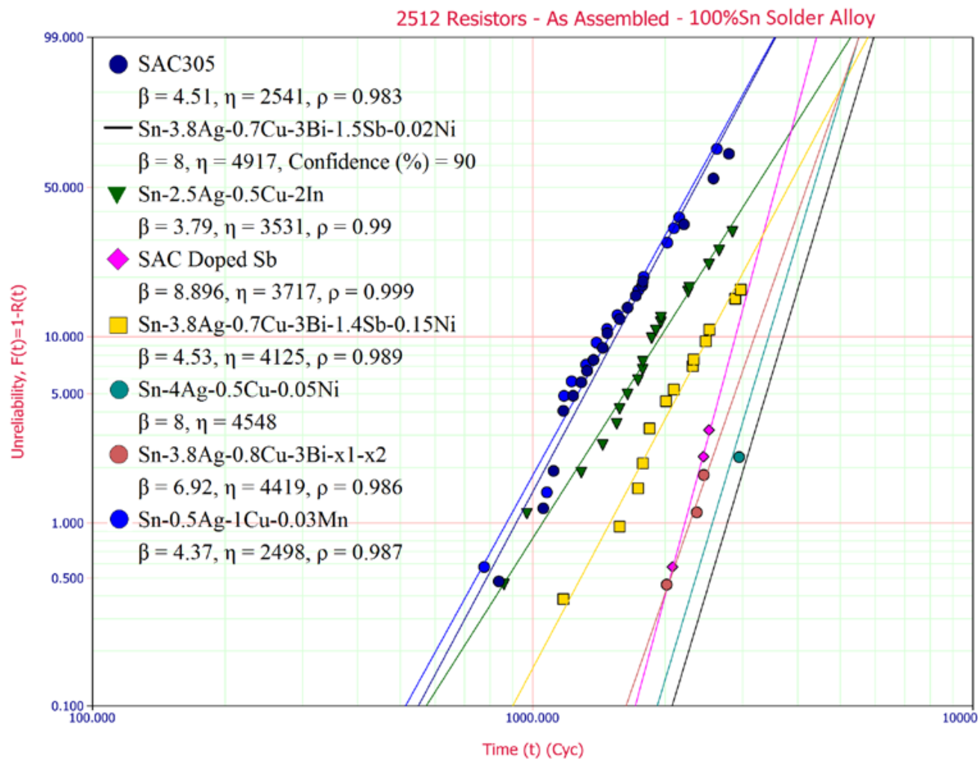


Figure 4.21 Weibull analysis for 2512 resistors with Sn solder alloy – As assembled

All the given solder pastes except Sn-0.5Ag-1Cu-0.03Mn solder paste did better than SAC305 solder paste. The Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste was ideal for 2512 resistors as it did not show any failures after 3000 cycles. The data for the given solder pastes with 2512 resistors after aging and thermal shock testing is shown in Figure 4.22. The Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste was comparatively better even after aging and testing.

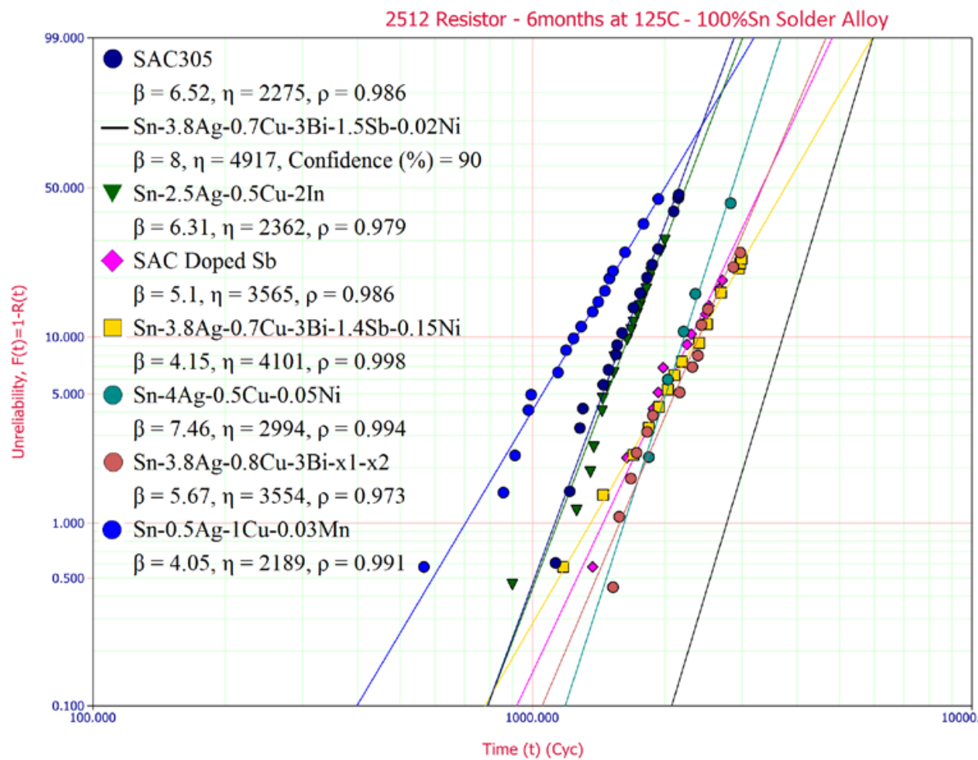


Figure 4.22 Weibull analysis for 2512 resistors with Sn solder alloy – 6 months at 125°C

The characteristics lifetime summary of 2512 resistors is shown in Figure 4.23. The solder paste with least degradation compared with SAC305 solder paste was Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and SAC doped Sb solder pastes. No failures were observed for Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste and its clear indication that it is suitable for 2512 resistor packages.

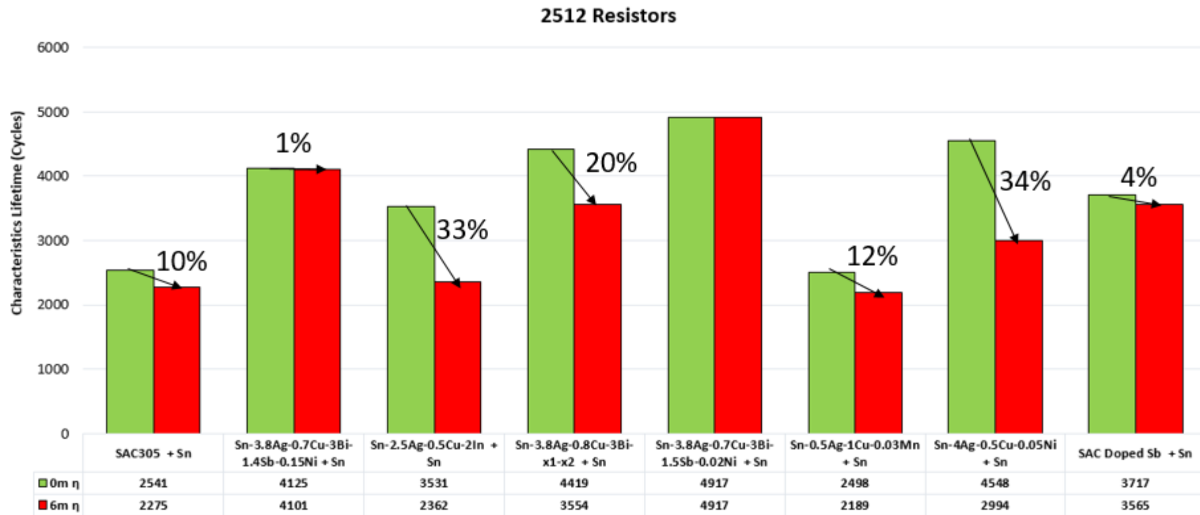


Figure 4.23 Characteristics lifetime summary of 2512 resistors

4.5 Failure Analysis for solder downselect test

The primary component used for failure analysis and IMC thickness measurement from solder downselect test was 15mm BGA package. Several 15mm BGA samples were cross-sectioned and polished for identification of the failure mechanism in each solder joint after assembly or after 6 months aging at 125°C. The cross-sectional SEM images were taken and no signs of incomplete mixing were seen in the solder joints. The thermomechanical fatigue failure was caused by the global mismatch in the coefficient of thermal expansion (CTE) between the PCB substrate vs the BGA package and local CTE mismatches between β-Sn grain matrices with different grain orientations during cyclic thermal loading [123], [124]. The common failure mechanism in the solder joint during thermal shock is recrystallization-assisted crack nucleation and propagation through the bulk solder interconnections [125].

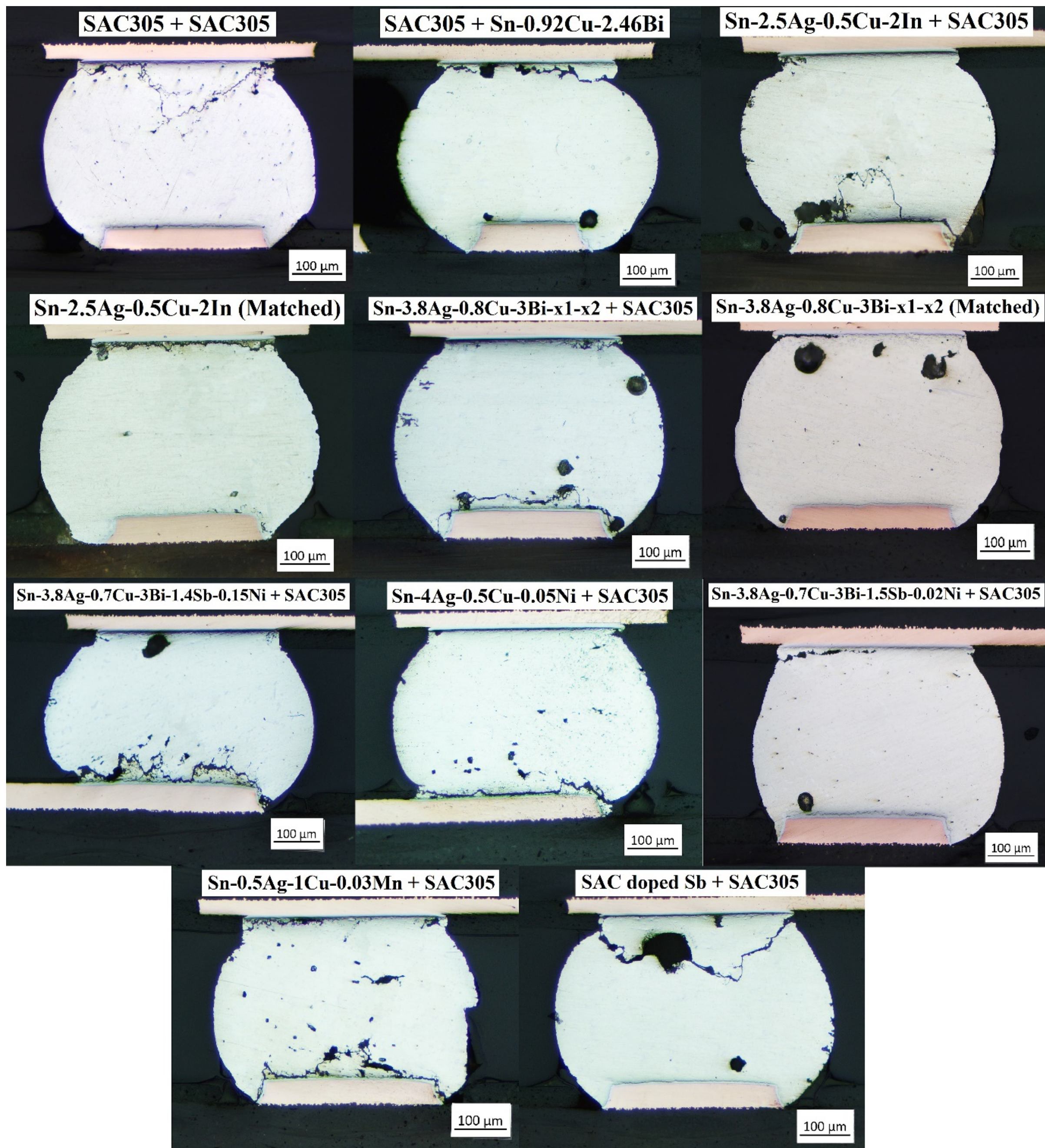


Figure 4.24 Optical microscopy images of Pb-free solder paste with Pb-free solder alloys

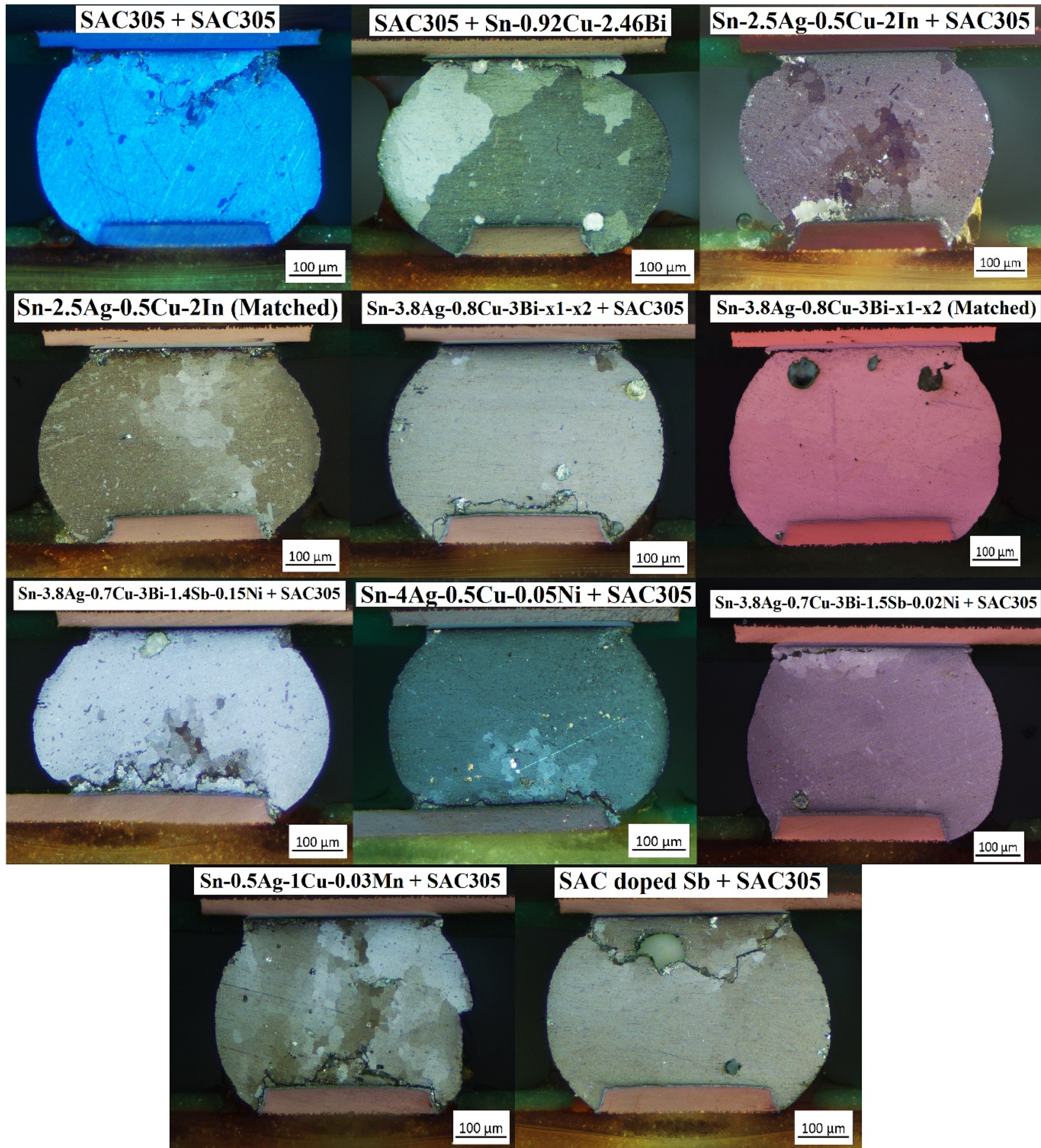


Figure 4.25 Cross-polarized optical microscopy images of Pb-free solder paste with Pb-free solder alloys

Figure 4.24 shows the failure mode in various Pb-free solder interconnects as-assembled or after 6 months of aging at 125°C and subsequently subjected to thermal shock. Figure 4.25 shows the cross-polarized optical microscopy images of solder joints shown in Figure 4.24. The

crack initiation was located in the corner of the solder joint, where the plastic deformation strain is the highest [42], [110]. Crack nucleation and propagation was also observed along the intermetallic layer at the board and package side. Most of these failures are initiated by recrystallization at high-stress positions of the solder ball, causing fatigue failures. Then, global recrystallization occurs near the BGA package where fatigue cracks start to propagate through the grain boundary network across the recrystallization region [123]. The cross-polarized optical images shown in Figure 4.25 indicate differences in recrystallization among the different Pb-free solder pastes. The crystal orientation distribution of the given solder pastes needs to be studied to understand the difference in recrystallization.

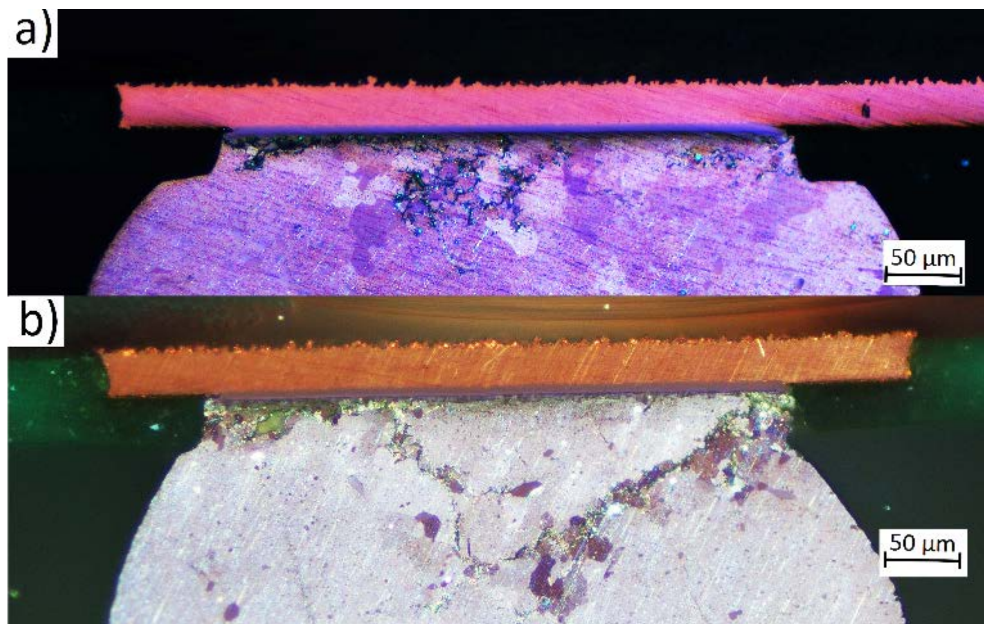


Figure 4.26 Cross-polarized image of Pb-free solder joints showing recrystallization phenomenon. a) Recrystallization initiation in representative aged SAC305 solder joints; b) Crack nucleation and growth

Figure 4.26 shows the recrystallization and crack propagation behavior in aged SAC305 ball alloys. The initiation of recrystallization typically occurs in the upper left portion of the solder

balls, shown in Figure 4.26a, while Figure 4.26b shows the crack progression via recrystallization-induced crack growth later in the test protocol.

Energy dispersive X-ray (EDX) spectroscopy was performed at the board side IMC, shown in Figure 4.27. Since Cu-OSP surface finish board was used in this test, the presence of Cu_6Sn_5 is visible at the board and bulk solder interface.

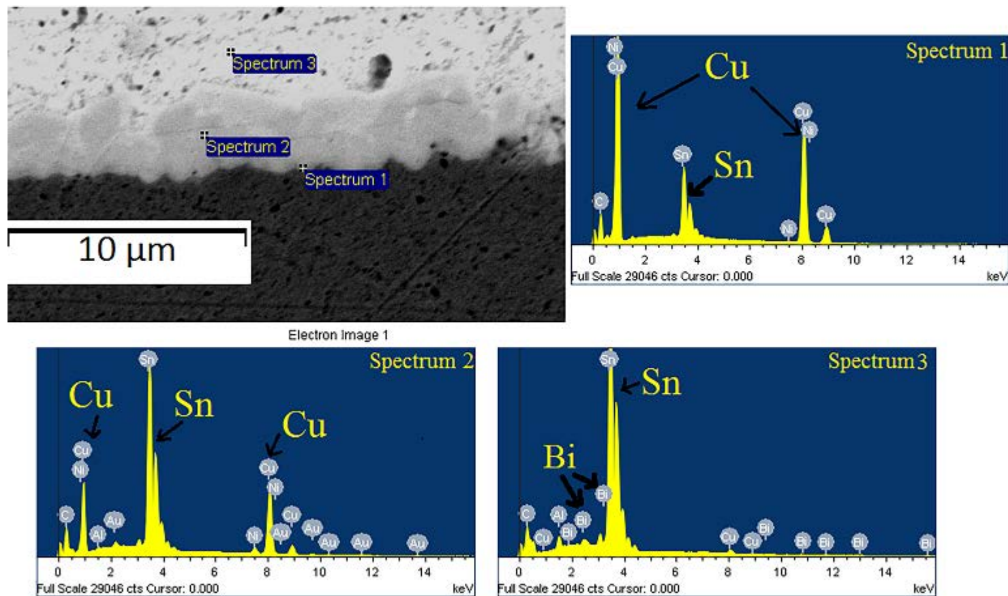


Figure 4.27 EDX analysis at the board side intermetallic layer in SAC305 paste with Sn-0.92Cu-2.46Bi ball alloy

After 6 months of aging, another layer of Cu-Sn intermetallic, Cu_3Sn is formed between the Cu_6Sn_5 layer and the Cu pad. This layer formation is commonly observed in aged SAC alloys on Cu based board finishes [125].

Since different doping elements have been used in this experiment, there is the possibility of additional elements in the Cu-Sn intermetallic compound on the board side. An investigation was done using elemental mapping in several solder joints. The elemental mapping did not show any significant presence of alloy dopants at the board interface IMC.

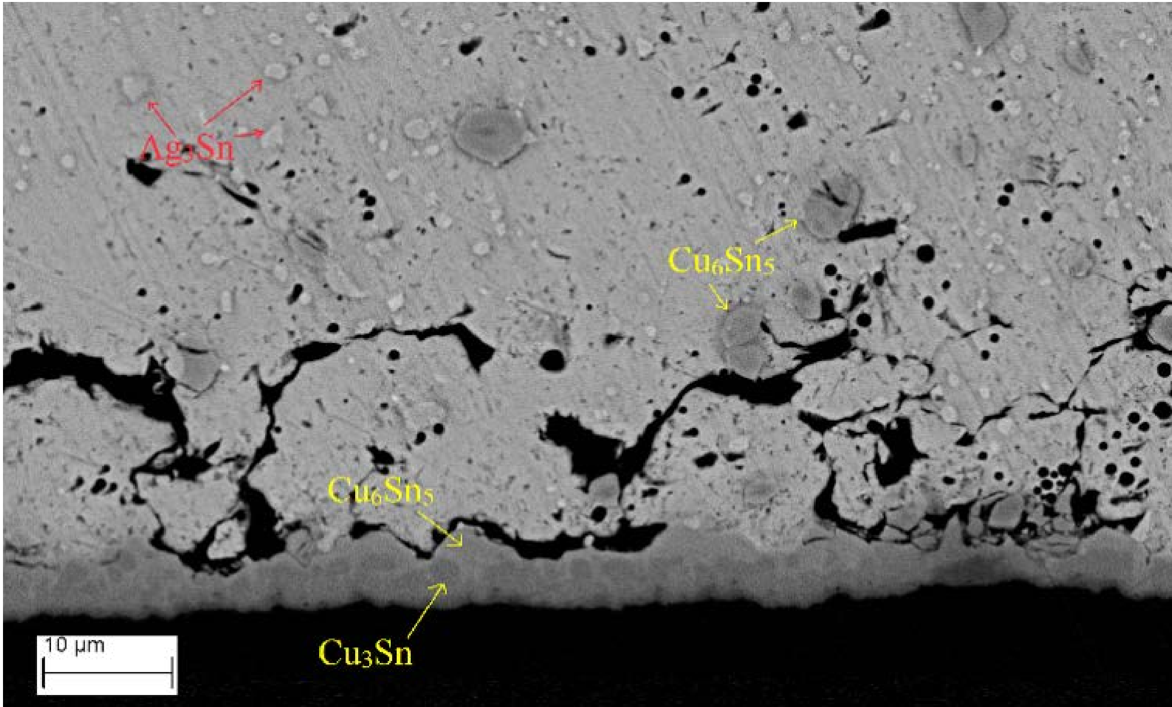


Figure 4.28 Ag_3Sn and Cu_6Sn_5 precipitates at the board side interface for Sn-0.5Ag-1Cu-0.03Mn paste with SAC305 ball alloy

Figure 4.28 examines the crack propagation at the board side of the joints. The Cu_6Sn_5 and Ag_3Sn precipitates act to alter the crack propagation pathway.

EDX analysis was also performed at the package side of the solder joints, shown in Figure 4.29. Due to the ENIG surface finish used on the package side, an expected $(Cu, Ni)_6Sn_5$ layer [125] is observed at the package side IMC. The Cu present at the package side IMC originates from the solder alloy itself (~ 0.5% by weight) and probably from a small amount of Cu diffusion through the alloy from the board Cu during the time at temperature aging process. While an area-averaged EDX was not taken to determine the solder joint composition after doping; the EDX spectra at various points within the alloy were compatible with stated alloy composition.

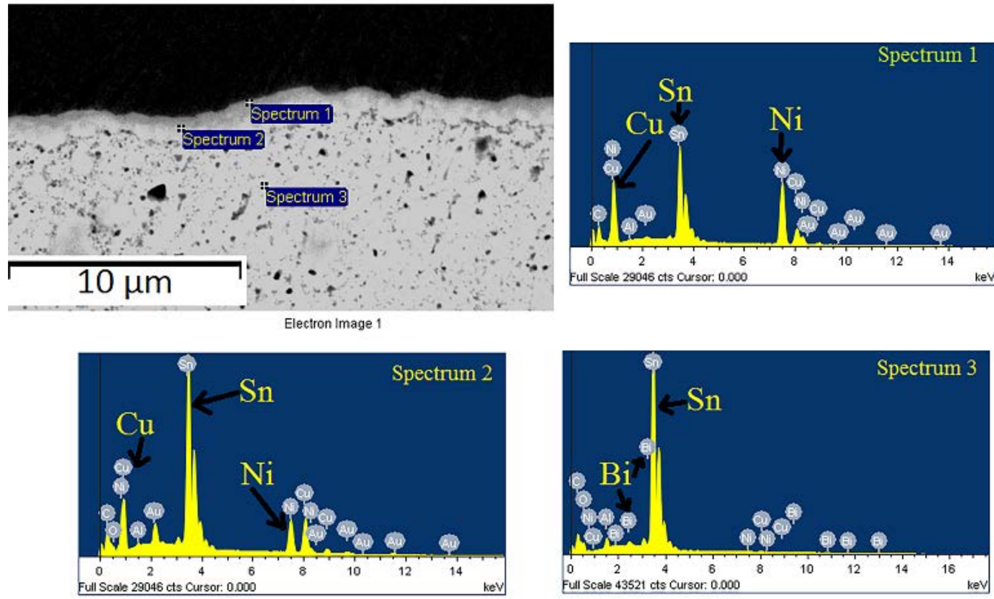


Figure 4.29 EDX analysis at the package side intermetallic for SAC305 paste with Sn-0.92Cu-2.46Bi ball alloy

Table 4.8 IMC Thickness at board side solder joints

Solder Paste	Solder Ball Alloy	Average IMC Thickness (µm)		Increase in IMC Thickness
		0m	6m	
SAC305	SAC305	5.67	7.11	25%
	Sn-0.92Cu-2.46Bi	2.82	3.78	34%
Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni	SAC305	4.77	6.42	35%
Sn-2.5Ag-0.5Cu-2In	SAC305	4.49	5.99	33%
	Matched	4.56	6.03	32%
Sn-3.8Ag-0.8Cu-3Bi-x1-x2	SAC305	4.33	7.46	72%
	Matched	5.5	6.67	21%
Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni	SAC305	4.72	6.1	29%
Sn-0.5Ag-1Cu-0.03Mn	SAC305	5.21	6.31	21%
Sn-4Ag-0.5Cu-0.05Ni	SAC305	4.34	5.33	23%
SAC Doped Sb	SAC305	4.31	5.99	39%

The average IMC thickness measurement of Cu-Sn intermetallic layer on the board side of the solder joint is shown in Table 4.8. The measurement was taken after thermal cycling for both as-assembled and 6 months aged samples. When comparing the baseline SAC305 paste with SAC305 ball alloy versus SAC305 paste with Sn-0.92Cu-2.46Bi ball alloy, the SAC305 paste with Sn-0.92Cu-2.46Bi ball alloy had a thinner IMC thickness due to the presence of Bi in the ball alloy. The impact of Bi in the SAC based solder pastes has effectively reduced the IMC thickness at the board, which is seen in Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni, Sn-3.8Ag-0.8Cu-3Bi-x1-x2, and Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder pastes.

Indium doped SAC paste and solder balls i.e. 95Sn-2.5Ag-0.5Cu-2In underperformed in terms of thermal shock performance compared with the baseline SAC305. The more indium is present in the SAC alloy, the greater the deterioration in microhardness after aging. The increase in average grain size of Sn-rich phase after aging is the cause of reduction in microhardness [117].

Another material which did not do well under thermal shock was the Sn-0.5Ag-1Cu-0.03Mn solder paste. On comparing the IMC thickness between Sn-0.5Ag-1Cu-0.03Mn and SAC305 paste, Sn-0.5Ag-1Cu-0.03Mn exhibits a thinner IMC thickness. Although Mn is known to reduce the thickness of the Cu_3Sn layer and the combined (Cu_3Sn + Cu_6Sn_5) intermetallic layer [103], it failed to outperform SAC305 solder paste. The IMC growth in SAC doped Sb was lower than SAC305 solder paste.

The average IMC thickness measurement of $(Cu, Ni)_6Sn_5$ at the component side interface is shown in Table 4.9. The presence of Ni reduces the rate of diffusion, resulting in a thinner IMC layer [105]–[107], [118]. But, at the board side, the diffusion of Cu-Sn IMC is higher compared with Cu-Ni-Sn IMC, which causes the IMC to be thicker at the board side compared to the package

side. The average increase in IMC thickness at the board side interface was 33% and 16% at the component side interface.

Table 4.9 IMC Thickness at component side solder joints

Solder Paste	Solder Ball Alloy	Average IMC Thickness (µm)		Increase in IMC Thickness
		0m	6m	
SAC305	SAC305	3.86	4.3	11%
	Sn-0.92Cu-2.46Bi	1.49	2.15	44%
Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni	SAC305	1.54	1.74	13%
Sn-2.5Ag-0.5Cu-2In	SAC305	3.42	3.51	3%
	Matched	2.74	2.87	5%
Sn-3.8Ag-0.8Cu-3Bi-x1-x2	SAC305	2.96	3.25	10%
	Matched	3.5	3.94	13%
Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni	SAC305	3.47	4.03	16%
Sn-0.5Ag-1Cu-0.03Mn	SAC305	3.06	4.02	31%
Sn-4Ag-0.5Cu-0.05Ni	SAC305	1.68	2.07	23%
SAC Doped Sb	SAC305	3.83	4.13	8%

4.6 Findings from downselect test

Doping antimony to SAC alloy has improved the lifetime of the solder joints compared with the baseline SAC305. Antimony has been found to enhance the mechanical properties of the solder joint [96] which were seen in Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni, Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, and SAC doped Sb. The addition of bismuth, antimony, and nickel have proved to be useful in enhancing the mechanical strength of the solder material in Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni pastes. A higher percentage of Ag also showed superior reliability due to an increasing number of Ag_3Sn precipitate in Sn-4Ag-0.5Cu-0.05Ni solder.

Intermetallic thickness measurements showed that solders with small weight percentages of the elements Bi, Ni, and Sb result in thinner IMC thicknesses than SAC305. The impact of bismuth in the SAC based solder pastes has effectively reduced the IMC thickness at the board, which is seen in Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder pastes. Nickel significantly mitigated the IMC growth in the package side interface because of its ability to inhibit diffusion.

The most promising candidates, when compared to SAC305 solder paste from the liquid to liquid thermal shock test which was measured by their superior reliability and reduced aging effects are

- Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni
- Sn-4Ag-0.5Cu-0.05Ni
- SAC doped with Sb

These materials were built for TC1-SJR Phase II (Thermal Cycling –Solder Joint Reliability) test using Megtron6 substrate, which will be covered in Chapter 5. The TC1-SJR Phase II test evaluates the effect of long term aging using the best solder materials chosen from Solder doping downselect test.

Chapter 5 Thermal Cycling – Solder Joint Reliability Phase II test

5.1 Accelerated Thermal Cycling Test

The test vehicle for Thermal Cycling – Solder Joint Reliability (TC-SJR) Phase II is similar to TC-SJR Phase I test [1], [81], [126]. It was built with a limited number of alternative solder materials and the overall test vehicle design from Phase I was being maintained for the Phase II testing. STI Electronics Inc. assembled the TC1-SJR Phase II test vehicles at their home location in Madison, Alabama. Board Assembly was done from October 20 to October 23, 2015.

5.2 Board Design and Assembly

5.2.1 Test Vehicle Design and Specifications

The TC1-SJR test vehicle was manufactured by TTM Technologies (Time-To-Market Interconnect Solutions), Chippewa Falls Division. Overall board dimensions are 254 x 173 mm, with a board thickness of 5.08 mm or 200 mil. For the Phase II build, only boards of the Megtron6 substrate material were used in the test matrix.

Boards were assembled single-sided, with components on only one side of the board. Two groups were assembled: in one group, components were placed on the 'Top' side of the board; in the second group, components were placed on the 'Bottom' side of the board. The top and bottom-side assembled boards are shown in Figure 5.1 and Figure 5.2, below. The TC1-SJR board has 6 copper layers and over 14,600 pins. Up to 19 components can be assembled on the top-side, while up to 39 components can be assembled on the bottom-side (counting each set of 5 daisy-chained resistors as one component).

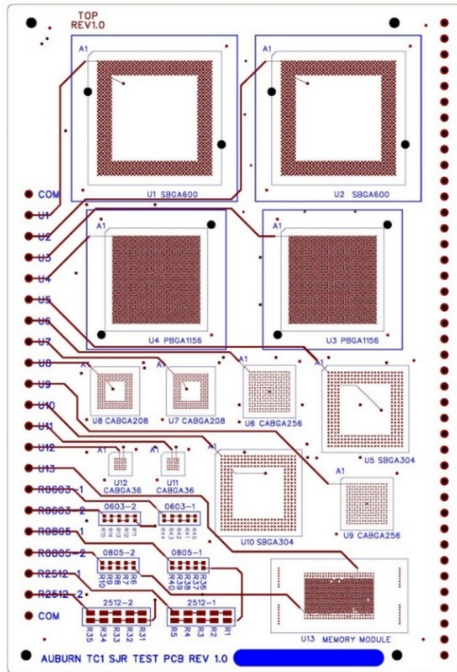
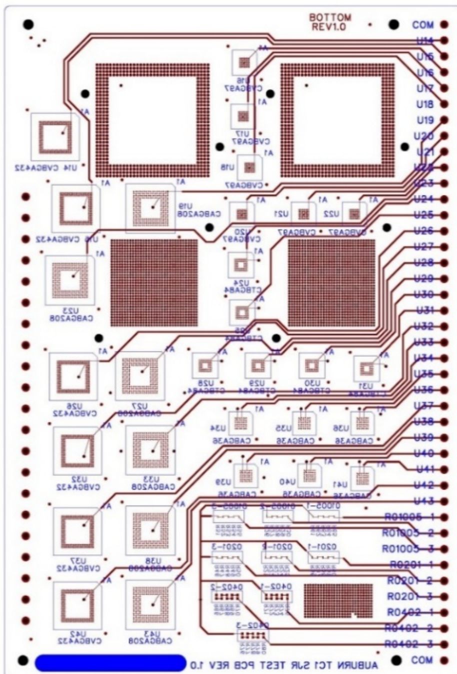


Figure 5.1 Phase II Test Vehicle: Top-side view



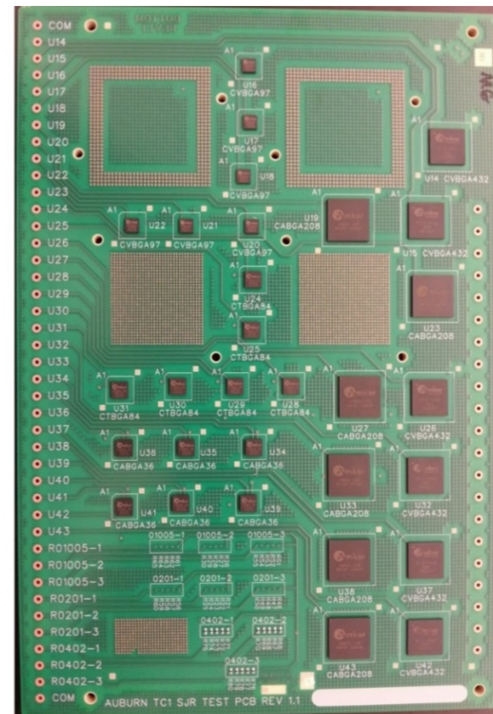


Figure 5.2 Phase II Test Vehicle: Bottom-side view

5.2.2 Test Plan

A total of 208 test boards were built, along with an additional 20 boards used solely for setup purposes during assembly. All test boards were Megtron6 substrate material; FR-406 boards were used for setup.

Four solder paste materials, shown in Table 5.1, were selected for incorporation in this test based on their performance in solder downselect test. Emphasis was given to materials that performed well in liquid shock testing. The materials were then randomly assigned a letter as a shorthand for tracking purposes.

Table 5.1 Material list

	Supplier	Composition
Material A	Inventec	Sn-4Ag-0.5Cu-0.05Ni
Material B	Henkel	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni (Type 3)
Material C	Alpha	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
Material D	Indium	SAC Doped Sb

Board group and test matrix are shown in Table 5.2. Four (4) isothermal aging times were included in the test plan: 0-month (No Aging), 6-month aging, 12-month aging, and 24-month aging. Boards were divided equally into these four aging groups. For each material, there were 9 top-side boards and 4 bottom-side boards for every aging group. There were 52 boards per material (36 top-side and 16 bottom-side), with 13 boards for each aging group.

Table 5.2 Phase II board groups and test matrix

	Material A-D				
CBA	Setup	0-m Aging	6-m Aging	12-m Aging	24-m Aging
Top	1	9	9	9	9
Bottom	1	4	4	4	4

Aging	Material	Top Side	Bottom Side	Total
No Aging	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
6 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
12 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
24 months	A	9	4	13
	B	9	4	13
	C	9	4	13
	D	9	4	13
		Total = 144	Total = 64	Total Boards = 208

5.2.3 Phase II Assembly Information

For the Phase II build, Megtron6 substrate material were used in the test matrix. Sufficient FR-406 material boards remained from the initial TC1-SJR build to serve as sacrificial setup boards during assembly only, reducing overall costs.

Boards were assembled single-sided, with components on only one side of the board. The top- and bottom-side components are shown in Table 5.3 and Table 5.4, below.

Table 5.3 Phase II Top-side components

Reference	Component	SAC Alloy	Pitch	Dimension	Place?
U1	SBGA 600	305	1.27mm	45mm	1
U2	SBGA 600	305	1.27mm	45mm	1
U3	PBGA 1156	305	1.00mm	35mm	1
U4	PBGA 1156	305	1.00mm	35mm	1
U5	SBGA 304	305	1.27mm	31mm	1
U6	CABGA 256	305	1.0mm	17mm	1
U7	CABGA 208	105	0.8mm	15mm	1
U8	CABGA 208	105	0.8mm	15mm	1
U9	CABGA 256	305	1.0mm	17mm	1
U10	SBGA 304	305	1.27mm	31mm	1
U11	CABGA 36	105	0.8mm	6mm	1
U12	CABGA 36	105	0.8mm	6mm	1
U13	Memory Module				0
R0603-1	0603 SMR	100%Sn			1
R0603-2	0603 SMR	100%Sn			1
R0805-1	0805 SMR	100%Sn			1
R0805-2	0805 SMR	100%Sn			1
R2512-1	2512 SMR	100%Sn			1
R2512-2	2512 SMR	100%Sn			1

Table 5.4 Phase II Bottom-side components

Reference	Component	SAC Alloy	Pitch	Dimension	Place?
U14	CVBGA 432	305	0.4mm	13mm	0
U15	CVBGA 432	305	0.4mm	13mm	1
U16	CVBGA 97	305	0.4mm	5mm	1
U17	CVBGA 97	305	0.4mm	5mm	1
U18	CVBGA 97	305	0.4mm	5mm	1
U19	CABGA 208	305	0.8mm	15 mm	1
U20	CVBGA 97	305	0.4mm	5mm	1
U21	CVBGA 97	305	0.4mm	5mm	1
U22	CVBGA 97	305	0.4mm	5mm	1
U23	CABGA 208	305	0.8mm	15 mm	1
U24	CTBGA 84	305	0.5mm	6mm	0
U25	CTBGA 84	305	0.5mm	6mm	1
U26	CVBGA 432	305	0.4mm	13mm	1
U27	CABGA 208	305	0.8mm	15 mm	1
U28	CTBGA 84	305	0.5mm	6mm	1
U29	CTBGA 84	305	0.5mm	6mm	1
U30	CTBGA 84	305	0.5mm	6mm	1
U31	CTBGA 84	305	0.5mm	6mm	1
U32	CVBGA 432	305	0.4mm	13mm	1
U33	CABGA 208	305	0.8mm	15 mm	1
U34	CABGA 36	305	0.8mm	6mm	1
U35	CABGA 36	305	0.8mm	6mm	1
U36	CABGA 36	305	0.8mm	6mm	1
U37	CVBGA 432	305	0.4mm	13mm	1
U38	CABGA 208	305	0.8mm	15 mm	1
U39	CABGA 36	305	0.8mm	6mm	1
U40	CABGA 36	305	0.8mm	6mm	1
U41	CABGA 36	305	0.8mm	6mm	1
U42	CVBGA 432	305	0.4mm	13mm	1
U43	CABGA 208	305	0.8mm	15 mm	1
R01005-1	01005 SMR	100%Sn			1
R01005-2	01005 SMR	100%Sn			1
R01005-3	01005 SMR	100%Sn			1
R0201-1	0201 SMR	100%Sn			1
R0201-2	0201 SMR	100%Sn			1
R0201-3	0201 SMR	100%Sn			1
R0402-1	0402 SMR	100%Sn			1
R0402-2	0402 SMR	100%Sn			1
R0402-3	0402 SMR	100%Sn			1

The screen printing machine used was a Speedline Technologies MPM Momentum (Figure 5.3). The stencil thickness used for the bottom-side assemblies was 3 mil and for the top-side assemblies, it was 5 mil.

Figure 5.3 Speedline Technologies MPM Momentum

Bottom-side boards were double printed to get adequate solder volume on the small pitch components. Print parameters were held constant for all assemblies.

Two pick and place machines were used for the Phase II assembly: the Juki KE-2080L (below, left) and Juki FX3 (below, right).

Figure 5.4 Juki KE-2080L (Left) and Juki FX3 (Right)

Solder reflow was done using a Heller 1913 MKIII reflow oven (shown below). Two different reflow profiles were used: one for the top-side boards and one for the bottom-side boards. The reflow profiles were designed to match as closely as possible the original TC1-SJR profile. It was selected based on solder paste manufacturer's recommendation while adjusting based on the realities of balancing time above liquidus and peak reflow temperature for a board of such high thermal mass.

Figure 5.5 Heller 1913 MKIII reflow oven

A test board was fitted with three thermocouples to get accurate thermal readings, as shown below in Figure 5.6. It was passed through the reflow oven while attached to a thermal readout and recording device (ECD Thermal Profiler). The oven temperature zones and pass through speed were adjusted iteratively until a feasible reflow profile was obtained. The reflow profiles shown in Figure 5.7 and Figure 5.8.

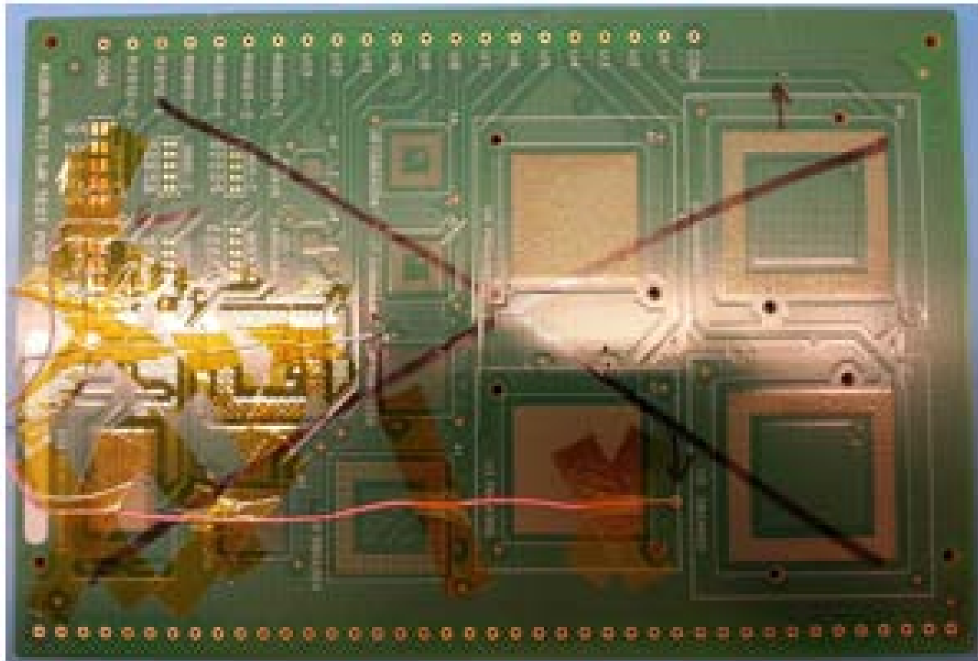


Figure 5.6 Test board

Setup boards were used for each material, top and bottom-side, in order to verify paste print and reflow before the production runs for that material. Print alignment, paste coverage, and solder volume were checked and corrective steps taken as necessary (i.e. minor alignment corrections) before running the corresponding set of test boards. Post-reflow wetting was also verified. The analysis was done using a Keyence optical microscope.

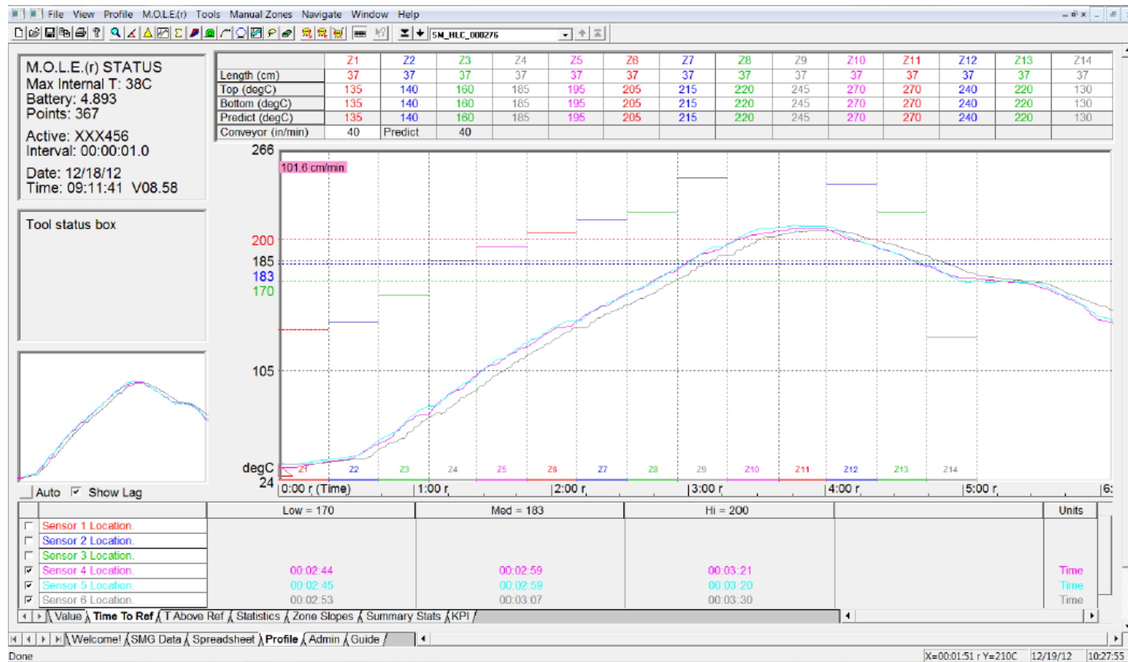


Figure 5.7 Phase II Top-side reflow profile

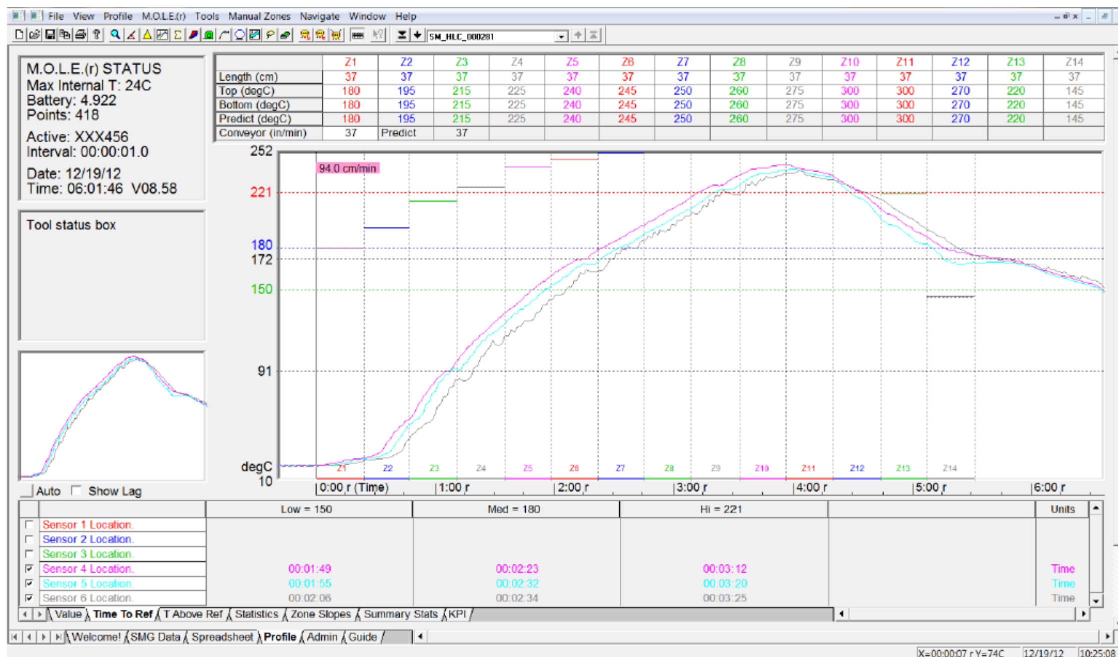


Figure 5.8 Phase II Bottom-side reflow profile

5.2.4 Quality Assurance

Quality assurance steps were taken. The resistance of each daisy-chained circuit component was checked by hand following reflow to eliminate them from inclusion in further testing. Boards were also optically inspected, and X-ray analysis was used to determine typical solder joint quality following reflow. In one instance, several components on one of the boards were sacrificed in a 'pry test' in order to assure the mechanical strength of the solder joints as reflowed.

Overall build quality was found to be very good. There were some solder paste specific manufacturability issues, which are documented below in the material-specific sections. Some problems were found with the SBGA 600 components, of which a few components had missing or misaligned solder spheres/balls. In combination with the failure of the AOI algorithm for this component on the Juki KE-2080L, this led to the failure of several assembled SBGA 600 components.

The Sn-4Ag-0.5Cu-0.05Ni solder paste presented manufacturing difficulties for use with the TC1-SJR board, and this paste was by far the most challenging material to work with from a manufacturability standpoint.

Paste volume was very low for the fine-pitch components on the bottom-side assemblies and was merely adequate on the larger pitch components. Fewer problems were seen with the top-side assemblies, which have 0.8mm pitch and above components. Figure 5.9 shows a representative paste print analysis for a 0.4mm pitch component (CVBGA97) using the Sn-4Ag-0.5Cu-0.05Ni solder paste.

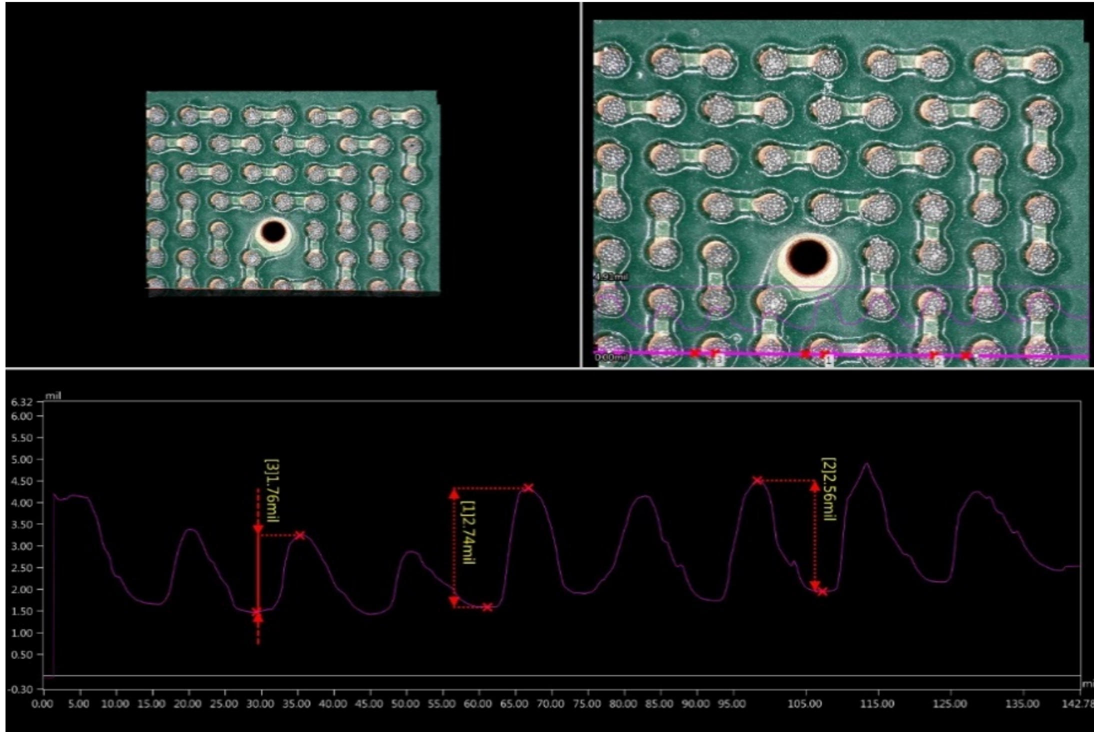


Figure 5.9 Representative paste print analysis: Sn-4Ag-0.5Cu-0.05Ni

As a result of the poor wetting seen, reflow was switched to nitrogen flow. The only test boards that were reflowed without nitrogen were the Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni bottom-side boards. All other test boards were subsequently reflowed under nitrogen atmosphere.

Even with nitrogen, solder bridging and tombstoning were observed with the 0603 SMRs, as well as one case of head-in-pillow with the SBGA600 component. Voiding was low using Sn-4Ag-0.5Cu-0.05Ni solder material. Figure 5.11 shows representative voiding images for this solder material.

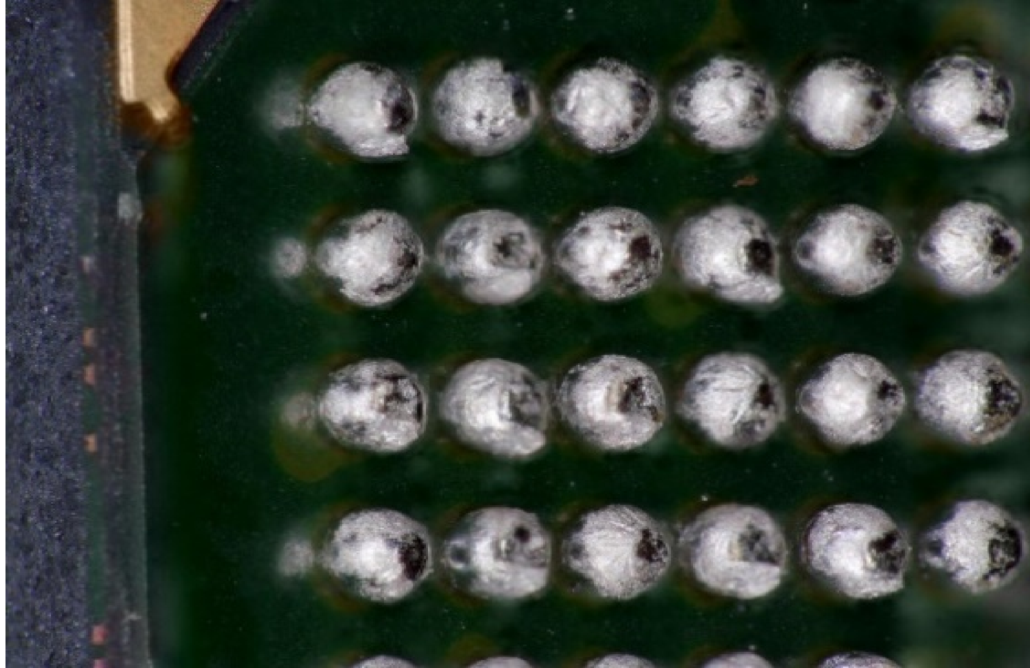


Figure 5.10 Post pry test: Sn-4Ag-0.5Cu-0.05Ni, Air-Reflowed

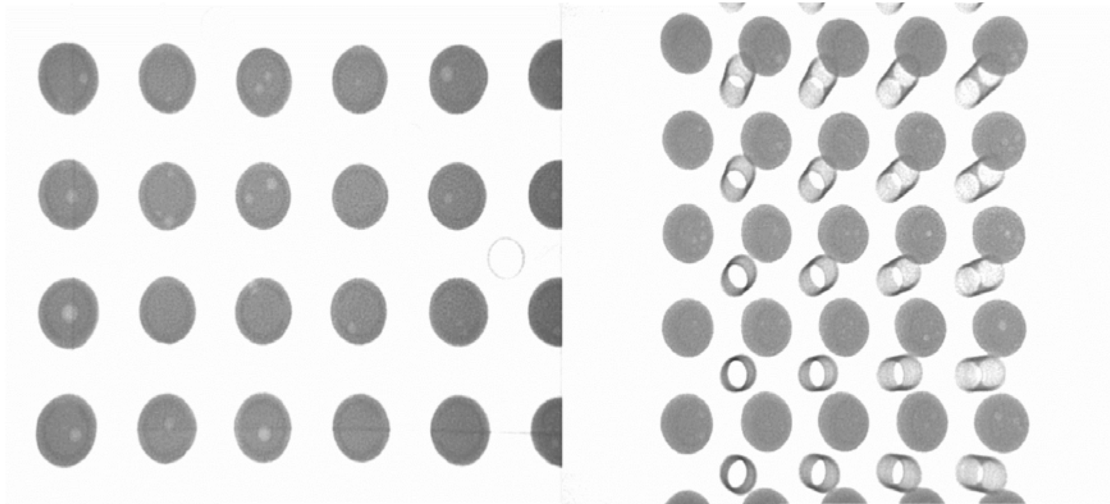


Figure 5.11 Representative voiding images: Sn-4Ag-0.5Cu-0.05Ni

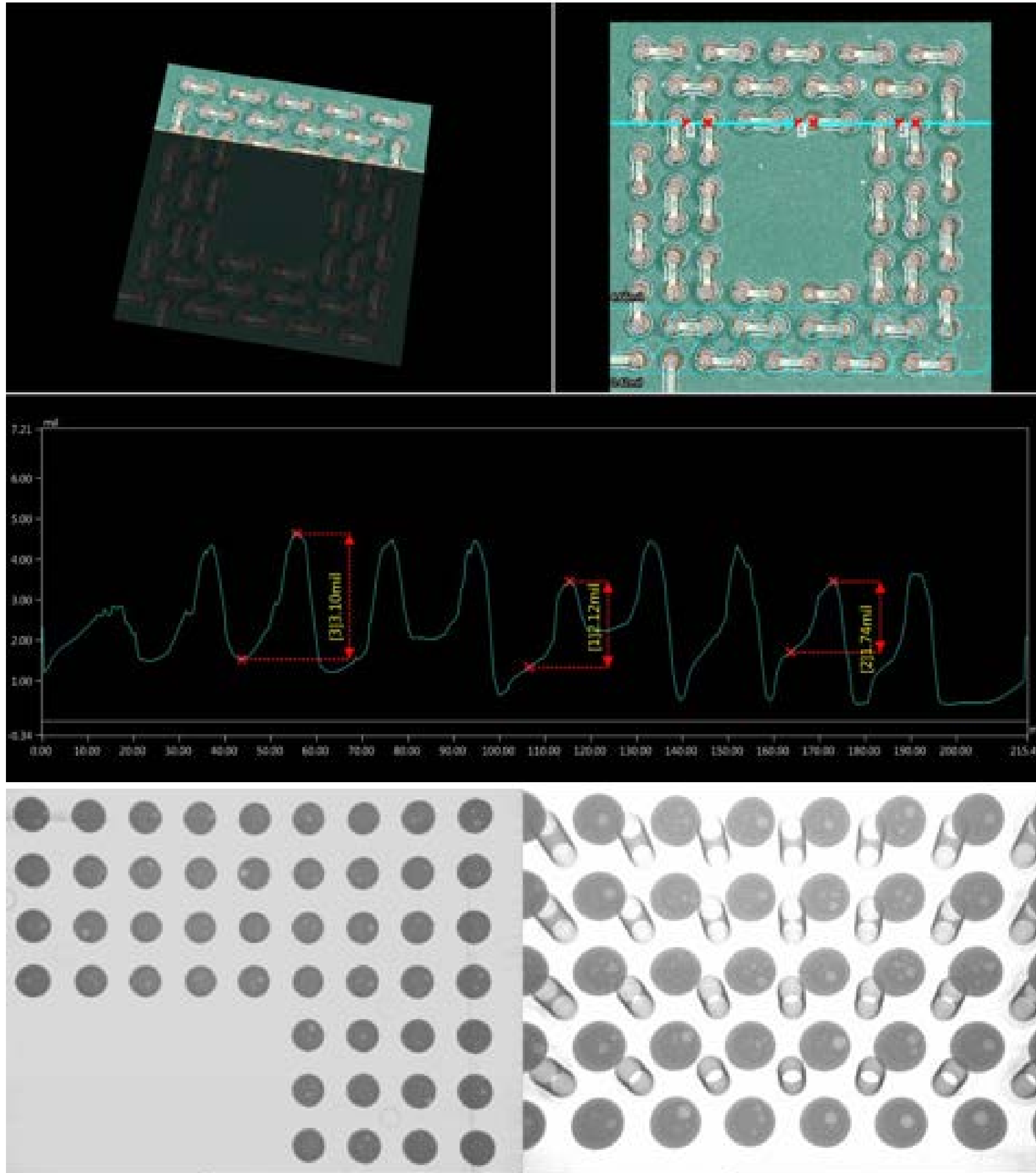


Figure 5.12 Representative paste print analysis and voiding images: Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni

The Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste did not present any significant manufacturability challenges. Voiding on the top-side assemblies was somewhat higher than other materials (up to an estimated 15-20% locally), as shown in Figure 5.12.

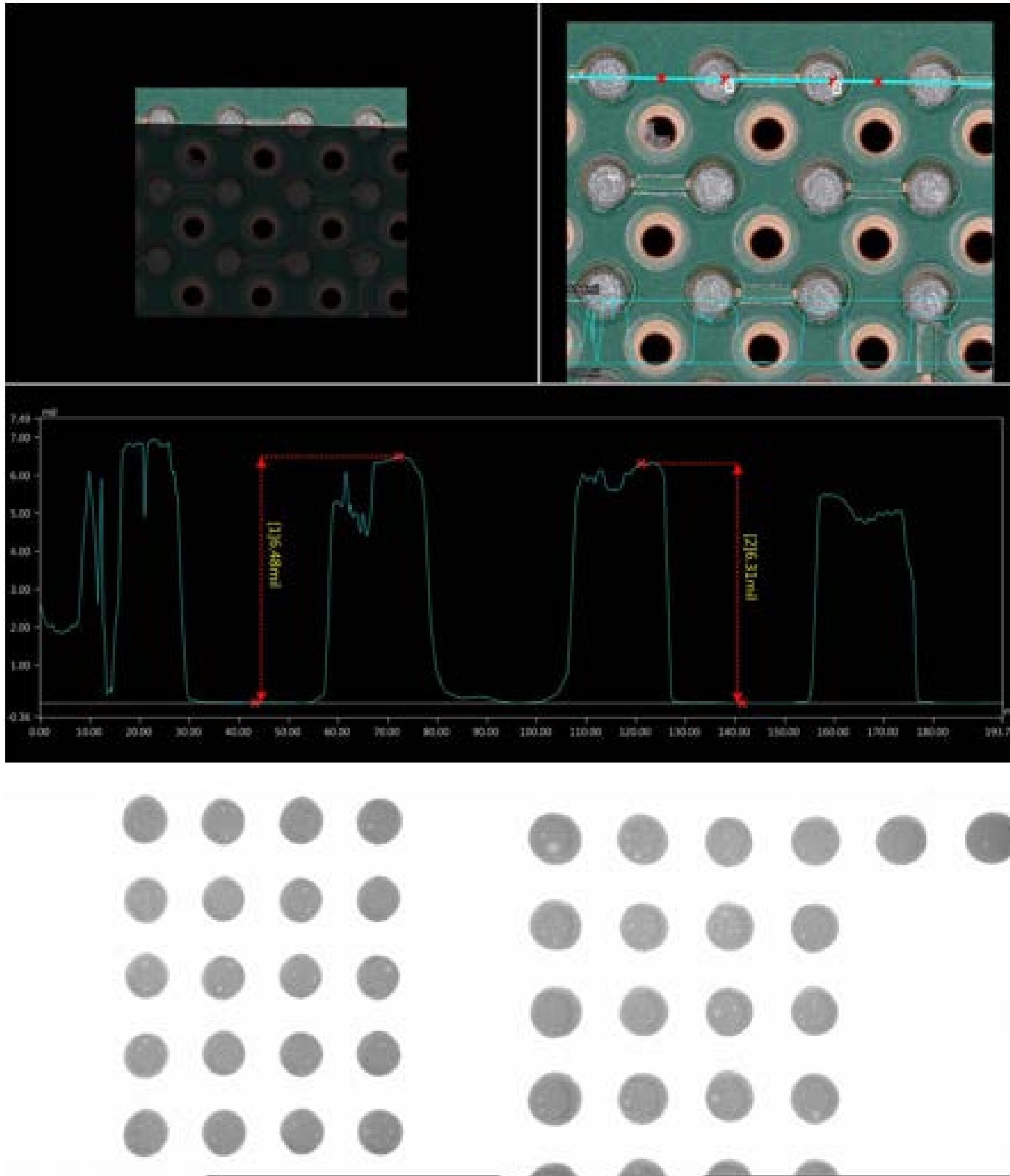


Figure 5.13 Representative paste print analysis: Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni (SBGA 600) and voiding images

The Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni did not present any significant manufacturability challenges. Figure 5.13 shows the Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste print and some voiding images.

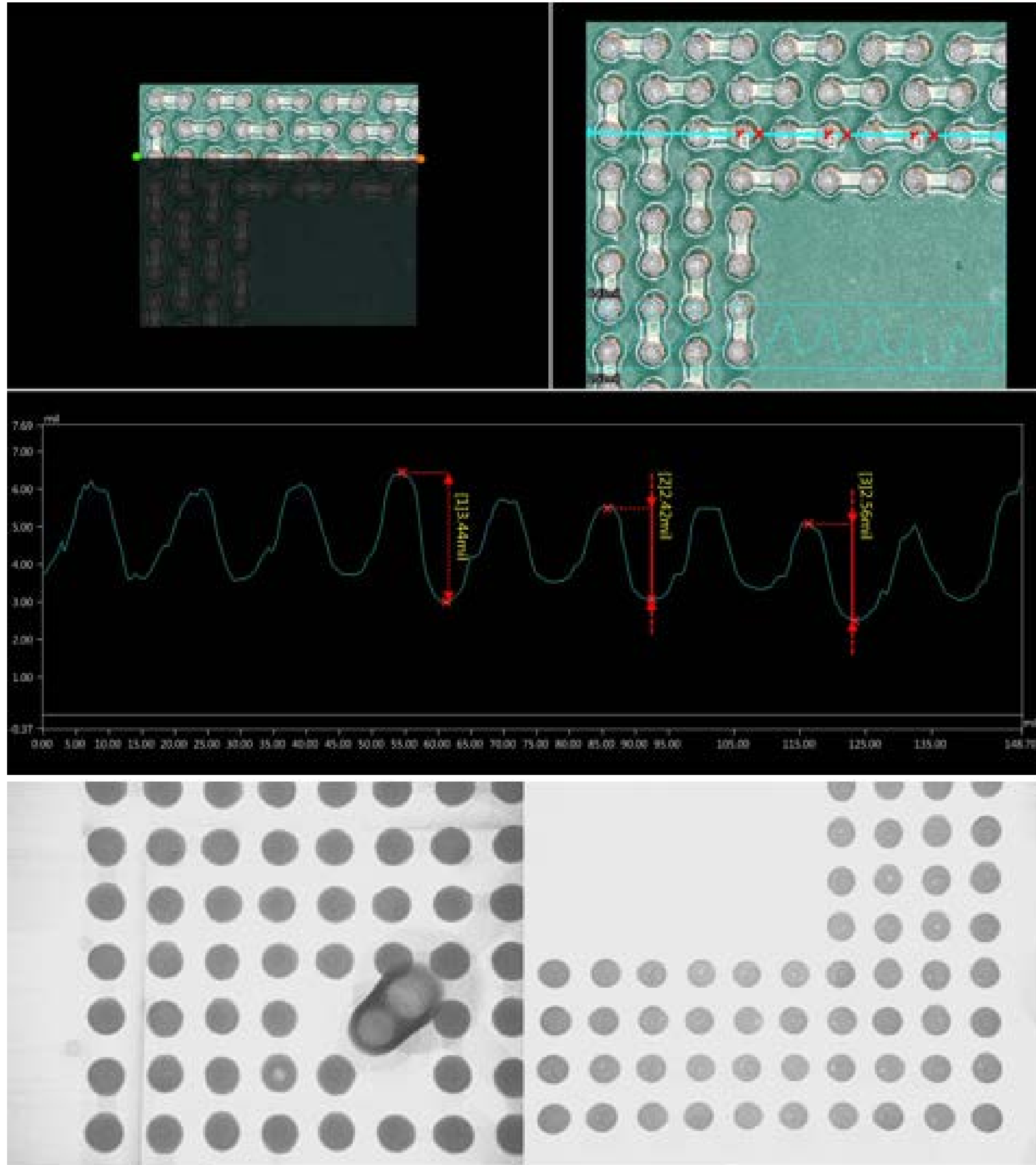


Figure 5.14 Representative paste print analysis: SAC doped Sb (Before stencil re-alignment) and voiding images

The SAC doped Sb material did not present any significant manufacturability challenges. Print volume was excellent for this material. Figure 5.14 shows the SAC doped Sb solder paste print and some representative voiding images.

5.3 Experimental Setup

As per the test plan, the assemblies were subjected to thermal cycling testing. A modified JEDEC JESD22-A104-B standard high and low-temperature test in a single zone environment chamber is used to assess the solder joint performance. The cycles have dwell temperatures of -40°C to +125°C and a ramp rate of 15°C per minute. This results in a thermal profile with a ramp time of 45 minutes, dwell time of 15 minutes and 120 minutes for an overall cycle. Each test group were subjected to 3000 thermal cycles. Figure 5.15 shows the thermal profile.

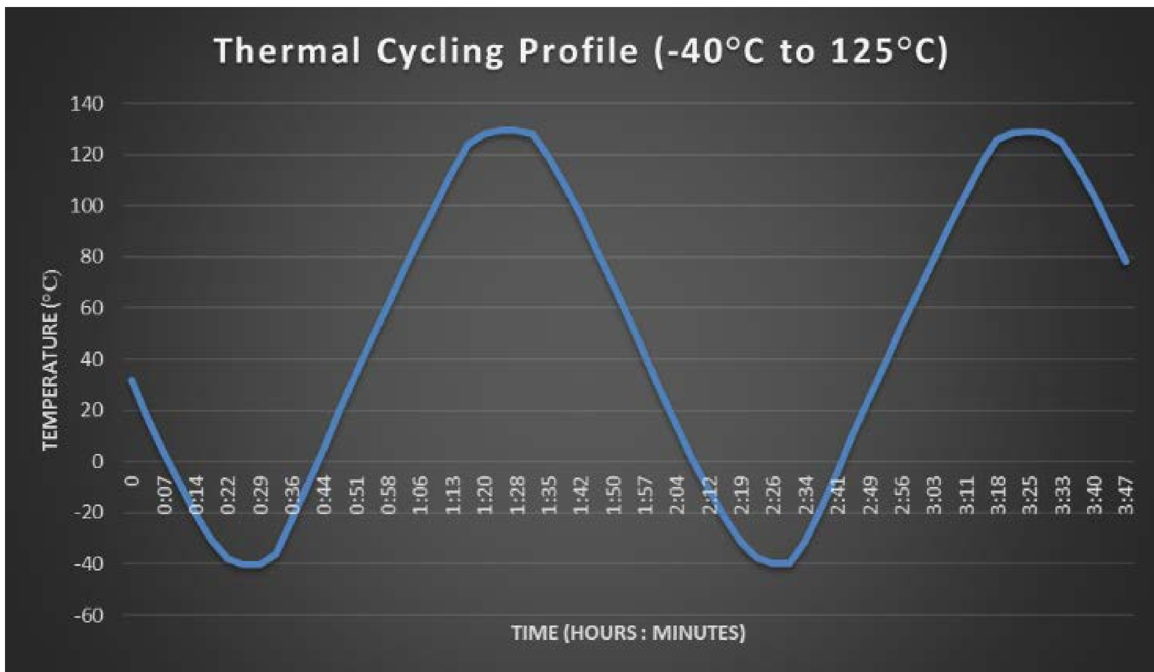


Figure 5.15 Thermal profile

Thermotron thermal cycling chambers, shown in Figure 5.16, were used for the thermal cycling testing.

Figure 5.16 Thermal cycling chambers

The electrical components used for this experiment were 'daisy-chained' for electrical continuity testing. The electrical resistance for each component was independently monitored. For thermal cycling testing, the test boards were mounted vertically on heat-resistant plastic dividers before placing them inside the chamber. Temperature resistance wires were hand soldered to each active data channel and ground channel for all the test boards. A LabVIEW based data acquisition system developed by Dr. Thomas Sanders of Auburn University [1] was used. A switch scanning system was coupled with a digital multimeter to monitor the resistance change of components continuously. This system is coupled with LabVIEW software to control and record the test results. IPC-9701 standard was used to define the solder joint failure when resistance increased (from baseline) by over 100 ohms for 5 sequential resistance measurements.

Figure 5.17 Full monitoring system (left) Keithley switching system and Digital Multimeter (DMM) from the front (right, top) and back (right, bottom). The DMM is sitting on top of the switching system [1]

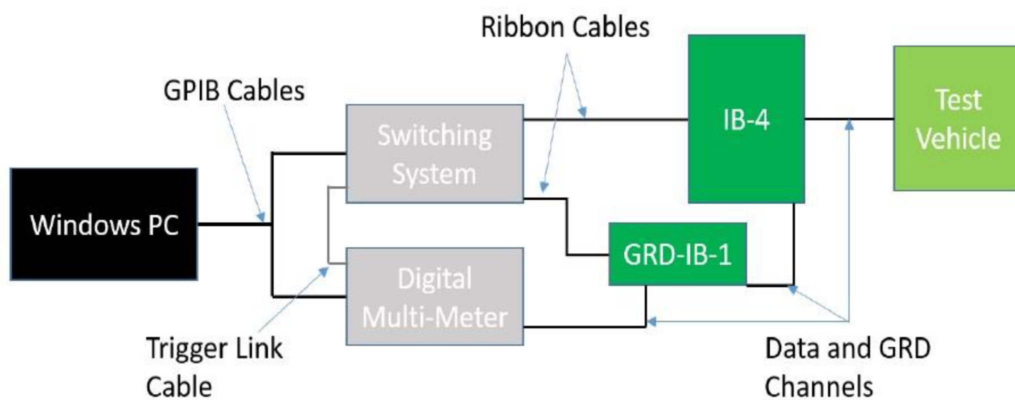


Figure 5.18 Schematic diagram of LabVIEW monitoring system [1]

Figure 5.17 and Figure 5.18 shows the data acquisition system and the schematic design of the monitoring system.

5.4 Result and Analysis from TC-SJR Phase II Test

The material properties of Megtron6 board substrate and BGA package used in thermal cycling are shown below in Table 5.5 and Table 5.6. The BGA package attributes are shown in Table 5.7. Material properties for these packages are similar to CABGA208 shown in Table 4.5 except the variability in package geometry.

Table 5.5 Material properties of Megtron6 substrate [122]

Material	Elastic Modulus (GPa)	CTE (ppm/°C) T (°C): 25 to 125
Megtron-6	16.9 (xy) @25℃	16.32 x 10^{-6} (xy)
	10.5 (xy) @125℃	
	13.8 (z) @25℃	16.37 x 10^{-6} (z)
	8.7 (z) @125℃	

Table 5.6 Material properties of BGA package [121]

Material	Elastic Modulus (GPa)	CTE (ppm/°C) T (°C): -40 to 125
Copper Pad	129	16.3 x 10^{-6}
Silicon Die	152	2.5 x 10^{-6}
Die Adhesive	6.77	83.6 x 10^{-6}
Solder Mask	3.1	30.0 x 10^{-6}
Mold	23.52	10.0 x 10^{-6}
BT Substrate	17.89 (xy)	12.42 x 10^{-6} (xy)
	7.85 (z)	57 x 10^{-6} (z)

Table 5.7 Package Attributes for 13mm, 15mm, and 17mm BGA

Attribute	CVBGA432	CABGA208	CABGA256
Package Size	13 x 13mm	15 x 15mm	17 x 17mm
Package Substrate	Bismaleimide Triazine (BT)	Bismaleimide Triazine (BT)	Bismaleimide Triazine (BT)
Package Type	Plastic	Plastic	Plastic
Package Thickness	0.66mm	1.0mm	1.0mm
Package Surface Finish	Electroless Nickel Immersion Gold (ENIG)	Electroless Nickel Immersion Gold (ENIG)	Electroless Nickel Immersion Gold (ENIG)
Die Size	9.96 x 9.96mm	12.7 x 12.7mm	14.9 x 14.9mm
Solder Ball Count	432	208	256
Solder Ball Pitch	0.4mm	0.8mm	1.0mm
Solder Ball Metallurgy	SAC305	SAC305	SAC305
Solder Ball Alignment	Perimeter	Perimeter	Perimeter
Solder Ball Diameter	0.28mm	0.36 ± 0.05mm	0.36 ± 0.05mm
Solder Ball Height	0.18mm	0.30 ± 0.05mm	0.30 ± 0.05mm

A 2-parameter weibull (β, η) was used to analyze the reliability data for the 13mm BGA's, 15mm BGA's, 17mm BGA's, and 2512 resistor packages. The BGA packages mentioned earlier had failed before 1000 cycles and were picked as the primary components to compare different solder pastes.

5.4.1 15mm BGA (CABGA 208)

The 15mm BGA component is found only on the bottom-side of the board with a stencil thickness of 3 mil. The pitch for 15mm BGA was 0.8 mm. The solder ball diameter and height was 0.53 mm and 0.3 mm.

Figure 5.19 shows the complete failure data for the Megtron6 substrate with various solder pastes and SAC305 solder alloy for no aged group. It is shown that Sn-4Ag-0.5Cu-0.05Ni outperformed other solder pastes after assembly and temperature cycling.

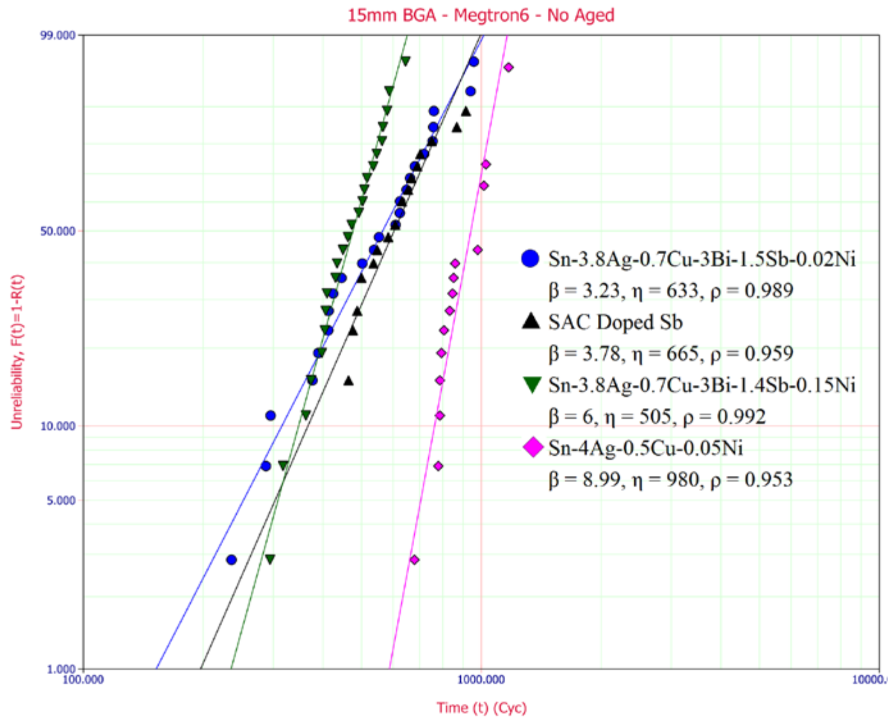


Figure 5.19 Weibull analysis for 15mm BGA with SAC305 solder ball alloy – As assembled

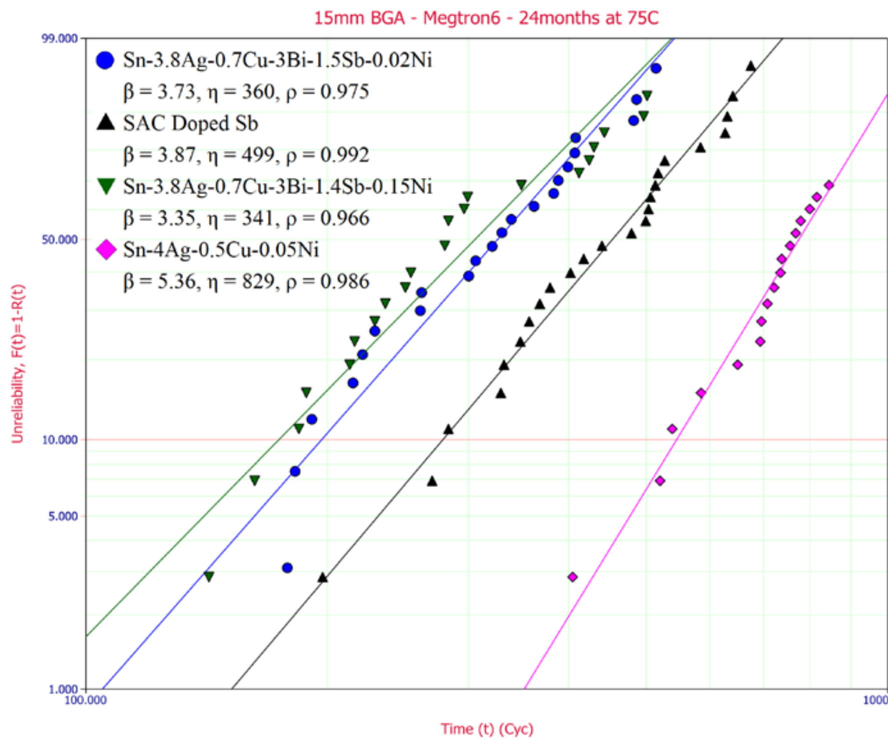


Figure 5.20 Weibull analysis for 15mm BGA with SAC305 solder ball alloy – 24 months at 75°C

Failure data for the given lead-free solder pastes with SAC305 solder alloy after 24 months of aging and thermal cycling is shown in Figure 5.20. The trend is similar even after 24 months of aging having Sn-4Ag-0.5Cu-0.05Ni as the best solder paste for 15mm BGA package.

Figure 5.21 shows the characteristic lifetime trend for the 15mm BGA package built using Megtron6 board substrate and solder materials tested from TC1-SJR Phase II test [127]–[129] and SAC305 solder paste from TC1-SJR Phase I test [1] across all aging subgroups. From the TC1-SJR Phase I test, SAC305 solder paste with SAC305 solder ball alloy has shown 38% degradation in lifetime after 24 months of aging and testing.

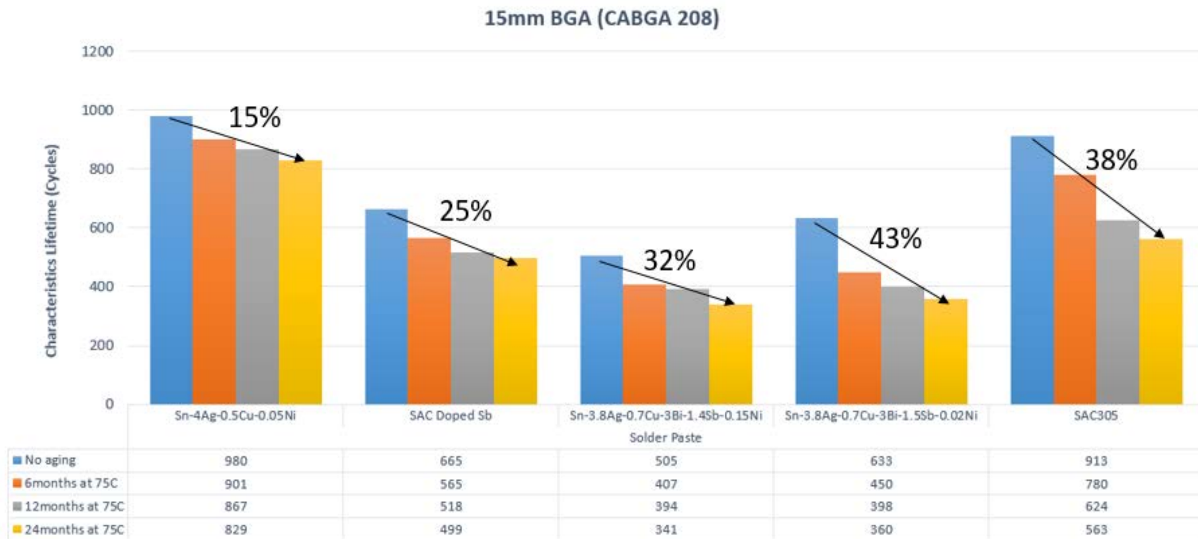


Figure 5.21 Characteristics Lifetime summary of 15mm BGA packages compared with SAC305 [1] from TC1-SJR Phase I test

Based on the summary, it is shown that Sn-4Ag-0.5Cu-0.05Ni is better than other pastes for all age groups having 15% deterioration after 24 months of aging. Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni showed highest deterioration of 43%, Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste showed 32% deterioration, and SAC doped Sb solder paste showed 25% degradation in lifetime.

5.4.2 17mm BGA (CABGA 256)

The 17mm BGA component is found only on the top-side of the board. The stencil thickness used for printing the solder paste for top-side assembly was 5 mil thickness. The pitch for 17mm BGA was 1.0 mm. The solder ball diameter and height was 0.52 mm and 0.31 mm. Figure 5.22 shows the complete failure data for the Megtron6 substrate with various solder pastes and SAC305 solder ball alloy for no aged group. Sn-4Ag-0.5Cu-0.05Ni solder paste showed superior reliability similar to 15mm BGA after assembly and temperature cycling.

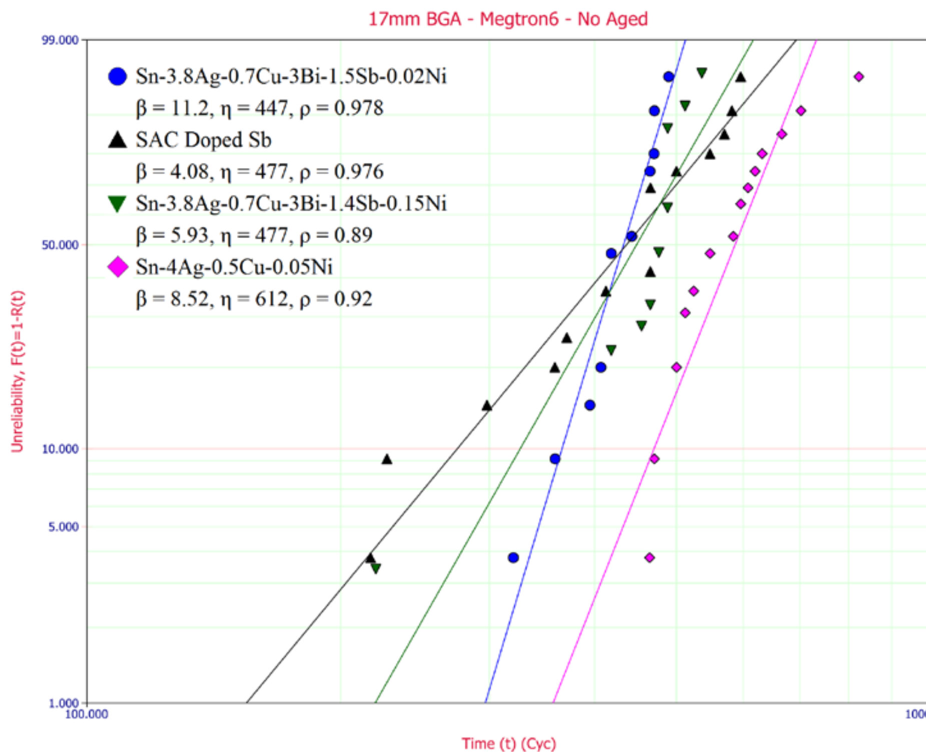


Figure 5.22 Weibull analysis for 17mm BGA with SAC305 solder ball alloy – As assembled

Failure data for the given lead-free solder pastes with SAC305 solder alloy after 24 months of aging and thermal cycling is shown in Figure 5.23. The trend is similar even after 24 months of aging, having Sn-4Ag-0.5Cu-0.05Ni as the best solder paste for 17mm BGA package.

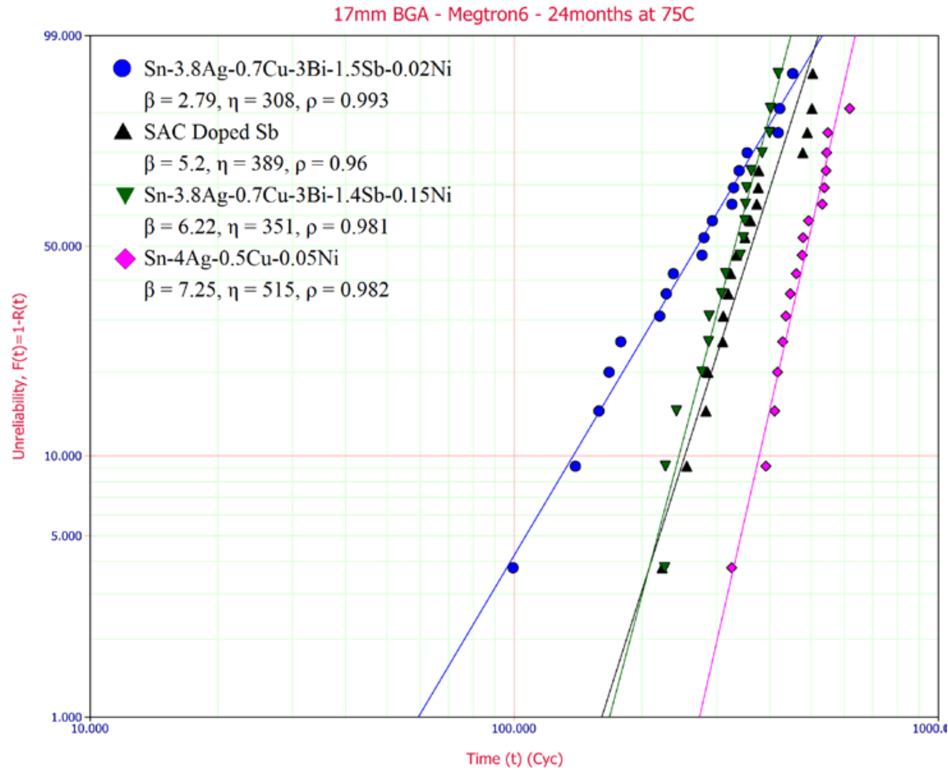
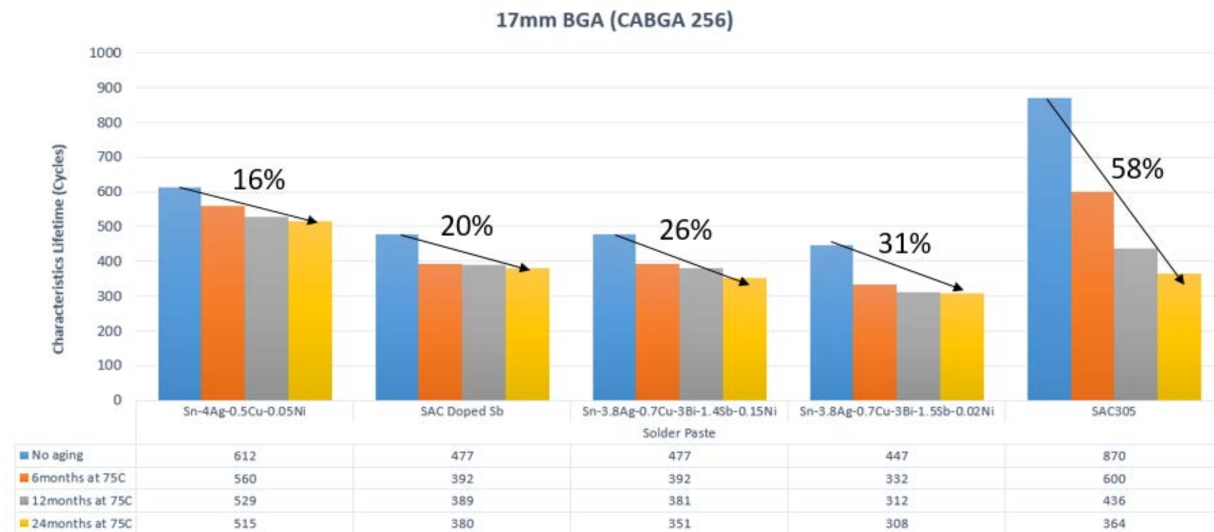


Figure 5.23 Weibull analysis for 17mm BGA with SAC305 solder ball alloy – 24 months at 75°C



	Sn-4Ag-0.5Cu-0.05Ni	SAC Doped Sb	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni	SAC305
No aging	612	477	477	447	870
6months at 75C	560	392	392	332	600
12months at 75C	529	389	381	312	436
24months at 75C	515	380	351	308	364

Figure 5.24 Characteristics lifetime summary of 17mm BGA packages compared with SAC305 [1] from Phase I test

Figure 5.24 shows the characteristic lifetime trend for the 17mm BGA package built using Megtron6 board substrate and solder materials tested from TC1-SJR Phase II test [127]–[129] and SAC305 solder paste from TC1-SJR Phase I test [1] across all aging subgroups. From the TC1-SJR Phase I test, SAC305 solder paste with SAC305 solder ball alloy has shown 58% degradation in lifetime after 24 months of aging and testing.

Based on the summary, it is shown that Sn-4Ag-0.5Cu-0.05Ni is better than other pastes for all age groups having 16% deterioration after 24 months of aging. Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni showed highest deterioration of 31%, Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste showed 26% deterioration, and SAC doped Sb solder paste showed 20% degradation in lifetime.

5.4.3 13mm BGA (CVBGA 432)

The 13mm BGA component is found only on the bottom-side of the board with a stencil thickness of 3 mil. The pitch for 13mm BGA was 0.4 mm. The solder ball diameter and height was 0.28 mm and 0.18 mm.

Figure 5.25 shows the complete failure data for the Megtron6 substrate with various solder pastes and SAC305 solder alloy for no aged group. It is shown that SAC doped Sb performed better than other solder pastes after assembly and temperature cycling. This trend is different from 15mm and 17mm BGA packages.

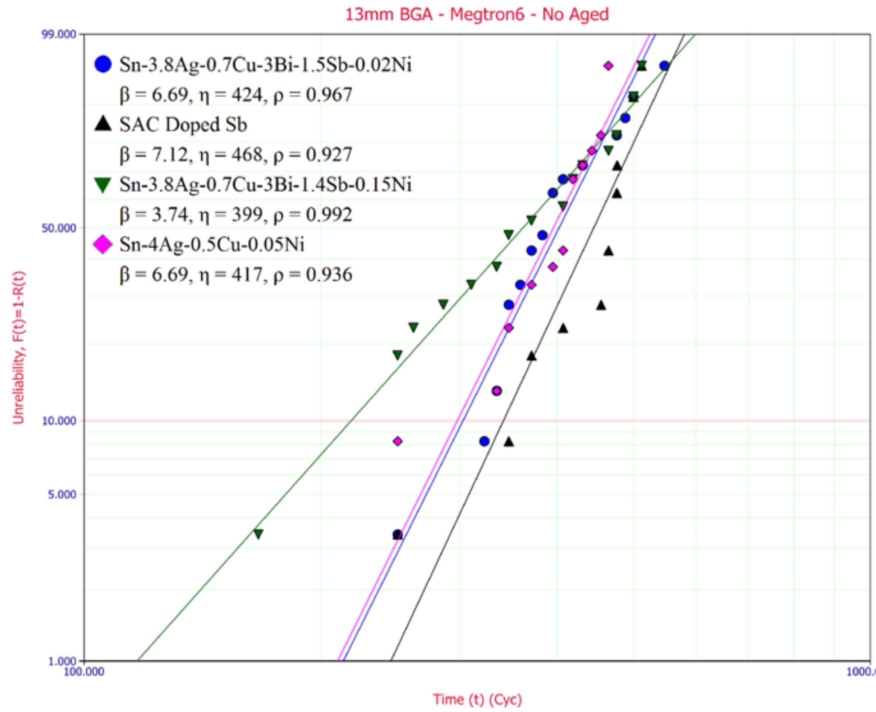


Figure 5.25 Weibull analysis for 13mm BGA with SAC305 solder ball alloy – As assembled

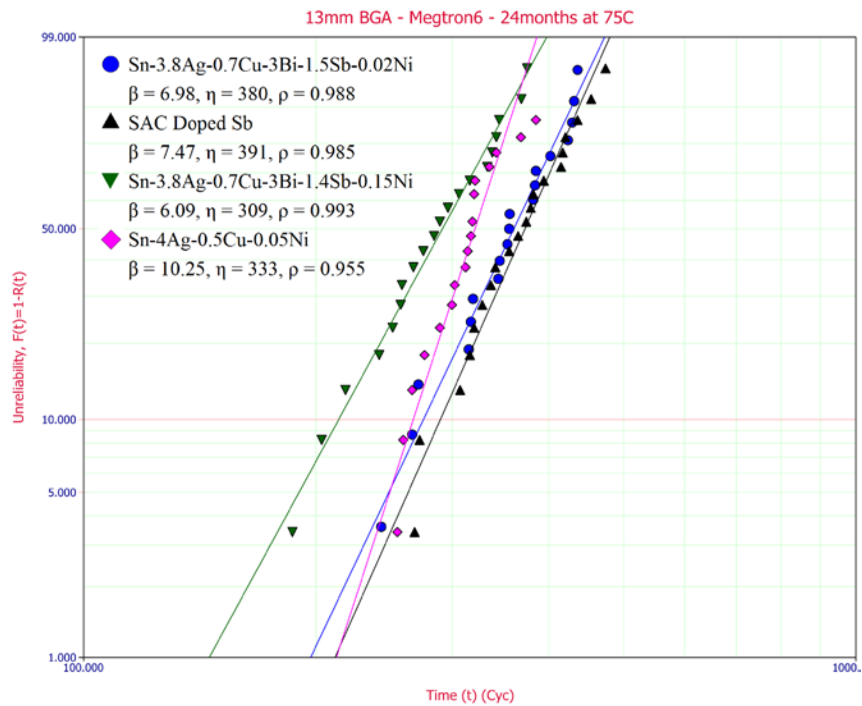


Figure 5.26 Weibull analysis for 13mm BGA with SAC305 solder ball alloy – 24 months at 75°C

Failure data for the given lead-free solder pastes with SAC305 solder alloy after 24 months of aging and thermal cycling is shown in Figure 5.26. The trend is similar even after 24 months of aging having SAC doped Sb as the best solder paste for 13mm BGA package.

Figure 5.27 shows the characteristic lifetime trend for 13mm BGA package built using Megtron6 board substrate and solder materials tested from TC1-SJR Phase II test [127]–[129] and SAC305 solder paste from TC1-SJR Phase I test [1] across all aging subgroups. From the TC1-SJR Phase I test, SAC305 solder paste with SAC305 solder ball alloy has shown 22% degradation in lifetime after 24 months of aging and testing.

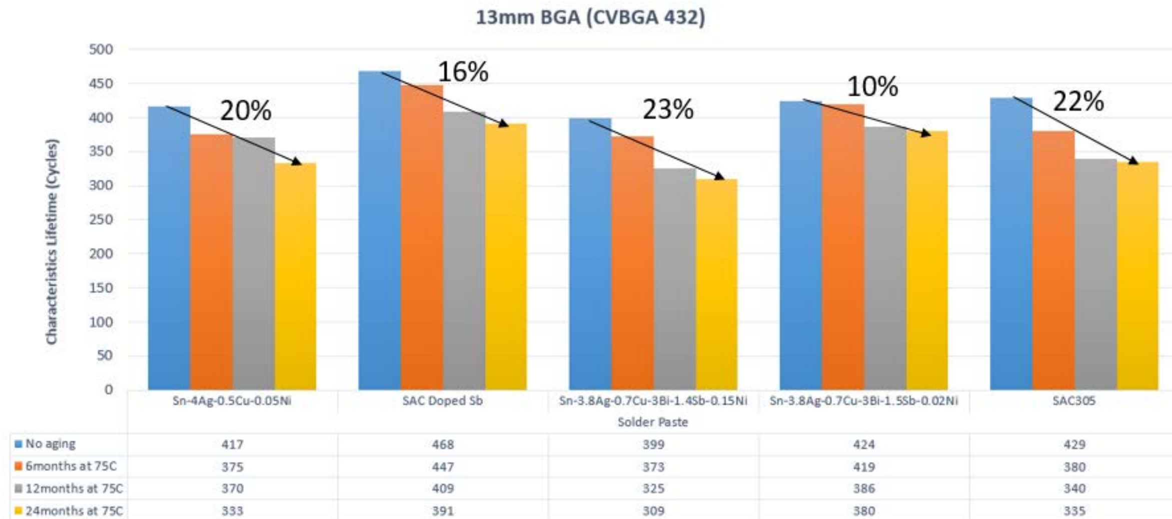


Figure 5.27 Characteristics lifetime summary of 13mm BGA packages compared with SAC305 [1] from Phase I test

Based on the summary, it is shown that SAC doped Sb is better than other pastes for all age groups having 16% deterioration after 24 months of aging. Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni showed lowest deterioration of 10%, Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste showed 23% deterioration and Sn-4Ag-0.5Cu-0.05Ni solder paste showed 20% degradation in lifetime.

5.4.4 2512 Resistors

The 2512 Resistor is a passive component which consists of 100% Sn and it is found in all top-side boards with a footprint of 0.025" x 0.12".

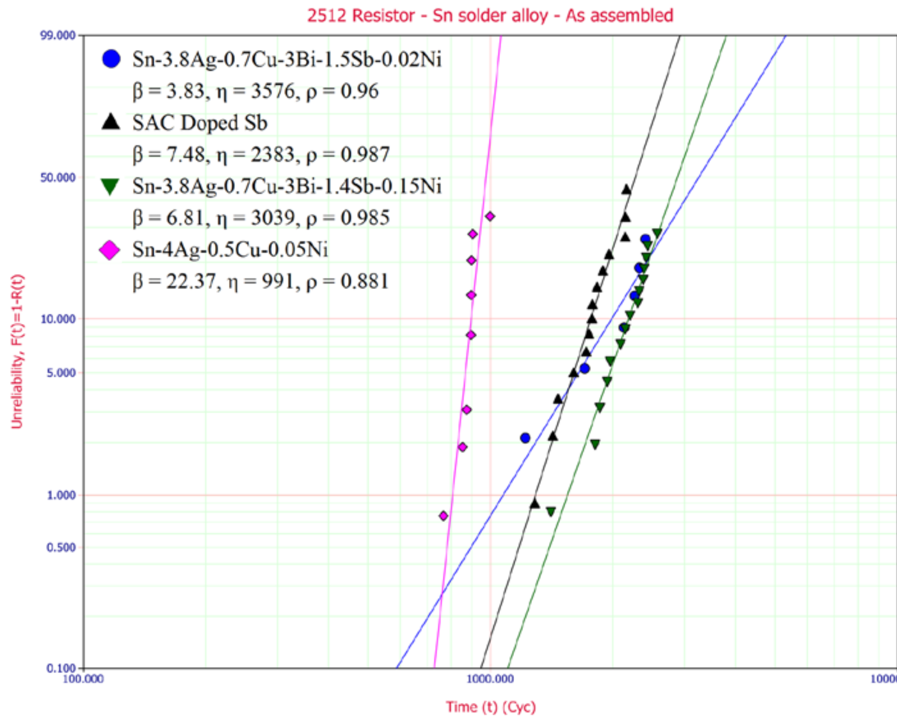


Figure 5.28 Weibull analysis for 2512 resistors with Sn solder ball alloy – As assembled

Figure 5.28 shows the failure data for 2512 resistors with various lead-free solder pastes with Sn alloy after assembly (No aged) and temperature cycling. It is shown that though Sn-4Ag-0.5Cu-0.05Ni solder paste was reliable for the 15mm and 17mm BGA package, it was weakest for the 2512 resistors. The material with the highest characteristics lifetime for 2512 resistors was Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni. Even in LLTS test, a similar trend was seen where Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni was the best. Based on the data, it is shown that Bi, Ni, and Sb were the critical elements which improved the reliability of resistors as shown in Sn-3.8Ag-0.7Cu-3Bi-

1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni. It is possible due to the absence of SAC305 ball alloy doped with solder pastes.

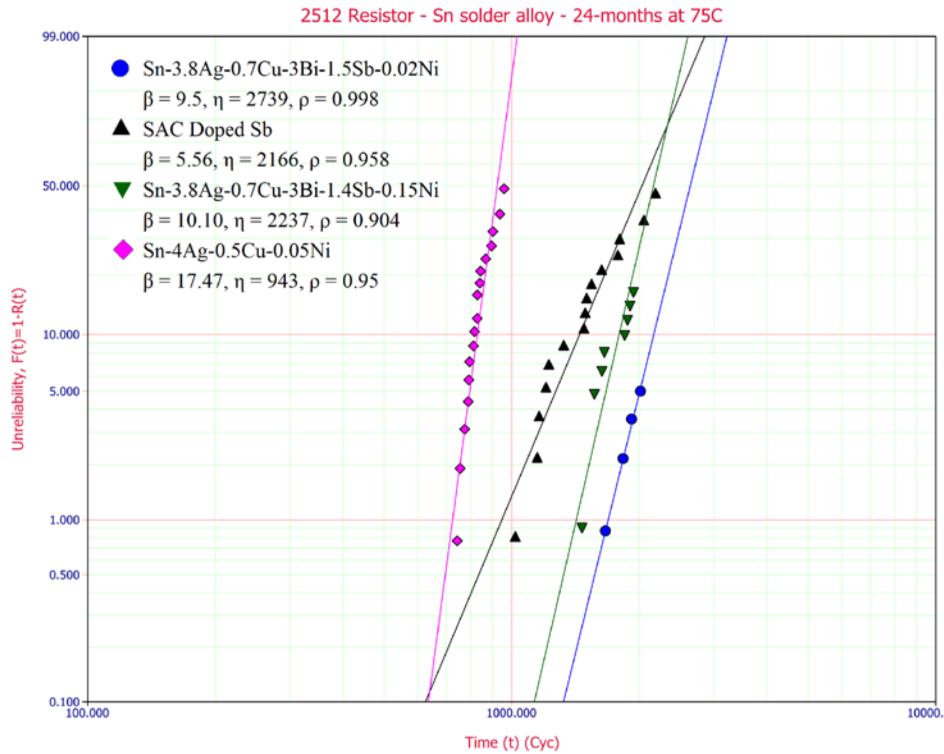


Figure 5.29 Weibull analysis for 2512 resistors with Sn solder ball alloy – 24 months at 75°C

The data for the given solder pastes with 2512 resistors after 24 months of aging and thermal cycling is shown in Figure 5.29. The Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste was comparatively better even after aging and testing. The same solder paste did not do well in BGA packages. The Sn-4Ag-0.5Cu-0.05Ni solder paste was still the worst after aging.

The solder paste which performed better than other pastes for all age groups was Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni with 23% deterioration. Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni showed the highest deterioration of 26%. Sn-4Ag-0.5Cu-0.05Ni and SAC doped Sb showed degradation of 5% and 9%, respectively.

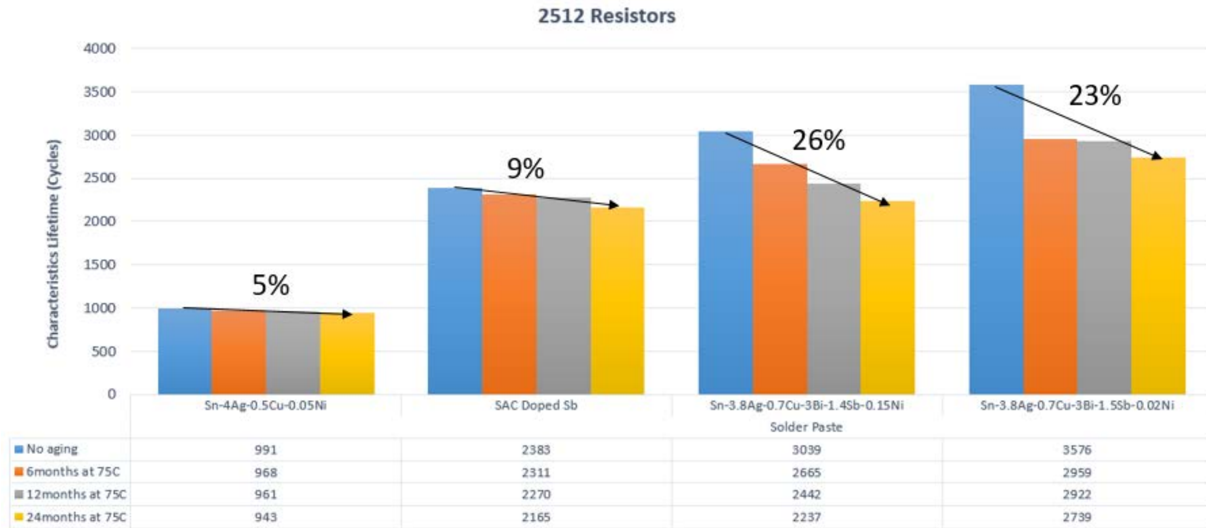


Figure 5.30 Characteristics lifetime summary of 2512 resistors

The above figure shows that Sn-4Ag-0.5Cu-0.05Ni solder paste was superior compared to other solder pastes for CABGA packages; however, it was the poorest for resistors.

5.5 Failure Analysis for Thermal cycling test

5.5.1 15mm BGA (CABGA 208)

Optical microscopy and cross-polarized images were taken to study the failure modes in the solder joints with four lead-free solder pastes and SAC305 solder paste from TC1-SJR Phase I [1], [130] for all 15mm BGA packages as shown in Figure 5.31 to Figure 5.35.

The failure modes for solder joints with Sn-4Ag-0.5Cu-0.05Ni solder paste was crack initiation and propagation at the top and bottom of the solder joint for all aging subgroups, which can be seen in Figure 5.31.

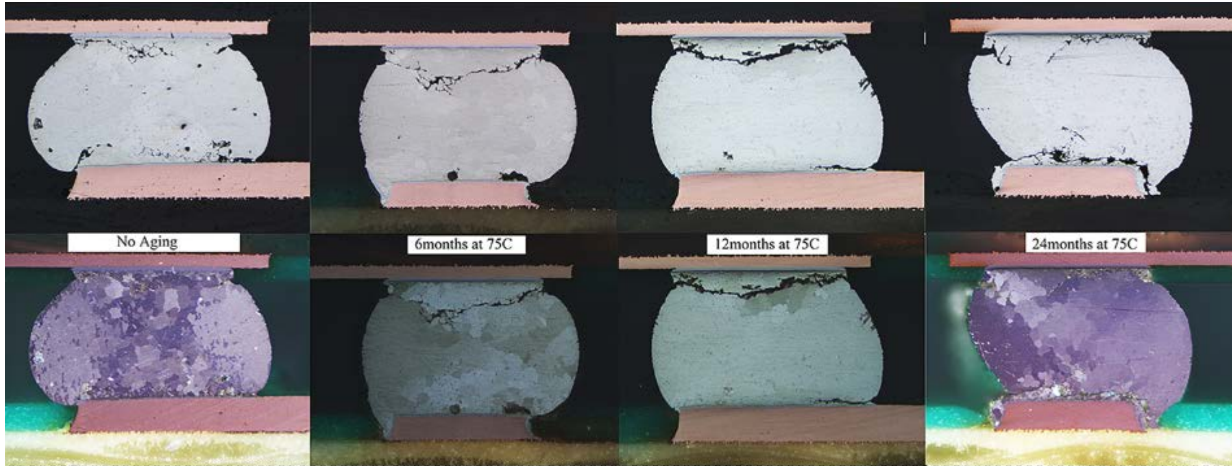


Figure 5.31 Optical microscopy images (1st row) and cross-polarized image (2nd row) of 15mm BGA with Sn-4Ag-0.5Cu-0.05Ni solder paste

For the no aged sample, crack initiation was observed at top right and bottom left. Crack initiation and propagation were seen in the top left and bottom right of the solder joint. The crack initiation typically occurs in the corner region of the solder joint where plastic deformation is the highest.

The crack propagation through the bulk solder at the top of the joint was seen for the 6-month and 12-month sample. For the 24-month sample, crack propagation occurred at bottom of the joint above the IMC layer. From the cross-polarized images, significant recrystallization was seen for no aged and 24-month aged samples.

Similar failure modes were seen for Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste with SAC305 solder ball alloy, as shown in Figure 5.32. Slight recrystallization was seen for the 24-month aged sample.

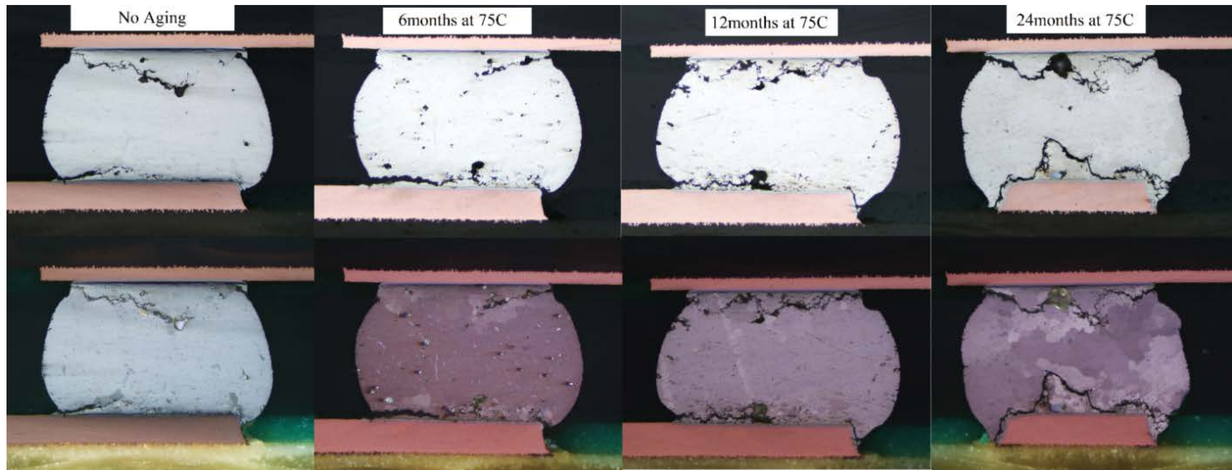


Figure 5.32 Optical microscopy images (1st row) and cross-polarized image (2nd row) of 15mm BGA with Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste

For Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste shown in Figure 5.33 below, crack initiation occurred at the top of the joint below the $(Cu, Ni)_6Sn_5$ IMC layer for no aged sample whereas crack propagation occurred at the bottom of the joint above $(Cu_3Sn + Cu_6Sn_5)$ IMC layer for all aged samples.

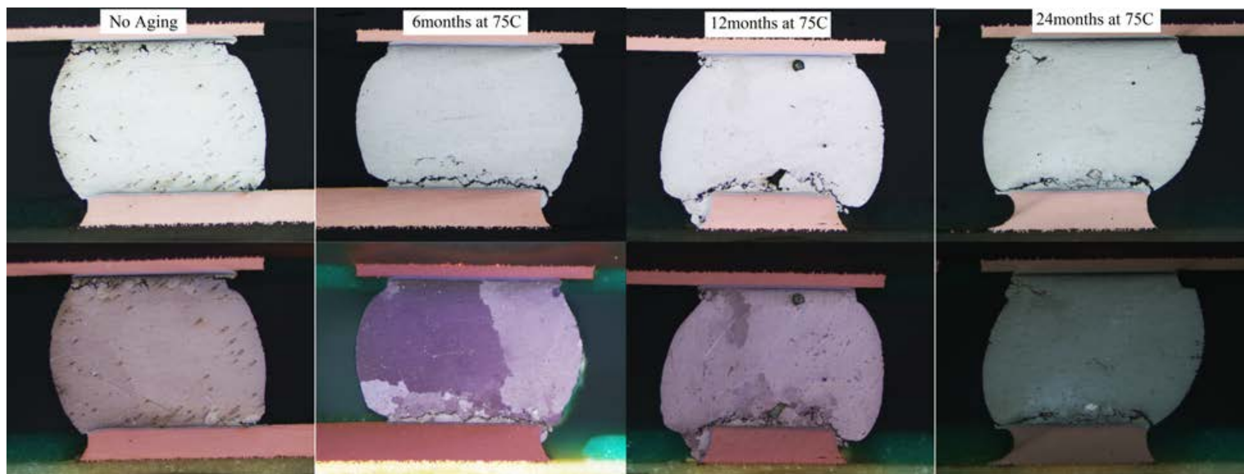


Figure 5.33 Optical microscopy images (1st row) and cross-polarized image (2nd row) of 15mm BGA with Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste

The crack propagation was seen for SAC doped Sb for all aging subgroups at the bottom of the joint above the IMC layer, as shown in Figure 5.34. Also, for the 6-month aged sample, the

crack propagated at the top of the joint below (Cu, Ni)$_6$Sn$_5$ IMC layer. From the 24-month aged sample, there appears to be an interaction of crack propagation from the top left and bottom of the joint. Recrystallization was seen for the 24-month aged sample.

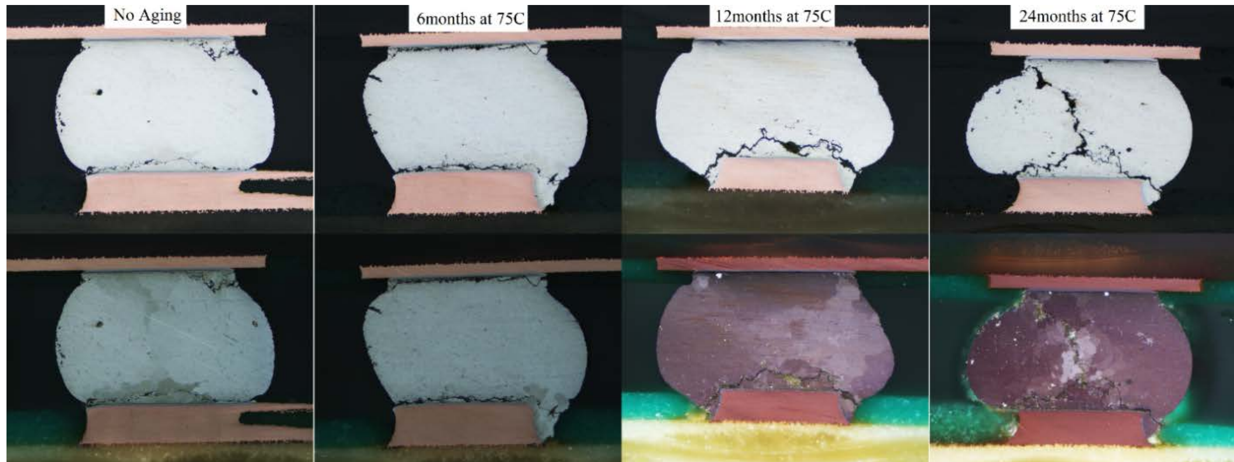


Figure 5.34 Optical microscopy images (1st row) and cross-polarized image (2nd row) of 15mm BGA with SAC doped Sb solder paste

The failure modes for SAC305 solder paste from TC1-SJR Phase I were no different compared to the ones shown previously. From the cross-polarized images, massive recrystallization was seen for the 24-month aged sample.

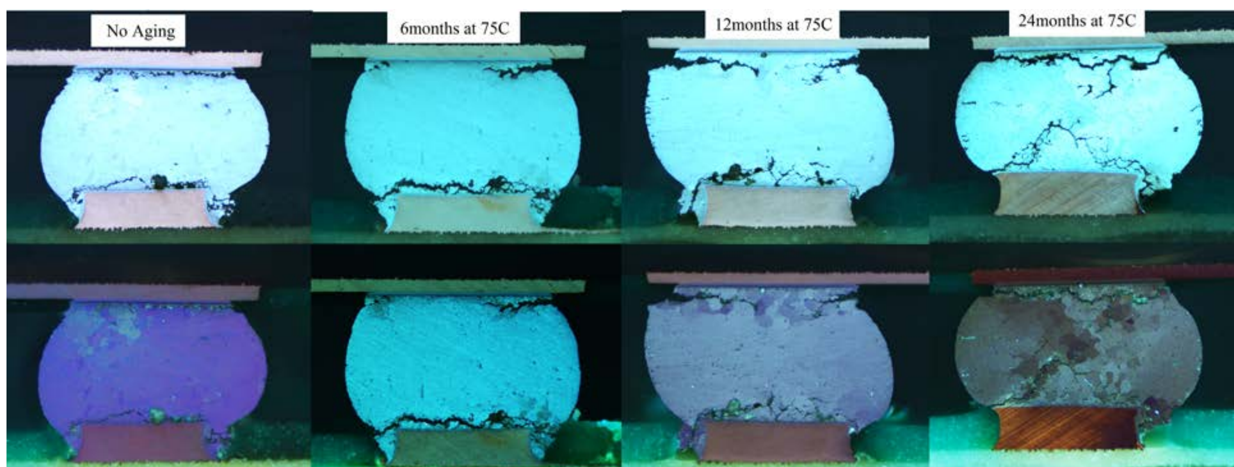


Figure 5.35 Optical microscopy images (1st row) and cross-polarized image (2nd row) of 15mm BGA with SAC305 solder paste

5.5.2 17mm BGA (CABGA 256)

Optical microscopy images of the solder joints from 17mm BGA packages are shown in Figure 5.36. Crack propagation was seen for SAC305 solder paste with SAC305 solder ball alloy at the top and bottom of the joint through bulk solder. For the Sn-4Ag-0.5Cu-0.05Ni solder paste with SAC305 solder ball alloy, crack propagation was observed at the top and bottom of the solder joint through the bulk solder. The Cu_6Sn_5 IMC appeared to be changing the path of crack propagation at the bottom of the joint [127].

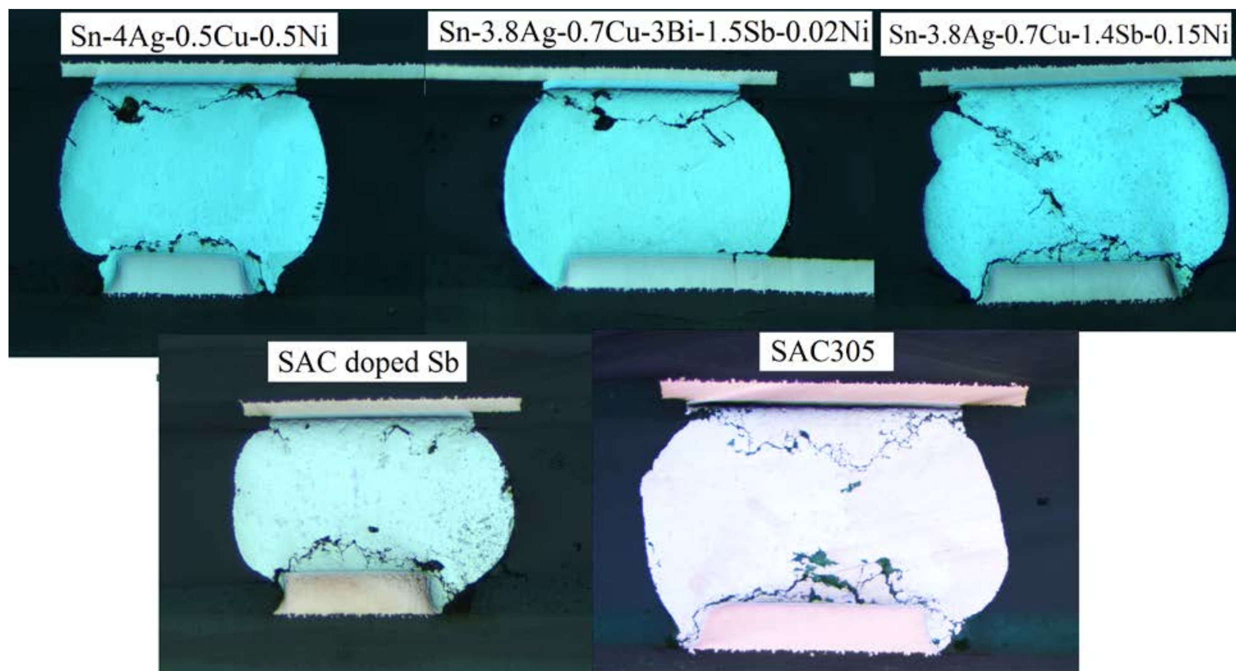


Figure 5.36 Optical microscopy images of 17mm BGA with various lead-free solder pastes

The crack propagation was seen at the bottom of the solder joint for Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste. The crack initiation and propagation were observed at the top of the solder joint.

For SAC doped Sb solder paste with SAC305 solder ball alloy, the crack propagation was observed on the top and bottom of the solder joint through the bulk solder.

Crack propagation through the bulk solder was seen for Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste with SAC305 solder ball alloy.

5.5.3 13mm BGA (CVBGA 432)

Figure 5.37 shows optical microscopy images of the solder joints from 13mm BGA packages which have a finer pitch. Failure modes are similar to 15mm and 17mm BGA packages for SAC305, Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, and SAC doped Sb solder pastes.

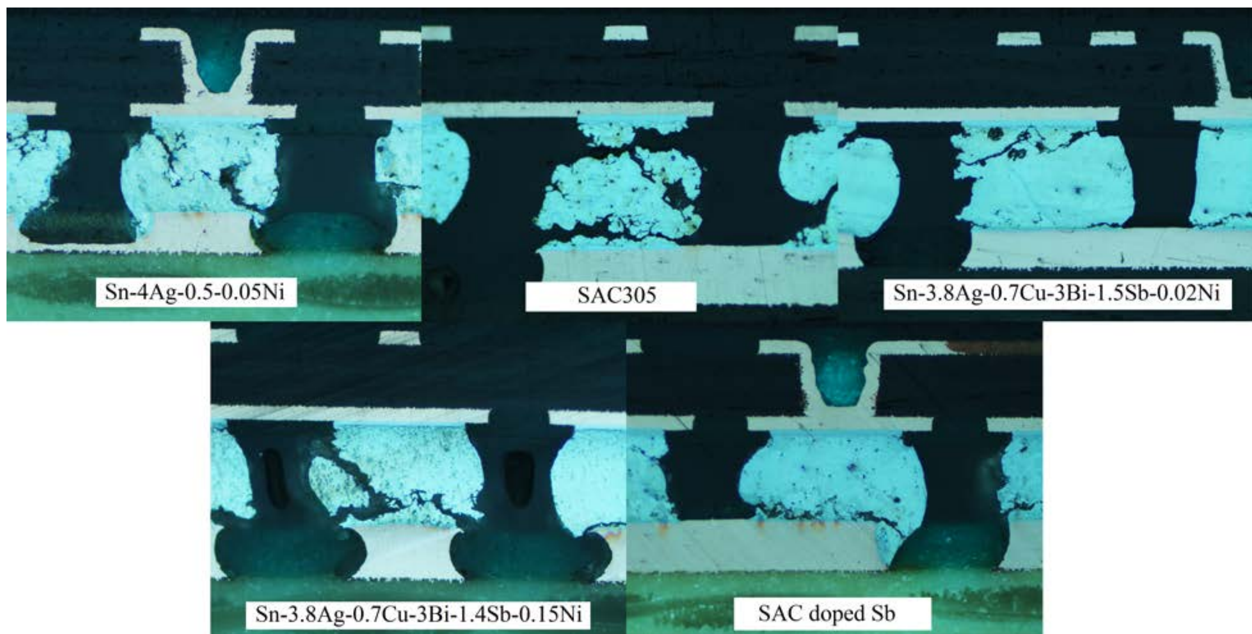


Figure 5.37 Optical microscopy images of 13mm BGA with various lead-free solder pastes

Crack propagation direction for Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder is the same as the 24-month aged 15mm BGA with SAC doped Sb solder paste. For the Sn-4Ag-0.5Cu-0.05Ni

solder paste, the crack initiation appeared to originate from the top left and bottom right. Then the crack propagation interaction occurred at the bulk solder as shown in the figure.

5.5.4 2512 resistors

Optical microscopy images of 2512 resistors are shown in Figure 5.38. The 2512 resistors with SAC305 solder paste were not built in TC-SJR Phase I test since smaller resistors were used during that test.

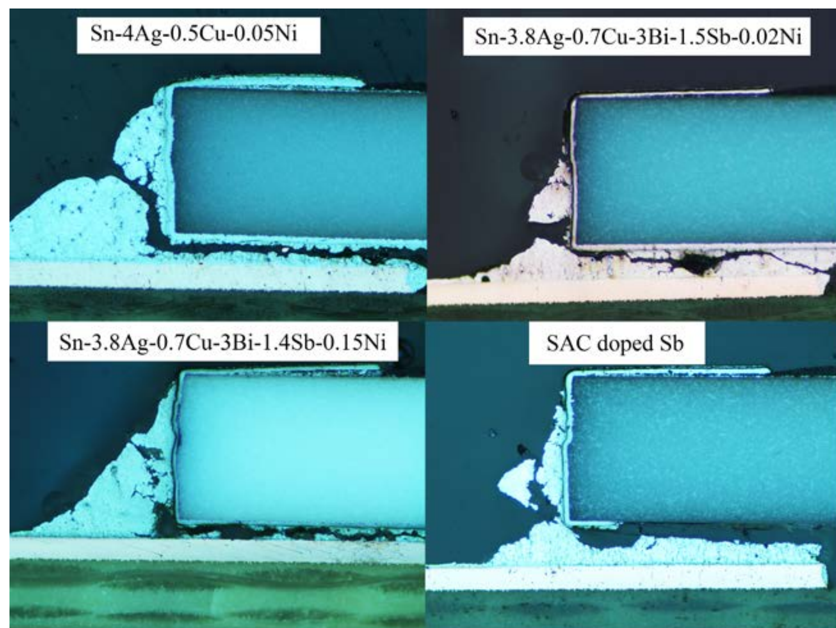


Figure 5.38 Optical microscopy images of 2512 resistors with various lead-free solder pastes

Failure modes observed in these resistors were solder joint cracking, and failure mechanisms associated with this failure mode were creep and fatigue. The creep-fatigue crack initiation occurs under the resistor and then follows a path parallel to the resistor, turns around the corner at the resistor edge, and then proceeds until complete separation has occurred [131].

5.5.5 IMC Thickness Analysis

The average IMC thickness measurement of 4 lead-free solder pastes from TC1-SJR Phase II and SAC305 solder paste from TC1-SJR Phase I under different aging groups was measured for the 17mm BGA package, as shown in Figure 5.39.

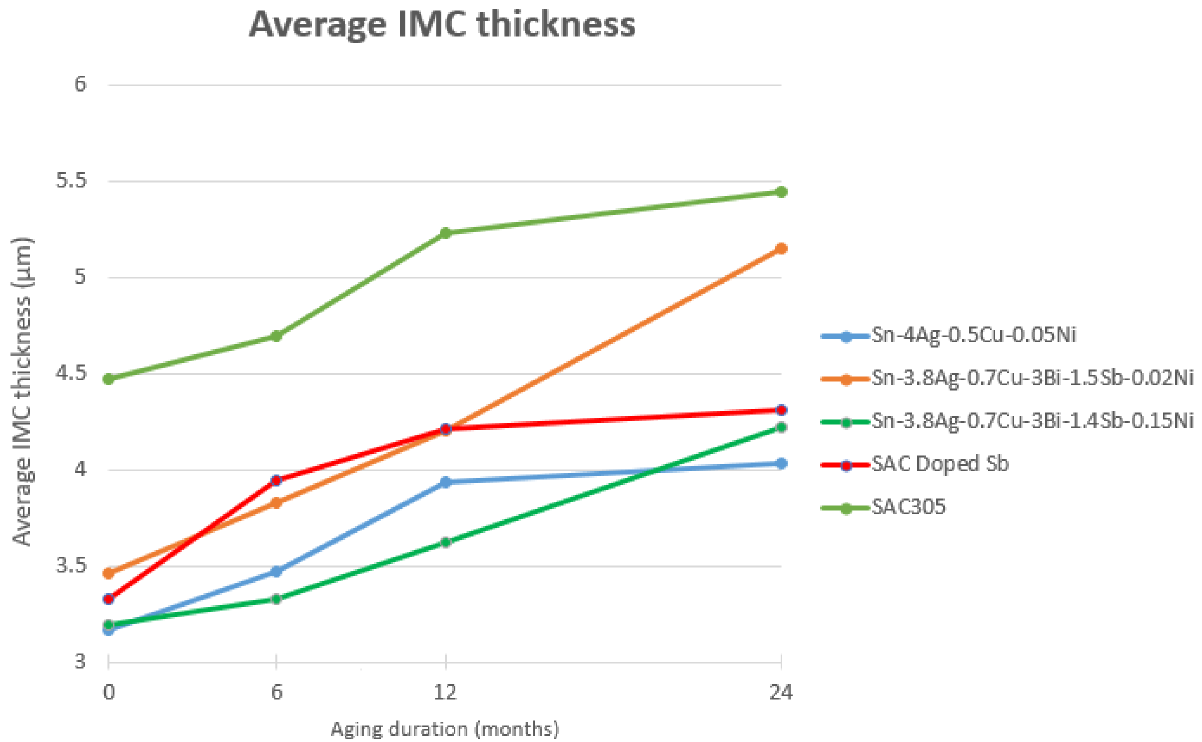


Figure 5.39 Average Intermetallic Thickness trend

The IMC thickness for SAC305 solder paste is the highest compared with the other pastes, which correlate to 58% degradation in characteristics lifetime. The IMC growth curve for Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni is higher than Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste. This is possibly due to the presence of additional nickel present in Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste that inhibited the growth of Cu_3Sn IMC layer. The IMC thickness for SAC doped Sb is higher than that of Sn-4Ag-0.5Cu-0.05Ni solder paste. The presence of nickel in SAC

alloy reduced the growth of IMC for both Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-4Ag-0.5Cu-0.05Ni solder paste [127].

5.5.6 Findings from TC-SJR Phase II test

The thermal cycling reliability of doped lead-free solder pastes from TC1-SJR Phase II and SAC305 solder paste from TC1-SJR Phase I built using Megtron6 board substrate were compared. The only material that outperformed the SAC305 solder paste across all aging groups was Sn-4Ag-0.5Cu-0.05Ni solder paste.

A high level of degradation was seen for the SAC305 material throughout the test for the 15mm and 17mm BGA packages followed by Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste. Sn-4Ag-0.5Cu-0.05Ni exhibited a much lesser degradation rate which showed improved reliability for all aging groups.

Failure analysis for BGA packages showed crack propagation in failed interconnects at the top and bottom of the solder joint. Intermetallic thickness measurements showed that the growth curve was least for Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-4Ag-0.5Cu-0.05Ni solder paste compared with Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, SAC doped Sb, and SAC305. Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-4Ag-0.5Cu-0.05Ni solders indicated slower growth in (Cu_3Sn + Cu_6Sn_5) IMC thickness layer after aging. Though the (Cu_3Sn + Cu_6Sn_5) IMC layer for SAC305 increased faster than Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste, SAC305 was still better than Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni. From TC1-SJR Phase I [1], Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste did better than SAC305 for FR-406 board substrate. Material characterization and detailed grain structure need to be investigated to analyze the cause behind this trend.

For 13mm BGA (CVBGA 432), Sn-4Ag-0.5Cu-0.05Ni performed slightly worse after 24 months aging than most materials. However, the difference was small (within 50 cycles for most measurements). Overall, Sn-4Ag-0.5Cu-0.05Ni performed best across the BGA design followed by SAC doped Sb.

Top-performing materials for 2512 resistors were Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and the same materials performed poorly for BGA packages. Sn-4Ag-0.5Cu-0.05Ni proved to be the worst material for resistors. The primary difference between surface mount resistors and all other components is the absence of solder balls. All other components had the SAC305 solder ball attached to the component, which added a dopant material.

Chapter 6 Summary and Conclusion

The solder joint reliability of doped Pb-free solder pastes was evaluated by conducting liquid to liquid thermal shock test. Component lifetime after assembly and 6-month aged were compared. It is shown that doping antimony to SAC alloy has improved the lifetime of the solder pastes such as 3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni, and SAC doped Sb compared with the baseline SAC305. The addition of bismuth, antimony, and nickel have proved to be useful in enhancing the mechanical strength of the solder material in Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni pastes. A higher percentage of Ag also showed superior reliability due to an increase in the number of Ag_3Sn precipitate in Sn-4Ag-0.5Cu-0.05Ni solder.

IMC thickness measurements showed that solders with small weight percentages of the elements Bi, Ni, and Sb result in thinner IMC thicknesses than SAC305. The impact of bismuth in the SAC based solder pastes has effectively reduced the IMC thickness at the board, which was seen in Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni and Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder pastes.

Nickel significantly mitigated the IMC growth in the package side interface because of its ability to inhibit diffusion. A higher percentage of Ag showed superior thermal shock reliability due to the increasing number of Ag_3Sn precipitate in Sn-4Ag-0.5Cu-0.05Ni solder.

The materials which showed reduced degradation of characteristics lifetime after aging and superior reliability compared with SAC305 are

- Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni
- Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni
- Sn-4Ag-0.5Cu-0.05Ni

- SAC doped with Sb

The primary component used for qualifying the solder pastes to evaluate aging effects was 15mm BGA. Considering long term aging effects, these materials were chosen for the TC-SJR Phase II test.

The thermal cycling reliability of doped Pb-free solder pastes from TC1-SJR Phase II and SAC305 solder paste from TC1-SJR Phase I built using Megtron6 board substrate were compared. The only material that outperformed the SAC305 from TC-Phase I and other Pb-free pastes across all aging groups was Sn-4Ag-0.5Cu-0.05Ni solder paste.

A high level of degradation was seen for the SAC305 material throughout the test for 15mm and 17mm BGA packages followed by Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder paste. Sn-4Ag-0.5Cu-0.05Ni exhibited a much lesser degradation rate which showed improved reliability for all aging groups.

Failure analysis for BGA packages showed crack propagation in failed interconnects at the top and bottom of the solder joint. Intermetallic thickness measurements showed that the growth curve was least for Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-4Ag-0.5Cu-0.05Ni solder paste compared with Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni, SAC doped Sb, and SAC305. Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-4Ag-0.5Cu-0.05Ni solder paste indicated slower growth in (Cu_3Sn + Cu_6Sn_5) IMC layer after aging. Though the (Cu_3Sn + Cu_6Sn_5) IMC thickness layer for SAC305 was higher than Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste, SAC305 was still better than Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste. From TC1-SJR Phase I [1], Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste did better than SAC305 for FR-406 board substrate. Material characterization and detailed grain structure need to be investigated to analyze the cause behind this trend.

For 13mm BGA (CVBGA 432), Sn-4Ag-0.5Cu-0.05Ni performed slightly worse after 24 months aging than most materials. However, the difference was small (within 50 cycles for most measurements). Overall, Sn-4Ag-0.5Cu-0.05Ni performed best across the BGA design followed by SAC doped Sb.

Top-performing materials for 2512 resistors were Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni and Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni. These materials performed poorly for BGA packages. Sn-4Ag-0.5Cu-0.05Ni proved to be the worst material for resistors. The primary difference between surface mount resistors and all other components is an absence of solder balls in resistors. All other components had the SAC305 solder ball attached to the component, which added a dopant material.

Chapter 7 Future Work

The thermal shock and thermal cycling reliability of Pb-free solders were highlighted. These results may vary for mechanical shock tests depending on the solder joint's material composition and ductility. Mechanical testing such as drop, vibration, and shear tests are essential to determine the solution to reliability and aging issues for solder interconnection subjected to mechanical drop or impact loading.

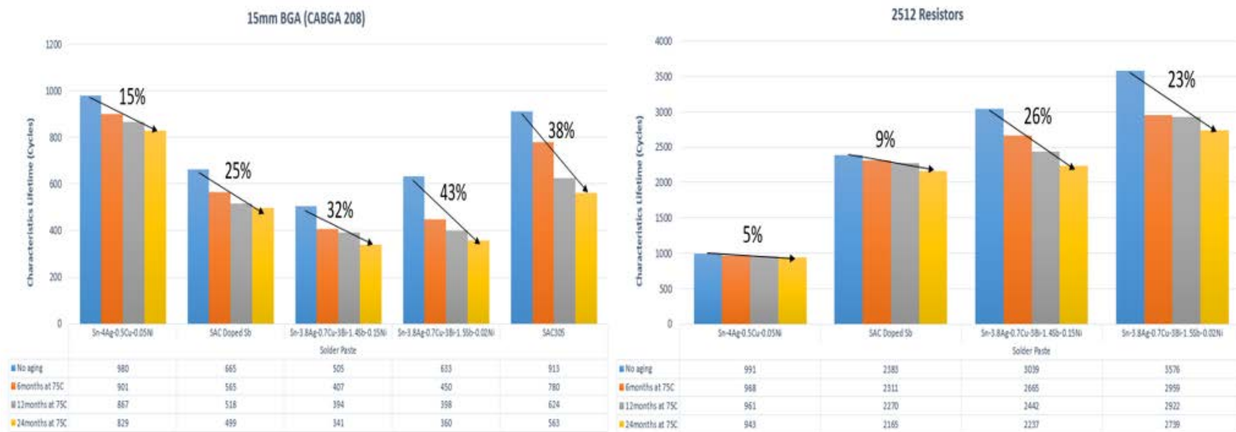


Figure 7.1 TC-SJR Phase II with Megtron6 substrate for 15mm BGA package (Left), TC-SJR Phase II with Megtron6 substrate for SMR2512 resistors (Right)

As shown in Figure 7.1, TC-Phase II test indicated that Sn-4Ag-0.5Cu-0.05Ni performed better than other solder pastes with BGA packages but was the lowest-performing material for SMR resistors. Further testing must be performed to understand how the reliability of materials is affected by doping with various levels of SAC305. The SMR2512 was built on the TC-Phase II test vehicles, and therefore no comparison data was available between Phase I and Phase II.

This test would serve as a starting point to optimize the level of dopants in solder joints for various harsh environment applications. In addition, comprehensive testing is also required. The

characterization of these materials must be completed to determine physical and mechanical properties. Fatigue and prediction models can then be developed to find the actual operating lifetime in the field.

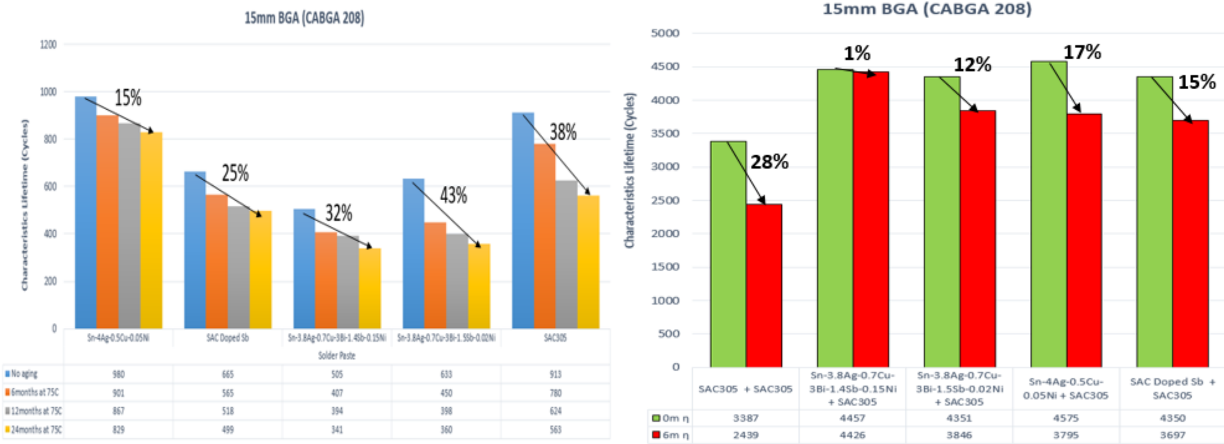


Figure 7.2 TC-SJR Phase II with Megtron6 substrate after 24 months of aging at 75°C (Left), Solder downselect test with FR-406 substrate after 6 months of aging at 125°C (Right)

From solder downselect test results shown in Figure 7.2 (right), four materials performed better than SAC305 solder paste even after aging at 6 months. Materials except Sn-4Ag-0.5Cu-0.05Ni solder underperformed compared with SAC305 solder paste. Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni solder paste did better than SAC305 for FR-406 board substrate in TC1-SJR Phase I [1] and solder downselect test. Material properties need to be determined to find the cause behind this trend.

The failure data summary of 15mm BGA package (as assembled) across all the thermal tests is shown in Table 7.1. This table considers the effect of thermal tests, board thickness and its substrate. Data collected from experiments covered in this dissertation is highlighted in red. The non-highlighted ones were collected from literature and '?' indicates non-availability of data.

Table 7.1 Failure data of 15mm BGA for all thermal tests

Board thickness (mm)	Solder Paste	Test	Board substrate			
			FR-406		Megtron6	
			β	η	β	η
1.57	SAC305	Thermal Shock	7.32	3387	?	?
	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni		5.81	4457	?	?
	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni		4.287	4351	?	?
	Sn-4Ag-0.5-0.05Ni		6.31	4575	?	?
	SAC Doped Sb		13.77	3457	?	?
	SAC305 [88]	Thermal Cycling	3.516	3743	?	?
	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni [132]		3.64	3542	?	?
5.08	SAC305 [1]		6.02	1590	11.76	846
	Sn-3.8Ag-0.7Cu-3Bi-1.4Sb-0.15Ni		4.64 [1]	1947 [1]	6	505
	Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni		?	?	3.23	633
	Sn-4Ag-0.5-0.05Ni		?	?	8.99	980
	SAC Doped Sb		?	?	3.78	665

Understanding the behavior of BGA considering the board substrate difference (1.57mm thickness) for thermal shock test and thermal cycling test is essential. Also, the thermal cycling behavior of SAC doped Sb, Sn-4Ag-0.05Ni, and Sn-3.8Ag-0.7Cu-3Bi-1.5Sb-0.02Ni solder pastes for FR-406 board substrate (5.08mm thickness) need to be determined.

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