# DIE STRESS CHARACTERIZATION AND INTERFACE DELAMINATION STUDY IN FLIP CHIP ON LAMINATE ASSEMBLIES

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# DIE STRESS CHARACTERIZATION AND INTERFACE DELAMINATION STUDY IN FLIP CHIP ON LAMINATE ASSEMBLIES

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# DIE STRESS CHARACTERIZATION AND INTERFACE DELAMINATION STUDY IN FLIP CHIP ON LAMINATE ASSEMBLIES

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# VITA

Md. Kaysar. Rahim, son of Md. Abdur Rahim and Shamima Akhtar, was born on January 1, 1972, in Rajshahi, Rajshahi Province, Bangladesh. He graduated from Rajshahi University School and College in 1989. He went to Bangladesh University of Engineering and Technology, and graduated with the degree of Bachelor of Mechanical Engineering in July of 1996. After his graduation, he joined the faculty of the Mechanical Engineering Department of Bangladesh Institute of Technology, and performed his teaching and research duties in the area of structural design, and experimental mechanics. He started his graduate studies in the Mechanical Engineering Department, Auburn University, Alabama, in September 1998.

# DISSERTATION ABSTRACT

# DIE STRESS CHARACTERIZATION AND INTERFACE DELAMINATION STUDY IN FLIP CHIP ON LAMINATE ASSEMBLIES

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Thermo-mechanical reliability of flip chip on laminate packaging is a major concern when the assemblies are exposed to harsh operating environments such as space or automotive underhood applications. In this study, structural and thermal reliability of flip chip packages have been investigated during the assembly process and accelerated life testing using piezoresistive stress sensing test chips. Both 5 x 5 mm (FC200) and 10 x 10 mm (FC400) test chips fabricated on (111) silicon were utilized to characterize the complete die stress state on the device side of the chip in flip chip on laminate assemblies. The FC200 chip includes 11 eight-element sensor rosettes, a diode for temperature measurement, an eight-bit fuse style chip ID, and contains 200 μm (8 mil)

pitch perimeter solder bumps. The FC400 chip includes 19 stress sensor rosettes, 2 diodes for temperature measurement, a 10-bit fuse style chip ID, an embedded full coverage heater for heat transfer or power cycling experiments, and also contains 200 μm pitch perimeter solder bumps.

This flip chip study is divided into four parts. In the first part of this work, transient die stress measurements have been made during underfill cure, and the room temperature die stresses in final cured assemblies have been compared for several different underfill encapsulants. The experimental stress measurements in the flip chip samples were then correlated with finite element predictions for the tested configurations. It is well known that underfill has significant impact on flip chip package reliability. To investigate the effects of underfill on thermo-mechanical behavior of flip chip packages, three different underfill materials were used in this study. A total of 75 flip chip test boards (1 die size x 3 underfills x 25 samples per combination) were assembled at the CAVE SMT Line at Auburn University. In each assembly, the three-dimensional die surface stresses have been recorded during underfill cure, and after underfill cure (room temperature).

In the second part of this work, the silicon die stresses occurring in flip chip assemblies have been characterized and modeled at extremely low temperatures. Stress measurements have been made down to -180 $^{o}$C using test chips incorporating piezoresistive sensor rosettes. The obtained stress measurement data have been correlated with the predictions of nonlinear finite element models. A microtester has been used to characterize the stress-strain behavior of the solder and underfill encapsulant from -180 to 150 $^{o}$C to aid in this modeling effort.

In the third part of this work, the stress variations occurring during thermal cycling from -40 to +125 $^{o}$C have been characterized. These measurements have been correlated with the delaminations occurring at the die passivation to underfill interface measured using C-mode Scanning Acoustic Microscopy (C-SAM). With this approach, the stress distributions across the chip, and the stress variations at particular locations at the die to underfill interface have been interrogated for the entire life of the flip chip assembly. In order to correlate the stress changes at the sensor sites with delamination onset and propagation, CSAM evaluation of the test assemblies was performed after every 125 thermal cycles.

A total of 75 flip chip assemblies with 3 different underfills have been evaluated. For each assembly, the complete histories of three-dimensional die surface stresses and delamination propagation have been recorded versus the number of thermal cycles. The stress histories that lead to delamination initiation for each underfill encapsulant, and the variation of the stresses that occur before and during delamination propagation have been identified. The progressions of stress and delamination have been mapped across the entire surface of the die, and a series of stress/delamination videos have been produced. One of the most important discoveries is that the shear stresses occurring at the corners of flip chip die have been demonstrated to be a suitable proxy for prognostic determination of future delamination initiations and growth. Thus, shear stress sensors have great potential as health-monitoring devices in flip chip packaging.

In the fourth and final part of this work, die stress characterization was performed in flip chip assemblies utilizing a new low expansion coefficient laminate material. The new substrate material is a hybrid laminate formed using a combination of standard glass

fiber reinforced resin outer layers (FR-4), with a carbon fiber reinforced resin core layer. The carbon fiber based central core (STABLCOR) features both high stiffness and high thermal conductivity, as well as near zero thermal expansion coefficient. Because of the extremely low expansion coefficient of the carbon fiber core and the bonded nature of the laminate, the surface CTE of the hybrid laminate PCB stack-up is typically in the range of 2.0-4.0 ppm/$^{o}$C over the temperature range of -55 to 150 $^{o}$C, which is much lower than the typical 13.0-20.0 ppm/$^{o}$C seen with standard FR-4 based laminates. In addition, the high stiffness of the carbon fiber based core can help reduce PCB warpage issues, as well as vastly improve the net heat conduction characteristics of the PCB substrate

FC200 and FC400 flip chip test die were packaged on the low expansion laminates, and the die surface stresses were measured throughout the assembly process. Die stress measurements have been made during underfill cure, and at room temperature after final assembly. The results have been compared to those from analogous FR-406 substrate assemblies. Significant stress reductions have been observed when using the low expansion coefficient laminate.

# ACKNOWLEDGEMENTS

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# CHAPTER 1

# INTRODUCTION

Structural reliability of integrated circuit (IC) chips in electronic packages continues to be a major concern due to ever-increasing die size, circuit densities, power dissipation, operating temperatures, and the use of a wide range of low-cost packaging materials. Stress related problems are prevalent in every stage of semiconductor manufacturing. When a semiconductor wafer undergoes fabrication processes, it is stressed due to the coefficient of thermal expansion mismatches between the silicon substrate and the deposited thin film layers. Localized stresses also occur due to discontinuities in these films. In addition to these wafer level stresses, assembly and packaging processes induce additional mechanical stresses on the chip and other packaging materials. These stresses can affect the quality and reliability of the assembled components. Such stresses arise due to several reasons including coefficient of thermal expansion mismatches, geometrical discontinuities, cyclical and random thermal loadings and handling during assemblies operations.

Typical IC packages are comprised of a variety of materials ranging from brittle materials (e.g. silicon) to ductile materials (e.g. solder). All of these materials expand and contract at different rates and have different elastic moduli. When such assemblages of materials are heated or cooled, the coefficient of thermal expansion mismatches lead to thermal stresses. A silicon chip has a very uneven surface on a microscopic level after it has gone through the wafer fabrication process. In addition, local amplifications in stress can result from stress raisers such as sharp edges on the die, lead fingers, and die pad, or voids in the molding compound or die attach material. Typical reliability tests for IC packages involve thermal cycling them between hot and cold extreme temperatures. These cyclical temperature excursions can lead to delaminations and/or fatigue. Moreover, whenever devices on the chip are powered on and off, the associated ohmic heating and subsequent cooling produces additional thermal loading of the package. These cyclic and random thermal loadings are unavoidable, and the design of the packages must be optimized so that these stresses can be minimized. Mishandling or misprocessing during assembly can produce unacceptable peak stresses. Examples are improper wafer dicing, local unbonded areas in die attachment operations, and excessive pressure or ultrasonic energy applied during wire bonding. The stresses in this category can be managed by optimizing of assembly processes. Although each assembly step is potentially a stress producing operation, most of the stresses in the semiconductor chip are induced during die attachment (bonding) and during encapsulation such as the molding of plastic packages or underfilling of flip chip on laminate assemblies.

The microelectronics industry continues to seek higher density packaging and more chip complexity. This results in larger chips but smaller packages, so that the die is becoming a larger portion of the total package volume. Thus, mechanical stress levels in the silicon die continue to increase as the chip becomes a more significant structural element in the package. Also, the area array solder bump interconnection schemes used in Direct Chip Attach (DCA) can put non-uniform loads across the die. These stress distributions can change rapidly over small length scales.

Stress analyses of electronic packages and their components have been performed using analytical, numerical, and experimental methods. Analytical investigations have been primarily concerned with finding closed-form elasticity solutions for layered structures, while numerical studies have typically considered finite element solutions for sophisticated package geometries. Experimental approaches have included the use of test chips incorporating piezoresistive stress sensors (semiconductor strain gages), and the use of optical techniques such as holographic interferometry, moiré interferometry, and photoelasticity.

Piezoresistive stress sensors are a powerful tool for experimental structural analysis of electronic packages. Figure 1.1 illustrates the basic application concepts. The structures of interest are semiconductor (e. g. silicon) chips that are incorporated into electronic packages. The sensors are resistors that are conveniently fabricated into the surface of the die using current microelectronic technology. The sensors are not mounted on the chips. Rather, they are an integral part of the structure (chip) to be analyzed by the way of the fabrication process. The stresses in the chip produce resistance changes in the sensors (due to the piezoresistive effect) that can be measured. Therefore, the sensors are capable of providing non-intrusive measurements of surface stress states on a chip even within encapsulated packages (where they are embedded sensors). If the piezoresistive sensors are calibrated over a wide temperature range, thermally induced stresses can be measured. Finally, a full-field mapping of the stress distribution over the surface of a die can be obtained using specially designed test chips, which incorporate an array of sensor rosettes.

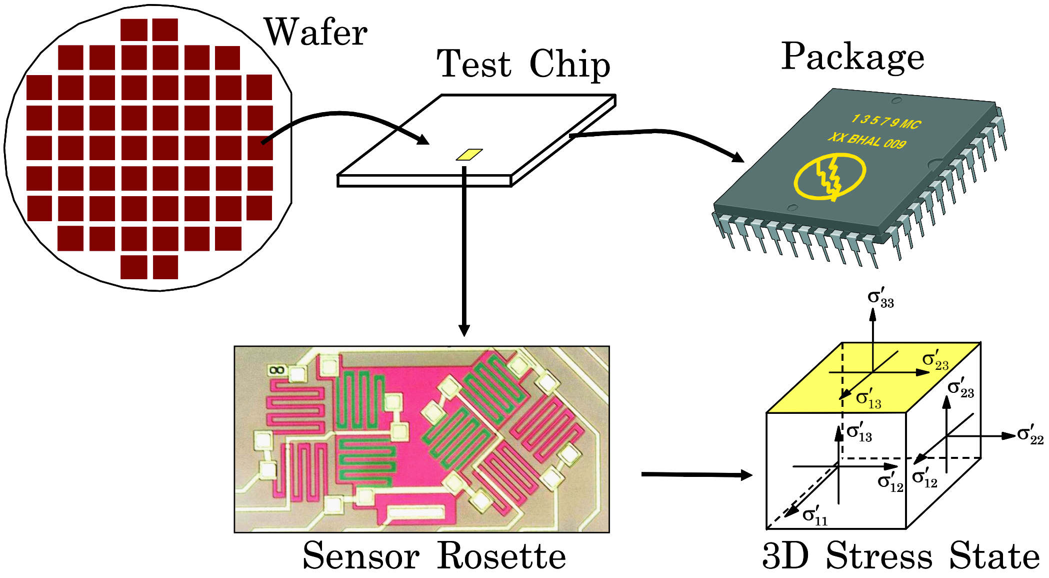

Wafer
Test Chip
Package
13579MC
XX BHAL 009
Sensor Rosette
3D Stress State
$\sigma'_{33}$
$\sigma'_{23}$
$\sigma'_{13}$
$\sigma'_{23}$
$\sigma'_{13}$
$\sigma'_{22}$
$\sigma'_{12}$
$\sigma'_{12}$
$\sigma'_{11}$

Figure 1.1 – Piezoresistive Sensor Concept

Prior publications on stress sensing test chips have included sensor rosettes with up to eight resistors. Using n-type and p-type sensors at various orientations, several or all the stress components on the die surface can be measured. By monitoring packaging stresses using stress sensing test chips, a variety of accomplishments have been achieved. For instance, test chips have been used to provide a better understanding of the shear stress failure mechanisms in encapsulated packages. In addition, thermal stresses due to die attachment, molding, and temperature variation have been characterized. The effects of die size and package configuration on the stresses after molding have also been quantified for various package pin counts. Piezoresistive measurements have allowed molding compound materials to be evaluated with respect to their thermal-induced stress levels. Also, the effects of thermal cycling and delamination at the chip/encapsulant interface can be explored using test chips. Recently, thermal stress measurements of epoxy underfilled flip-chip on board devices were reported, and the effects of the curing conditions of the underfill were investigated. Details of these studies are discussed in the subsequent chapter (literature review).

Theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon. In particular, optimized rosettes on (111) silicon can be used to measure the complete state of stress (six stress components) at a point on the top surface of the die, while optimized rosettes on (100) silicon can measure at most four stress components. Also, optimized sensors on (111) silicon offer the unique capability of measuring four temperatures compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities.

Furthermore, it has been established that the (111) plane offers the opportunity to measure the highest number of stress components in a temperature compensated manner. This is particularly important, given the large thermally induced errors, which can often be found in stress sensor data. The four stress components, which can be measured in a temperature compensated manner using (111) silicon sensors, are the three shear stress components and the difference of the in-plane normal stress components. Details of these theoretical considerations are reviewed in chapter 3.

In this work, (111) silicon test chips containing an array of optimized piezoresistive stress sensor rosettes have been successfully applied within flip chip packaging configurations. Calibrated and characterized stress test chips were flip chip bonded on laminate substrate, and then the post packaging resistances of the sensors were recorded. These packaging resistances were monitored at room temperature, as a function of temperature excursion, and during long term packaging reliability qualification tests (thermal cycling). The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purposes, three-dimensional nonlinear finite element simulations of the flip chip packages were also performed, and the stress predictions were correlated with the experimental test chip data.

In the early chapters of this thesis, silicon piezoresistive theory has been reviewed to allow for understanding of the equations utilized for stress calculation on the die surface. General resistance change equations have been expressed in the unprimed crystallographic system, and in an arbitrarily rotated primed coordinate system. The ensuing resistance change equations for (111) silicon wafer planes were then extracted. The (111) silicon test chips used in this study contain sensors rosettes with p-type and n-type sensor sets, each with resistor elements making angles of $\phi$ = 0, $\pm 45$, 90$^{o}$ with respect to $x_1'$-axis perpendicular to the wafer flat. For the (111) silicon case, this eight-element dual polarity rosette has been optimized to measure all six-stress components (four in a temperature compensated manner). This is a particularly important attribute, given the large errors which can be introduced into non-temperature compensated stress sensor data when the temperature change T is not precisely known. The four measurable temperature compensated stress components are $(\sigma_{11}' - \sigma_{22}')$, $\sigma_{12}'$, $\sigma_{13}'$, $\sigma_{23}'$.

In this work, an extensive study on thermo-mechanical evaluation of flip chip packages has been performed. The use of flip chip technology is increasing with the demands for high-density packaging and electronics miniaturization. It is an attractive solution for many system designs, including digital watches, cellular phones, disk drives, and personal digital assistants, which are constrained by size, I/O density, electrical performance (e.g., signal speed), reliability, or cost. Flip chip technology offers high I/O density on a small footprint with fast signal processes, due to the short electrical interconnect length. Flip chip assembly refers to a method by which a solder bumped bare integrated circuit (IC) die is attached, face down, directly to a substrate (ceramic, silicon, or laminate). A schematic of a flip chip on laminate assembly is shown in Figure 1.2. This attachment method eliminates the need for conventional first level IC packaging. Die that are to be used as flip chips leave the wafer fabrication and are maintained in wafer form until the bumping operations are complete. By batch processing wafers, millions of I/O can be bumped at once, in contrast to wire bonds, which are generated one I/O at a time. It is important to note that flip chips have been used by IBM in electronic systems since the 1960's. Widespread use of flip chip as a

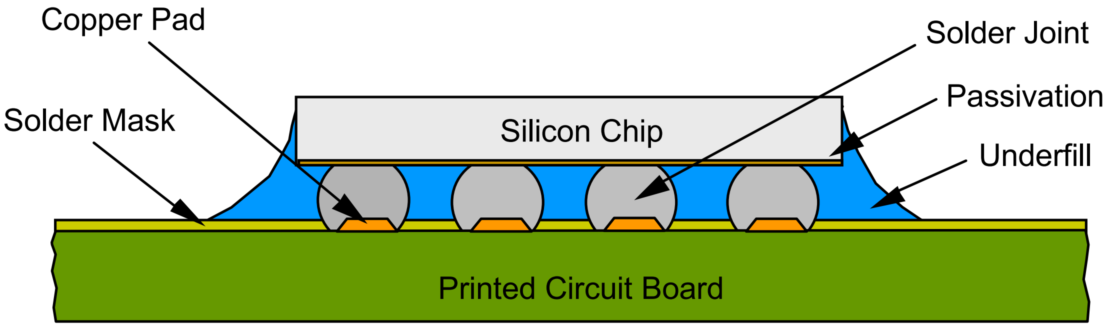

Copper Pad
Solder Joint
Passivation
Solder Mask
Silicon Chip
Underfill
Printed Circuit Board

Figure 1.2 - Typical Cross-Section of a Flip Chip Package

surface mount alternative has been slow to develop due to the multi-million dollar investment in capital equipment required to bump wafers using traditional bumping techniques (i.e. vapor deposition, photolithography, electroplating, etc.). Over the past decade, many advances have been made towards generating low cost flip chip on laminate solutions.

Thermo-mechanical reliability of flip chip on laminate packaging is a major concern when the assemblies are exposed to harsh operating environments such as space or automotive underhood applications. In this study, structural and thermal reliability of flip chip packages have been investigated during the assembly process and accelerated life testing using piezoresistive stress sensing test chips. Both 5 x 5 mm (FC200) and 10 x 10 mm (FC400) test chips fabricated on (111) silicon were utilized to characterize the complete die stress state on the device side of the chip in flip chip on laminate assemblies. The FC200 chip includes 11 eight-element sensor rosettes, a diode for temperature measurement, an eight-bit fuse style chip ID, and contains 200 μm (8 mil) pitch perimeter solder bumps. The FC400 chip includes 19 stress sensor rosettes, 2 diodes for temperature measurement, a 10-bit fuse style chip ID, an embedded full coverage heater for heat transfer or power cycling experiments, and also contains 200 μm pitch perimeter solder bumps.

This flip chip study is divided into four parts. In the first part of this work, transient die stress measurements have been made during underfill cure, and the room temperature die stresses in final cured assemblies have been compared for several different underfill encapsulants. The experimental stress measurements in the flip chip samples were then correlated with finite element predictions for the tested configurations.

It is well known that underfill has significant impact on flip chip package reliability. To investigate the effects of underfill on thermo-mechanical behavior of flip chip packages, three different underfill materials were used in this study. A total of 75 flip chip test boards (1 die size x 3 underfills x 25 samples per combination) were assembled at the CAVE SMT Line at Auburn University. In each assembly, the three-dimensional die surface stresses have been recorded during underfill cure, and after underfill cure (room temperature).

In the second part of this work, the silicon die stresses occurring in flip chip assemblies have been characterized and modeled at extremely low temperatures. Stress measurements have been made down to -180 $^{o}$C using test chips incorporating piezoresistive sensor rosettes. The obtained stress measurement data have been correlated with the predictions of nonlinear finite element models. A microtester has been used to characterize the stress-strain behavior of the solder and underfill encapsulant from -180 to 150 $^{o}$C to aid in this modeling effort.

In the third part of this work, the stress variations occurring during thermal cycling from -40 to +125 $^{o}$C have been characterized. These measurements have been correlated with the delaminations occurring at the die passivation to underfill interface measured using C-mode Scanning Acoustic Microscopy (C-SAM). With this approach, the stress distributions across the chip, and the stress variations at particular locations at the die to underfill interface have been interrogated for the entire life of the flip chip assembly. In order to correlate the stress changes at the sensor sites with delamination onset and propagation, CSAM evaluation of the test assemblies was performed after every 125 thermal cycles.

A total of 75 flip chip assemblies with 3 different underfills have been evaluated. For each assembly, the complete histories of three-dimensional die surface stresses and delamination propagation have been recorded versus the number of thermal cycles. The stress histories that lead to delamination initiation for each underfill encapsulant, and the variation of the stresses that occur before and during delamination propagation have been identified. The progressions of stress and delamination have been mapped across the entire surface of the die, and a series of stress/delamination videos have been produced. One of the most important discoveries is that the shear stresses occurring at the corners of flip chip die have been demonstrated to be a suitable proxy for prognostic determination of future delamination initiations and growth. Thus, shear stress sensors have great potential as health-monitoring devices in flip chip packaging.

In the fourth and final part of this work, die stress characterization was performed in flip chip assemblies utilizing a new low expansion coefficient laminate material. The new substrate material is a hybrid laminate formed using a combination of standard glass fiber reinforced resin outer layers (FR-4), with a carbon fiber reinforced resin core layer. The carbon fiber based central core (STABLCOR) features both high stiffness and high thermal conductivity, as well as near zero thermal expansion coefficient. Because of the extremely low expansion coefficient of the carbon fiber core and the bonded nature of the laminate, the surface CTE of the hybrid laminate PCB stack-up is typically in the range of 2.0-4.0 ppm/$^{o}$C over the temperature range of -55 to 150 $^{o}$C, which is much lower than the typical 13.0-20.0 ppm/$^{o}$C seen with standard FR-4 based laminates. In addition, the high stiffness of the carbon fiber based core can help reduce PCB warpage issues, as well as vastly improve the net heat conduction characteristics of the PCB substrate

FC200 and FC400 flip chip test die were packaged on the low expansion laminates, and the die surface stresses were measured throughout the assembly process. Die stress measurements have been made during underfill cure, and at room temperature after final assembly. The results have been compared to those from analogous FR-406 substrate assemblies. Significant stress reductions have been observed when using the low expansion coefficient laminate.

# CHAPTER 2

# LITERATURE REVIEW

Structural reliability of electronic packages has become an increasing concern for a variety of reasons including the advent of higher integrated circuit densities, power density levels, and operating temperatures. Electronic packaging typically involves several thermal and mechanical processes and also many different kinds of materials. As electronic packages are comprised of dissimilar materials, the assembly and operation reliability issues are often present due to the coefficient of thermal expansion (CTE) mismatch between these materials. Due to the CTE mismatch, mechanical stresses are usually built in at virtually every stage of manufacture or during application. These stresses may cause degradation of device characteristics and failure of the interconnections, cracking of the die or package, etc. Thus, die stress evaluation is a major concern for insuring reliability of packages.

Dale and Oldfield [1] addressed stress generation in packaging processes such as wafer preparation, oxidation, diffusion, metalization, die and wire bonding, encapsulation, and curing. Lau [2] has discussed several problems associated with stress, including package cracking, wire damage, and thin film cracking on the die. Stress generation mechanisms were also discussed with respect to die attachment, encapsulation, surface mounting processes, and bending during application. Nguyen [3] has presented current reliability issues involved with typical postmold IC packages. One of the four major concerns is stress. Issues such as stress mechanisms and measurement were reviewed. Mechanical and electrical failures due to induced thermal stresses have been documented since the 1970's. Within a plastic package, out-of-plane shear stresses act on the chip surface with the traction direction toward the center of the chip, causing deformation of the die metalization. With chips coated with passivation glass, these deformations can cause passivation cracking. Microcracks in the plastic encapsulant or delamination at the die-encapsulant interface promote metal deformation, since they reduce the restrictions on plastic movement at the chip surface [4-8]. Isagawa, et al. [4] observed the deformation of aluminum metalization during thermal shock tests of plastic packages. The deformations were related to encapsulant properties, chip size, test temperature range, etc. Thomas [5] performed thermal cycling on molded packages containing unpassivated test chips. Lundström and Gustafsson [6], Lesk, et al. [7], and Edwards, et al. [8] also described metal shift or damage during thermal shock or thermal cycling tests.

Shear stresses are heavily concentrated at the corners and edges of the silicon die, and can result in thin film brittle passivation cracking or interlayer dielectric film cracking [9-15]. Okikawa, et al. [9-10] and Shirley, et al. [11] presented studies of thin film cracks due to thermal stresses. Foehringer, et al. [12] described a model that explained the interactions among the key variables related to thin film cracking. The effort to model the failure rate as a function of environmental stress severity was done by Blish and Vaney [13]. A special test chip was designed by Gee, et al. [14] to detect thin film cracking in PLCC packages with various pin counts, die sizes, thermal cycling numbers, etc. Inayoshi [15] demonstrated that stresses could disrupt the chip passivation, permitting moisture to penetrate through to the underlying aluminum metalization causing corrosion.

Delamination at the chip-encapsulant interface is believed to be the result of critical shear stresses on the die surface, and usually occurs during reliability tests, such as temperature cycling and Highly Accelerated Stress Testing (HAST). The delamination typically starts at the corners of the silicon die, and proceeds toward the chip center [16-23]. Nishimura, et al. [16] confirmed the delamination at the die-encapsulant interface using ultrasonic inspection techniques. Doorselaer, et al. [17] revealed the relation between electrical failures and delamination. Moore, et al. [18-20] applied C-SAM (C-Mode Scanning Acoustic Microscopy) technique to inspect delamination and cracks in IC packages. The evaluations were performed with various molding compounds, lead frame finishes, and die surface conditions. A comparison of delamination effects between temperature cycling and HAST tests was carried out by van Gestel, et al. [21-22]. Delaminations at the chip-encapsulant interface of 240 pin QFP packages were also found by Zou, et al. [23] even before reliability tests. Interfacial adhesion is one of the key factors to achieve delamination free packaging. Nguyen, et al. [24-26], conducted evaluations of various interfaces in plastic packages.

The occurrence of microcracks in the encapsulant is another serious reliability issue with plastic packages. The microcracks usually initiate at the chip edges, then propagate into the encapsulant at roughly a $135^{o}$ angle from the chip surface [5].

Nishimura, et al. [16, 27] performed thermal cycling between –55 and 150 $^{o}$C on Dual Inline Packages. Package cracking was observed as a function of the number of temperature cycles for different encapsulant and lead frame materials. The presence of microcracks in the encapsulant dramatically changes the stress distribution in a package. A tentative model was proposed by Schroen, et al. [28] to describe the stress relief and oscillation measurements during temperature cycling tests. The stresses causing the cracks are so high that may cut through silica filler particle [7]. To avoid high stress, suggestions such as development of plastic encapsulant with low CTE, low elasticity modulus, high strength, optimized plastic curing processes, and prevention of moisture absorption, have been proposed or practiced [28-31].

Large residual stresses introduced during packaging procedures, especially die attachment and encapsulation steps, can also cause die cracks. Since silicon is an extremely brittle material, minor surface flaws can act as crack starters in the presence of tensile stresses [32, 33]. Improper dicing of silicon wafers is another contributor to die cracking [1].

Electronic characteristic changes occur in IC chips due to mechanical stresses introduced by packaging processes. The resistivity of diffused resistor shifts due to piezoresistive effects so that piezoresistive stress sensors can be developed [34-36]. Other device characteristics shifts were also experimentally studied, or observed in actual plastic packaged devices [37-50]. Using the relations between MOS drain current change and the applied mechanical stress, stress sensors based on piezoresistive field effect transistors (PIFET's) and bipolar transistors were proposed and designed [43-50].

In addition, Mian, et al. have studied the sensitivity of the resistance of Van der Pauw structures to applied stress [51-52]. Frutt, et al. [53] have discussed techniques for minimization of the piezoresistive effect for integrated p-type implanted resistors.

To understand the stress developed in plastic packages during packaging processes, reliability tests, and actual applications, researchers have performed stress analyses using analytical, numerical, and experimental methodologies. Suhir [54-57] and Liew, et al. [58] suggested analytical methods for evaluation of the interfacial stresses in bimetal thermostats based on elementary beam (or long-and-narrow plate) theory. Tay, et al. [59-61] discussed the mechanics of interfacial delamination, and presented analytical methods to describe moisture-induced delamination growth during solder reflow. These analytical models were correlated with experimental observations to help understand failure mechanisms. Miura, et al. [62] also discussed the temperature distribution in the IC plastic package during solder reflow process.

Finite element simulations provide useful insight into the stress distributions produced in plastic packages during die attachment, encapsulation, and reliability tests. Various package configurations, packaging material combinations, and conditions related to package processes and reliability tests can be investigated by means of finite element methods [63-76]. In early finite element modeling, Groothuis, et al. [63] and Pendse [64] displayed the effects of material choices and structure changes on stress variation within a DIP package. Kelly, et al. [65-68] demonstrated how thermal stresses are developed within a plastic package, and suggested innovations in processes such as a side buffer of soft material, etc. Mertol [69] studied the thermal stresses in a high pin count PQFPs.

In two-dimensional finite element simulations of plastic packages, plane strain analyses would be more suitable for prismatic bodies (DIPs and SOPs), while packages with square features (PLCC, PQFP) could be represented by coaxial rings using axis-symmetric analyses [3]. Van Gestel, et al. [70] used three layers of special interface elements to simulate delamination behavior when plastic packages were subjected thermal cycling. Sweet, et al. [71], applied a linear viscoplastic model to predict die surface stresses. Effects of various delamination conditions to die surface stress distributions were also evaluated. Liu, et al. [72-73] built finite element models to predict thermal deformation and delamination in PQFP's and made comparison with moiré interferometry testing data. Yeung, et al. [74] and Park, et al. [75] used finite element analysis to evaluate the thermal residual stress in a PQFP assuming viscoelastic stress-strain behavior of the molding compounds.

Analytical solutions are difficult to achieve for complex packaging configurations. Although the finite element method (FEM) is a reliable modeling tool to predict stress distributions within packages, the computational results have to be verified by experimental analysis. In addition, finite element simulations are limited by the availability of packaging material properties, accurate understanding of packaging processes, and other assumptions and approximations. Thus, it is desirable to develop experimental stress analysis methods for electronic packages. Bastawros, et al. [76], Han and Guo [77], and Liu, et al. [72-73] to measure thermal deformations within packages applied moiré interferometry. Shadow moiré methods were effective in evaluating the warpage of packages [78-79]. Some other testing and measurement techniques were reviewed by Guo and Sarihan [80].

The piezoresistive effect is caused by the change of resistivity of semiconductors as a function of applied stresses. Smith [81] first proposed to use the piezoresistive behavior of semiconductors for stress and strain measurements. Since then, Tufte and Stezer [82] and Suhling, et al. [83-84] have investigated the temperature dependence of piezoresistive coefficients of silicon or germanium. Kanda [85] represented the piezoresistive coefficients graphically. Yamada, et al. [86] addressed the nonlinearity of the piezoresistive effect. Dally and Riley [87] discussed the properties and performance characteristics of semiconductor strain gauges. Bittle, et al. [35, 88] derived the detailed theory for silicon piezoresistive sensors, and Kang [89] developed piezoresistive theory for silicon on various wafer planes and for silicon carbide.

Piezoresistive sensors are a powerful tool for experimental structural analysis of electronic packages. The sensors are resistors that are conveniently fabricated into the surface of the die using current microelectronic technology, and are capable of providing non-intrusive measurements of surface stress state on a chip even within encapsulated packages [90-93]. A comprehensive review of piezoresistive sensor issues has been given by Sweet [34].

Several investigators have used stress test chips based on piezoresistive sensors to examine die stresses in plastic encapsulated packages. In early studies, Edwards and co-workers [8, 28, 94-95], Groothuis, et al. [63], and van Kessel, et al. [32] used (100) silicon test chips based on 0-90 two-element sensor rosettes to examine stresses in small pin count packages. Resistance changes of sensors during thermal cycling and pressure cooker environment tests were compared [28]. Die stress studies were utilized to direct the selection of packaging materials and the control of packaging processes [94-95]. The mechanism of structure failures were also investigated [32, 42, 63].

Gee and co-workers [96-98] have mapped die surface stress distributions using (111) test chips containing an array of four element 0-±45-90$^o$ sensor rosettes. In these studies, tests were also performed to understand the effects of package geometrical parameters and thermal cycling on the die stress levels. Further investigations with these chips were performed on 40 pin Dual in-Line packages (DIPs) by van Gestel and co-workers [99-100]. In addition, Lead frames and molding compounds were studied by Lundström, et al. [6] using a (111) silicon test chip with p-type four-element rosettes. Temperature dependent stress state measurements after die attachment and encapsulation were examined by Natarajan, et al. using n-type (100) silicon test chips [101].

Miura, et al. [36, 39, 102-105] have used (100) test chips incorporating four-element dual-polarity rosettes (0-90$^o$ n-type resistors and ±45$^o$ p-type resistors) to characterize thermally-induced die stresses in DIPs. Their sensor rosette design was the first capable of measuring the out-of-plane normal stress perpendicular to the die surface. In one of these studies, the effects of internal structure on plastic packaging reliability were explored [104]. The level of die stress was studied as a function of temperature changes and thermal cycling test [36]. Delamination at the interface of die/encapsulant was also correlated to varied stress magnitudes [39]. Zou, et al. [106] have recently used (100) test chips based on a similar rosette with reversed doping polarities (0-90$^o$ p-type resistors and ±45$^{\circ}$ n-type resistors) to characterize the stresses in plastic leaded chip carrier (PLCC) packages that were encapsulated using several different molding compounds. Sweet and co-workers [34, 71, 107-109] have used the (100) silicon Sandia ATC-04 test chip to investigate liquid encapsulation of integrated circuit die mounted directly on ceramic substrates, and to study 160 pin quad flat packs (QFP's). The ATC-04 contains a multiplexed array of sensor rosettes. Each dual-polarity rosette contains eight resistors (0-±45$^{\circ}$-90$^{\circ}$ orientations for both p-type and n-type resistors). An improved third generation version of the Sandia test chip has recently been designed and prototyped [110]

Other experimental studies using test chips with piezoresistive stress sensors can be found in the literature [111-123]. Skipor, et al. [111] compared both stress measurements using test chips and displacement measurements using moiré interferometry with FEM calculations for 64 pin TQFP and 68 pin PLCC packages. Lo, et al. [112-113] and Bossche, et al. [114-115] described the design, fabrication, and calibration of their own stress test chips. Ducos, et al. [116] presented the in-situ stress measurements during package assembly. Nysaether, et al. [117-118] examined the thermally induced stresses in glob-on-top pressure sensor samples. Rey, et al. [119] associated creep of the solder joints in leaded components with stress measurements in the silicon die. They used experimental data together with the FEM simulations to find a mathematical model for creep in the solder. Palmer, et al. [120] attempted to measure the stress variation during plastic package molding. Sensor resistance measurements for test chips assembled into TBGA, MBGA, and ViperBGA$^{\text{TM}}$ packages were made by Thomas, et al. [121]. The die stresses induced in TO220 packages using different mold compounds has been investigated using test chips by Caruso, et al. [122]. Another test chip for studing packaging induced stress has been developed by Jia, et al. [123].

Mayer, et al. [124-126] have measured in-situ transient stresses during ball bonding using integrated piezoresistive microsensors. In their studies, the devices were fabricated using a commercial CMOS process, exploiting p plus diffusion as the piezoresistive sensing material. The resistors were fabricated with the commercial 2 μm CMOS process alp2lv of EM Microelectronic-Marin SA, Switzerland. The NMOS source/drain diffusion with a sheet resistance of approximately 21 Ω was used for the resistors [126]. The design and fabrication process of piezoresistive sensors for packaging stress measurements were also discussed by Lwo, et al. [127-128]. In these studies, test chips with both p-type and n-type piezoresistive stress sensors, as well as a heat source, were designed, and then manufactured by a commercialized foundry so that the uniformity of the test chips was expected. Both temperature and stress calibrations were performed through a special designed MQFP (Metal Quad Flat Package) and four-point bending (4PB) structure, respectively.

Stresses developed on the silicon surface due to encapsulation and molding process have also been discussed in several other publications [129-136]. van den Bogert, et al. [129] have analyzed a bilayer beam structure to determine the relationship between the material properties of the molding compound and the generated thermal stresses. Three commercial molding compounds were studied. The stress levels were determined by the thermal expansion difference between the molding compound and silicon, the moduli, and the amount of relaxation that occurs during the experiment due to the viscoelastic nature of the molding compound. Kitoh, et al. [130] measured the internal stresses produced in three cylinder models simulating the structures of epoxy resin encapsulated electronic components by using strain gages. The mechanism of stress generation was very different between an open type structure that has one surface of the resin free, and a closed type that does not. Slattery, et al. [131] described the use of finite-element techniques and piezoresistive strain sensors to determine package stress levels. The effect of delaminations at the interfaces of the package materials was also discussed, and the scanning acoustic microscope was introduced as a complimentary tool to identify stress-related defects in plastic packages. Mei, et al. [132] developed a nonlinear finite element model for predicting the deformation, stress, and fracture behavior of delaminated plastic packages induced by mechanical and hygro-thermal loads. The model consists of a sequentially coupled hygro-thermo-mechanical analysis considering moisture absorption, evaporation and interface contact and fracture analysis. Mixed mode fracture modes were discussed.

An analysis of environment induced stresses in silicon sensors has been performed by Voloshin, et al. [133-134]. In these studies, an experimental technique, Digital Image Analysis Enhanced Moiré Interferometry (DIAEMI), was used to measure the in-situ out-of-plane displacements of the die due to the die-attachment process. This information was related to the residual stresses in the die. Several test die, with and without coating, were prepared and two different bonding materials, “low-stress” and "high-stress”, were used for analysis of the induced stresses. The initial and final (after die-attach) surface contour patterns of the die were observed and recorded. Out-of-plane displacements of the die were obtained and induced stresses were calculated by a hybrid finite element method.

Bjorneklett, et al. [135] measured the stress induced during the chip attachment process using integrated piezoresistive strain sensors on test chips. The stress was found to be different for different adhesives. The effect of temperature cycling (i.e., stress cycling) was investigated by measuring the thermal resistance between chip and substrate. An increasing thermal resistance that strongly depends on the mismatch in thermal expansion was found. The wear-out mechanisms were crack growth and detachment. Alpern, et al. [136] used Scanning Acoustic Microscopy (SAM) to evaluate the degradation of adhesion on a blown up sample, i.e., a Si-beam coated only on the passivated side with the molding compound under consideration.

In recent applications of piezoresistive stress sensors, mechanical stresses in epoxy underfilled flip-chip on board packages were studied [137-147]. In-situ flip-chip assembly mechanical stress measurements using piezoresistive test chip were first reported by Peterson and co-workers [137]. In that work, die stresses were evaluated for several underfill materials. Nysaether, et al. [138] and Palaniappan, et al. [139] investigated the impact of curing parameters on the die stresses induced in flip-chip assembly processes. In reference [138], stress measurements were presented as a function of temperature when the underfill was cured at temperatures of 85 $^{o}$C, 120 $^{o}$C, and 150 $^{o}$C. In reference [139], the residual die stresses were found to be strongly dependent on several underfill properties including CTE, storage modulus, $T_g$, and ultimately the underfill cure process. Palaniappan, et al. [140-141] reported on the effects of the choice of encapsulation material on the stresses during underfill cure and also made preliminary stress measurements during thermal cycling.

Measurement of die stresses in flip chip on laminate assemblies was performed by Rahim, et al. [142-144]. In these flip chip studies, the authors have investigated the mechanical stresses present on the backside (top side) [142] and the device side (bottom side) [143-144] of the die at each stage of the flip chip assembly process. The die stress variations were observed during underfill curing, and the room temperature die stresses in the final cured assemblies have been compared for several different underfill encapsulants. Finally, stress variations have been monitored in the assembled flip chip die as the test boards were subjected to slow temperature changes from -40 to +150 $^{o}$C. Schwizer, et al. [145], reported on the latest member of a test chip family for packaging process characterization, containing a novel flip-chip microsensor that can measure forces in all three directions, acting on each of its solder balls.

Several researchers have studied the effect of thermomechanical properties of underfill and underfill technology on flip chip packages reliability [146-156]. Qi, et al. [146] examined the manufacturing steps required for flip chip on laminate assembly and the impact of these new materials on production cycle time. Adhesion testing, liquid-to-liquid thermal shock, and thermal cycling have been used to examine the reliability of the underfilled flip chip on laminate. New underfill materials provided a cost-effective option for flip chip-on-laminate applications. Wang, et al. [147] have compared different types of reworkable underfill formulations as well as the methodologies for developing such materials. Furthermore, generic concepts for new underfilling processes including no-flow, molding, and wafer-level were introduced. Okura, et al. [148] have investigated the effect of thermo-mechanical properties of underfill, such as coefficient of thermal expansion (CTE) and stiffness (Young's modulus), on reliability of flip chip on board (FCOB) assemblies under thermal cycling stresses.

Luo, et al. [149] used the three-liquid-probe method to investigate the surface properties of solder mask and different passivation materials including benzocyclobutene (BCB), polyimide (PI), silicon oxide ($SiO_2$), and silicon nitride ($Si_3N_4$). Dai, et al. [150] characterized underfill materials for flip chip packages. Chen, et al. [151] have investigated the effects of underfill on thermo-mechanical behavior of two types of flip chip packages with different bumping size and stand-off height under thermal cycling. Both experimental testing and two-dimensional finite element simulations were used. Viscoelasticity of the underfill and viscoplasticity of the solder were considered in the simulations.

Ernst, et al. [152-153] have studied the effect of curing induced residual stresses on flip chip failure. In their studies, cure-dependent material parameters were determined using experimental data from unit-step relaxation tests performed during cure. Yang and co-workers [154-155] have studied and investigated the effects of cure-dependant underfill properties on flip chip failures. In these studies, a cure-dependent viscoelastic constitutive relation was applied to describe the curing process of epoxy underfill in flip chip on board (FCOB) assemblies. The chemical shrinkage of the epoxy underfill during the curing process was applied via incremental initial strains. Thus, the stress and strain build-up, caused by the simultaneous increase in stiffness and shrinkage during the curing process, were simulated. Islam, et al. [156] have characterized the stress-strain curves and elastic modulus of underfill as a function of temperature by uniaxial testing using a microscale tension-torsion testing machine.

Die cracking is a major failure mode observed during flip chip on laminate assembly or during subsequent package thermal cycling reliability tests [157-161]. Hu, et al. [157] discussed die cracking criteria for flip chip on board assemblies. Their analysis suggested that a defect size of more than 35 microns will results in die cracking failure after solder reflow. The numerical results also revealed that a good tolerance of defects can be achieved by limiting the board thickness to be less than twice that of the die. Mercado, et al. [158] completed an extensive finite element analysis to investigate die edge cracking. In their study, a fracture mechanics approach was used to evaluate the effect of various package parameters on die edge initiated fractures. Chengalva [159] has investigated the problem of flip chip die cracking from an industry prospective with two separate approaches. The first involved the determination of the intrinsic strength of production-intent flip chip die using bend testing. The second involved the determination of stress levels in flip chip assemblies during manufacture and service using simulations.

Michaelides, et al. [160] have developed an integrated process reliability modeling methodology to determine the stresses at the backside of the die during underfill cure and subsequent thermal cycling. Based on underfill cure and thermal cycling models for specific cases, the critical flaw size to induce catastrophic die cracking has been calculated using linear-elastic fracture mechanics. Shim, et al. [161] have performed a parametric study to understand the influence of die and substrate thickness, and metal attachment on die cracking. It was found that the combination of thinner die and thicker substrate led to the best results.

Hanna, et al. [162] have reported on a theoretical and experimental study that was carried out to understand the development and evolution of stresses on the active side of flip chip die during thermal cycling. Finite element stress analysis of the test vehicle after underfill cure and subsequent thermal cycling was performed. Peterson, et al. [163] have performed a study on flip chip BGA packages using the ATC4.2 test chip. In their work, the BGA substrates employed 'build-up' dielectric layers containing micro-vias over conventional fiberglass laminate cores. Experimental data from die stress sensors and die bending measurements were correlated to closed-form and finite element calculations. Through use of bounding conditions in the simulations, cracking and delamination failures were associated with debonding of the underfill fillet from the die edge that caused stresses to shift to weaker areas of the package.

Theoretical analysis by Suhling and co-workers [35, 90-93, 164] has established that properly designed sensor rosettes on the (111) silicon wafer plane have several advantages relative to sensors fabricated using standard (100) silicon. Optimized rosettes on (111) silicon can be used to measure the complete state of stress (six stress components) at a point on the top surface of the die, and offer the unique capability of measuring four temperatures compensated combined stress components. Suhling, et al. [91, 165] have used the (111) silicon BMW-1 test chip to make the first measurements of the complete state of stress (six stress components) on the surface of an encapsulated die.

The BMW-1 chip incorporates dual-polarity eight element rosettes (0-±45$^o$-90$^o$ orientations for both p-type and n-type resistors). In these studies, stresses were measured in chip on board (COB) packages where the test chips were bonded to FR-4 substrates and over-molded using “glob-top” liquid encapsulant. In addition to the in-plane stress components measured in the above studies, the first measurements of out-of-plane (interfacial) shear stresses at the die to encapsulant interface were recorded. The majority of the measurements were made at room temperature, but a demonstration of the variation of the die surface stresses with package temperature was also made. Results were correlated with the predictions of finite element simulations.

The (111) silicon BMW-1 test chip was also applied by Zou, et al. [23] to detect delamination at the interface of the die and encapsulant. The stress distributions on the die surface in delaminated packages were compared with those in non-delaminated packages. The (111) silicon BMW-2 test chip was utilized by Zou, et al. [166-170] to characterize die surface stresses in various packaging configurations. The characterization of transient die stresses throughout the cure cycles of several Chip on Board (COB) encapsulants was performed [166-167]. High temperature die attachment adhesives were evaluated during thermal cycling and thermal aging tests in 281 pin Ceramic Pin Grid Array (CPGA) packages [168-169]. A comparison of die level stresses in COB packages processed with convection and variable frequency encapsulant curing was also made [170]. The experimental results were correlated to FEM simulations, and reasonable agreements were obtained [166-170].

Several researchers have studied delamination and interfacial stresses in flip chip assemblies during thermal cycling reliability tests [171-179]. Fan, et al. [171] have established a criterion for delamination initiation under thermal cycling. The maximum circumferential stress criterion was adopted in their work. The impact of the underfill failures on solder joint reliability was also discussed. Mercado, et al. [172] have utilized a fracture mechanics approach to evaluate the impact of interface delamination on package reliability. In their work, interfacial fracture mechanics was coupled with finite element analysis to determine the critical interface fracture parameters. The proposed methodology was validated against analytical solutions and a flip chip PBGA package with underfill delamination was studied. The effects of temperature, initial delamination length, package geometry and materials on the fracture parameters were evaluated.

Cheng, et al. [173-174] have analyzed the delamination propagation behavior at the interface between chip and underfill both by experimental measurement and finite element simulation. In their study, the delamination propagation rates at the chip-underfill interface have been measured by using C-SAM inspection of flip chip assemblies under thermal cycle loading. Pang, et al. [175] have investigated a flip chip assembly with underfill delamination resulting from thermal cycling by using the finite element method and interfacial fracture mechanics. Numerical evaluations of the mixed mode stress intensity factors and mode mixity parameter for interface cracks located at the silicon/underfill and silicon/FR4 interfaces were carried out in this study. Zhai, et al. [176] have studied the effects of various design variables including underfill material properties, fillet dimensions, and die overhang on underfill delamination fracture parameters.

Jackshick, et al. [177] have used optical microscopy to observe delamination propagation rates with glass die, while Hirohata and co-workers [178] have introduced a new mechanical fatigue test method for predicting the delamination resistance of underfill interfaces. Nguyen, et al. [179] have studied the effects of underfill fillet configuration on flip chip reliability. In their study, configurations with and without fillets were made with different underfills for flip chip die on ceramic substrates. The packages were thermally cycled, electrically tested, and scanned with acoustic microscopy to check for interfacial delaminations. Finite element models were also generated for the different configurations and materials. The results indicated that the presence of fillets is equally important as the selection made for the underfill material to achieve the best thermal cycling performance.

Stress test chips need to be calibrated to obtain the piezoresistive coefficients required for the stress calculation. A four-point bending calibration procedure is typically used. Details of this method are discussed by Beaty, et al. [180], Bittle, et al. [35, 88], Suhling, et al. [83-84, 93], Jaeger, et al. [181-185], and van Gestal [100]. Cordes [186] and Suhling, et al. [187-188] developed a wafer-level calibration technique. A hydrostatic calibration method for (111) silicon test chips was developed and applied by Kang [89], and Suhling, et al. [93, 189]. Lwo, et al. [190] designed and fabricated a simple assembled structure for calibration.

An analysis of the errors associated with the design and calibration of piezoresistive stress sensors in (100) silicon has been made by Jaeger, et al. [191-192]. The significance of thermally induced errors in the calibration and application of silicon piezoresistive stress sensors was also demonstrated by Jaeger, et al. [185]. A study on optimal temperature compensated piezoresistive stress sensor rosettes was presented by Suhling, et al. [164].

# CHAPTER 3

# REVIEW OF PIEZORESISTIVITY THEORY

## 3.1 General Resistance Change Equations

An arbitrarily oriented silicon filamentary conductor is shown in Figure 3.1. The unprimed axes $x_1$ = [100], $x_2$ = [010], and $x_3$ = [001] are the principal crystallographic directions of the cubic (m3m) silicon crystal. The primed coordinate system is arbitrarily rotated with respect to this unprimed crystallographic system. For this conductor, the normalized change in resistance can be expressed in terms of the off-axis (primed) stress components using:

$$\begin{aligned}\frac{\Delta R}{R} &= (\pi'_{1\alpha}\sigma'_{\alpha})l'^2 + (\pi'_{2\alpha}\sigma'_{\alpha})m'^2 + (\pi'_{3\alpha}\sigma'_{\alpha})n'^2 \\ &+ 2(\pi'_{4\alpha}\sigma'_{\alpha})l'n' + 2(\pi'_{5\alpha}\sigma'_{\alpha})m'n' + 2(\pi'_{6\alpha}\sigma'_{\alpha})l'm' \qquad (3.1) \\ &+ [\alpha_1 T + \alpha_2 T^2 + \ldots \quad ]\end{aligned}$$

Where $\pi'_{\alpha\beta}\ (\alpha,\beta = 1, 2, \ldots, 6)$ are the off-axis temperature dependent piezoresistive coefficients, $\alpha_1, \alpha_2, \ldots$ are the temperature coefficients of resistance, $T = T_m - T_{ref}$ is the difference between the measurement temperature and reference temperature (where the unstressed resistance R is measured), and $l', m', n'$ are the direction cosines of the conductor

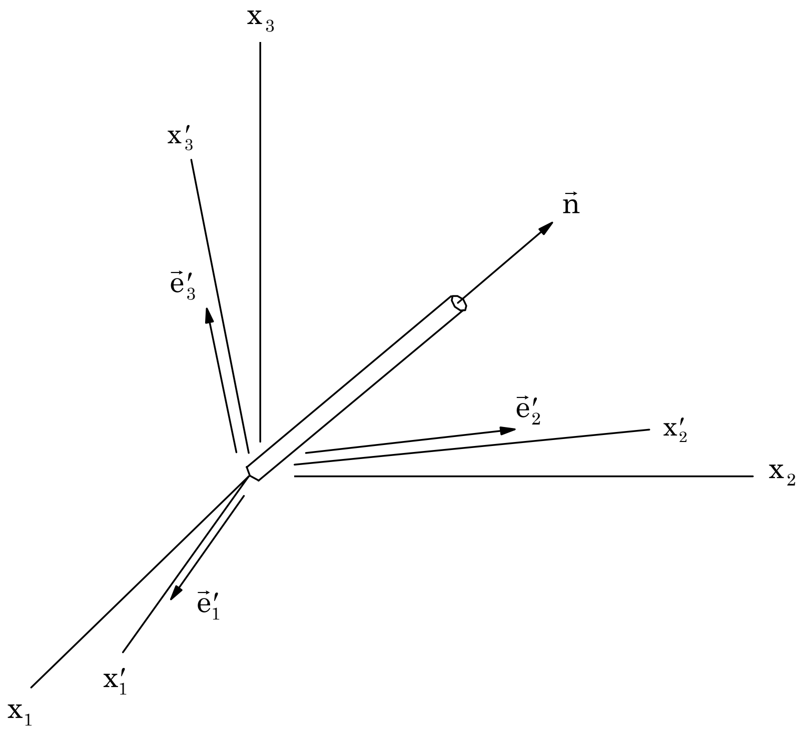

$x_3$
$x'_3$
$\vec{n}$
$\vec{e}'_3$
$\vec{e}'_2$
$x'_2$
$x_2$
$\vec{e}'_1$
$x'_1$
$x_1$

Figure 3.1 - Filamentary Silicon Conductor

orientation with respect to the $x'_1, x'_2, x'_3$ axes, respectively [35, 89, 91, 164]. In Eq. (3.1) and future indicial notation expressions, the summation convention is implied for repeated indices, and reduced index notation has been used for the stress components:

$$\begin{aligned} \sigma'_1 &= \sigma'_{11}, \ \sigma'_2 = \sigma'_{22}, \ \sigma'_3 = \sigma'_{33} \\ \sigma'_4 &= \sigma'_{13}, \ \sigma'_5 = \sigma'_{23}, \ \sigma'_6 = \sigma'_{12} \end{aligned} \tag{3.2}$$

The 36 off-axis piezoresistive coefficients in Eq. (3.1) are related to the three unique on-axis piezoresistive coefficients $\pi_{11}, \pi_{12}, \pi_{44}$ (evaluated in the unprimed coordinate system aligned with the crystallographic axes) using the transformation

$$\pi'_{\alpha\beta} = T_{\alpha\gamma}\, \pi_{\gamma\delta}\, T^{-1}_{\delta\beta} \tag{3.3}$$

where

$$[\pi_{ij}] = \begin{bmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{bmatrix} \tag{3.4}$$

is the on-axis piezoresistive coefficient matrix, and

$$[T_{\alpha\beta}] = \begin{bmatrix} l_1^2 & m_1^2 & n_1^2 & 2\,l_1\,n_1 & 2\,m_1\,n_1 & 2\,l_1\,m_1 \\ l_2^2 & m_2^2 & n_2^2 & 2\,l_2\,n_2 & 2\,m_2\,n_2 & 2\,l_2\,m_2 \\ l_3^2 & m_3^2 & n_3^2 & 2\,l_3\,n_3 & 2\,m_3\,n_3 & 2\,l_3\,m_3 \\ l_1\,l_3 & m_1\,m_3 & n_1\,n_3 & l_1\,n_3 + l_3\,n_1 & m_1\,n_3 + m_3\,n_1 & l_1\,m_3 + l_3\,m_1 \\ l_2\,l_3 & m_2\,m_3 & n_2\,n_3 & l_2\,n_3 + l_3\,n_2 & m_2\,n_3 + m_3\,n_2 & l_2\,m_3 + l_3\,m_2 \\ l_1\,l_2 & m_1\,m_2 & n_1\,n_2 & l_1\,n_2 + l_2\,n_1 & m_1\,n_2 + m_2\,n_1 & l_1\,m_2 + l_2\,m_1 \end{bmatrix} \tag{3.5}$$

is the six by six transformation matrix whose elements are related to the direction cosines of the primed coordinate directions with respect to the unprimed coordinate directions. The inverse of this transformation matrix can be expressed as:

$$[T_{\alpha\beta}]^{-1} = \begin{bmatrix} l_1^2 & l_2^2 & l_3^2 & 2\,l_1 l_3 & 2\,l_2 l_3 & 2\,l_1 l_2 \\ m_1^2 & m_2^2 & m_3^2 & 2\,m_1 m_3 & 2\,m_2 m_3 & 2\,m_1 m_2 \\ n_1^2 & n_2^2 & n_3^2 & 2\,n_1 n_3 & 2\,n_2 n_3 & 2\,n_1 n_2 \\ l_1 n_1 & l_2 n_2 & l_3 n_3 & l_1 n_3 + l_3 n_1 & l_2 n_3 + l_3 n_2 & l_1 n_2 + l_2 n_1 \\ m_1 n_1 & m_2 n_2 & m_3 n_3 & m_1 n_3 + m_3 n_1 & m_2 n_3 + m_3 n_2 & m_1 n_2 + m_2 n_1 \\ l_1 m_1 & l_2 m_2 & l_3 m_3 & l_1 m_3 + l_3 m_1 & l_2 m_3 + l_3 m_2 & l_1 m_2 + l_2 m_1 \end{bmatrix} \qquad (3.6)$$

In Eqs. (3.5, 3.6), the direction cosines for the axes of the primed coordinate system are given by

$$[a_{ij}] = \begin{bmatrix} a_{11} & a_{12} & a_{13} \\ a_{21} & a_{22} & a_{23} \\ a_{31} & a_{32} & a_{33} \end{bmatrix} = \begin{bmatrix} l_1 & m_1 & n_1 \\ l_2 & m_2 & n_2 \\ l_3 & m_3 & n_3 \end{bmatrix} \qquad (3.7)$$

where

$$a_{ij} = \cos(x'_i,\ x_j) \qquad (3.8)$$

When the primed axes are aligned with the unprimed (crystallographic) axes, the transformation matrix in Eq. (3.5) reduces to the 6 x 6 identity matrix. Thus, Eq. (3.3) reduces to

$$\pi'_{\alpha\beta} = \pi_{\alpha\beta} \qquad (3.9)$$

and Eq. (3.1) simplifies to

$$\begin{aligned}\frac{\Delta R}{R} &= [\pi_{11}\sigma_{11} + \pi_{12}(\sigma_{22} + \sigma_{33})]l^2 + [\pi_{11}\sigma_{22} + \pi_{12}(\sigma_{11} + \sigma_{33})]m^2 \\ &\quad + [\pi_{11}\sigma_{33} + \pi_{12}(\sigma_{11} + \sigma_{22})]n^2 + 2\pi_{44}[\sigma_{12}lm + \sigma_{13}ln + \sigma_{23}mn] \\ &\quad + [\alpha_1 T + \alpha_2 T^2 + \ldots]\end{aligned} \tag{3.10}$$

where l, m, n are the direction cosines of the conductor orientation with respect to the unprimed (crystallographic) axes. Eq. (3.10) demonstrates that the resistance change of an arbitrarily oriented silicon resistor depends on all six stress components. As will be shown below, resistive sensor rosettes can be fabricated in certain silicon wafer planes which take advantage of this property and allow several stress components to be extracted from monitoring resistance changes.

### 3.2 Resistance Change Equations for Silicon Wafer Planes

For a given wafer orientation, Eq. (3.1) can be used to obtain the resistance change equation for an arbitrarily oriented in-plane resistor. In the current microelectronics industry, it is most common for silicon devices to be fabricated using (100) silicon wafers. A general (100) silicon wafer is shown in Figure 3.2. The surface of the wafer is a (100) plane, and the [001] direction is normal to the wafer plane. The axes of the natural wafer coordinate system $x_1' = [110]$ and $x_2' = [\bar{1}10]$ are parallel and perpendicular to the primary wafer flat. To use Eq. (3.1), the off-axis piezoresistive coefficients in the primed coordinate system must be evaluated using Eq. (3.3) by substitution of the unprimed values in Eq. (3.4) and the appropriate direction cosines.

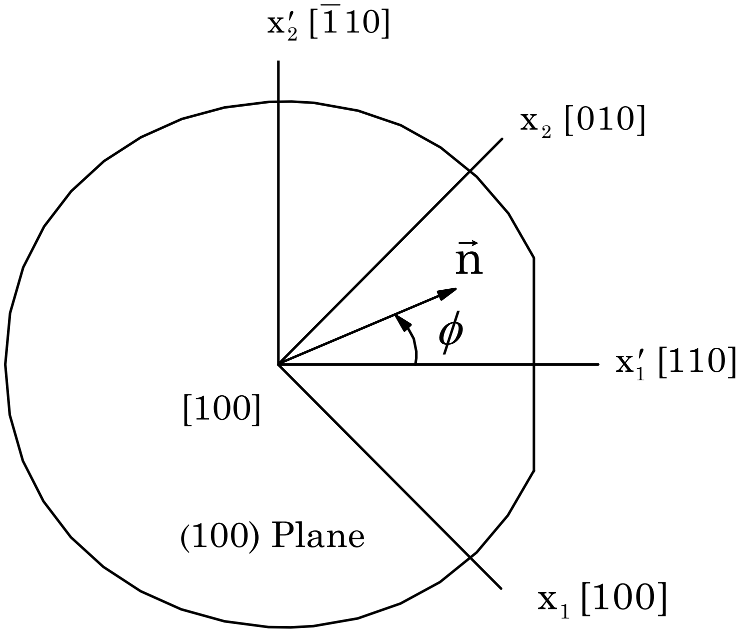

$x_2'$ $[\bar{1}10]$
$x_2$ $[010]$
$\vec{n}$
$\phi$
$x_1'$ $[110]$
$[100]$
(100) Plane
$x_1$ $[100]$

Figure 3.2 - (100) Silicon Wafer

For the unprimed and primed coordinate systems shown in Figure 3.2, the direction cosines are:

$$[a_{ij}] = \begin{bmatrix} \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ -\frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 1 \end{bmatrix} \tag{3.11}$$

Substitution of the off-axis piezoresistive coefficients calculated in the manner described above into Eq. (3.1) yields

$$\begin{aligned} \frac{\Delta R}{R} &= \left[ \left( \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \right) \sigma'_{11} + \left( \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) \sigma'_{22} \right] \cos^2\phi \\ &+ \left[ \left( \frac{\pi_{11} + \pi_{12} - \pi_{44}}{2} \right) \sigma'_{11} + \left( \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \right) \sigma'_{22} \right] \sin^2\phi \\ &+ \pi_{12}\sigma'_{33} + (\pi_{11} - \pi_{12})\sigma'_{12}\sin 2\phi + [\alpha_1 T + \alpha_2 T^2 + \ldots] \end{aligned} \tag{3.12}$$

where

$$l' = \cos\phi \quad m' = \sin\phi \quad n' = 0 \tag{3.13}$$

has been introduced, and $\phi$ is the angle between the $x'_1$-axis and the resistor orientation. Equation (3.12) indicates that the out-of-plane shear stresses $\sigma'_{13}$ and $\sigma'_{23}$ do not influence the resistances of stress sensors fabricated on (100) wafers. This means that a sensor rosette on (100) silicon can at best measure four of the six unique components of the stress tensor. All three of the unique piezoresistive coefficients for silicon $(\pi_{11}, \pi_{12}, \pi_{44})$ appear in Eq. (3.12). These parameters must be calibrated before stress component values can be extracted from resistance change measurements.

The other common silicon crystal orientation used in semiconductor fabrication is the (111) surface. A general (111) silicon wafer is shown in Figure 3.3. The surface of the wafer is a (111) plane, and the [111] direction is normal to the wafer plane. The principal crystallographic axes $x_1 = [100]$, $x_2 = [010]$, and $x_3 = [001]$ do not lie in the wafer plane and have not been indicated. As mentioned previously, it is convenient to work in an off-axis primed wafer coordinate system where the axes $x'_1, x'_2$ are parallel and perpendicular to the primary wafer flat. Using Eq. (3.1), the resistance change of an arbitrarily oriented in-plane sensor can be expressed in terms of the stress components resolved in this natural wafer coordinate system. The off-axis piezoresistive coefficients in the primed coordinate system must be first evaluated by substituting the unprimed values given in Eq. (3.4) and the appropriate direction cosines for the primed coordinate directions with respect to the unprimed (crystallographic) coordinate directions into the transformation relations given in Eq. (3.3). For the primed coordinate system indicated in Figure 3.3, the appropriate direction cosines for the primed axes are

$$[a_{ij}] = \begin{bmatrix} \frac{1}{\sqrt{2}} & -\frac{1}{\sqrt{2}} & 0 \\ \frac{1}{\sqrt{6}} & \frac{1}{\sqrt{6}} & -\frac{2}{\sqrt{6}} \\ \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} & \frac{1}{\sqrt{3}} \end{bmatrix} \tag{3.14}$$

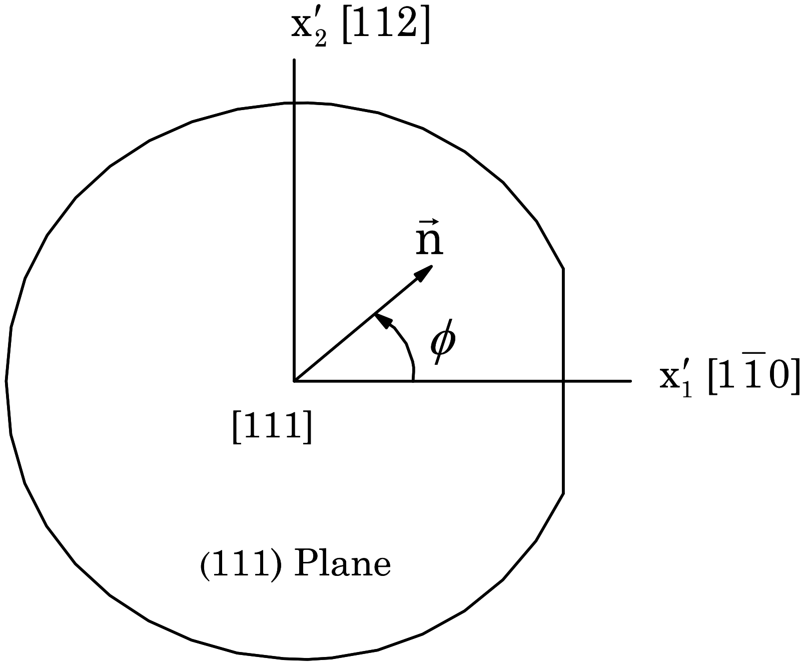

$x_2'$ $[11\bar{2}]$
$\vec{n}$
$\phi$
$x_1'$ $[1\bar{1}0]$
[111]
(111) Plane

Figure 3.3 - (111) Silicon Wafer

Substitution of the off-axis piezoresistive coefficients, calculated in the manner described above, into Eq. (3.1) yields

$$\begin{aligned}\frac{\Delta R}{R} &= [B_1 \sigma'_{11} + B_2 \sigma'_{22} + B_3 \sigma'_{33} + 2\sqrt{2}(B_3 - B_2)\sigma'_{23}]\cos^2\phi \\ &+ [B_2 \sigma'_{11} + B_1 \sigma'_{22} + B_3 \sigma'_{33} - 2\sqrt{2}(B_3 - B_2)\sigma'_{23}]\sin^2\phi \\ &+ [2\sqrt{2}(B_3 - B_2)\sigma'_{13} + (B_1 - B_2)\sigma'_{12}]\sin 2\phi \\ &+ [\alpha_1 T + \alpha_2 T^2 + \ldots]\end{aligned} \tag{3.15}$$

where $\phi$ is again the angle between the $x'_1$-axis and the resistor orientation. The coefficients

$$\begin{aligned}B_1 &= \frac{\pi_{11} + \pi_{12} + \pi_{44}}{2} \\ B_2 &= \frac{\pi_{11} + 5\pi_{12} - \pi_{44}}{6} \\ B_3 &= \frac{\pi_{11} + 2\pi_{12} - \pi_{44}}{3}\end{aligned} \tag{3.16}$$

are a set of linearly independent temperature dependent combined piezoresistive parameters. These parameters must be calibrated before stress component values can be extracted from resistance change measurements. Eq. (3.15) indicates that the resistance change for a resistor in the (111) plane is dependent on all six of the unique stress components. Therefore, the potential exists for developing a sensor rosette that can measure the complete three-dimensional state of stress at points on the surface of a die.

Besides the ability to measure two additional stress components, theoretical analysis has established that properly designed sensor rosettes on the (111) silicon wafer plane have other advantages relative to sensors fabricated using standard (100) silicon [91, 93, 162]. In particular, optimized sensors on (111) silicon are capable of measuring four temperature compensated combined stress components, while those on (100) silicon can only be used to measure two temperature compensated quantities. In this discussion, temperature compensated refers to the ability to extract the stress components directly from the resistance change measurements (without the need to know the temperature change T). This is a particularly important attribute, given the large errors which can be introduced into non-temperature compensated stress sensor data when the temperature change T is not precisely known. Furthermore, it has been established that the (111) plane offers the opportunity to measure the highest number (four) of stress components in a temperature compensated manner (considering all possible silicon wafer orientations). The four stress components, which can be measured in a temperature compensated manner using (111) silicon sensors, are the three shear stress components and the difference of the in-plane normal stress components.

# CHAPTER 4

# (111) SILICON TEST CHIPS

## 4.1 JSE (111) Silicon Test Chips (FC200)

### 4.1.1 Optimized Eight-Element Rosette

The (111) silicon eight-element dual polarity rosette in Figure 4.1 has been developed at Auburn University for measurement of the complete state of stress at points on the surface of a packaged semiconductor die. It has been optimized to measure all six stress components (four in a temperature compensated manner). It can be readily calibrated using uniaxial and hydrostatic testing. A six-element rosette (without the $-45^{o}$ resistors) can also be used to extract the complete stress state. However, including the two extra resistors allows for more convenient bridge measurements of the resistance changes and better stress measurement localization [92].

The rosette in Figure 4.1 contains p-type and n-type sensor sets, each with resistor elements making angles of $\phi = 0, \pm 45^{o}, 90^{o}$ with respect to the $x'_1$-axis. Use of both p-type and n-type sensors is required to measure more than three stress components [35], since there are only three unique resistance changes for a set of sensors of one doping type/level which are fabricated in a single plane.

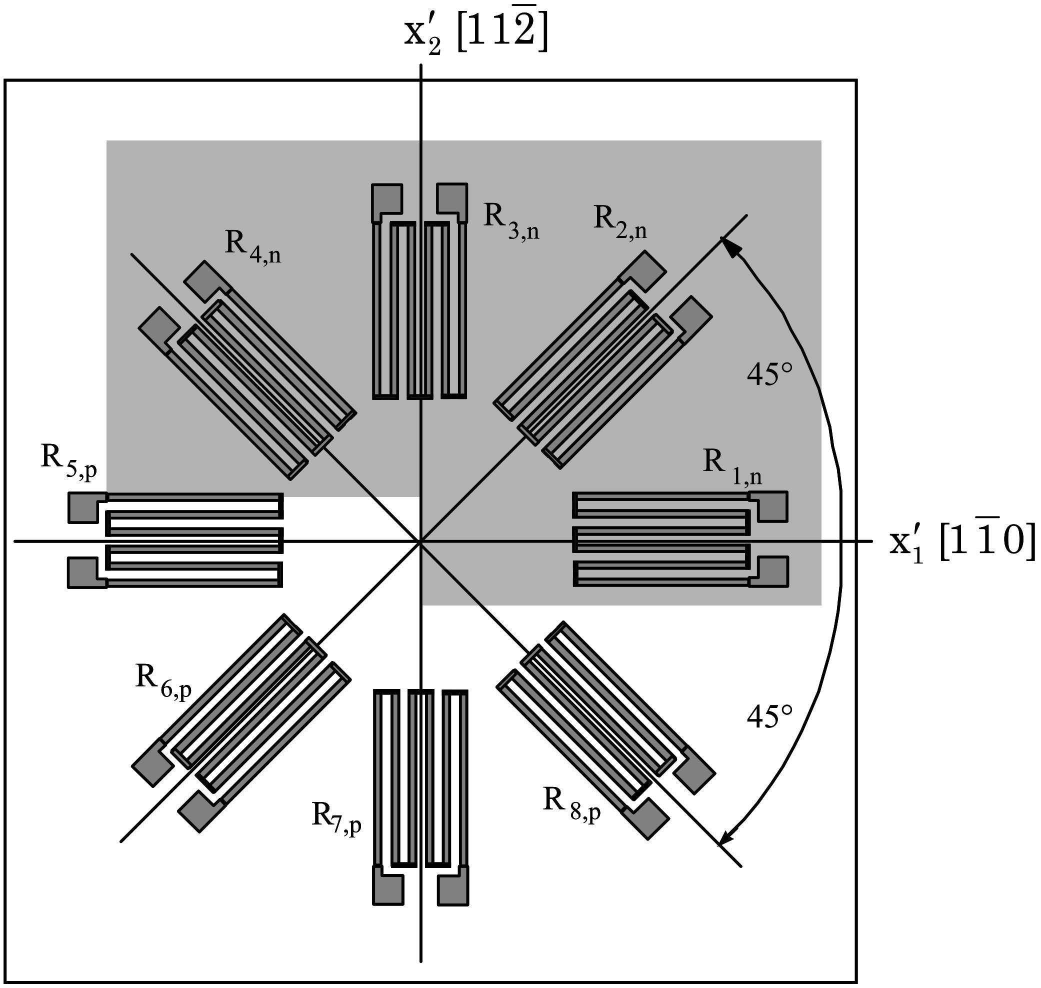

x′₂ [11$\bar{2}$]
R₃,n
R₂,n
R₄,n
45°
R₅,p
R₁,n
x′₁ [1$\bar{1}$0]
R₆,p
45°
R₇,p
R₈,p

Figure 4.1 - Optimized Eight-Element Rosette

Repeated application of Eq. (3.15) to each of the piezoresistive sensing elements leads to the following expressions for the stress-induced resistance changes:

$$
\begin{aligned}
\frac{\Delta R_1}{R_1} &= B_1^n\sigma'_{11} + B_2^n\sigma'_{22} + B_3^n\sigma'_{33} + 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{23} \\
&\quad + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_2}{R_2} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n\sigma'_{33} + 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{13} \\
&\quad + (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_3}{R_3} &= B_2^n\sigma'_{11} + B_1^n\sigma'_{22} + B_3^n\sigma'_{33} - 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{23} \\
&\quad + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_4}{R_4} &= \left(\frac{B_1^n + B_2^n}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^n\sigma'_{33} - 2\sqrt{2}(B_3^n - B_2^n)\sigma'_{13} \\
&\quad - (B_1^n - B_2^n)\sigma'_{12} + [\alpha_1^n T + \alpha_2^n T^2 + \ldots] \\
\frac{\Delta R_5}{R_5} &= B_1^p\sigma'_{11} + B_2^p\sigma'_{22} + B_3^p\sigma'_{33} + 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{23} \\
&\quad + [\alpha_1^p T + \alpha_2^p T^2 + \ldots] \\
\frac{\Delta R_6}{R_6} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p\sigma'_{33} + 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{13} \\
&\quad + (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^p T + \alpha_2^p T^2 + \ldots] \\
\frac{\Delta R_7}{R_7} &= B_2^p\sigma'_{11} + B_1^p\sigma'_{22} + B_3^p\sigma'_{33} - 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{23} \\
&\quad + [\alpha_1^p T + \alpha_2^p T^2 + \ldots] \\
\frac{\Delta R_8}{R_8} &= \left(\frac{B_1^p + B_2^p}{2}\right)(\sigma'_{11} + \sigma'_{22}) + B_3^p\sigma'_{33} - 2\sqrt{2}(B_3^p - B_2^p)\sigma'_{13} \\
&\quad - (B_1^p - B_2^p)\sigma'_{12} + [\alpha_1^p T + \alpha_2^p T^2 + \ldots]
\end{aligned}
\tag{4.1}
$$

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively.

For an arbitrary state of stress, these expressions can be inverted to solve for the six stress components in terms of the measured resistance changes:

$$
\begin{aligned}
\sigma'_{11} &= \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} \\
&\quad + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \\[2ex]
\sigma'_{22} &= -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} \\
&\quad + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \\[2ex]
\sigma'_{33} &= \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)B_3^p - (B_1^p + B_2^p)B_3^n]} \\[2ex]
\sigma'_{13} &= \frac{\sqrt{2}}{8}\left[\frac{(B_1^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - (B_1^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right] \\[2ex]
\sigma'_{23} &= \frac{\sqrt{2}}{8}\left[\frac{-(B_1^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + (B_1^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n}\right] \\[2ex]
\sigma'_{12} &= \frac{-(B_3^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + (B_3^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]}
\end{aligned}
\tag{4.2}
$$

From the expressions in Eq. (4.2), it is clear that the extraction of the three shear stresses $\sigma'_{12}, \sigma'_{13}, \sigma'_{23}$ from the measured resistance changes is temperature compensated (independent of T). Evaluation of the normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change T experienced by the sensing elements. The temperature coefficients of resistance $\alpha_1, \alpha_2,...$ must also be known for each doping type. They can be obtained using thermal cycling calibration experiments where the resistances of the sensing elements are monitored as a function of temperature. The measured resistance change versus temperature response is fit with a general polynomial to extract the temperature coefficients of resistance. Typically, only first and second order temperature coefficients are needed.

Jaeger, et al. [184, 191] have previously discussed the difficulties in obtaining accurate temperature change values over the long time spans typical of measurements made with piezoresistive sensors (e.g. before and after die encapsulation). In addition, it has been demonstrated that temperature measurement errors of as little as .25 $^{o}$C can cause serious errors in the experimental values of the stresses extracted with non temperature compensated formulas such as the first three expressions in eq. (4.2). Thus, it has been recommended to restrict measurement efforts to temperature compensated stress combinations where the temperature coefficient of resistance terms cancel in the stress extraction equations. Besides the three shear stresses, an additional temperature compensated quantity can be obtained by subtracting the expressions for the in-plane normal stresses $\sigma'_{11}$ and $\sigma'_{22}$ in Eq. (4.2):

$$\sigma'_{11} - \sigma'_{22} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{[(B_2^p - B_1^p)B_3^n + (B_1^p - B_3^p)B_2^n + (B_3^p - B_2^p)B_1^n]} \tag{4.3}$$

This result assumes that the temperature coefficients of resistance are well matched for sensing elements of the same doping type.

The expressions in Eq. (4.2) indicate that a calibration procedure must be performed to determine all six of the combined piezoresistive parameters $B_1^n$, $B_2^n$, $B_3^n$, $B_1^p$, $B_2^p$, $B_3^p$ prior to using this sensor rosette. A combination of uniaxial and hydrostatic pressure testing can be utilized to complete this task. Uniaxial calibration testing is typically performed via the four point bending method where the wafer is cut into strips that are flexed as beams [186]. For the beam loading geometry shown in Figure 4.2a, the normal stress induced at points on the top surface of the strip that are between the bottom supports is given by

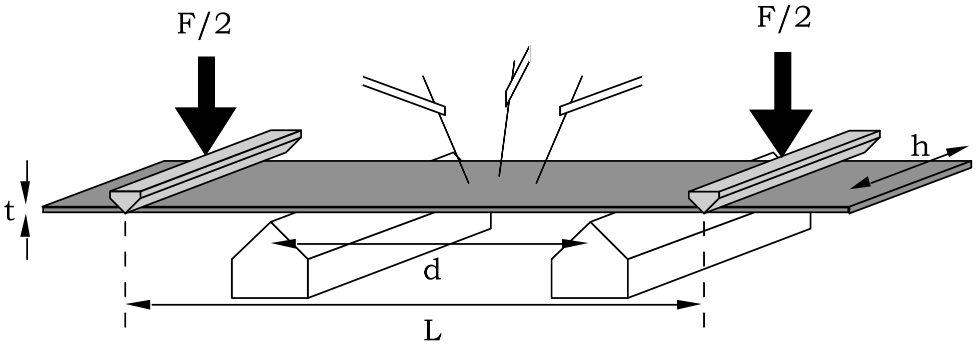
$$\sigma = \frac{3F(L-d)}{t^2 h} \tag{4.4}$$

If a wafer strip along the $x_1'$ direction is subjected to four point bending and a known uniaxial stress $\sigma_{11}' = \sigma$ is applied in the $x_1'$-direction, the expressions in Eq. (4.1) for the 0-90° oriented sensors yield the following resistance changes:

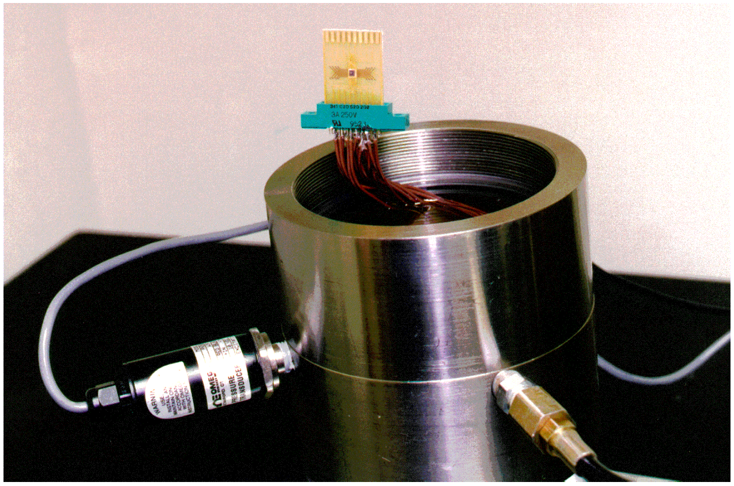
$$\begin{aligned} \frac{\Delta R_1}{R_1} &= B_1^n \sigma + \alpha_1^n T \qquad \frac{\Delta R_3}{R_3} = B_2^n \sigma + \alpha_1^n T \\ \frac{\Delta R_5}{R_5} &= B_1^p \sigma + \alpha_1^p T \qquad \frac{\Delta R_7}{R_7} = B_2^p \sigma + \alpha_1^p T \end{aligned} \tag{4.5}$$

From these expressions, it is clear that the constants $B_1^n$, $B_2^n$, $B_1^p$, $B_2^p$ can be easily determined through a controlled isothermal application of uniaxial stress to a sensor rosette while monitoring the resulting resistance changes.

A pressure vessel for subjecting test chips to hydrostatic compression is shown in Figure 4.2b. If a sensor rosette is subjected to hydrostatic pressure $(\sigma'_{11} = \sigma'_{22} = \sigma'_{33} = -p)$, the relations in Eq. (4.1) give:



(a) Four Point Bending Loading Geometry



(b) Hydrostatic

Figure 4.2 – Calibration Methods to Obtain Piezoresistive Coefficients

$$\frac{\Delta R_1}{R_1} = \frac{\Delta R_2}{R_2} = \frac{\Delta R_3}{R_3} = \frac{\Delta R_4}{R_4} = -[B_1^n + B_2^n + B_3^n]p + \alpha_1^n T$$
$$\frac{\Delta R_5}{R_5} = \frac{\Delta R_6}{R_6} = \frac{\Delta R_7}{R_7} = \frac{\Delta R_8}{R_8} = -[B_1^p + B_2^p + B_3^p]p + \alpha_1^p T \tag{4.6}$$

Therefore, the combinations $(B_1^n + B_2^n + B_3^n)$ and $(B_1^p + B_2^p + B_3^p)$ can be evaluated through a controlled isothermal application of a hydrostatic pressure to a sensor rosette while monitoring the resulting resistance changes. The individual values of $B_3^n$ and $B_3^p$ can then be obtained by combining the hydrostatic pressure calibration results with the uniaxial stress calibration results.

### 4.1.2 FC200 Silicon Test Chip

For packaging studies, special (111) silicon test chips (FC200) have been fabricated that incorporate an array of the optimized eight-element dual polarity measurement rosettes shown in Fig. 4.1, and that are capable of measuring the complete state of stress at the die surface (including the interfacial shear stresses). Figure 4.3 shows the layout of the FC200 flip chip test die used in this study. The basic chip image has dimensions of 5 x 5 mm (200 x 200 mils), and contains 200 $\mu$m (8 mil) pitch perimeter solder bumps. This chip includes 11 eight-element sensor rosettes, a diode for temperature measurement, and an eight-bit fuse style chip ID. A close up photograph of one of the FC200 sensor rosettes is shown in Figure 4.4. Analogous perimeter bumped chips of other sizes (2.5 x 2.5 mm and 10 x 10 mm) have also been fabricated. A cross-sectional schematic of the resistors appears in Fig. 4.5. Process simulations and experimental calibration results from a processing matrix have been used to verify that relatively large values of the piezoresistive coefficients have been achieved.

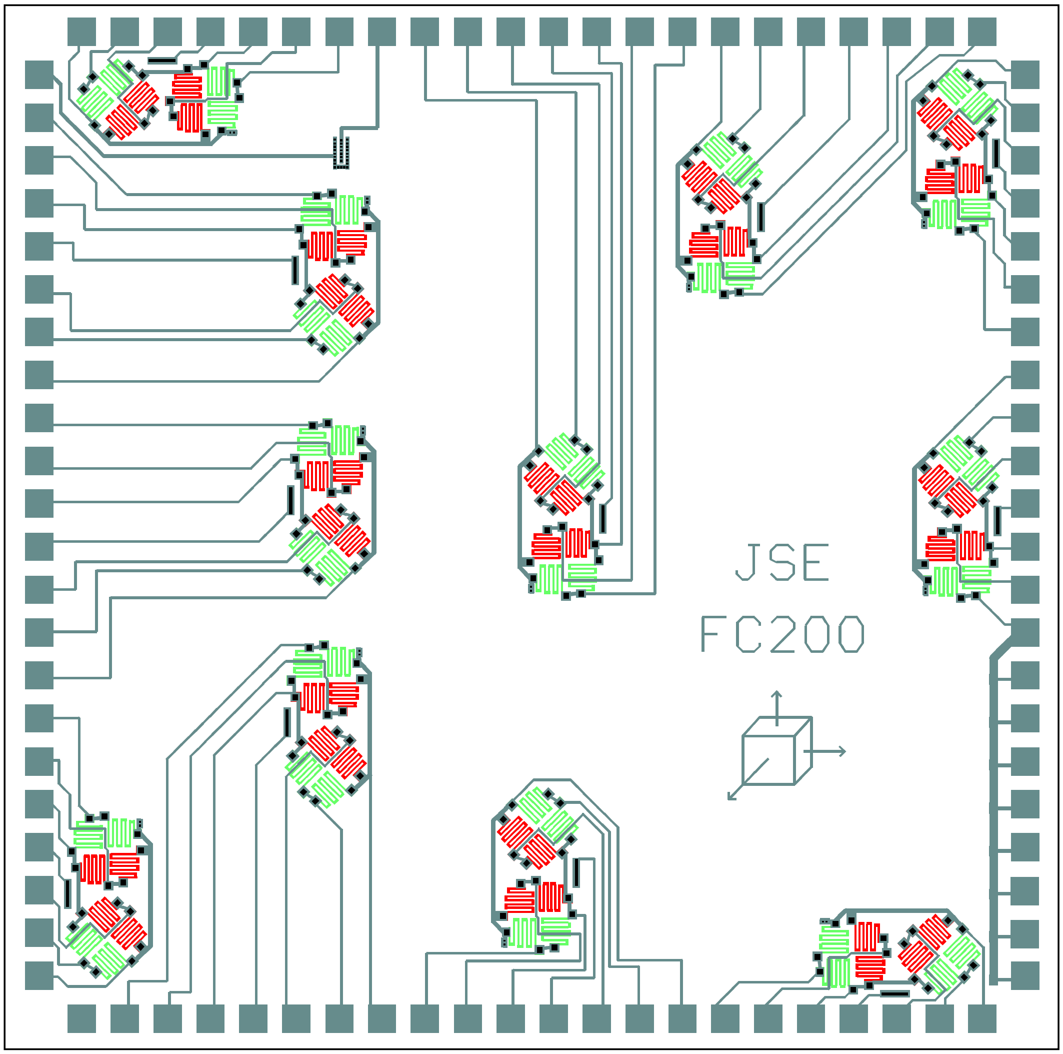


Figure 4.3 - FC200 Flip Chip Test Die (5 x 5 mm)

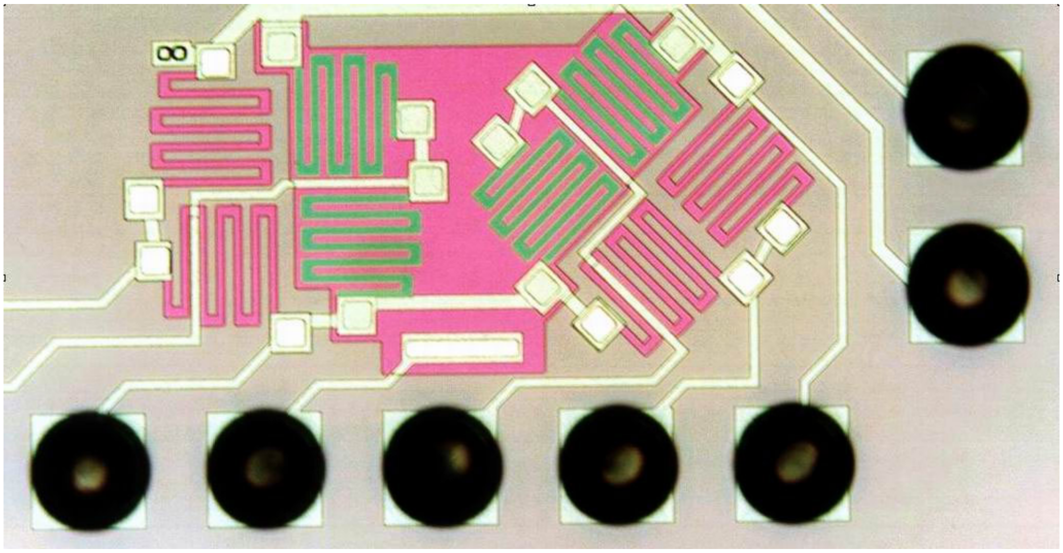


Figure 4.4 - Photograph of FC200 Sensor Rosette

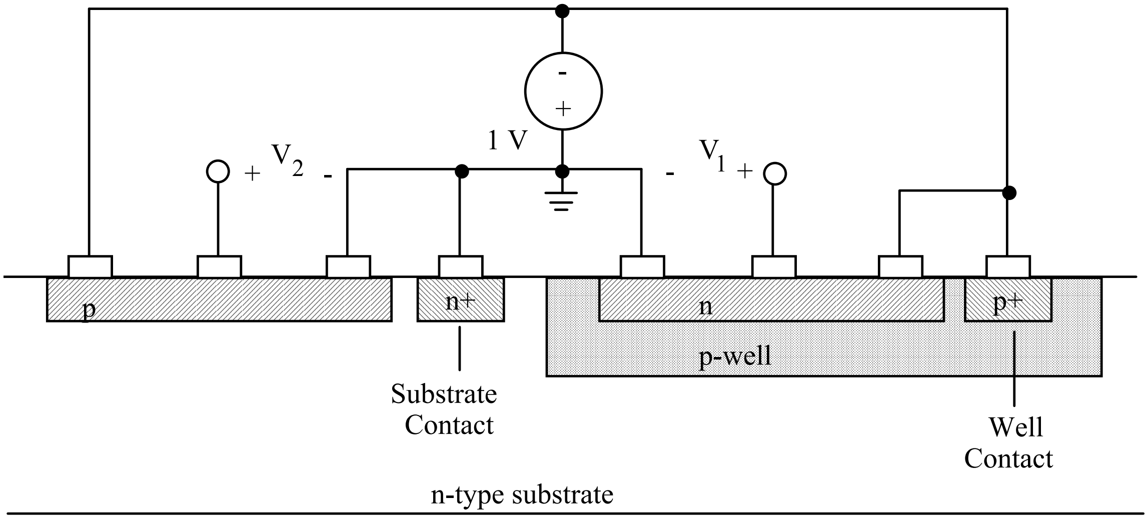

-
+
1 V
+
V2
-
-
V1
+
p
n+
n
p+
p-well
Substrate
Contact
Well
Contact
n-type substrate

Figure 4.5 - Cross Sectional Schematic of FC200 Resistors

Several wafers containing (111) silicon flip chip test chips have been used in the packaging stress studies discussed in later chapters. The wafers include FC200 chips shown in Figure 4.3 and both smaller FC100 chips and larger FC400 chips. All of the wafers were passivated with silicon nitride. Calibration procedures to determine the piezoresistive coefficients were performed as described below.

## 4.2 Calibration Results for the FC200 and FC400 Test Chips

### 4.2.1 Four-Point Bending Tests

As described earlier, the piezoresistive coefficients $B_1$ and $B_2$ for both the p- and n-type sensors on a (111) silicon test chip can be obtained by using the four-point bending method. Four point bending calibration of the sensors in the FC200/FC400 wafer lot was performed in this study. Strips oriented along the $x_1'$-axis $[1\bar{1}0]$ and having planar dimensions of 0.2 x 6.0 inches and 0.4 x 6.0 inches were cut from the flip chip wafers and subjected to four point bending in the loading fixture shown in Figure 4.6. At several levels of applied loading, the resistances of the 0-90 p-type and 0-90 n-type sensors were measured via probing. The four point bending loads produced typical resistance changes of several hundred ohms, and the normal sensor unstressed resistance values were on the order of 10-11 kΩ. The recorded data were manipulated to yield plots of the normalized resistance changes versus the applied uniaxial stress. Typical results for the p-type and n-type sensors are shown in Figures 4.7 and 4.8, respectively. Using Eqs. (4.5), the slopes of the straight-line fits to the data in these plots should be the

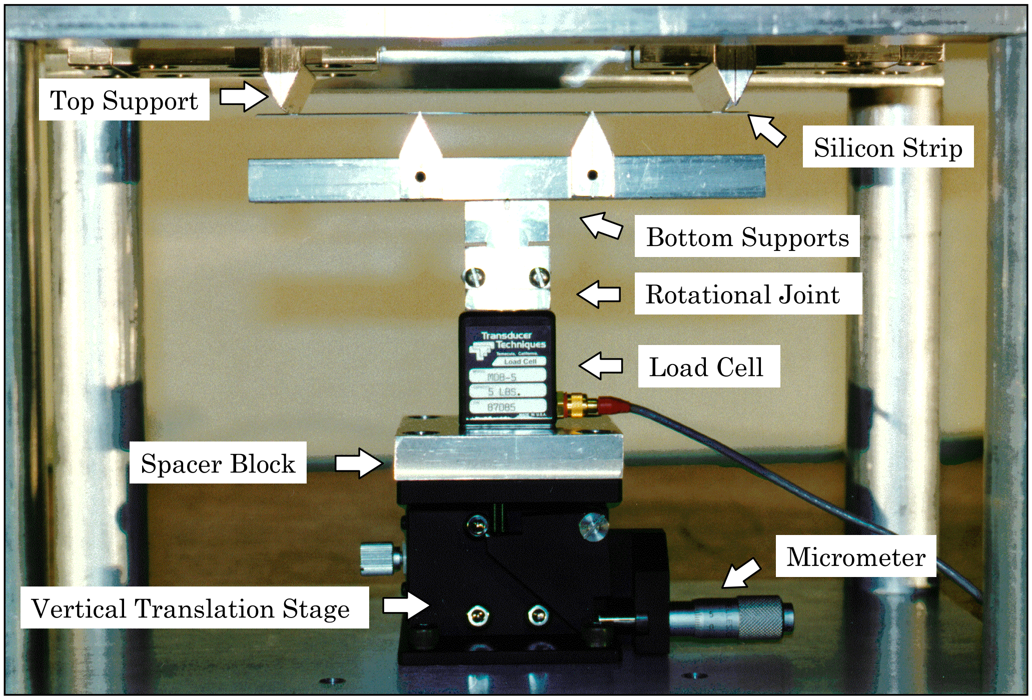

Top Support
Silicon Strip
Bottom Supports
Rotational Joint
Load Cell
Transducer Techniques
MDB-5
5 LBS.
87085
Spacer Block
Micrometer
Vertical Translation Stage

Figure 4.6 – Four Point Bending Loading Fixture

desired piezoresistive coefficients $B_1$ and $B_2$. The obtained coefficients for all of the performed tests are listed in Table 4.1 (p-Type Sensors) and Table 4.2 (n-Type Sensors).

| Specimen | $B_1^p$ ( 1/TPa ) | $B_2^p$ ( 1/TPa ) | $B_1^p - B_2^p$ ( 1/TPa ) |
|---|---|---|---|
| S1P1 | 489.7 | -97.3 | 587.0 |
| S2P1 | 439.8 | -80.4 | 520.2 |
| S1P3 | 464.2 | -83.6 | 547.9 |
| S1P4 | 456.3 | -98.6 | 554.9 |
| S1P5 | 457.4 | -103.8 | 561.2 |
| S1P6 | 451.0 | -93.5 | 544.5 |
| S1P7 | 451.3 | -91.4 | 542.7 |
| S1P8 | 467.5 | -102.5 | 570.0 |
| S1P9 | 465.3 | -96.9 | 562.2 |
| S1P10 | 447.5 | -88.0 | 535.5 |
| *Average* | 459.0 | -93.6 | 552.6 |
| *St. Dev.* | 13.8 | 7.8 | 18.8 |

Table 4.1 – Four Point Bending Calibration Results for the FC200/FC400 p-Type Sensors

| Specimen | $B_1^n$ ( 1/TPa ) | $B_2^n$ ( 1/TPa ) | $B_1^n - B_2^n$ ( 1/TPa ) |
|---|---|---|---|
| S1N1 | -161.1 | 137.3 | -298.4 |
| S1N2 | -161.0 | 157.2 | -318.2 |
| S2N1 | -112.7 | 151.7 | -264.4 |
| S1N4 | -155.6 | 130.4 | -286.0 |
| S1N5 | -161.3 | 137.9 | -299.2 |
| S1N6 | -145.7 | 130.8 | -276.5 |
| S1N7 | -144.2 | 137.1 | -281.3 |
| S1N8 | -152.4 | 145.8 | -298.2 |
| S1N9 | -153.7 | 141.5 | -295.2 |
| S1N10 | -140.2 | 135.2 | -275.4 |
| *Average* | -148.8 | 140.5 | -289.3 |
| *St. Dev.* | 14.7 | 8.7 | 15.6 |

Table 4.2 – Four Point Bending Calibration Results for the FC200/FC400 n-Type Sensors

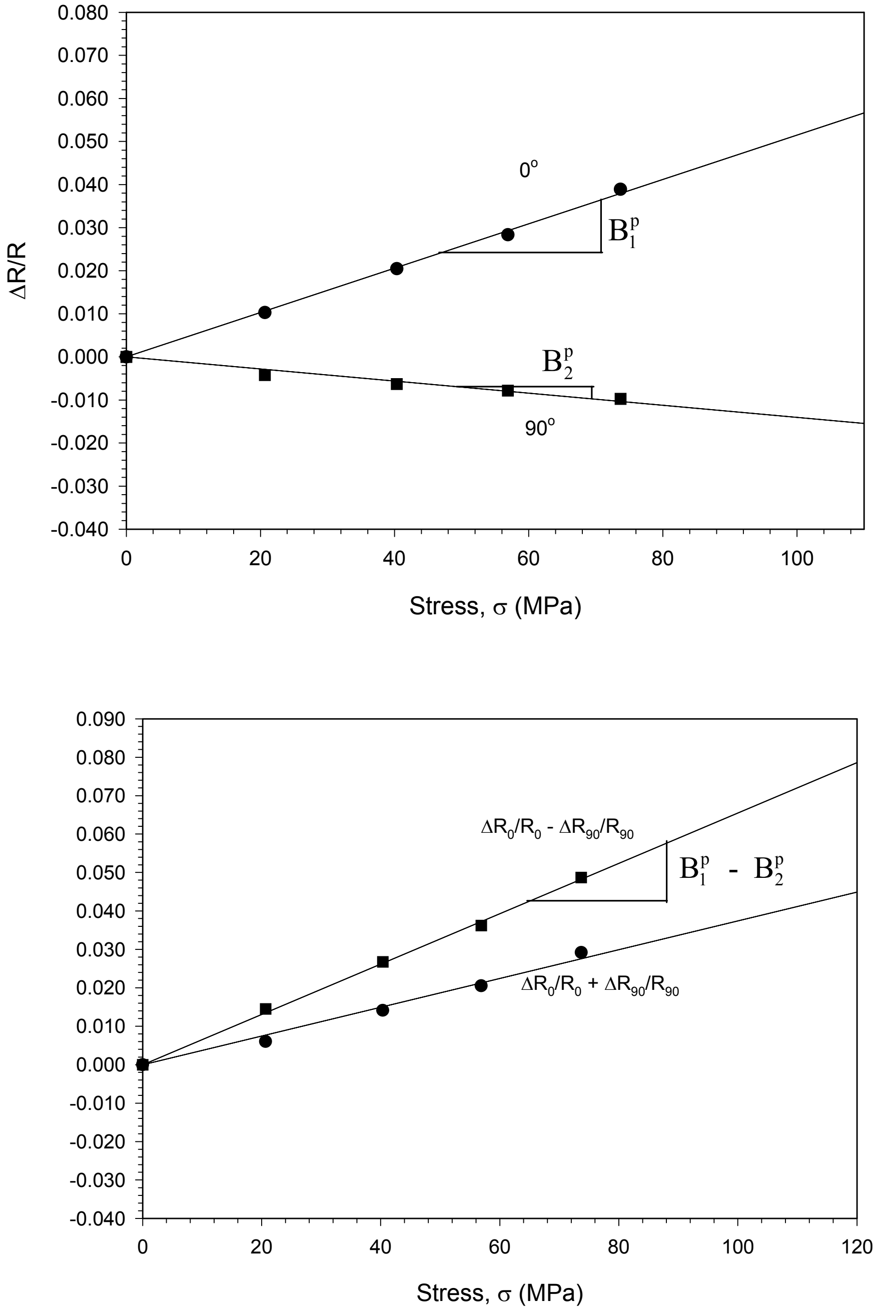


Figure 4.7 – Typical Normalized Resistance Change vs. Uniaxial Stress Data for the FC200/FC400 Flip Chip p-Type sensors

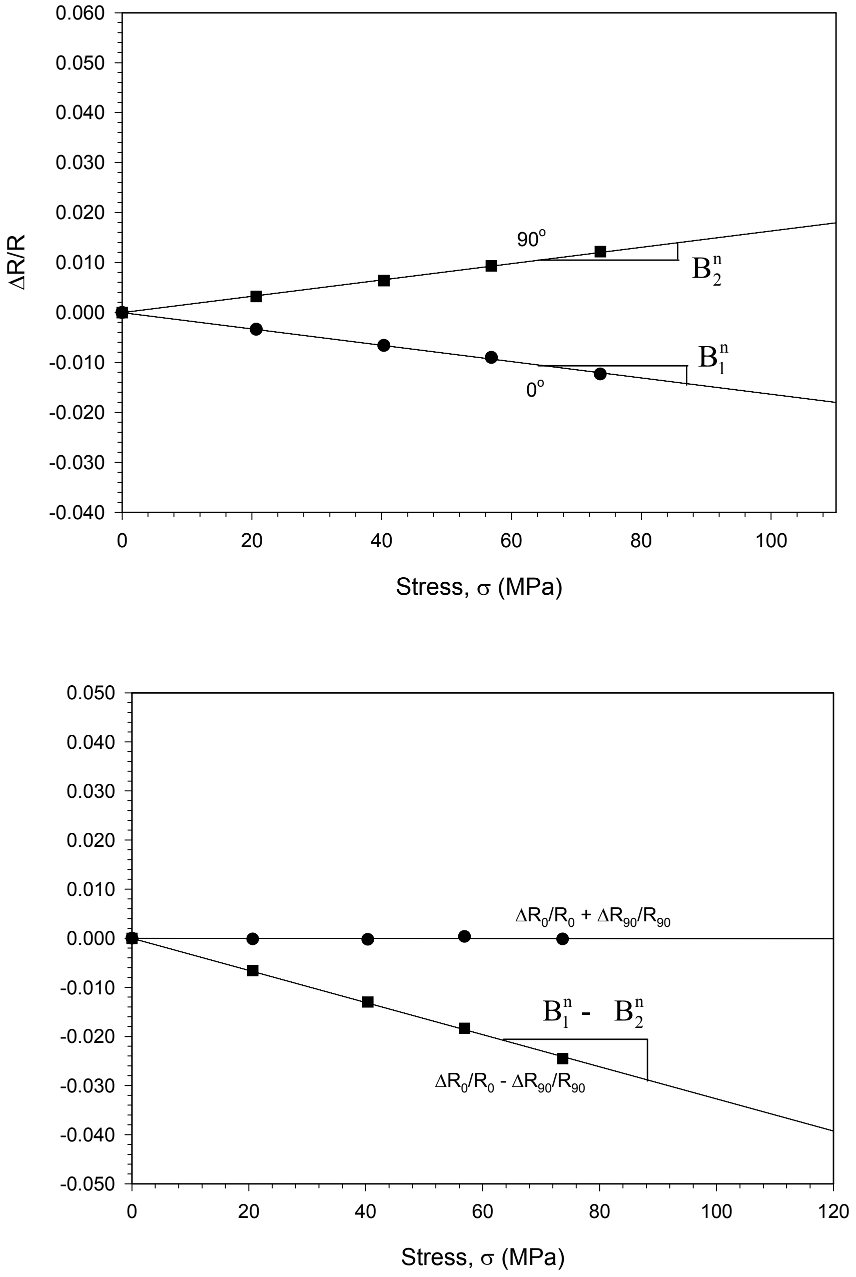


Figure 4.8 – Typical Normalized Resistance Change vs. Uniaxial Stress Data for the FC200/FC400 Flip Chip n-Type sensors

### 4.2.2 Hydrostatics Tests

As described earlier, the piezoresistive coefficient $B_3$ for both the p- and n-type sensors can be extracted by means of the hydrostatic calibration technique. If a sensor rosette is subjected to hydrostatic pressure $(\sigma'_{11} = \sigma'_{22} = \sigma'_{33} = -p)$, the pressure coefficient $\pi_p$ in eq. (4.6) can be defined by

$$\pi_p = -(\pi_{11} + 2\pi_{12}) = -(B_1 + B_2 + B_3) \tag{4.7}$$

Also the normalized resistance change equation for uniform pressure can be written as

$$\frac{\Delta R}{R} = -(\pi_{11} + 2\pi_{12})p + \alpha_1 T = \pi_p p + \alpha_1 T \tag{4.8}$$

The normalized resistance used in eq. (4.8) is defined by

$$\frac{\Delta R}{R} = \frac{R(\sigma,T) - R(0,0)}{R(0,0)} \tag{4.9}$$

where $R(\sigma,T)$ is the stressed resistance component and $R(0,0)$ is the unstressed resistance component. It can be noted here that eq. (4.8) is true for the sensors on both (100) and (111) wafer planes and is also independent of the sensor orientation. Thus, the pressure coefficient $\pi_p$ is orientation independent. Since, eq. (4.8) is orientation independent, it implies that under the application of a hydrostatic pressure load, a silicon conductor remains isotropic. Therefore, the pressure coefficients, $\pi_p$ for both p- and n-type sensors can be evaluated through an application of a hydrostatic pressure to a sensor rosette while monitoring the resulting resistance and fluid temperature changes.

### 4.2.3 TCR Measurements

In the case of hydrostatic calibration, a high capacity pressure vessel was used to subject FC100 die (2.5 x 2.5 mm) to triaxial compression. As indicated by eq. (4.8), it is not possible to make temperature compensated hydrostatic measurements. Thus, the temperature effect is always a problem. In this study, it has been observed experimentally that the hydraulic fluid temperature change due to a 14 MPa pressure change is about 0.8 $^{o}$C. Therefore, the temperature effects must be removed from hydrostatic calibration data before evaluating $\pi_p$, and accurate determination of the TCR $\alpha_1$ of a sensor must be done prior to pressure coefficient measurement. For zero stress TCR measurement conditions, eq. (4.8) becomes

$$\frac{\Delta R}{R} = \alpha_1 T \tag{4.10}$$

The TCR $\alpha_1$ can be extracted by measuring the resistance change versus temperature change of a sensor in a controllable oven. Once TCR measurements are performed, eq. (4.8) can be used to extract the values of $\pi_p$ for p- and n-type resistors using hydrostatic tests.

### 4.2.4 Hydrostatic Test Procedure

In the present study, several sets of hydrostatic calibration tests were performed on the (111) Silicon FC100 test chips. The die were attached to specially designed printed circuit boards. The PCB was designed using Lavenir software and a schematic is shown in Figure 4.9. The chips were attached only at one corner to the PCB and then wire-bonded to get electrical access to the sensors. A picture of a die-attached and wire-

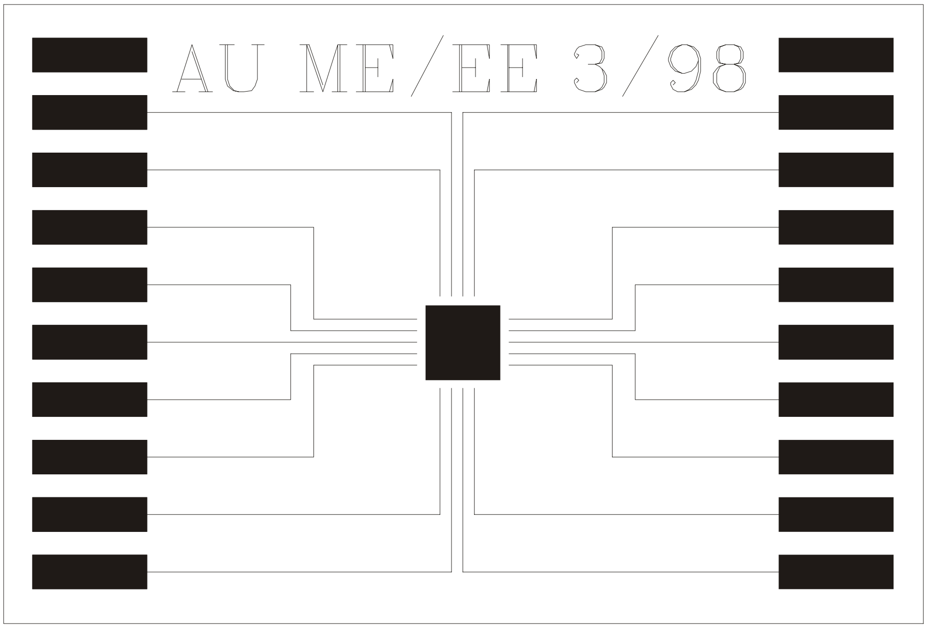


Figure 4.9 - TCR and Hydrostatic Printed Circuit Board

bonded die is shown in Figure 4.10. The wire-bonded die was first subjected to temperature change from below the room temperature to above room temperature, and resistances of the sensors were monitored at each temperature. A LabView program was developed to automatically control the oven temperature and to measure the sensor resistances at each temperature using computer-controlled GPIB devices. A similar bias setup to that shown in Appendix A was used for the measurements. During the TCR tests, no mechanical loads were applied to the sensor. These procedures were established in earlier research work at Auburn University by Mian and Kang [52, 89, 93, 189].

Once the TCR measurements were completed for every sensor, the chips were then subjected to hydrostatic pressure using the hydrostatic test setup shown in Figure 4.11. Figure 4.12 illustrates close-up views of the hydrostatic pressure vessel. To apply the pressure loading, the die were first inserted into the oil-filled pressure vessel and the vessel was sealed. A pump connected to the vessel was used to pressurize the chamber. During the tests, the resistances of the sensors were recorded using GPIB devices, and the fluid temperature was monitored at every load step. Another data acquisition program was developed using LabView. Typical TCR and hydrostatic calibration data similar to those found in this work are given in references [89] and [189]. The average experimentally measured values and standard deviations of all six piezoresistive coefficients $B_1$, $B_2$, and $B_3$ (for both p and n-type sensors) are listed in Table 4.3.

| | $B_1^p$ (1/TPa) | $B_2^p$ (1/TPa) | $B_3^p$ (1/TPa) | $B_1^n$ (1/TPa) | $B_2^n$ (1/TPa) | $B_3^n$ (1/TPa) |
|---|---|---|---|---|---|---|
| *Average* | 459.0 | -93.6 | -452.6 | -148.8 | 140.5 | -75.5 |
| *St. Dev.* | 13.8 | 7.8 | 5.1 | 14.7 | 8.7 | 4.4 |

Table 4.3 - All Six Calibrated Piezoresistive Coefficients

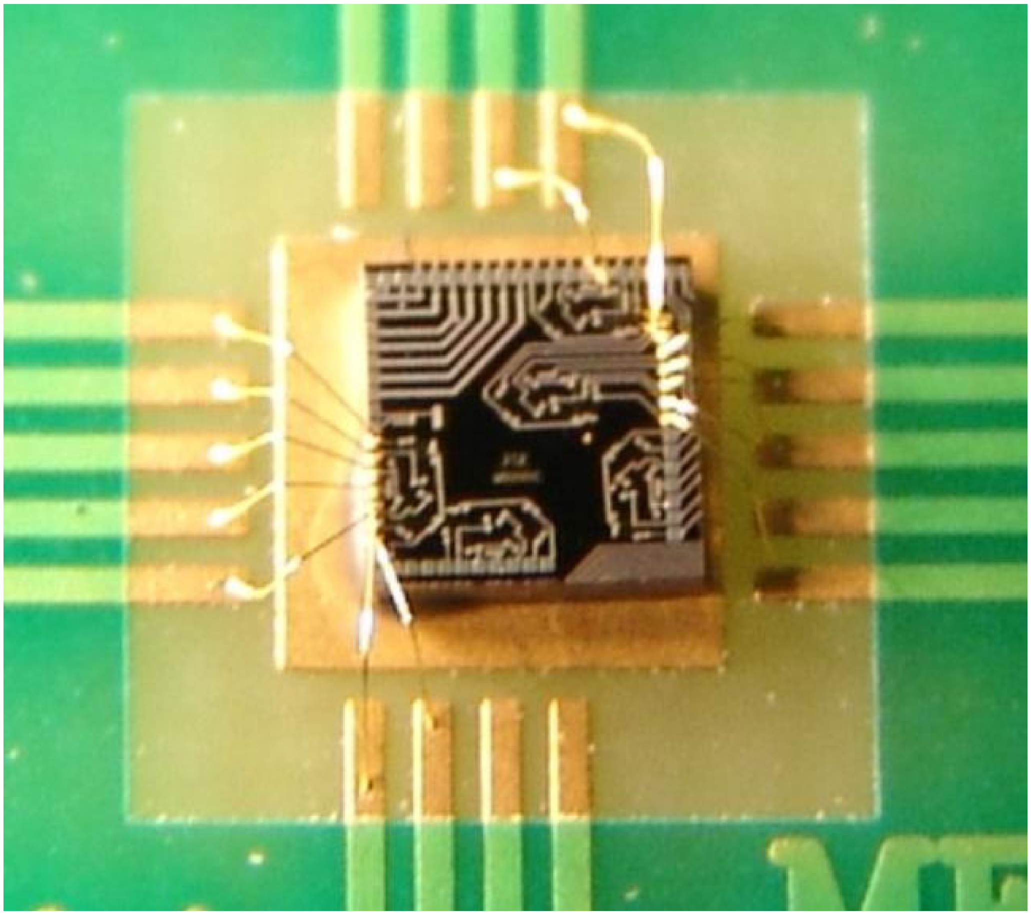


Figure 4.10 - Wire-Bonded Die for TCR and Hydrostatic Tests

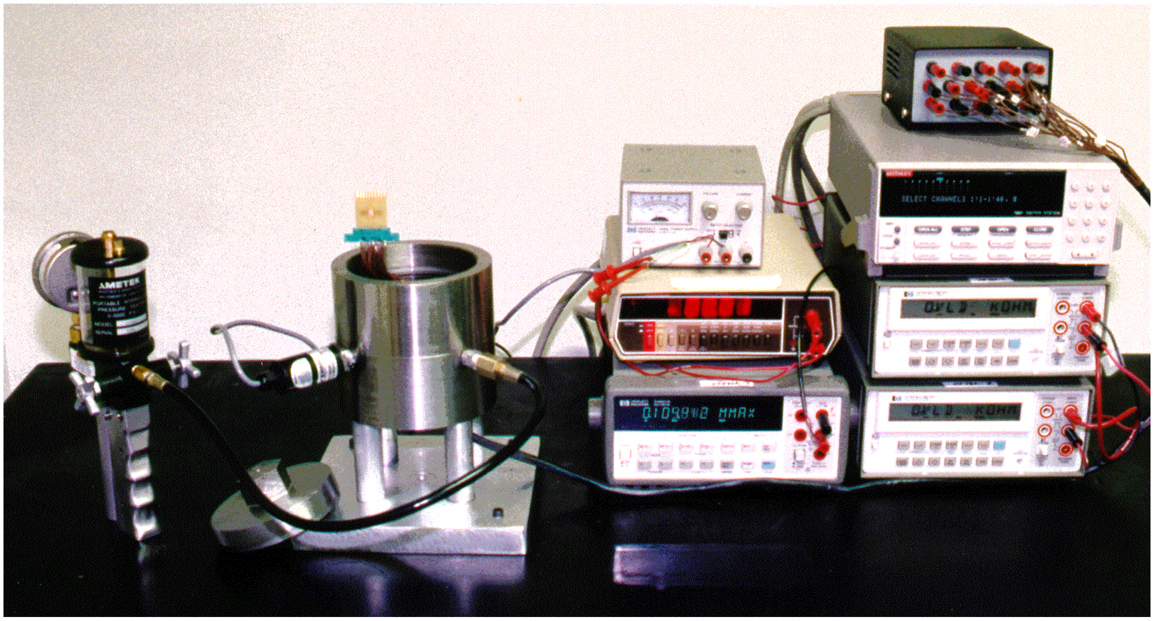
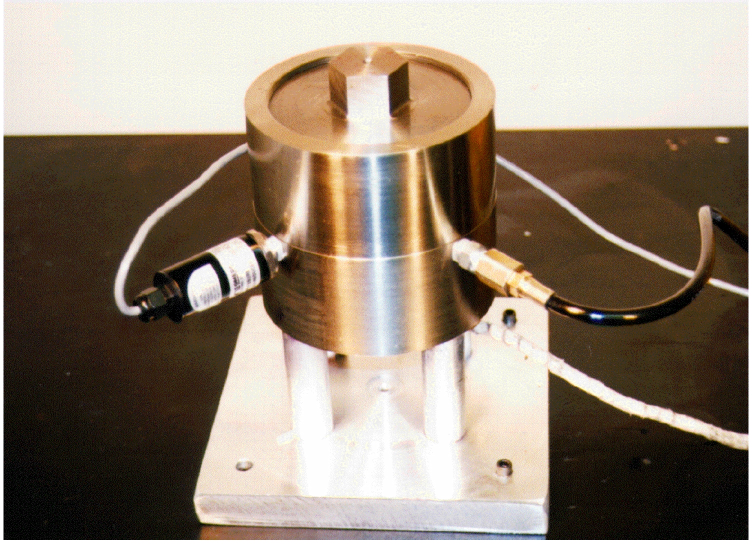
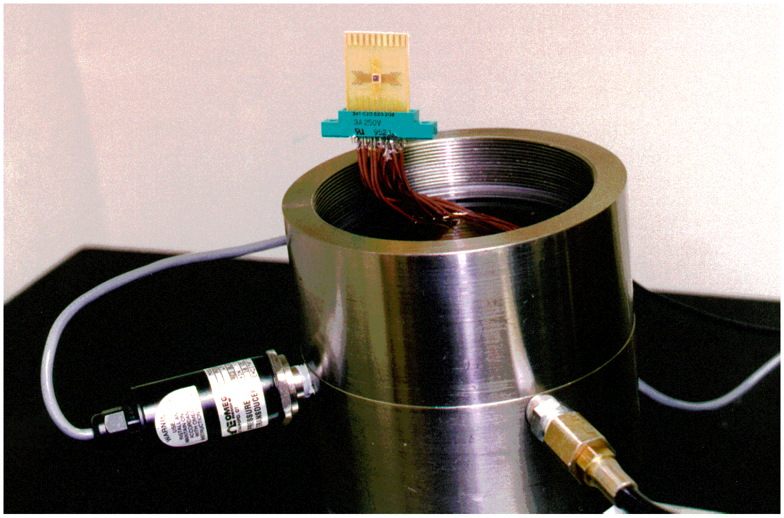


Figure 4.11 - Hydrostatic Test Setup



(a)



(b)

Figure 4.12 - Hydrostatic Pressure Vessel

## 4.3 Test Chip Application Procedure

The procedure used in this study for test chip applications includes wafer fabrication, initial resistance characterization, stress sensor calibration, packaging assembly, resistance measurements after packaging, and stress calculation. The (111) silicon FC200 test chips (Figure 4.3) used in this work were fabricated using 6 inch silicon wafers and a (111) silicon bipolar process. Silicon nitride passivation was applied on the wafer surface to provide protection. Some of the wafers were then sawed into strips, and four-point bending and hydrostatic calibrations were performed. The strips and remaining wafers were then diced into individual die. The calibrated test chips were packaged in flip chip on laminate assemblies using the SMT line at the Center for Advanced Vehicle Electronics (CAVE) in Auburn University. The sensor resistances were measured at various stages of the packaging process. The stress components at the sensor rosette locations on the die surface were then extracted from the measured resistance changes. Some additional details on the procedure for test chip application are reviewed below. These procedures were established in earlier research work at Auburn University by Zou [193].

### 4.3.1 Resistance Measurements

The resistances of the sensor rosettes were measured using a GPIB controlled data acquisition system. Using the measured resistance changes and eqs. (4.2-4.3), the die stresses can be calculated. In this work, initial resistance measurements were measured after solder joint reflow. Subsequent resistance measurements were made at several points after underfill dispense. The general procedure for making resistance measurements with the FC200 test chips is now discussed.

The equipment utilized in the experimental procedure included:

- Computer

A PC-based computer was used to control the instrumentation for resistance measurements through a GPIB board. The controll programs were written in LabView, and the program logic and program interface are shown in Figures 4.13 and 4.14, respectively.

- Keithley 7002 Switch System (Scanner)

The scanner was controlled to turn on or off either one or multiple channels to make the resistance measurements. Up to five scanners boards were used for packaged sample measurements with the FC400 test chip.

- HP Multimeter #1

The first HP multimeter was used to determine the current through the measured resistors.

- Power Supply

When measuring the resistance of sensors on the FC200 test chips, a power supply was used to provide bias in the circuit to prevent current leakage, and to provide voltage to the measured resistors. In this study, the voltage across a resistor sensor was set to be 1V.

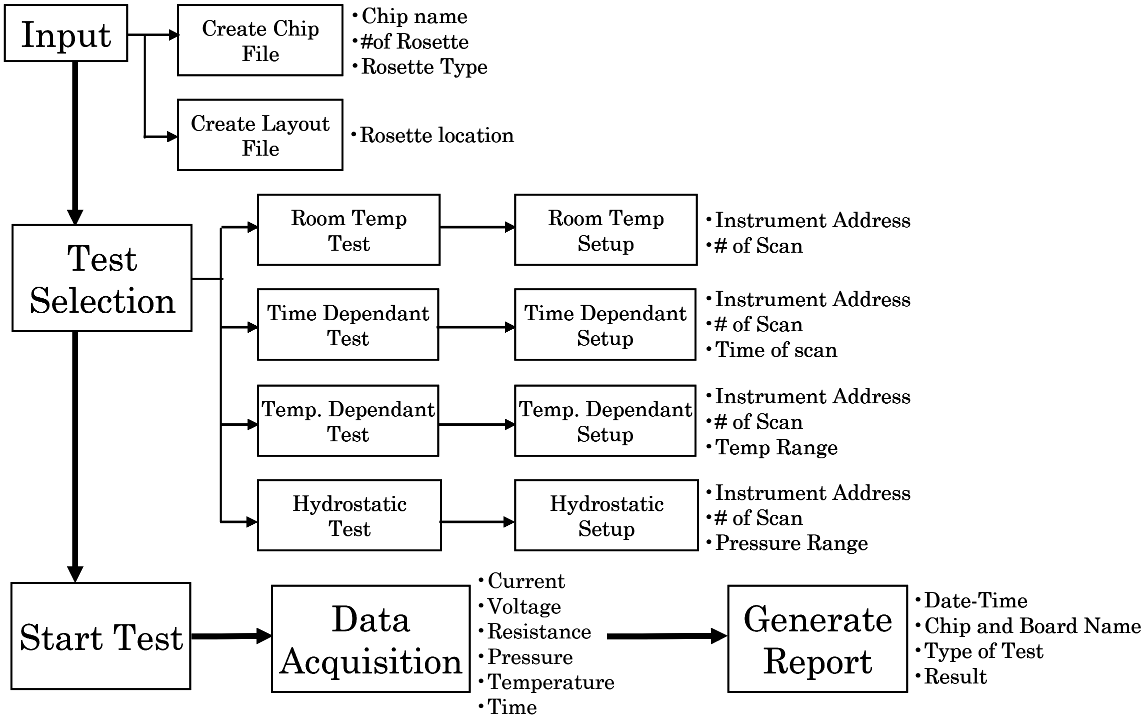
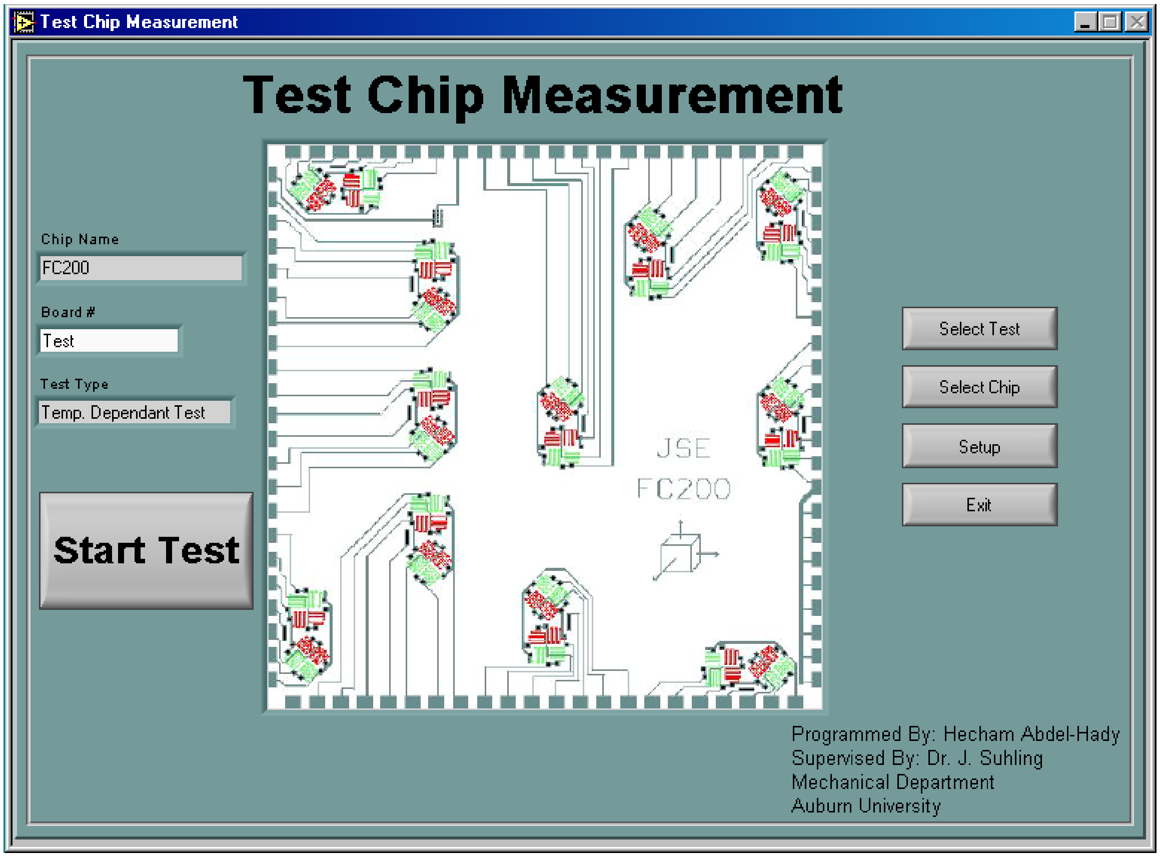

Input
Create Chip File
•Chip name
•#of Rosette
•Rosette Type
Create Layout File
•Rosette location
Test Selection
Room Temp Test
Room Temp Setup
•Instrument Address
•# of Scan
Time Dependant Test
Time Dependant Setup
•Instrument Address
•# of Scan
•Time of scan
Temp. Dependant Test
Temp. Dependant Setup
•Instrument Address
•# of Scan
•Temp Range
Hydrostatic Test
Hydrostatic Setup
•Instrument Address
•# of Scan
•Pressure Range
Start Test
Data Acquisition
•Current
•Voltage
•Resistance
•Pressure
•Temperature
•Time
Generate Report
•Date-Time
•Chip and Board Name
•Type of Test
•Result

Figure 4.13 – LabView Program Logic for Test Chip Measurements


Test Chip Measurement
Test Chip Measurement
JSE
FC200
Select Test
Select Chip
Setup
Exit
Start Test

Chip Name
FC200

Board #
Test

Test Type
Temp. Dependant Test

Programmed By: Hecham Abdel-Hady
Supervised By: Dr. J. Suhling
Mechanical Department
Auburn University

Figure 4.14 – LabView Program Interface for Test Chip Measurements

- HP Multimeter #2

A second HP multimeter was used to measure the exact voltage applied to the sensor resistors. The reading of the multimeter should be around the bias voltage, which was set to be 1V. This voltage reading was later used for the resistance calculations.

- HP Multimeter #3

A third multimeter was connected to a resistance thermometer (thermistor) that was set beside the package sample being measured. In this way, the time dependent temperature change of the assembly could be recorded. The temperature measurements were important when the packaged die surface stresses were studied as a function of temperature, or when the die surface stresses were investigated during an encapsulant cure cycle.

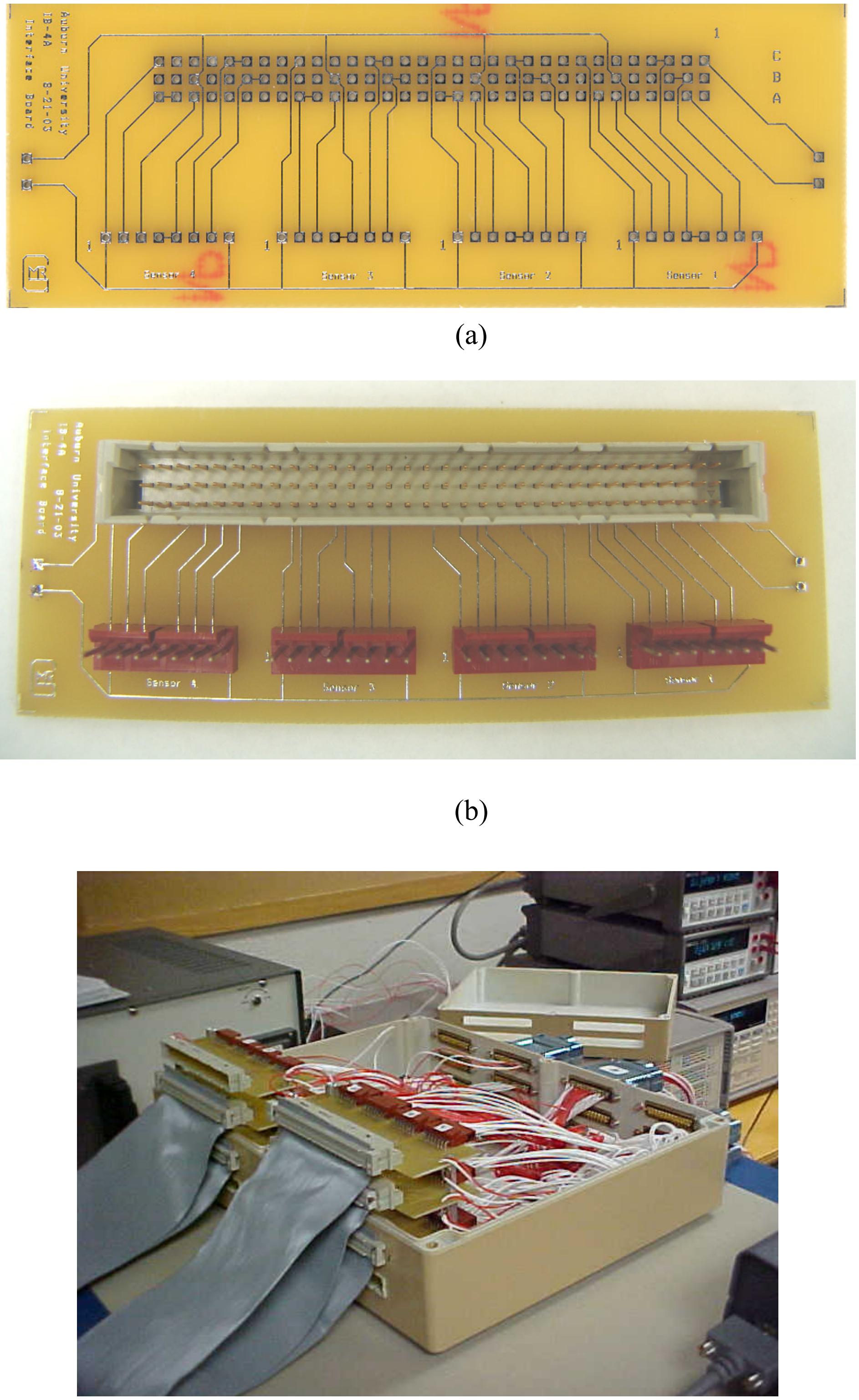
- Delta Design 9010 Temperature Controller

A Delta Design oven was also controlled by the computer through the GPIB board, and used to provide known temperature changes for characterization of packaging samples. The temperature was typically swept over a large range from a low temperature (as low as -180 $^{o}$C) to a high temperature (as high as 170 $^{o}$C). The increment of the temperature between sensor readings was usually set to be 5 $^{o}$C, and the temperature at each step was maintained for at least 5 minutes before measurements were taken to ensure a uniform temperature distribution within the packaging sample.

- Accessories

For the flip chip on laminate measurements, a pair of edge connectors were used to contact to gold plated tabs on the perimeter of the substrates. Ribbon cables and connectors (50-100 pins) were also needed to provide electrical connections between the edge connectors and the measurement equipment. Specially designed interface boards were used to interconnect between the scanner cards and the board edge connectors through 96 wire ribbon cables. Pictures of the interface board and junction box specially designed for the test chip measurements in this work are shown in Figure 4.15. Each interface board is capable of measuring up to 4 sensor rosettes or 32 resistor sensors. Ribbon cable connectors were attached directly to the interface boards by using wave soldering technique [Figure 4.15b].

In every eight element rosette on the FC200 and FC400 test chips, there are four p-type and four n-type resistors orientated at angles of $0^o$, $90^o$, $+45^o$, $-45^o$ from the $x_1'$-direction. These resistors are denoted as P1, P2, P3, P4, and N1, N2, N3, N4. As shown in Figure 4.16, the basic rosette image occurs in both horizontal and vertical formats on a test chip. When comparing the two configurations, the orientation of a particular rosette element will switch from $0^o$ to $90^o$, or from $+45^o$ to $-45^o$. In the FC200 (200 x 200 mil) test chip (shown in Figure 4.17), 88 resistors are organized into 11 rosettes. Rosettes 1, 2, 4, 5, 6, 7, 8, 10, 11 belong to type 1 (horizontal), and rosettes 3, 9 are type 2 (vertical). In Figure 4.18, the methods utilized for measuring the resistances of sensor P1 in a horizontal rosette and sensor P2 in a vertical rosette are given. The power supply provides a 1 V voltage. Referring to Figure 4.18, the multimeter (ammeter) serves as a shunt to prevent current from entering the lower sensor, and also measure the current passing through the upper sensor. Thus, the resistance of the upper sensor is simply the applied voltage of 1 V divided by the measured current.

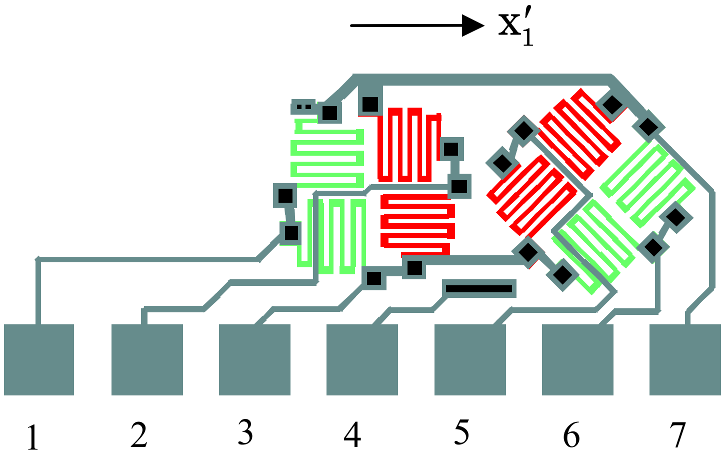

Auburn University
IB-4A 8-21-03
Interface Board
C
B
A
Sensor 4
Sensor 3
Sensor 2
Sensor 1

(a)

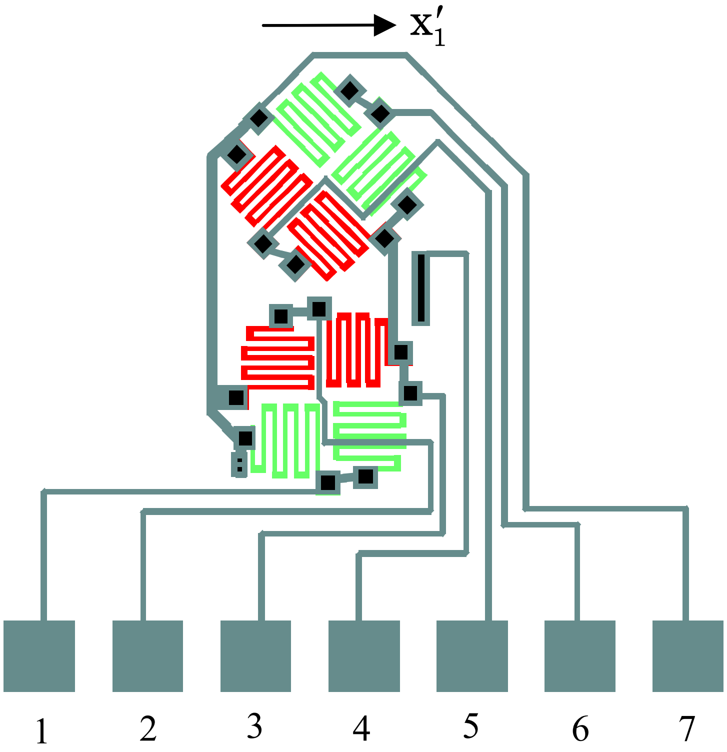
(b)

(c)

Figure 4.15 – Interface Board and Junction Box for Test Chip Measurements



Rosette from FC200 Test Chip (Type 1)



Rosette from FC200 Test Chip (Type 2)

Figure 4.16 – Rosette Types 1 and 2 (Horizontal and Vertical)

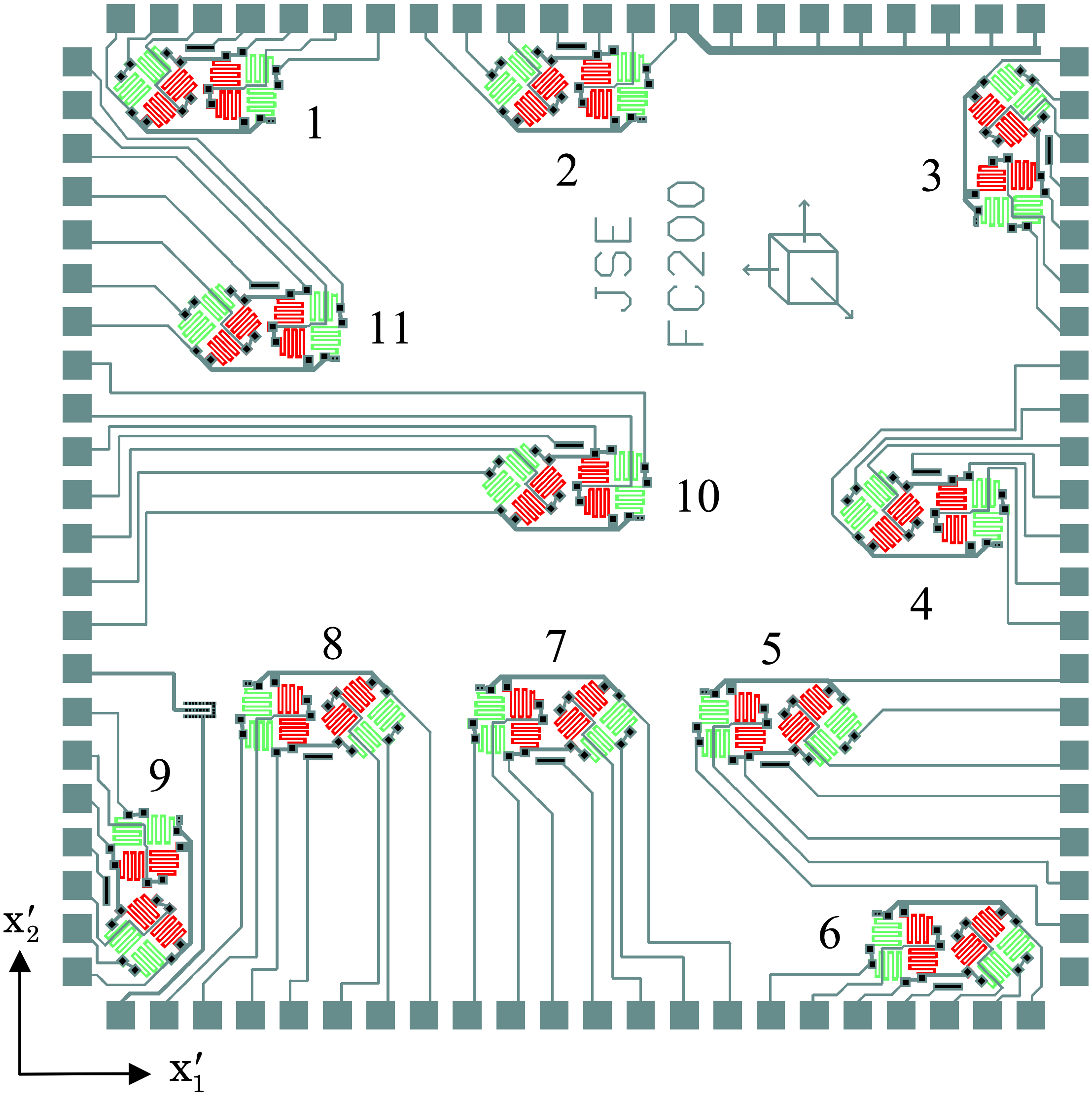
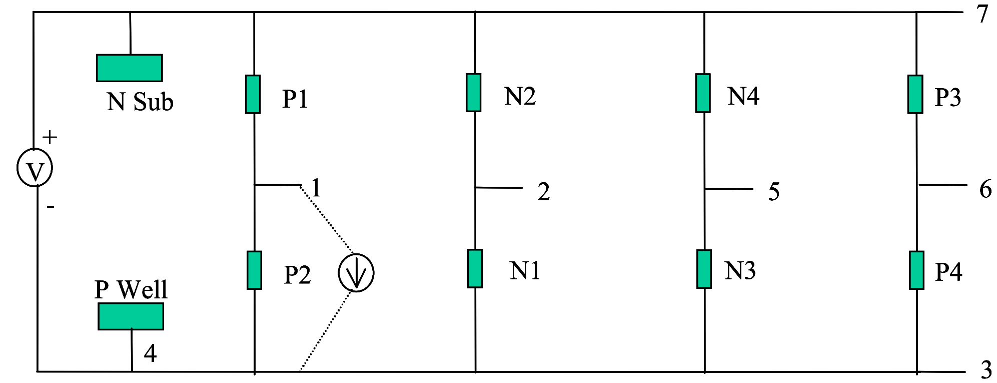
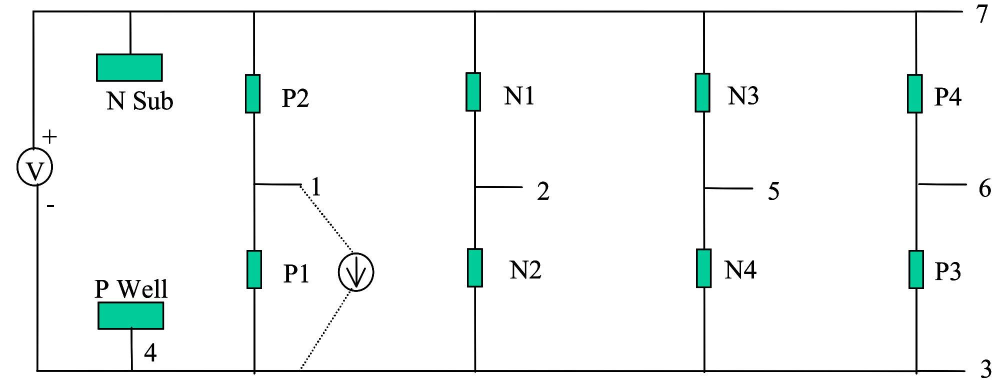

1
2
3
4
5
6
7
8
9
10
11
JSE
FC200
$x_2'$
$x_1'$

Figure 4.17 - Measurement Rosette Numbering on a 200 x 200 mil FC200 Test Chip


7
N Sub
P1
N2
N4
P3
+
V
-
1
2
5
6
P Well
P2
N1
N3
P4
4
3

Wiring to Evaluate Sensor P1 in a Horizontal (Type 1) Rosette


7
N Sub
P2
N1
N3
P4
+
V
-
1
2
5
6
P Well
P1
N2
N4
P3
4
3

Wiring to Evaluate Sensor P2 in a Vertical (Type 2) Rosette

Figure 4.18 - Typical Resistance Measurement Wiring Diagram for the FC200 Test Chip Rosette

One bank in a scanner card can be used to measure the resistances of of all sensors in one rosette. There are four banks in a scanner card. Therefore, three scanner cards are needed to measure all 11 of the sensor rosettes that are accessible by perimeter pads in a 200 x 200 mil FC200 test chip. Table 4.4 shows the utilized connections between the bonding pads of a rosette in Figure 4.16 and the channel numbers of a bank in a scanner card.

| | Channel Status | |
|---|---|---|
| Pad Number | H | L |
| 7 | 1 | |
| 1 | 2 | 3 |
| 2 | 5 | 6 |
| 3, 4 | | 4 |
| 5 | 7 | 8 |
| 6 | 9 | 10 |

Table 4.4 - Connection between Bonding Pads and Channels in a Bank of One Scanner Card

As shown in Figure 4.18, the 8 sensor in a rosette are configured as the parallel connection of four two-element half bridges. For measurements using the half-bridges, the substrate is grounded, and a bias of -1 V is applied to both the p-well and the common connection at the top of the half-bridge resistors as indicated in Fig. 4.19. The output voltages at the nodes $V_1$ … $V_4$ are then proportional to the four normalized resistance change difference terms present in the expressions in Eqs. (4.2-4.3).

For example, $V_1$ is proportional to

$$V_1 \propto \left( \frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3} \right) \tag{4.11}$$

for small fractional resistance variations. In this particular work, however, the individual resistor changes were measured directly utilizing the techniques shown in Figures 4.20 and 4.21, and as described above and shown in Figure 4.18. For the case in Figure 4.20, an ammeter is used to force the current in upper resistor $R_U$ to bypass lower resistor $R_L$ and flow through the ammeter. The ammeter must force the voltage across $R_L$ to be zero and should be implemented using a high quality digital multimeter or an electrometer (such as the Keithley 6512). The circuit in Figure 4.21 functions in a similar manner. In this case the ammeter forces the current in resistor $R_U$ to be zero, and the measured current is due to resistor $R_L$ acting alone.

Wiring diagrams for the FC200 resistance measurements viewed as chip cross-sections are presented in Appendix A.

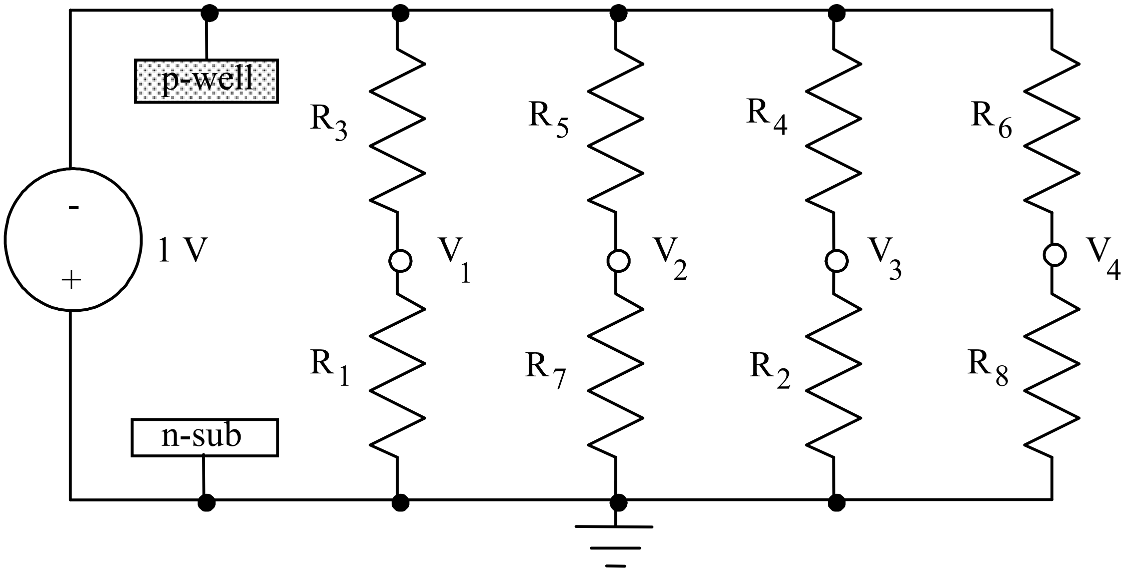

p-well
R3
R5
R4
R6
-
1 V
+
V1
V2
V3
V4
R1
R7
R2
R8
n-sub

Figure 4.19 - Bias for Half Bridge Resistance Measurements

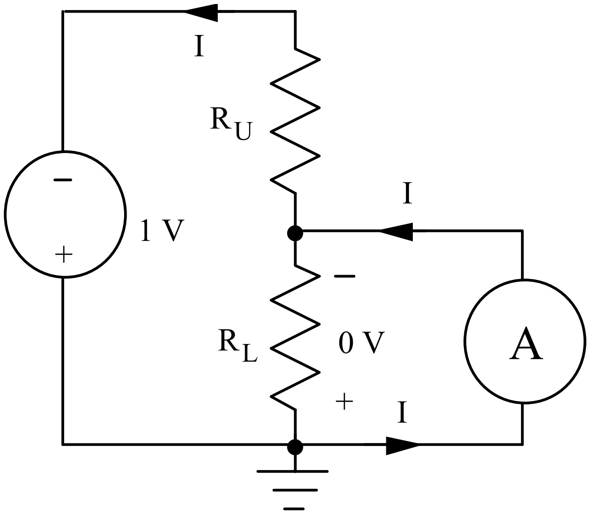

I
RU
I
1 V
–
+
–
RL
0 V
A
+
I

Figure 4.20 - Bias for Resistance Measurements (Upper Arm of Half-Bridge)

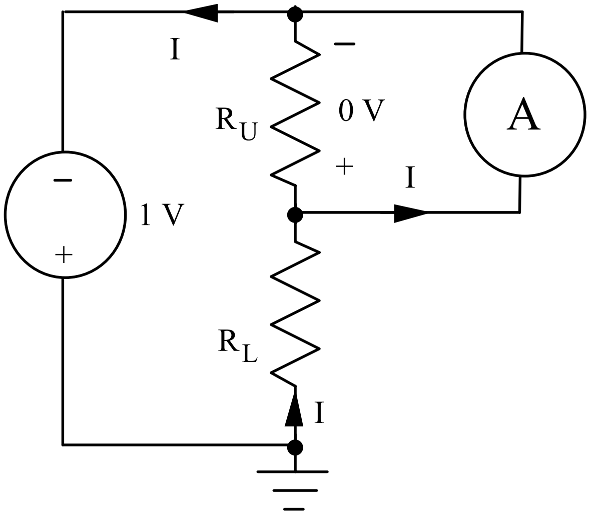

I
−
R_U
0 V
+
A
I
−
1 V
+
R_L
I

Figure 4.21 - Bias for Resistance Measurements (Low Arm of Half-Bridge)

# CHAPTER 5

# DIE STRESS CHARACTERIZATION IN FLIP CHIP ON LAMINATE ASSEMBLIES

## 5.1 Introduction

Minimizing device side die stresses is especially important when multiple copper/low-k interconnect redistribution layers are present. Mechanical stress distributions in packaged silicon die resulting during assembly or environmental testing can be accurately characterized using test chips incorporating integral piezoresistive sensors. A schematic of a flip chip assembly is shown in Figure 5.1. As shown in Figure 5.2, flip chip solder bumps can be subjected to large shear strains during thermal cycling. A typical solder bump failure in flip chip packages due to large shear strains is shown in Figure 5.3. Underfill encapsulation is used with flip chip die assembled to laminate substrates to distribute and minimize the solder joint strains, thus improving thermal cycling fatigue life. With the die coupled to the substrate through the underfill epoxy, the coefficient of thermal expansion mismatch between the silicon and the laminate produces a bending or curvature of the assembly (and thus the silicon die) upon changes of temperature [150]. This leads to a greatly reduced dependence of the solder bump shear strains on the distance from the chip center (neutral point). With underfill, delamination at the underfill/die interface often becomes the primary failure mode.

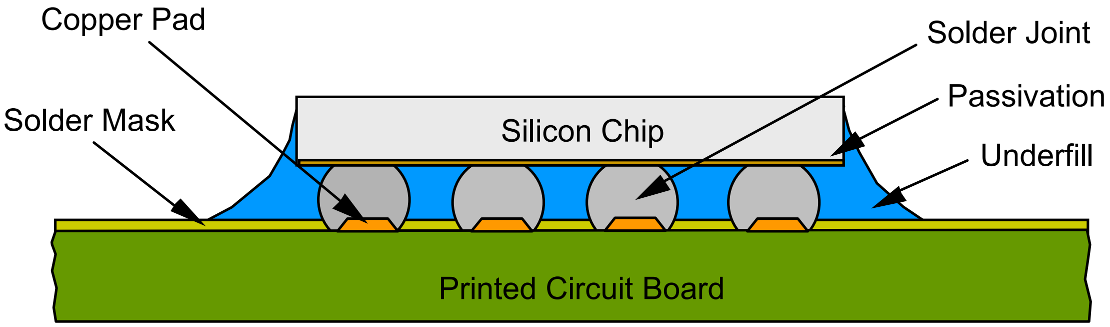

Copper Pad
Solder Joint
Passivation
Solder Mask
Silicon Chip
Underfill
Printed Circuit Board

Figure 5.1 - Typical Cross-Section of a Flip Chip Package

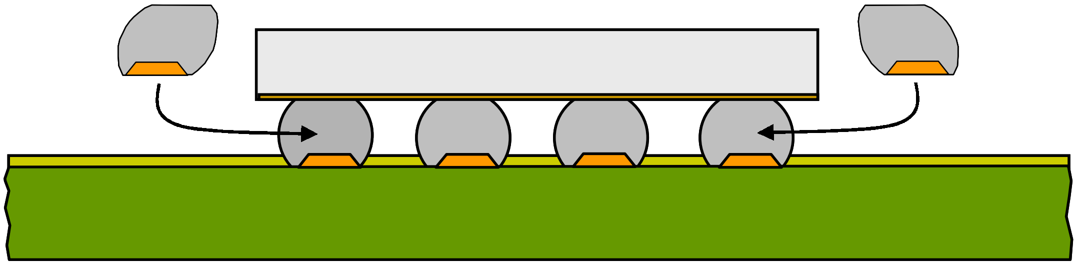


Figure 5.2 – Shearing of Solder Bumps During Temperature Cycling

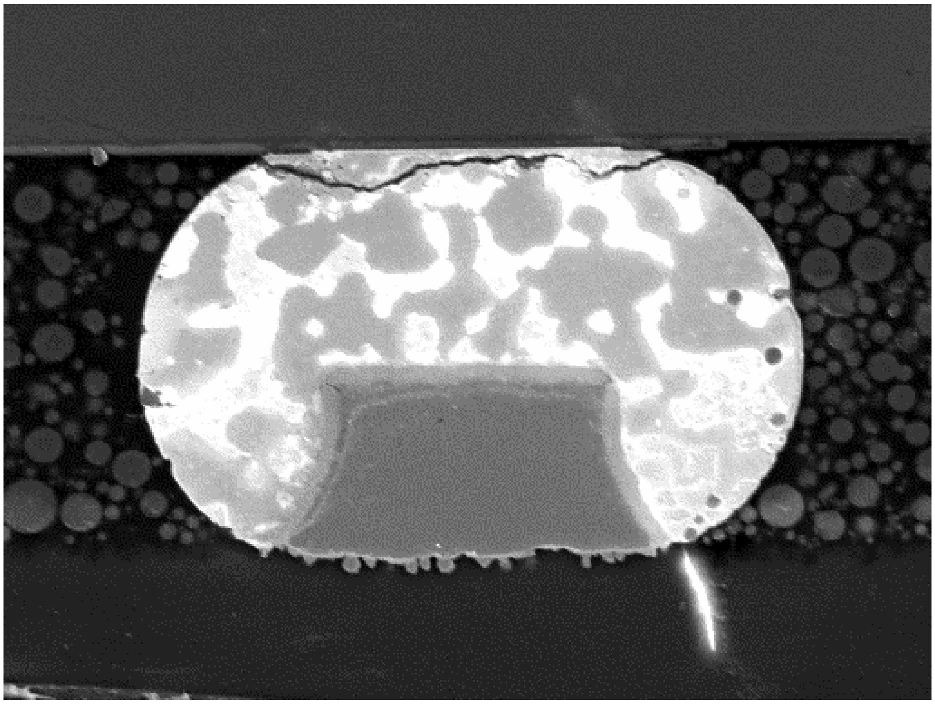
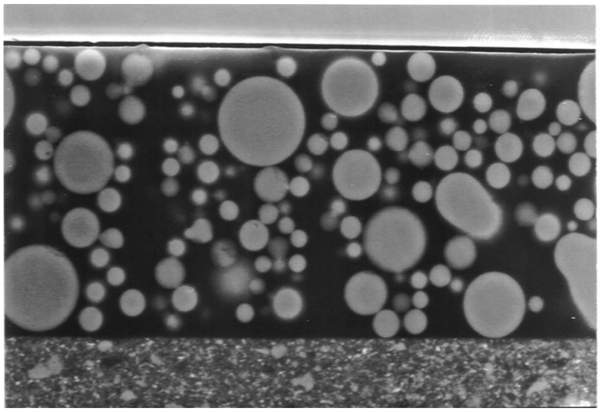


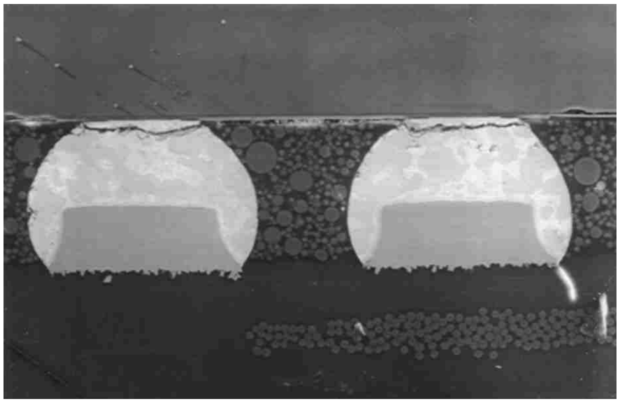
Figure 5.3 – Solder Joint Failure in a Flip Chip Package Due to Large Shear Strains

The typical underfill/die interface delamination failure in a flip chip assembly is shown in Figure 5.4(a). If interfacial cracks develop and propagate to the neighboring solder bumps, the previously described stress relief on the solder joints will be lost and the onset of solder joint fatigue cracking will be hastened (Shown in Figure 5.4b and 5.4c). At room temperature, high tensile normal stresses exist on the backside of the underflowed flip chip die (Figure 5.5), while compressive normal stresses are typically produced on the device side of the die containing the solder bump interconnections. These backside tensile stresses can lead to fracture (Figure 5.6), and are more severe for larger area die, larger thickness die, and die exposed to lower temperatures [157]. Fractures initiate at small flaws on the backside of the die have also been observed during the flip chip solder reflow process. Knowledge of the in-plane stress components and the interfacial (out-of-plane) shear stresses that occur at the die surface can be used to characterize underfill adhesion and reliability of the die passivation to underfill interface.

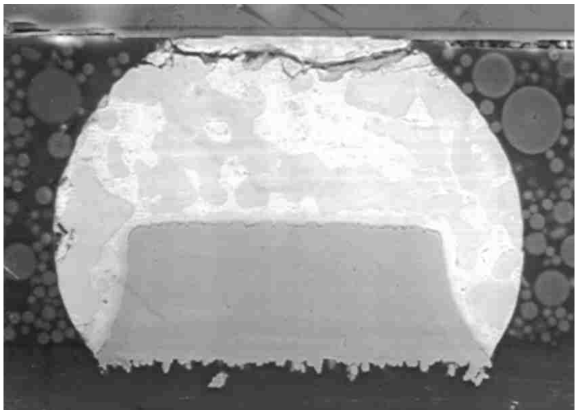
There are several additional reliability concerns with the latest generation of integrated circuit chips containing multiple copper/low-k high density interconnect layers, and minimizing the device side die stresses is especially important. The low-k dielectrics under development are often low modulus (soft) and porous, and have low fracture toughness. Thus, mechanical stresses imparted to the die surface by flip chip underfills (or wirebonding and molding) can lead to delaminations and/or cracking in the interlayer dielectric (ILD). The optimal flip chip packaging configuration for copper/low-k die is one which both minimizes die surface stresses and achieves



(a) Underfill/Die Interface Delamination Failure



(b) Interfacial Cracks Develop and Propagate to the Neighboring Solder Bumps



(c) Solder Joint Fatigue Cracking

Figure 5.4 – Underfill/Die Interface Delamination and Solder Joint Fatigue Failure

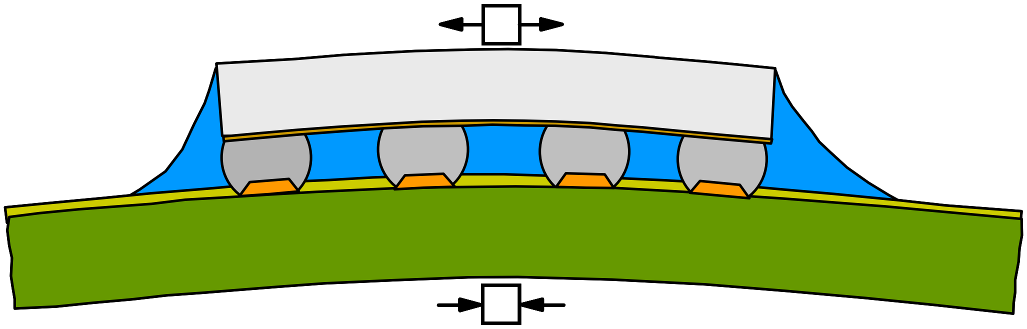


Figure 5.5 - Bending of a Flip Chip Assembly

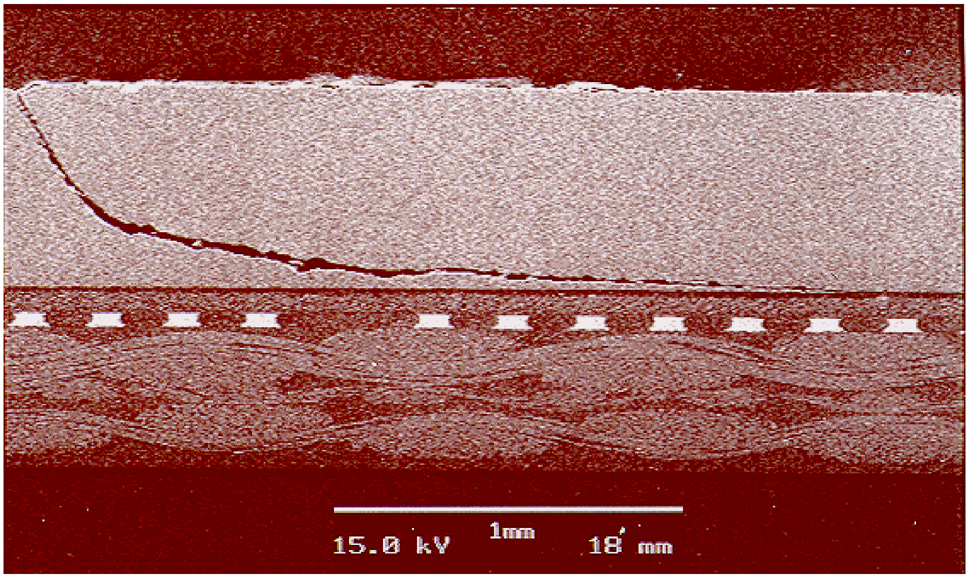

15.0 kV
1mm
18 mm

Figure 5.6 - Die Cracking

acceptable solder joint reliability in thermal cycling. For this reason, it is highly desirable to perform in-situ characterization of the in-plane stress components and the interfacial (out-of-plane) shear stresses that occur at the die surface in underfilled flip chip assemblies.

Stress sensing test chips are powerful tools for measuring in-situ stresses in electronic packages [90]. In prior work, investigators have used variations of the Sandia ATC04 test die to examine device side die stresses in flip chip on laminate assemblies [139, 141, 163]. In these studies, the wirebond ATC04 test chip was redistributed to have a full array of eutectic tin-lead solder balls, and the distribution of stress across the die surface and the variation of stress magnitudes with underfill material type has been studied. In addition, the buildup of stress during assembly cooldown after underfill cure has been observed. Finally, preliminary investigations on the variations in the die stresses during thermal cycling reliability tests have been performed.

As discussed above, typical failure modes in flip chip on laminate assemblies are delaminations between the silicon die and underfill (leading to solder ball fatigue), and backside (topside) die cracking due to assembly flexure. The previous work discussed above concern device side measurements made using (100) silicon test chips. The use of test chips fabricated in the (100) plane allow in-plane stresses to be characterized, but precludes the measurement of the interfacial (out-of-plane) shear stresses between the underfill layer and die surface. Such in-plane stress measurements can be useful for verification of finite element simulations. To further aid in investigation of flip chip failure phenomena, (111) silicon test chips that can be used to measure all of the die stress components including the interfacial shear stresses [23, 92, 167, 169] have developed. In previous studies, the authors have demonstrated the application of such chips for die stress characterization in molded quad flat packs [23], chip on board assemblies [167] and ceramic pin grid arrays [169]. In this work, (111) stress test chips are being used to measure die stress distributions in flip chip on laminate assemblies.

In my previous flip chip study [142, 194], the mechanical stresses present on the backside of the die at each stage of flip chip assembly process were investigated. Special backside bumped (111) silicon wirebond test chips were developed for this purpose. The backside die stress variation was observed during underfill curing, and nonlinear three-dimensional finite element models were developed to predict the tensile normal stress buildup during underfill cure. One of the most interesting results from this study was that a stress "overshoot" phenomenon was observed during the cooldown after cure. The maximum backside die stresses in the assembly were found to occur very quickly during the first 60 seconds of the cooldown; and the assembly then appeared to "relax". The mechanism believed to be responsible for the overshoot in the backside die stresses is differential cooling of the assembly. The backside of the die (location of the sensors) is exposed to the ambient air and cools more quickly than the inside of the assembly (solder balls and underfill), depending upon heat conduction and convection effects. When the temperature of the inside of the assembly "catches up" to the outside of the assembly, the stress levels on the backside of the die decrease. The observed overshoot of the backside tensile stresses occurring during cooldown typically peaked at 25-50% above the final steady state room temperature values. Therefore, the overshoot phenomenon is very important as it could lead to die cracking due to higher than expected transient peak tensile stress values resulting during the cooldown. It should be noted that this type of stress overshoot phenomena was not observed during curing and cooldown of Chip-on-Board packages where test chip sensors were encapsulated inside the package [167].

In this chapter, measurements of thermally induced stresses in flip chip on laminate assemblies are presented. The mechanical stresses on the device side of the flip chip die have been measured, where compressive normal stresses are developed due to bending of the flip chip on laminate assemblies. The utilized piezoresistive test chips were fabricated using (111) wafers, and the die where bumped with 200 $\mu$m (8 mil) pitch perimeter solder balls. The flip chip test die were then packaged, and die surface stresses were measured throughout the assembly process. Transient die stress measurements have been made during underfill cure, and the room temperature die stresses in final cured assemblies have been compared for several different underfill encapsulants. The experimental stress measurements in the flip chip samples were also correlated with finite element predictions for the tested configurations. In addition, stress variations have been monitored in the assembled flip chip die as the test boards were subjected to slow temperature changes from -40 to +150 $^{o}$C for three different underfill materials. Using these measurements and numerical simulations, valuable insight has been gained on the effects of assembly variables and underfill material properties on the reliability of flip chip packages.

## 5.2 Stress Equations for Test Chip Applications

Using the expressions generated through application of eq. (3.15) to each of the eight sensing elements, the following expressions for individual stress components were used for this study [90]:

$$\sigma'_{11} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)\,B_3^p - (B_1^p + B_2^p)\,B_3^n]}$$

$$\sigma'_{22} = -\frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{2[(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n]} + \frac{B_3^p\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] - B_3^n\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)\,B_3^p - (B_1^p + B_2^p)\,B_3^n]}$$

$$\sigma'_{33} = \frac{-(B_1^p + B_2^p)\left[\frac{\Delta R_1}{R_1} + \frac{\Delta R_3}{R_3} - 2\alpha_1^n T\right] + (B_1^n + B_2^n)\left[\frac{\Delta R_5}{R_5} + \frac{\Delta R_7}{R_7} - 2\alpha_1^p T\right]}{2[(B_1^n + B_2^n)\,B_3^p - (B_1^p + B_2^p)\,B_3^n]}$$

$$\tag{5.1}$$

$$\sigma'_{13} = \frac{\sqrt{2}}{8}\left[\frac{(B_1^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] - (B_1^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n}\right]$$

$$\sigma'_{23} = \frac{\sqrt{2}}{8}\left[\frac{-(B_1^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] + (B_1^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n}\right]$$

$$\sigma'_{12} = \frac{-(B_3^p - B_2^p)\left[\frac{\Delta R_4}{R_4} - \frac{\Delta R_2}{R_2}\right] + (B_3^n - B_2^n)\left[\frac{\Delta R_8}{R_8} - \frac{\Delta R_6}{R_6}\right]}{2[(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n]}$$

Superscripts n and p are used on the combined piezoresistive coefficients to denote n-type and p-type resistors, respectively. From the expressions in eq. (5.1), it is clear that the extraction of the three shear stresses $\sigma'_{12}, \sigma'_{13}, \sigma'_{23}$ from the measured resistance changes is temperature compensated (independent of T). Evaluation of the individual normal stress components requires measurement of the normalized resistance changes of the sensors and the temperature change T experienced by the sensing elements. The temperature coefficients of resistance $\alpha_1, \alpha_2, \ldots$ must also be known for each doping type. They can be obtained using thermal cycling calibration experiments where the resistances of the sensing elements are monitored as a function of temperature. The measured resistance change versus temperature response is fit with a general polynomial to extract the temperature coefficients of resistance. Typically, only first and second order temperature coefficients are needed.

Jaeger, et al. [184, 191] have previously discussed the difficulties in obtaining accurate temperature change values over the long time spans typical of measurements made with piezoresistive sensors. In addition, it has been demonstrated that temperature measurement errors of as little as 0.25 $^{o}$C can cause serious errors in the experimental values of the stresses extracted with non temperature compensated formulas such as the first three expressions in eq. (5.1). Thus, it has been recommended to restrict measurement efforts to temperature compensated stress combinations where the temperature coefficient of resistance terms cancel in the stress extraction equations. Besides the three shear stresses, the in-plane normal stress difference can be shown to be an additional temperature compensated quantity using the first two expressions in eq. (5.1):

$$\sigma'_{11} - \sigma'_{22} = \frac{(B_3^p - B_2^p)\left[\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right] - (B_3^n - B_2^n)\left[\frac{\Delta R_5}{R_5} - \frac{\Delta R_7}{R_7}\right]}{[(B_2^p - B_1^p)\,B_3^n + (B_1^p - B_3^p)\,B_2^n + (B_3^p - B_2^p)\,B_1^n]} \tag{5.2}$$

The results in eqs. (5.1, 5.2) assume that the temperature coefficients of resistance are well matched for sensing elements of the same doping type. In addition, a calibration procedure must be performed to determine all six of the combined piezoresistive parameters $B_1^n$, $B_2^n$, $B_3^n$, $B_1^p$, $B_2^p$, $B_3^p$ prior to using the sensor. A combination of uniaxial and hydrostatic pressure testing can be utilized to complete this task [90, 92].

## 5.3 Stress Test Chips

A series of (111) silicon stress test die have developed for use in flip chip investigations. The chip designs incorporate arrays of the optimized eight-element dual-polarity sensor rosettes (Figure 4.1) that are capable of measuring the complete state of stress at the die surface (including the interfacial shear stresses). Figure 5.7 shows the layout of the FC200 flip chip test die used in this study. The basic chip image has dimensions of 5 x 5 mm (200 x 200 mils), and contains 200 $\mu$m (8 mil) pitch perimeter solder bumps. This chip includes 11 eight-element sensor rosettes, a diode for temperature measurement, and an eight-bit fuse style chip ID. A close up photograph of one of the FC200 sensor rosettes is shown in Figure 5.8. Analogous perimeter bumped chips of other sizes (2.5 x 2.5 mm and 10 x 10 mm) have also been fabricated.

The eight rosette elements are routed to the die bond pads in a manner that allows them to be configured as four two-element half-bridges in order to simplify the resistor change measurements. A fully ion-implanted bipolar process has been used to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Wafer bumping was performed using the Flip Chip Technologies (Kulicke and Soffa) process with an aluminum, nickel vanadium, and copper under bump metallurgy

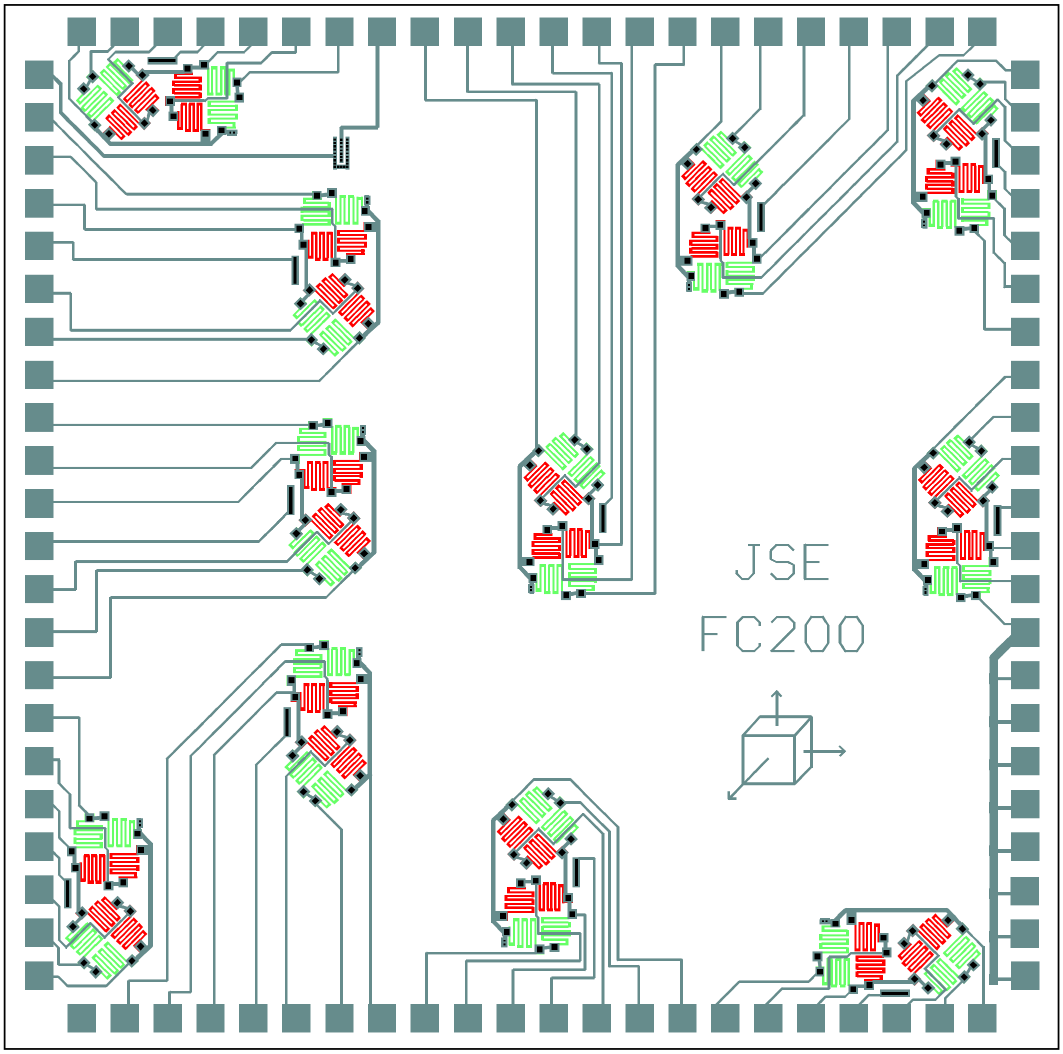


Figure 5.7 - FC200 Flip Chip Test Die (5 x 5 mm)

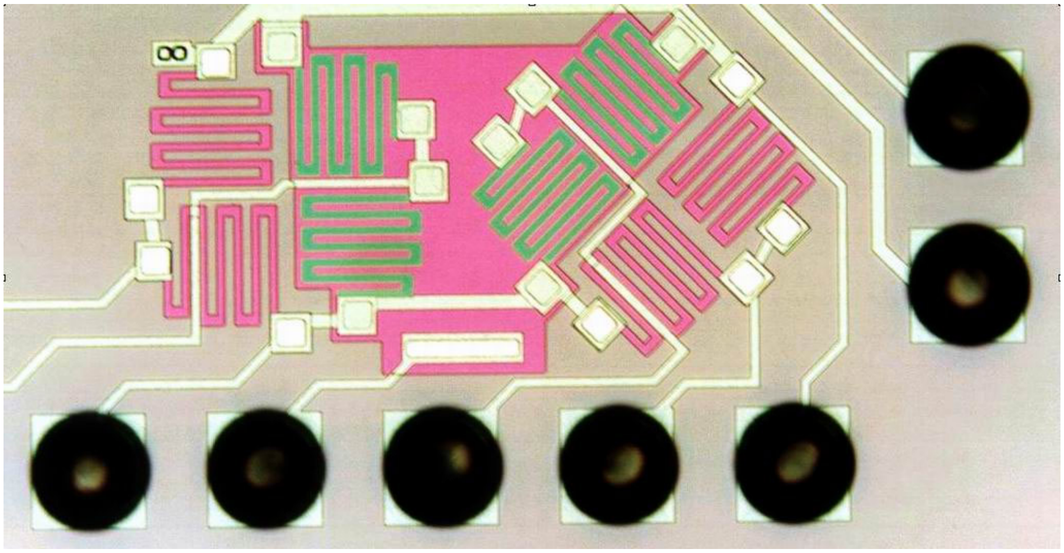


Figure 5.8 - Photograph of FC200 Sensor Rosette

and 63Sn-37Pb solder alloy. The die pads have dimensions of 125 x 125 μm (5 x 5 mils), with a 75 μm (3 mil) spacing between pads. As shown in Figures 5.7 and 5.8, the corner bumps were not included in the perimeter arrays solder ball arrays. This intentional omission eases PCB routing challenges and removes the least reliable solder joints from the design.

When assembled in an underfilled flip chip configuration, the test chips have the piezoresistive sensors electrically accessible through the solder balls. Using the theoretical expressions in eqs. (5.1, 5.2), the stresses can be calculated from the measured resistance changes. The piezoresistive coefficients $B_1$, $B_2$ and $B_3$ present in the rosette equations were obtained for the test chips in the work using four-point bending and hydrostatic calibration methods. The average experimentally measured values are listed in Table 5.1. Further details on the calibration tests can be found in references [90, 92].

| Piezoresistive Coefficients FC200 Test Chip ($TPa^{-1}$) | | | | | |
|---|---|---|---|---|---|
| $B_1^p$ | $B_2^p$ | $B_3^p$ | $B_1^n$ | $B_2^n$ | $B_3^n$ |
| 459.0 | 93.6 | -452.6 | -148.8 | 140.5 | -75.5 |

Table 5.1 - Calibrated Piezoresistive Coefficients

## 5.4 Test Board Assembly

The FC200 stress test chip wafers have a thickness of 625 μm (25 mils). In this study, wafers thinning process has not performed, so that the nominal dimensions of each test chip were 5.0 x 5.0 x 0.625 mm (200 x 200 x 25 mils). Test boards were designed and fabricated for preparation of the FC200 flip chip on laminate assemblies.

Each test board was designed to accommodate a single centrally bonded FC200 stress test chip and its 88 solder bumps along the perimeter of the die. The printed circuit board was designed using Lavenir software, and Figure 5.9 shows the layout of the PCB design. The test board dimensions were 114 x 83 x 0.75 mm, and they were fabricated using FR4-06 prepreg, and copper traces with an electroless Nickel immersion Gold finish. Photos of an assembled test board and an underfilled FC200 stress die are shown in Figure 5.10. The soldermask opening under the chip on the test board was designed with the so-called "finger" approach as shown in Figure 5.11, so that the ends of the PCB traces were used as bonding points for the flip chip solder balls.

The test boards were assembled at the SMT Line at Auburn University. Figure 5.12 schematically shows the steps of flip chip assembly and underfill process. Prior to placement, the test chip solder balls were dipped into a tacky, no-clean solder flux. The die were then aligned and placed on the test substrates using a Siemens SIPLACE $F^5$ high speed pick and place machine (Figure 5.12). Reflow was performed under a Nitrogen atmosphere in a Heller 1700 reflow oven.

After solder reflow, initial sensor resistance data were measured to establish the "zero stress state" sensor resistance values. In reality, there are small stresses present in the chip due to the reflow process. In our previous flip chip studies, we have measured the sensor resistances before and after reflow (die were manually probed before reflow), and then evaluated the stresses due to just the reflow process. The magnitudes of the measured die normal stresses due to die attachment were found to be universally small (e.g. 0-2 MPa). In this investigation, the die stresses due to solder reflow have been neglected to avoid the tedious process of probing the bumped stress chips before

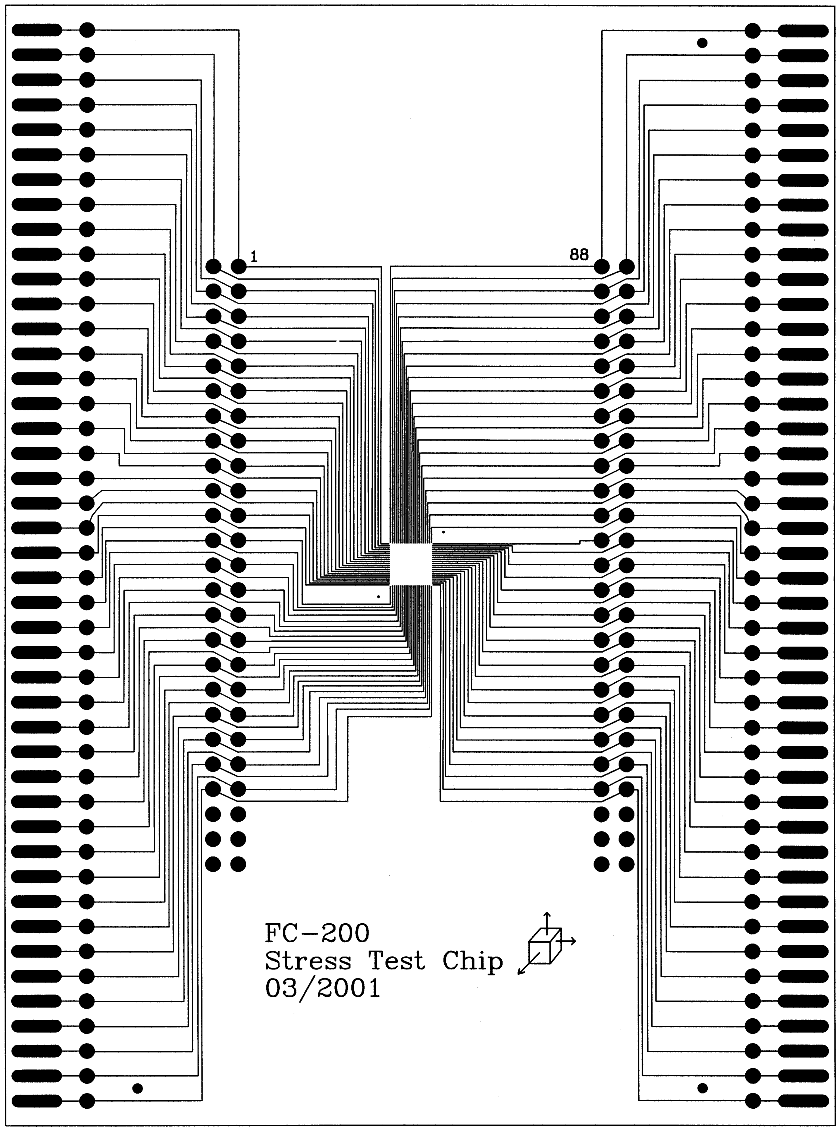

1
88
FC–200
Stress Test Chip
03/2001

Figure 5.9 - PCB Design Layout for FC200 Flip Chip Assembly

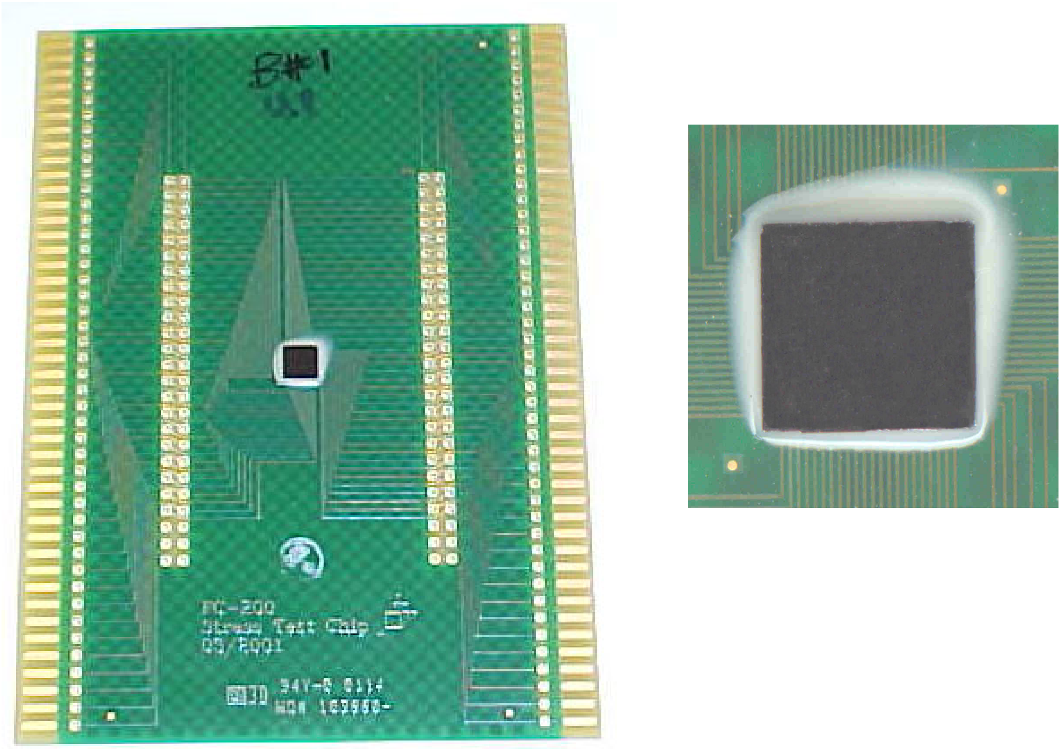

B#1
FC-200
Stress Test Chip
03/2001
94V-0 0114

Figure 5.10 - Photos of an Assembled Test Board and Test Chip

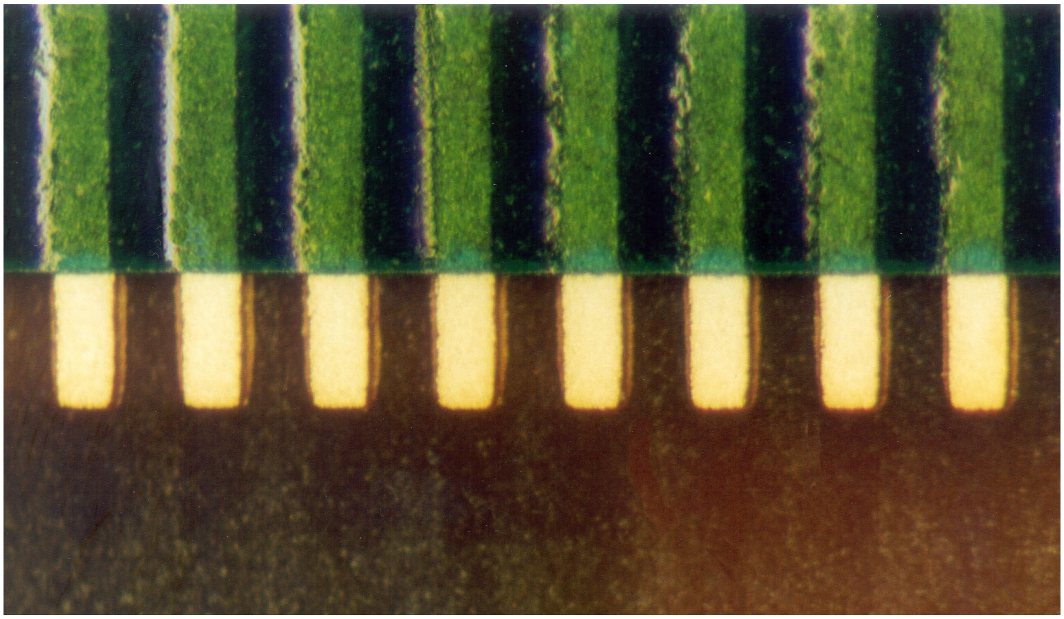


Figure 5.11 - Finger Soldermask Design

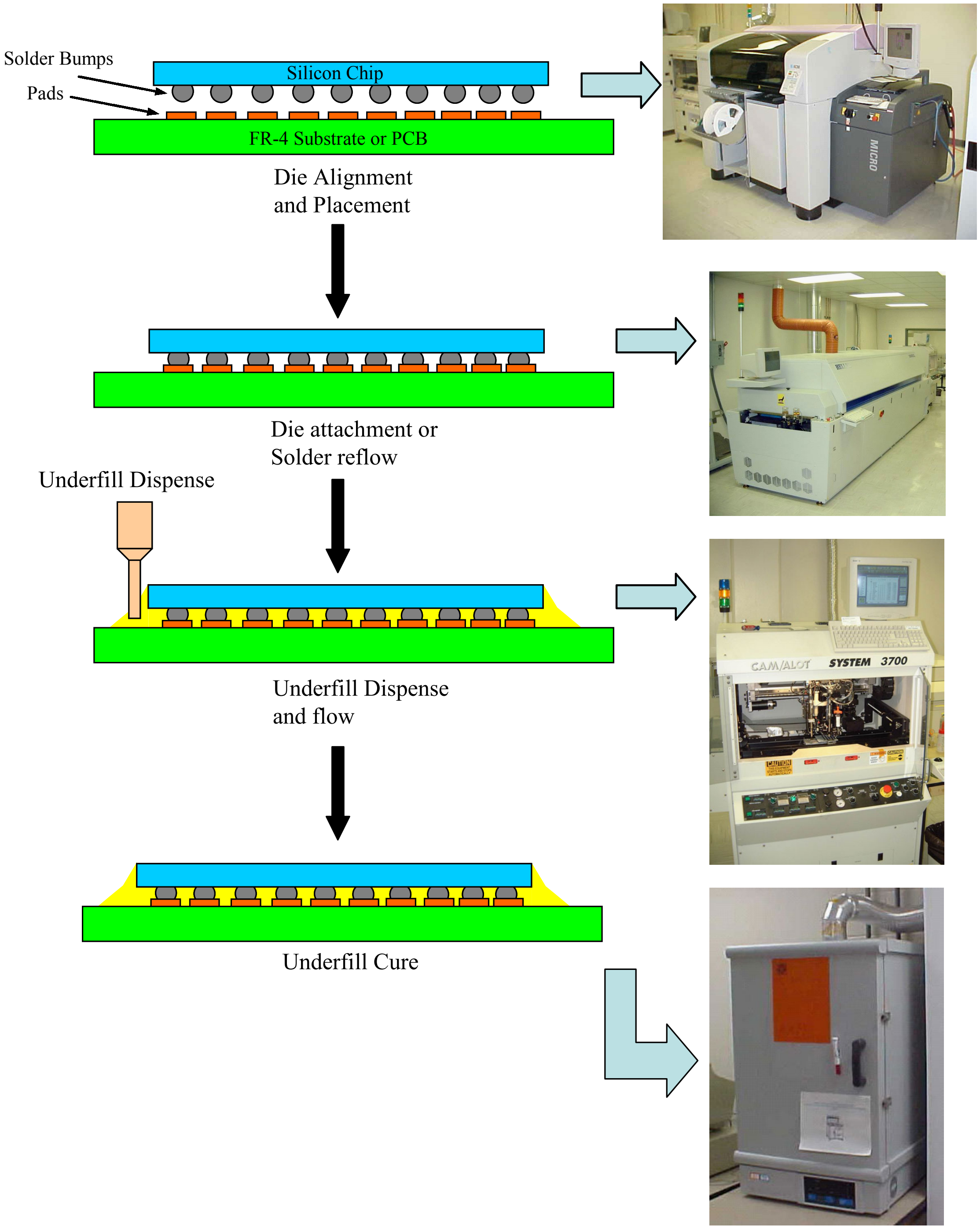
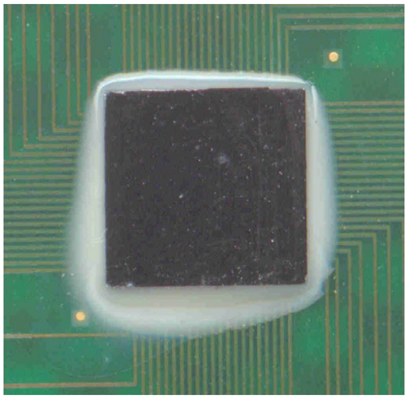

Solder Bumps
Pads
Silicon Chip
FR-4 Substrate or PCB
Die Alignment and Placement
MICRO
Die attachment or Solder reflow
Underfill Dispense
Underfill Dispense and flow
CAM/ALOT
SYSTEM 3700
CAUTION
Underfill Cure

Figure 5.12 – The Flip Chip Assembly and Underfilling Process Steps

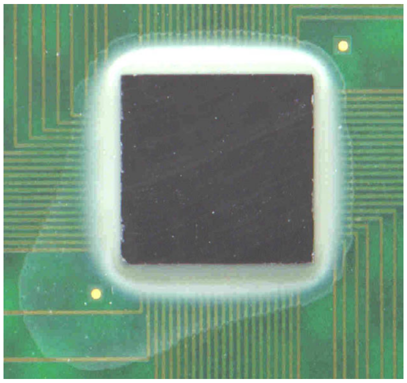
assembly. With this approach, the initial resistance values after reflow were assumed to be zero stress values, and all stress measurements are truly indicating the change in the die stress between the current state (where the final resistance values are measured) and the initial state (after reflow). Given the small magnitudes of the die stresses due to the reflow process, this approximation seems quite reasonable.

The test board design allowed for 3 options for electrical connection to the FC200 stress sensors including edge connector, through holes for soldering individual wires, or through holes for soldering a ribbon cable connector. For both flexibility and ease of implementation in a variety of thermal environments, edge connectors were used for all connections to the test assemblies. All resistance measurements were completed using a PC-based data acquisition system incorporating a GPIB scanning system and digital multimeters. After measuring the initial resistances after solder joint reflow, the test boards were subjected to an 8 hour dehydration bake to avoid any voids or bubbles in the underfill encapsulant due to moisture evolution from the substrate during the underfill cure cycle.

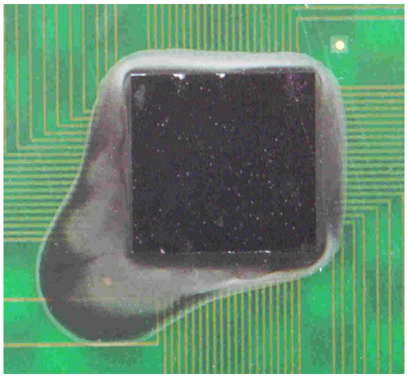
Three different capillary flow underfill encapsulant materials from different vendors were used in the FC200 stress chip experiments. Photographs of assemblies with the three different underfills are shown in Figure 5.13. Each material was a snap/quick cure underfill requiring 5-30 minutes of high temperature curing. The glass transition temperatures, coefficients of thermal expansion, and recommended cure conditions for the three underfills are given in Table 5.2. The underfills were dispensed at near one corner of the die using a CAM/ALOT 3700 dispensing system. The work



(a) Flip Chip Assembly with Underfill UF1



(b) Flip Chip Assembly with Underfill UF2



(c) Flip Chip Assembly with Underfill UF3

Figure 5.13 – Flip Chip Assembly with Different Underfills

holder supporting the assemblies was heated to 95 °C prior to underfill dispense, and the fast flow materials completely underfilled the die with one dot dispensed at the one corner.

| Underfill Material | $T_g$ | $\alpha$ (1/°C) (Below Tg) | Recommended Cure Conditions |
|---|---|---|---|
| UF1 | 130 °C | $35 \times 10^{-6}$ | 165 °C / 5 min |
| UF2 | 146 °C | $48 \times 10^{-6}$ | 165 °C / 10 min |
| UF3 | 137 °C | $25 \times 10^{-6}$ | 150 °C / 30 min |

Table 5.2 - Underfill Properties (Vendor Specified)

After dispense, the underfills were cured under the specified conditions in a box oven. Thermocouples were used to verify that proper durations of oven exposure were utilized and that the recommended cure temperature conditions were actually achieved within the underfill material. The transient sensor resistances were monitored during the cure cycle. After final assembly was completed, the sensor resistances were also measured at room temperature, and as a function of temperature during a slow change from -40 to +150 °C. Using the measured resistance change data from each step of the assembly procedure, the die stress variations were easily calculated using eqs. (5.1, 5.2).

A total of 25 specimens were prepared for each underfill encapsulant. For each board and FC200 chip, the 11 rosette sites (88 resistors) were monitored at each stress evaluation point. Figure 5.14 shows the rosette site designations for the resistance/stress measurements.

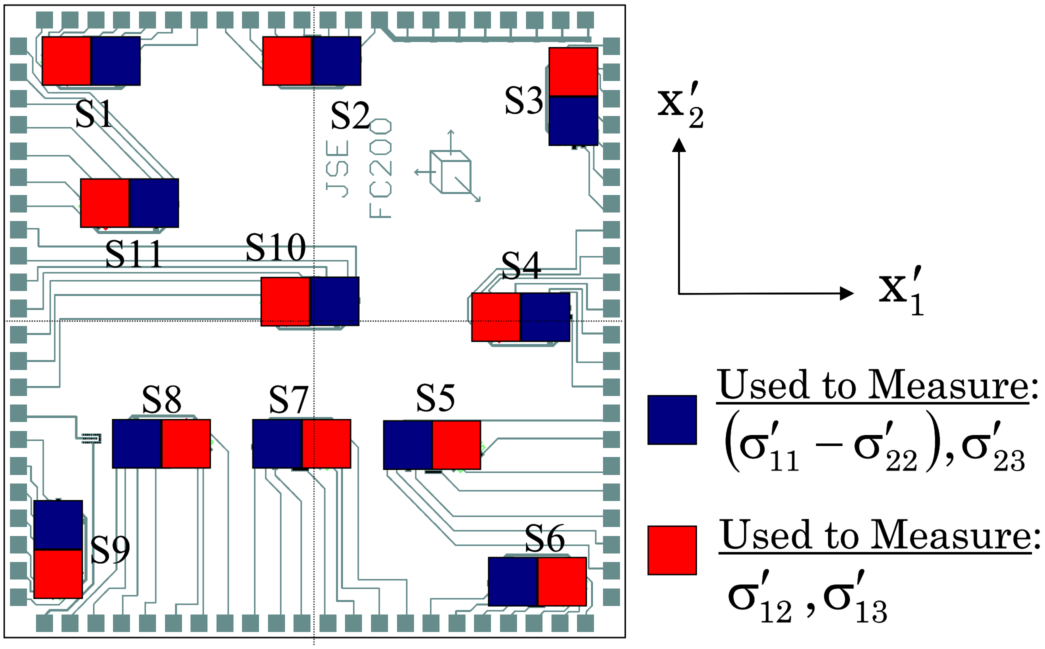

S1
S2
S3
JSE
FC200
S11
S10
S4
S8
S7
S5
S9
S6
$x_2'$
$x_1'$
Used to Measure:
$\left(\sigma_{11}' - \sigma_{22}'\right), \sigma_{23}'$
Used to Measure:
$\sigma_{12}', \sigma_{13}'$

Figure 5.14 - Rosette Sites for Stress Measurement

## 5.5 Flip Chip Stress Measurements

The FC200 test chip assemblies have been utilized to measure the die stresses in flip chip on laminate assemblies during underfill cure, and as a function of temperature after cure. Using these measurements and ongoing numerical simulations, valuable insight has been gained on processing induced variations and failure phenomena in flip chip on laminate assemblies.

### 5.5.1 Stress Variation During Underfill Cure

As mentioned previously, transient sensor resistances were monitored during the entire underfill encapsulant cure process. Typical results for the underfill temperature and stress histories during underfill curing (5 minute snap cure at 165 $^{o}$C for material UF1) are shown in Figures 5.15-5.21. Figure 5.15 illustrates the underfill temperature as monitored by a thermocouple placed within the underfill in one of the samples. It can be seen that it takes the underfill within the flip chip assembly approximately 3 minutes to come up to the 165 $^{o}$C temperature of the cure oven. For this reason, the samples were actually left in the oven for at least 8 minutes (480 seconds) to insure that the 5-minute snap cure condition at 165 $^{o}$C was realized.

Figure 5.16 shows the variation of the in-plane normal stress difference with time in one of the assemblies (Board 11, Underfill UF1) at the rosette located at site 2 (on the die boundary at the midpoint of one of the die sides). This site is the location of the maximum value on the die surface (see later measurement results and finite element simulation results for justification). Likewise, Figure 5.17 shows the variation of the in-plane shear stress with time in one of the assemblies (Board 30, Underfill UF1) at the

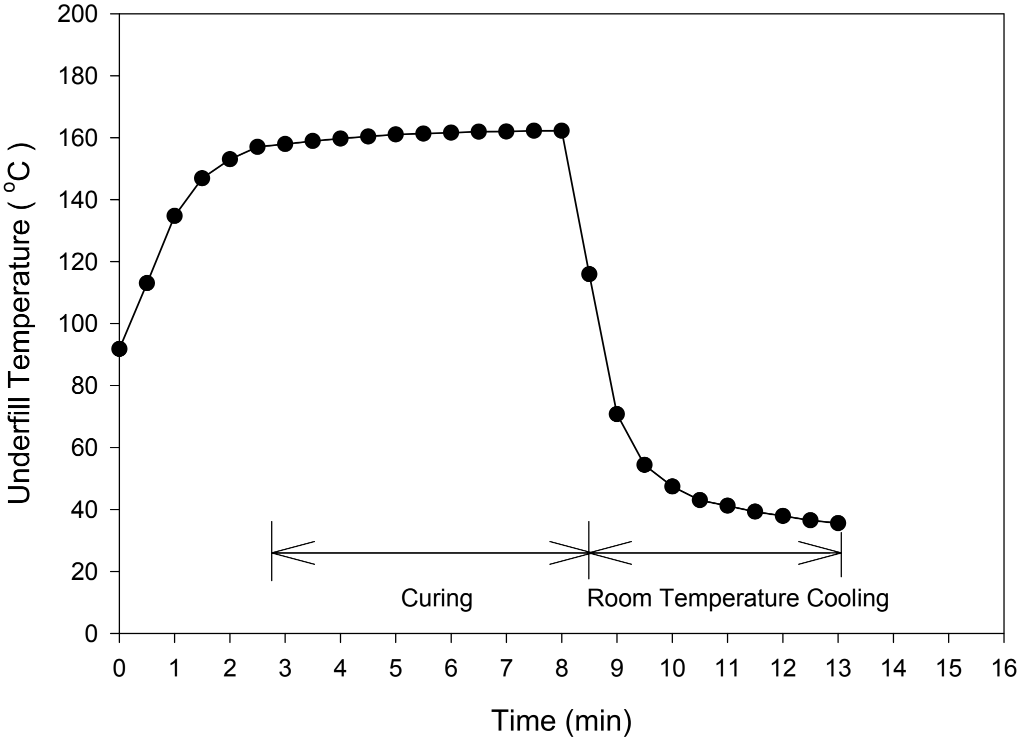


Figure 5.15 - Underfill Temperature Variation with Time in the Cure Oven

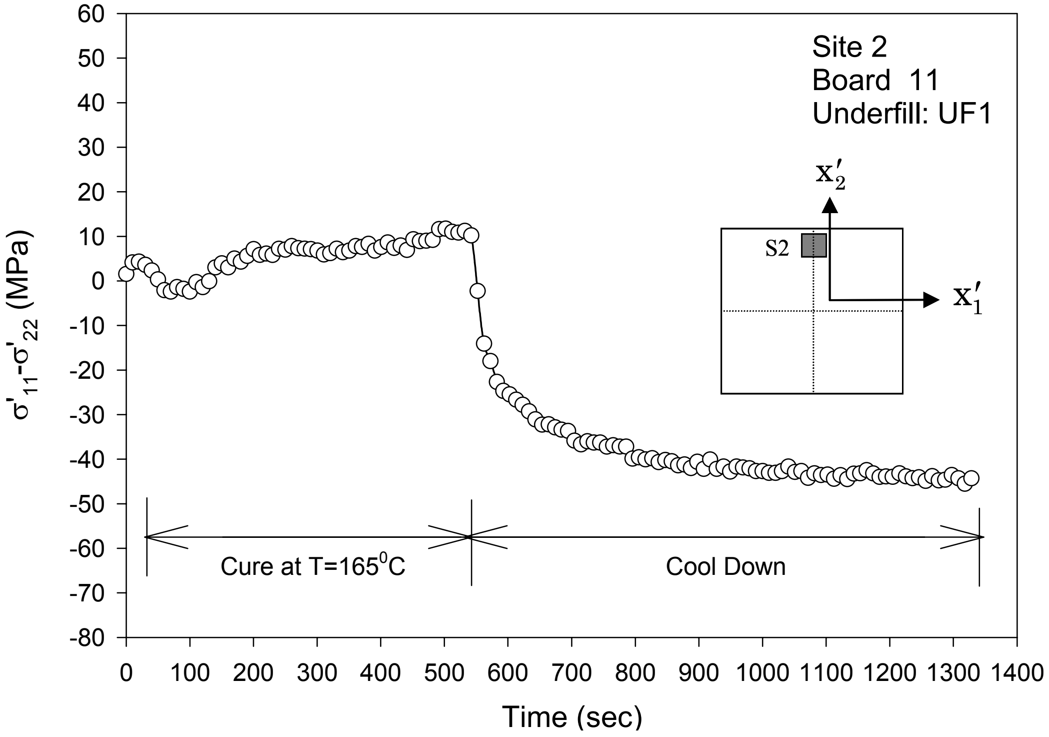


Figure 5.16 - Typical Normal Stress Variation During Underfill Cure

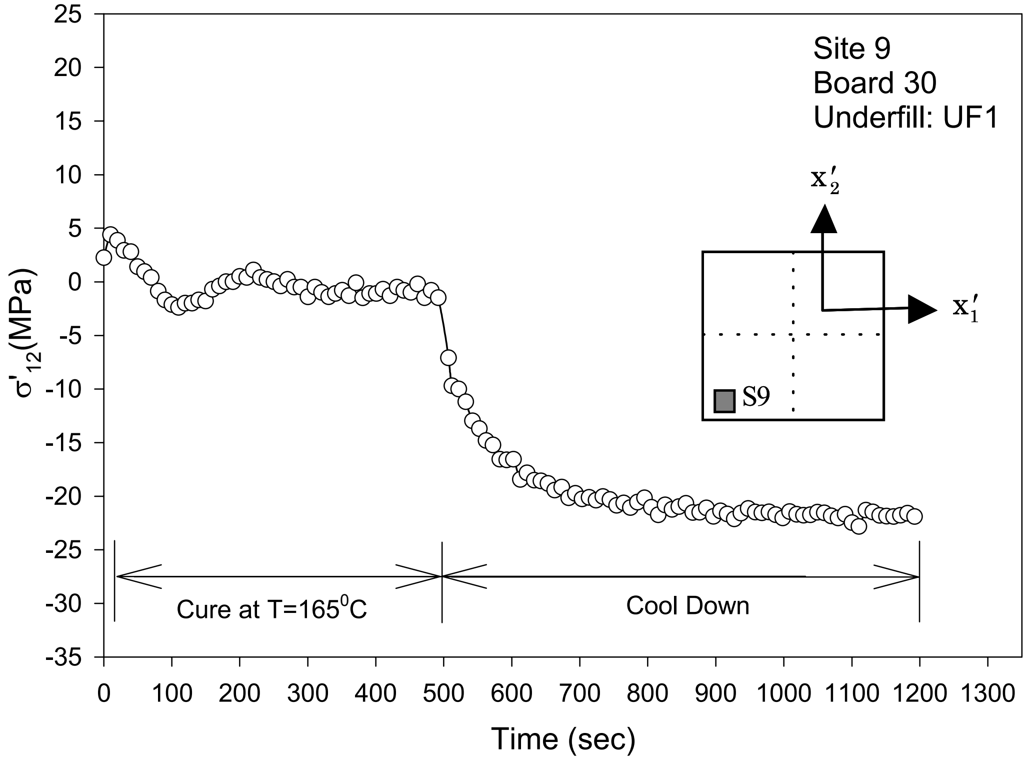


Figure 5.17 - Typical In-Plane Shear Stress Variation During Underfill Cure

rosette located at site 9 (in one of the die corners). Again, this corner site is expected to be the location of the maximum shear stress value (in magnitude) on the die surface.

Examining either Figure 5.16 or 5.17, we can attempt to explain the observed stress history during the cure cycle. At time t = 0, the boards have just been removed from the hot stage (95 $^{o}$C) in the CAM/ALOT 3700 dispensing system and carefully inserted in the data acquisition system edge connector and placed in the cure oven. The curing stress measurements were started as soon as the oven door was closed. At this point, the underfill encapsulant is still liquid, the assembly temperature is approximately 95 $^{o}$C (underfill dispense temperature), and the die stresses are nearly zero. The stresses at t = 0 should not be exactly zero because there will be some die stress produced in the assembly due to the change from the room temperature of 23 $^{o}$C (where the initial sensor resistances were measured) and the 95 $^{o}$C temperature of the assembly where measurement of the transient sensor resistances is initiated. These small stresses at t = 0 are due to the mismatch in expansion coefficient between the die and PCB, and the fact that the solder balls prevented either material from freely expanding.

During the first 8 minutes (480 seconds) of exposure to the 165 $^{o}$C temperature in the cure oven, the assembly temperature gradually is heated from 95 to 165 $^{o}$C. It is seen that this temperature change is accompanied by small changes in the stresses on the die surface contacting the underfill. These are likely due mostly to the encapsulant shrinkage during cure and other complicated changes in the polymeric underfill material as it hardens. All of the observed stress variations during the 165 $^{o}$C cure are “S” shaped, suggesting multiple types of material changes are happening simultaneously. Although no modeling of this complex behavior is attempted here, there have been several recent investigations that have explored stress prediction in flip chip assemblies during underfill cure [153-155].

Upon completion of the hold at 165 $^{o}$C, the boards were removed from the oven and allowed to cool on a flat table (chip side facing up) in a room temperature environment. As seen in Figures 5.16-5.17, the majority of the final assembly die stresses are built up during the cooling of the flip chip assembly after cure, where the underfill encapsulant is fully hardened and can provide a significant stiffness to cause the flip chip assembly to bend. The final die stress component magnitudes resulting during cooldown were typically observed to be 5-10 times larger than the maximum values observed while the sample was in the oven during the 165 $^{o}$C cure cycle. Unlike our earlier cure stress measurements on the backside of the flip chip die [142], no stress "overshoot" phenomena was observed for the device surface during cooldown. These results further support our hypothesis in reference [142] that the observed tensile stress overshoot on the die backside is due to differential cooling of the assembly.

The stress histories during underfill curing for other two underfill materials (UF2 and UF3) are shown in Figures 5.18-5.21. The variations of the in-plane normal stress difference with time for underfill UF2 (10 minute snap cure at 165 $^{o}$C) and for underfill UF3 (30 minute cure at 150 $^{o}$C) are shown in Figures 5.18 and 5.19, respectively. Similarly, the variations of the in-plane shear stress with time for underfill UF2 and for underfill UF3 are shown in Figures 5.20 and 5.21, respectively.

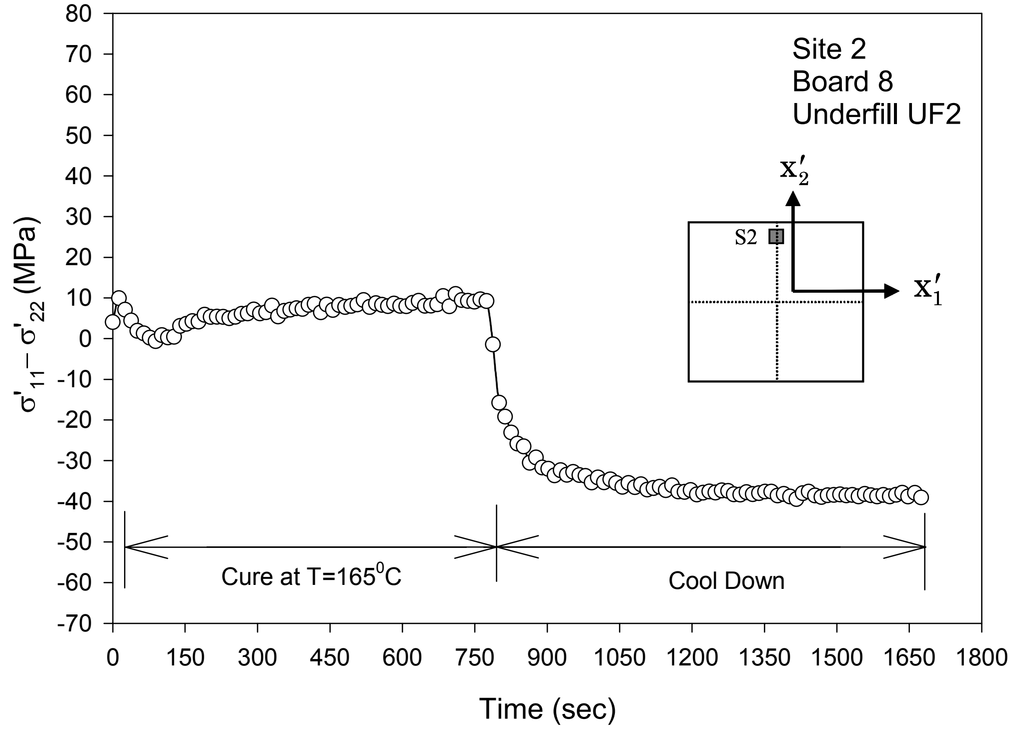


Figure 5.18 - Typical Normal Stress Variation During Underfill Cure for Underfill UF2

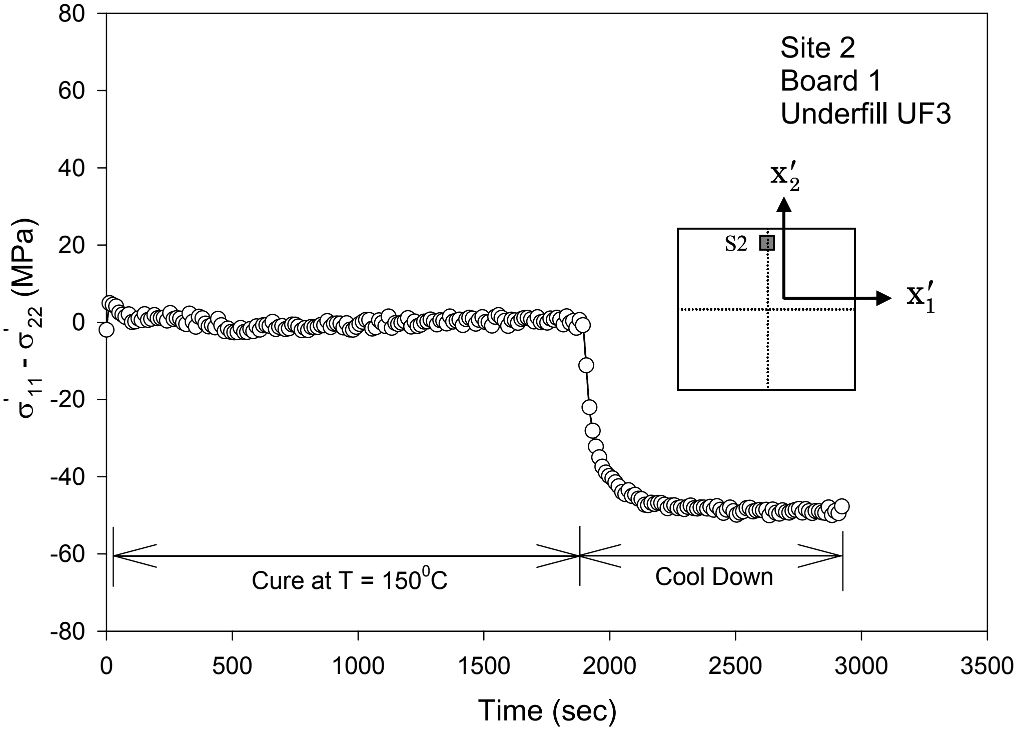


Figure 5.19 - Typical Normal Stress Variation During Underfill Cure for Underfill UF3

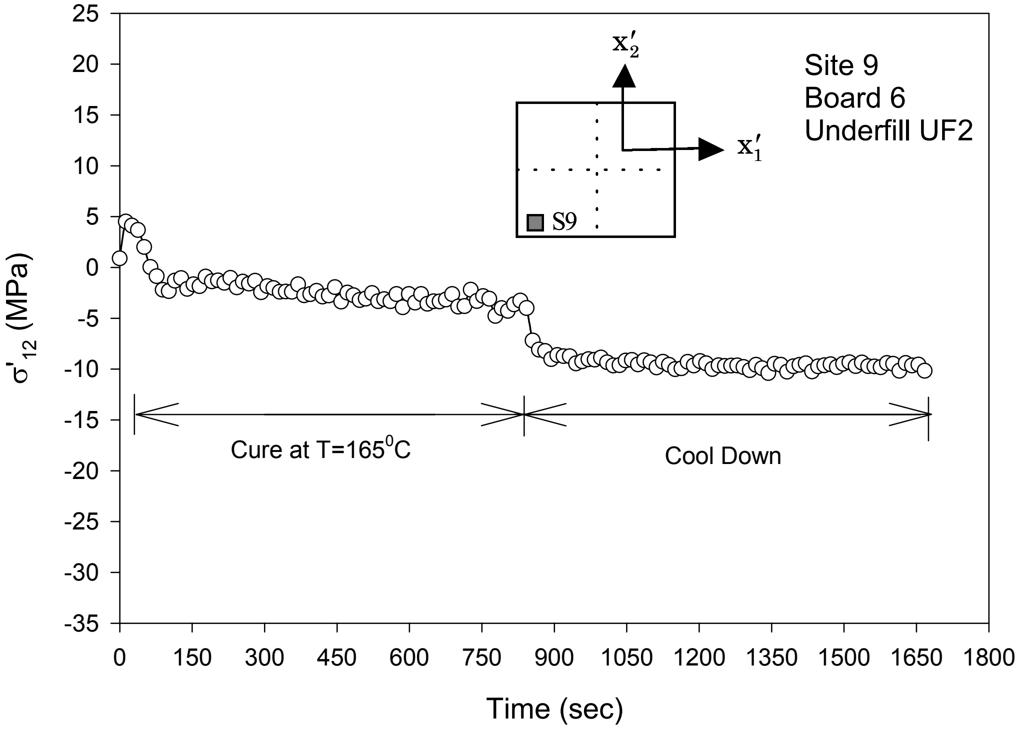


Figure 5.20 - In-Plane Shear Stress Variation During Underfill Cure for Underfill UF2

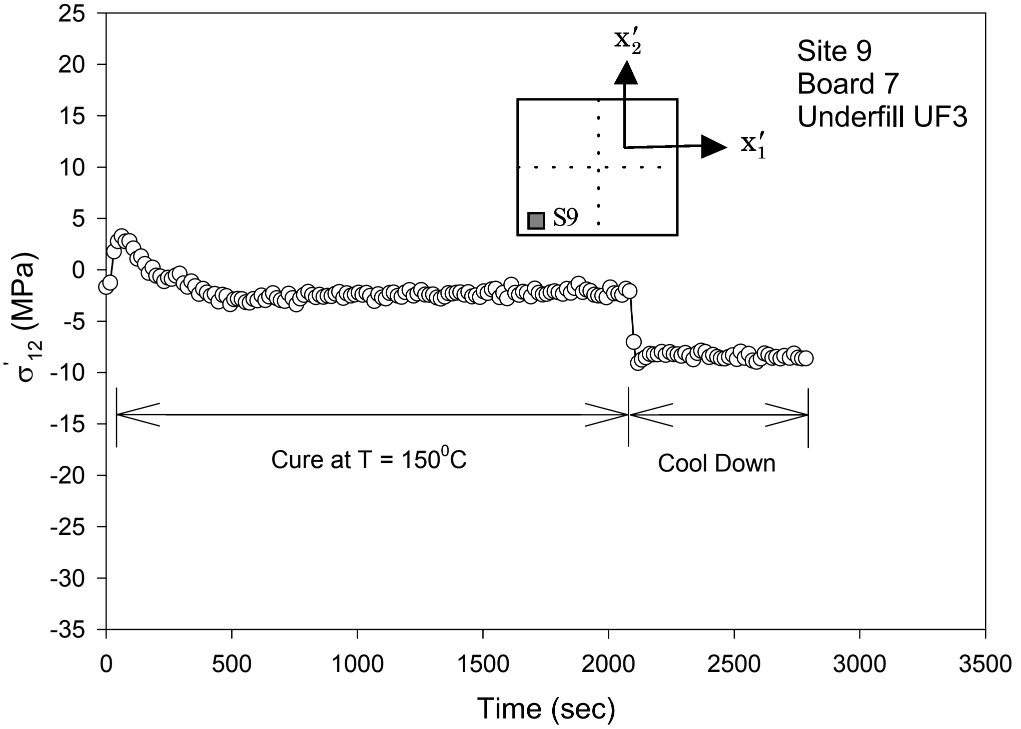


Figure 5.21 - In-Plane Shear Stress Variation During Underfill Cure for Underfill UF3

### 5.5.2 Stresses After Underfill Encapsulation

After underfill cure and cooldown, the final assembly room temperature die stresses were characterized. In this case, the initial and final sensor resistance measurements used to evaluate the stresses were both made at room temperature (23 °C). Thus, all thermal errors in application of the sensors will be minimized (T = 0). Figures 5.22-5.27 show the measured data for the in-plane normal stresses $\sigma'_{11}$ and $\sigma'_{22}$, in-plane normal stress difference $(\sigma'_{11} - \sigma'_{22})$, in-plane shear stress $\sigma'_{12}$, and out-of-plane shear stresses $\sigma'_{13}$ and $\sigma'_{23}$, respectively. At every rosette site in these plots, results are given for each of the 3 underfill encapsulants. The values beside each rosette site indicate the average and standard deviation from the 25 specimens used for each encapsulant.

As expected for an encapsulated die surface, the average in-plane normal stresses $\sigma'_{11}$ and $\sigma'_{22}$ were highly compressive over the entire die surface. The magnitudes were quite different for the three underfill materials, with the compressive die stresses for UF3 being the highest, followed by the stresses for UF2 and UF1, respectively. There is no single material property of the underfill that solely determines the die in-plane normal stress magnitudes. However, several properties including the elastic modulus, coefficient of thermal expansion, and glass transition temperature are known to make significant contributions to the magnitudes of the underfill encapsulation-induced die stress. For the materials in question, the elastic modulus has been characterized as a function of temperature by uniaxial testing using a microscale tension-torsion testing machine [156]. As shown in Figure 5.28, the elastic modulus of material UF3 is significantly higher than the other two materials at all temperatures. While this leads to higher die in-plane normal

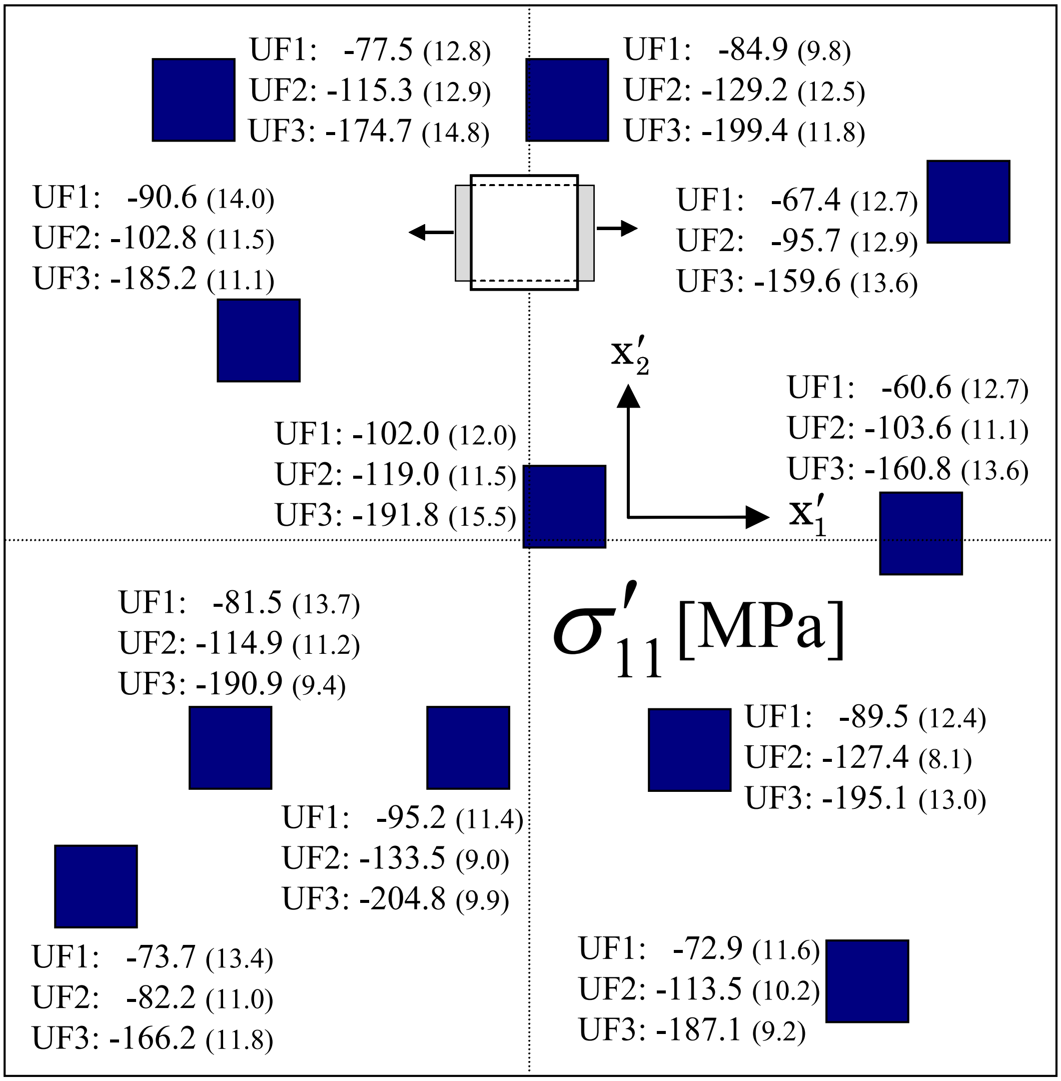

UF1: -77.5 (12.8)
UF2: -115.3 (12.9)
UF3: -174.7 (14.8)
UF1: -84.9 (9.8)
UF2: -129.2 (12.5)
UF3: -199.4 (11.8)
UF1: -90.6 (14.0)
UF2: -102.8 (11.5)
UF3: -185.2 (11.1)
UF1: -67.4 (12.7)
UF2: -95.7 (12.9)
UF3: -159.6 (13.6)
x'2
UF1: -60.6 (12.7)
UF2: -103.6 (11.1)
UF3: -160.8 (13.6)
UF1: -102.0 (12.0)
UF2: -119.0 (11.5)
UF3: -191.8 (15.5)
x'1
UF1: -81.5 (13.7)
UF2: -114.9 (11.2)
UF3: -190.9 (9.4)
σ'11 [MPa]
UF1: -89.5 (12.4)
UF2: -127.4 (8.1)
UF3: -195.1 (13.0)
UF1: -95.2 (11.4)
UF2: -133.5 (9.0)
UF3: -204.8 (9.9)
UF1: -73.7 (13.4)
UF2: -82.2 (11.0)
UF3: -166.2 (11.8)
UF1: -72.9 (11.6)
UF2: -113.5 (10.2)
UF3: -187.1 (9.2)

Figure 5.22 - Average Stresses after Underfill Cure

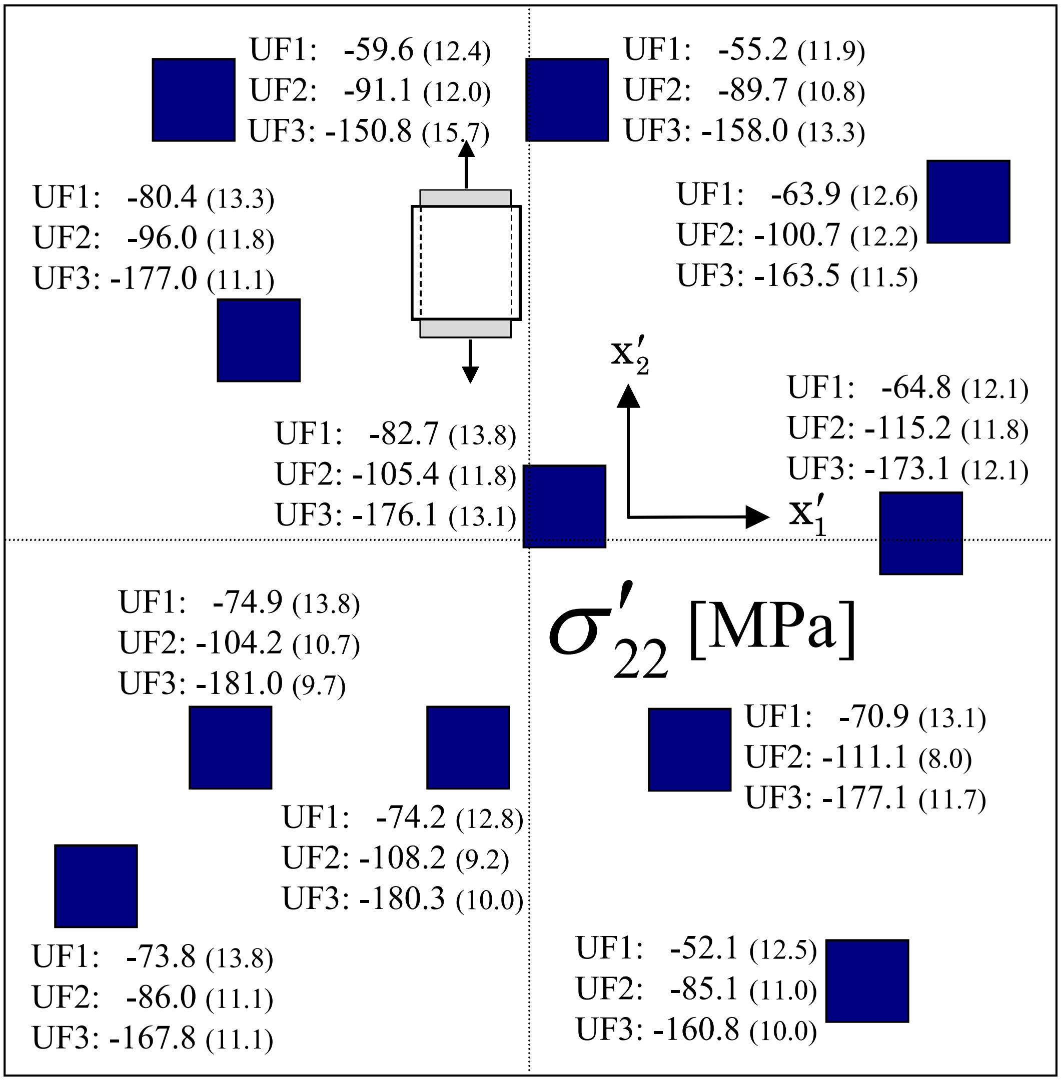

UF1: -59.6 (12.4)
UF2: -91.1 (12.0)
UF3: -150.8 (15.7)
UF1: -55.2 (11.9)
UF2: -89.7 (10.8)
UF3: -158.0 (13.3)
UF1: -80.4 (13.3)
UF2: -96.0 (11.8)
UF3: -177.0 (11.1)
UF1: -63.9 (12.6)
UF2: -100.7 (12.2)
UF3: -163.5 (11.5)
$x'_2$
UF1: -64.8 (12.1)
UF2: -115.2 (11.8)
UF3: -173.1 (12.1)
UF1: -82.7 (13.8)
UF2: -105.4 (11.8)
UF3: -176.1 (13.1)
$x'_1$
UF1: -74.9 (13.8)
UF2: -104.2 (10.7)
UF3: -181.0 (9.7)
$\sigma'_{22}$ [MPa]
UF1: -70.9 (13.1)
UF2: -111.1 (8.0)
UF3: -177.1 (11.7)
UF1: -74.2 (12.8)
UF2: -108.2 (9.2)
UF3: -180.3 (10.0)
UF1: -73.8 (13.8)
UF2: -86.0 (11.1)
UF3: -167.8 (11.1)
UF1: -52.1 (12.5)
UF2: -85.1 (11.0)
UF3: -160.8 (10.0)

Figure 5.23 - Average Stresses after Underfill Cure

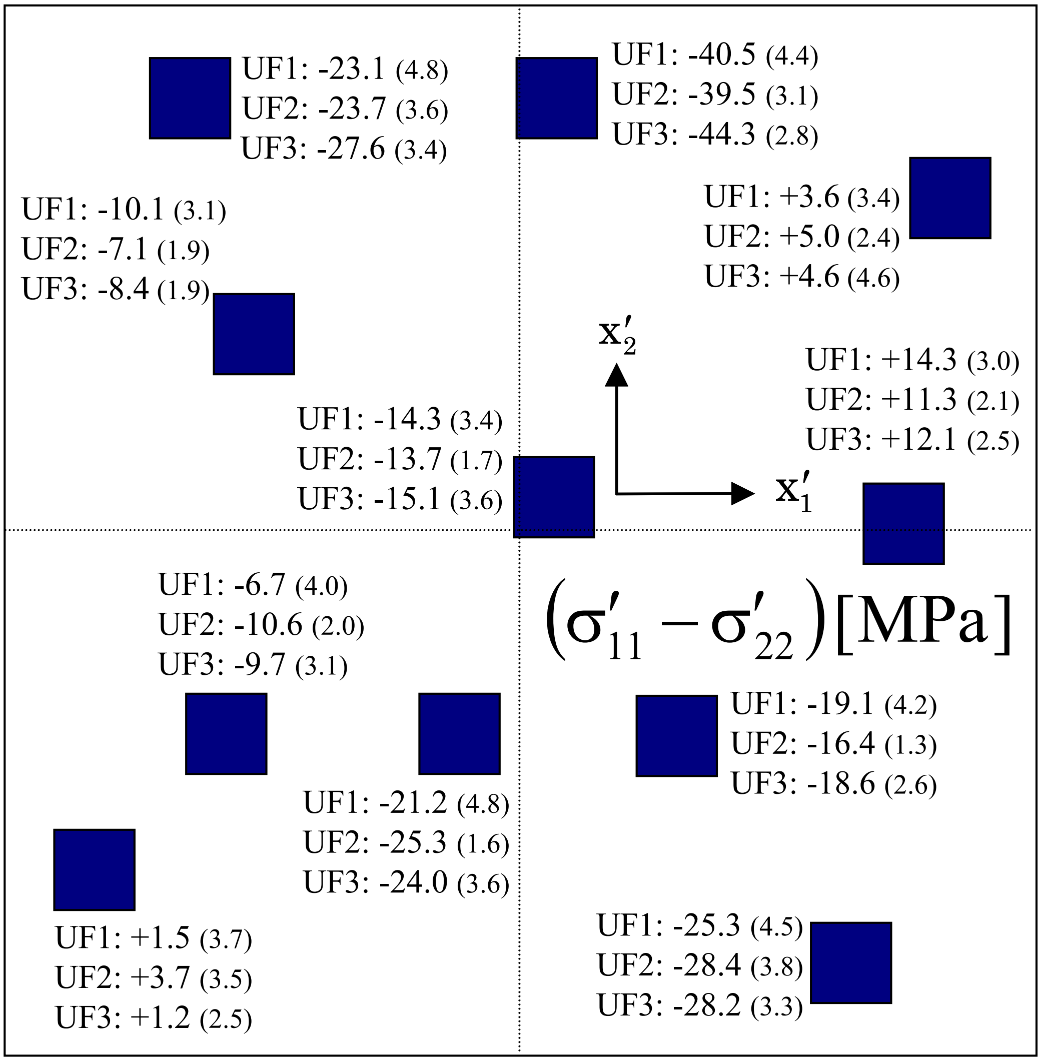

UF1: -23.1 (4.8)
UF2: -23.7 (3.6)
UF3: -27.6 (3.4)
UF1: -40.5 (4.4)
UF2: -39.5 (3.1)
UF3: -44.3 (2.8)
UF1: -10.1 (3.1)
UF2: -7.1 (1.9)
UF3: -8.4 (1.9)
UF1: +3.6 (3.4)
UF2: +5.0 (2.4)
UF3: +4.6 (4.6)
$x_2'$
UF1: +14.3 (3.0)
UF2: +11.3 (2.1)
UF3: +12.1 (2.5)
UF1: -14.3 (3.4)
UF2: -13.7 (1.7)
UF3: -15.1 (3.6)
$x_1'$
UF1: -6.7 (4.0)
UF2: -10.6 (2.0)
UF3: -9.7 (3.1)
$\left(\sigma_{11}' - \sigma_{22}'\right)[\mathrm{MPa}]$
UF1: -19.1 (4.2)
UF2: -16.4 (1.3)
UF3: -18.6 (2.6)
UF1: -21.2 (4.8)
UF2: -25.3 (1.6)
UF3: -24.0 (3.6)
UF1: +1.5 (3.7)
UF2: +3.7 (3.5)
UF3: +1.2 (2.5)
UF1: -25.3 (4.5)
UF2: -28.4 (3.8)
UF3: -28.2 (3.3)

Figure 5.24 - Average Stresses after Underfill Cure

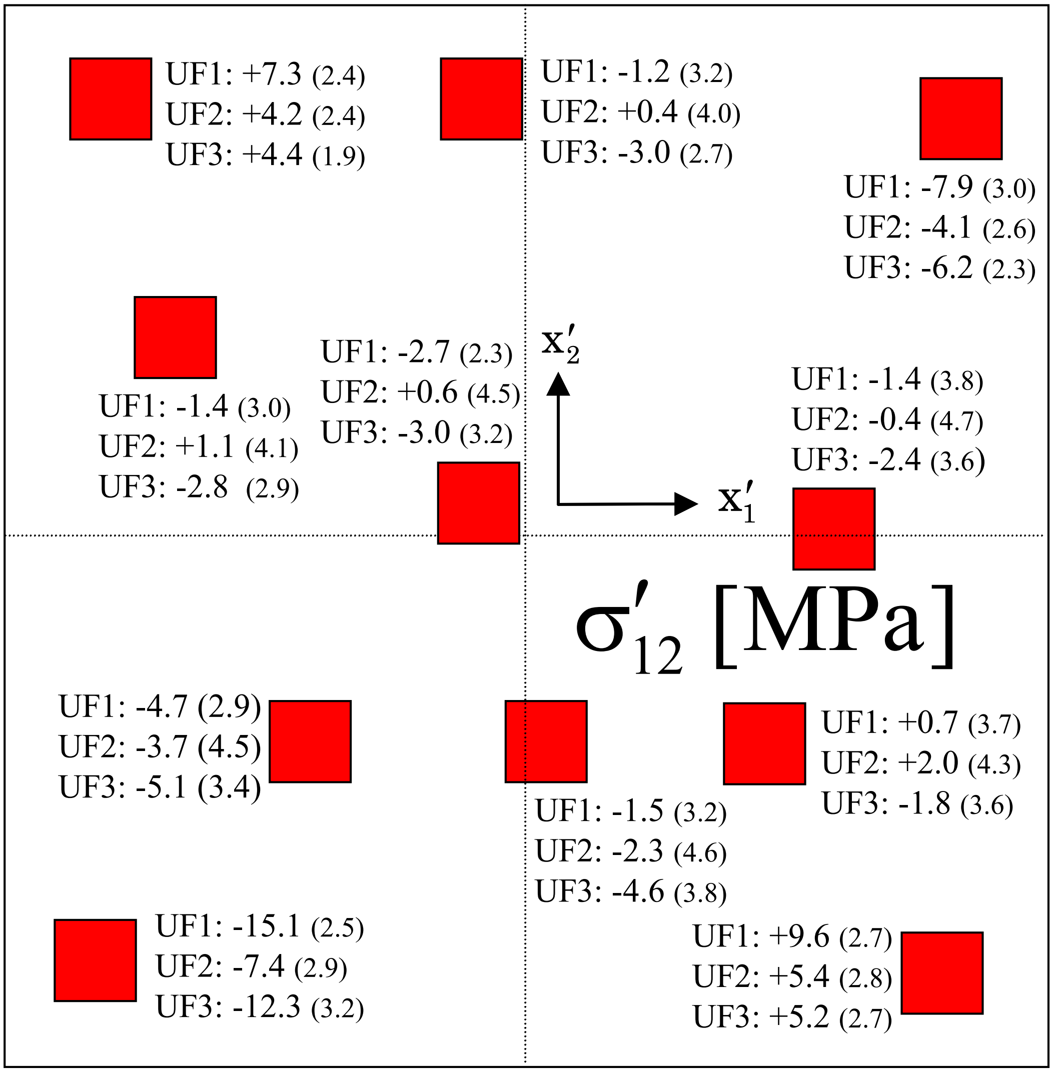

UF1: +7.3 (2.4)
UF2: +4.2 (2.4)
UF3: +4.4 (1.9)
UF1: -1.2 (3.2)
UF2: +0.4 (4.0)
UF3: -3.0 (2.7)
UF1: -7.9 (3.0)
UF2: -4.1 (2.6)
UF3: -6.2 (2.3)
UF1: -1.4 (3.0)
UF2: +1.1 (4.1)
UF3: -2.8 (2.9)
UF1: -2.7 (2.3)
UF2: +0.6 (4.5)
UF3: -3.0 (3.2)
$x_2'$
$x_1'$
UF1: -1.4 (3.8)
UF2: -0.4 (4.7)
UF3: -2.4 (3.6)
$\sigma_{12}'$ [MPa]
UF1: -4.7 (2.9)
UF2: -3.7 (4.5)
UF3: -5.1 (3.4)
UF1: -1.5 (3.2)
UF2: -2.3 (4.6)
UF3: -4.6 (3.8)
UF1: +0.7 (3.7)
UF2: +2.0 (4.3)
UF3: -1.8 (3.6)
UF1: -15.1 (2.5)
UF2: -7.4 (2.9)
UF3: -12.3 (3.2)
UF1: +9.6 (2.7)
UF2: +5.4 (2.8)
UF3: +5.2 (2.7)

Figure 5.25 - Average Stresses after Underfill Cure

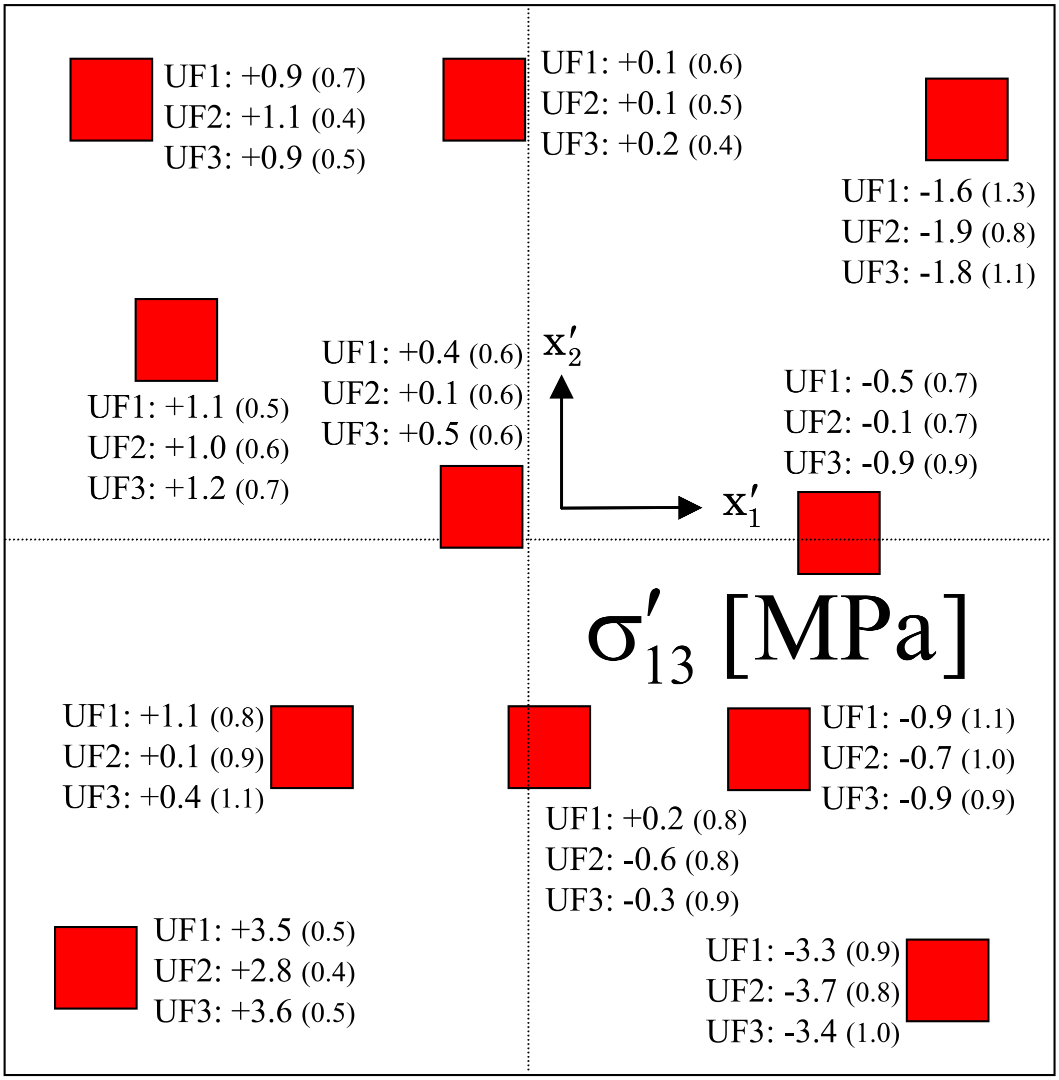

UF1: +0.9 (0.7)
UF2: +1.1 (0.4)
UF3: +0.9 (0.5)
UF1: +0.1 (0.6)
UF2: +0.1 (0.5)
UF3: +0.2 (0.4)
UF1: -1.6 (1.3)
UF2: -1.9 (0.8)
UF3: -1.8 (1.1)
UF1: +1.1 (0.5)
UF2: +1.0 (0.6)
UF3: +1.2 (0.7)
UF1: +0.4 (0.6)
UF2: +0.1 (0.6)
UF3: +0.5 (0.6)
x′2
x′1
UF1: -0.5 (0.7)
UF2: -0.1 (0.7)
UF3: -0.9 (0.9)
σ′13 [MPa]
UF1: +1.1 (0.8)
UF2: +0.1 (0.9)
UF3: +0.4 (1.1)
UF1: +0.2 (0.8)
UF2: -0.6 (0.8)
UF3: -0.3 (0.9)
UF1: -0.9 (1.1)
UF2: -0.7 (1.0)
UF3: -0.9 (0.9)
UF1: +3.5 (0.5)
UF2: +2.8 (0.4)
UF3: +3.6 (0.5)
UF1: -3.3 (0.9)
UF2: -3.7 (0.8)
UF3: -3.4 (1.0)

Figure 5.26 - Average Stresses after Underfill Cure

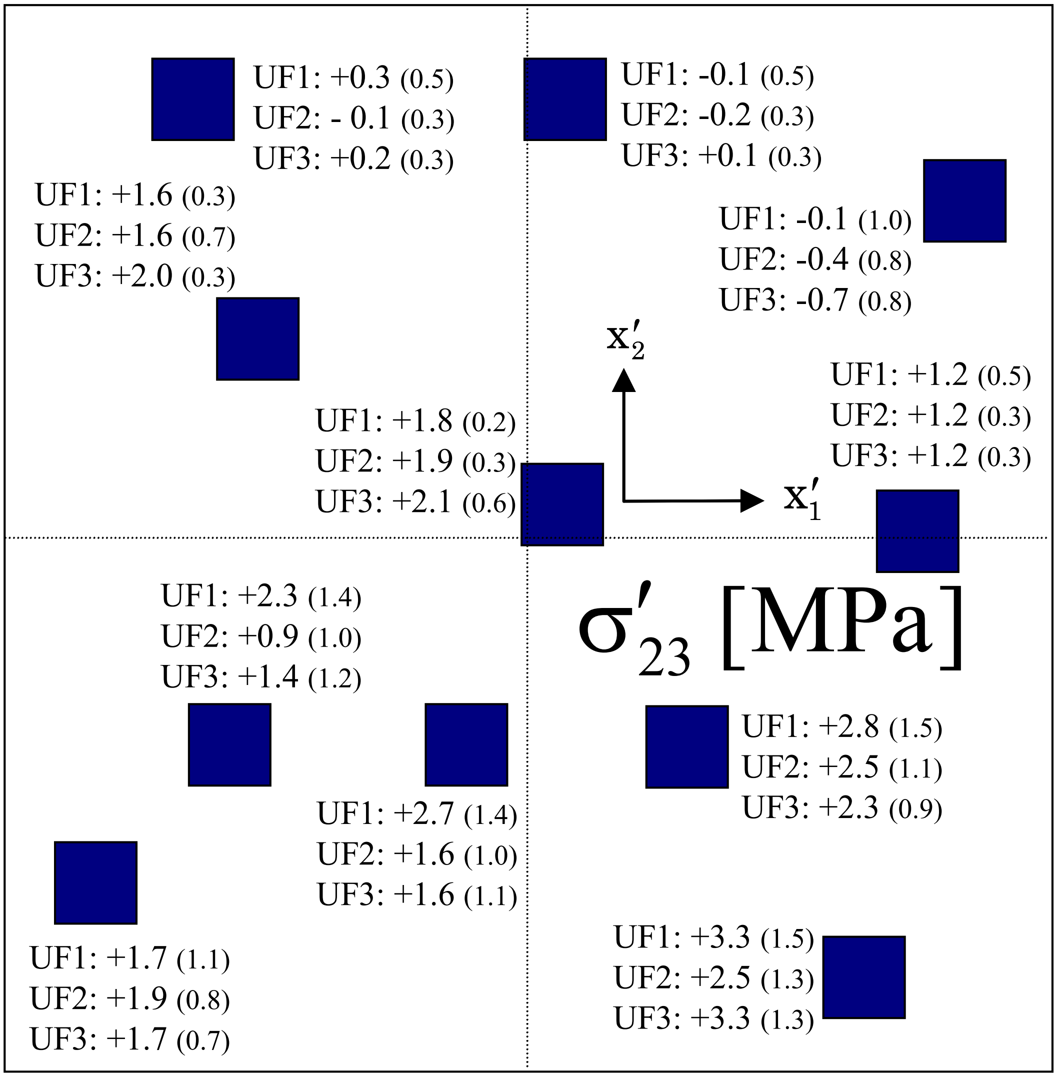

UF1: +0.3 (0.5)
UF2: - 0.1 (0.3)
UF3: +0.2 (0.3)
UF1: -0.1 (0.5)
UF2: -0.2 (0.3)
UF3: +0.1 (0.3)
UF1: +1.6 (0.3)
UF2: +1.6 (0.7)
UF3: +2.0 (0.3)
UF1: -0.1 (1.0)
UF2: -0.4 (0.8)
UF3: -0.7 (0.8)
$x'_2$
UF1: +1.2 (0.5)
UF2: +1.2 (0.3)
UF3: +1.2 (0.3)
UF1: +1.8 (0.2)
UF2: +1.9 (0.3)
UF3: +2.1 (0.6)
$x'_1$
UF1: +2.3 (1.4)
UF2: +0.9 (1.0)
UF3: +1.4 (1.2)
$\sigma'_{23}$ [MPa]
UF1: +2.8 (1.5)
UF2: +2.5 (1.1)
UF3: +2.3 (0.9)
UF1: +2.7 (1.4)
UF2: +1.6 (1.0)
UF3: +1.6 (1.1)
UF1: +1.7 (1.1)
UF2: +1.9 (0.8)
UF3: +1.7 (0.7)
UF1: +3.3 (1.5)
UF2: +2.5 (1.3)
UF3: +3.3 (1.3)

Figure 5.27 - Average Stresses after Underfill Cure

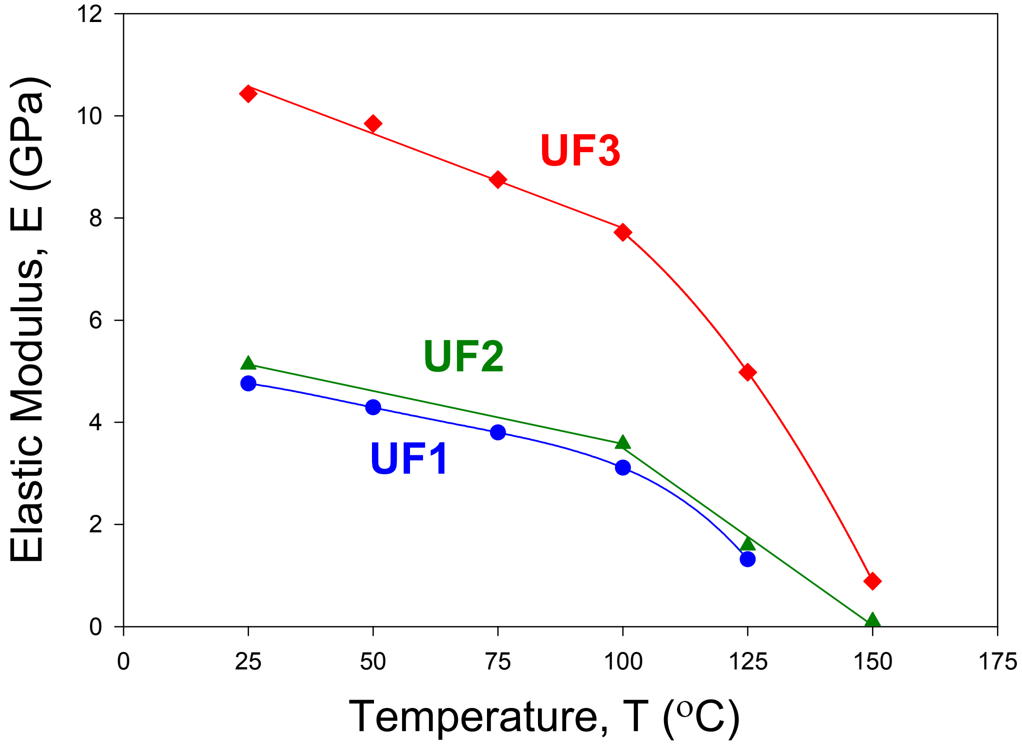


Figure 5.28 - Elastic Modulus vs. Temperature

stresses (see Figures 5.22-5.23), it also helps reduce solder joint fatigue by providing a more rigid coupling of the die to the board. The elastic modulus of materials UF1 and UF2 are nearly equal for all temperatures. However, material UF2 has significantly higher coefficient of thermal expansion and $T_g$ (see Table 5.2), and thus had a higher state of die in-plane compression than material UF1.

The data for the normal stress difference shown in Figure 5.24 indicate that all three underfill materials had similar stress magnitudes for this combined stress component. This was unexpected since the individual normal stresses are significantly different for the three materials. Therefore, while the in-plane normal stress difference is temperature compensated and can be measured accurately, it does not appear to be suitable for characterizing the variation in die stresses realized with different underfills.

The shear stress data in Figures 5.25-5.27 show that underfill UF2 had lower shear stress values at most rosette sites. This was especially true for the in-plane shear stress $\sigma'_{12}$ at the high stress regions at the four corners of the chip. For example, the in-plane shear stress magnitudes for underfill UF2 were 40-60% smaller than the corresponding values for UF1 at each of the four corners. At the maximum in-plane shear stress location (site S9, lower left corner), the in-plane shear stress for underfill UF2 was 50% smaller than the value for underfill UF1, and 40% smaller than the value for underfill UF3. The current efforts in characterizing underfill delaminations have indicated that the in-plane shear stress value is an excellent prognostic indicator of delamination initiation points and delamination propagation [195-196].

From the data in Figures 5.26-5.27, it can also be observed that the individual out-of-plane shear stress magnitudes are universally small (all less than 4 MPa). To fully understand the locations of the most severe interfacial shear stress at the underfill to die passivation interface, it is necessary to calculate the total out-of-plane shear stress at each site using:

$$\tau_{\text{Interfacial}} = \sqrt{(\sigma'_{13})^2 + (\sigma'_{23})^2} \tag{5.3}$$

The data in Figures 5.26-5.27 have been combined with this formula to yield the plot in Figure 5.29. From this result, the maximum total interfacial shear stresses were measured at sites S6 and S9 at the bottom edge of the die. It can also be seen that the interfacial shear stress values for underfill UF2 at these sites that were 5-15% smaller than the analogous values for materials UF1 and UF3. Based on other experiments, the underfill to die passivation shear strength (fracture) is in the range of 7-15 MPa for typical underfills have performed.

Another interesting observation from the shear stress data in Figure 5.25 is that the in-plane shear stress distribution did not illustrate the symmetry that might be expected. For a perfectly symmetrical assembly (underfill dispensed at all locations under the die simultaneously), the magnitudes (absolute value) of the shear stresses in the four corners should be equal. However, the results for all three underfills indicate that the average stress magnitudes in the lower left corner were 50-100% higher than the values at the other 3 corners. This corner is where the underfilled was dispensed. As can be observed in Figure 5.10 (where the dispense corner is in the upper right position), a larger fillet and slight buildup of encapsulant is produced at the dispense corner. The presence of this non-uniform fillet is further emphasized in the cross-sectional photo shown in Figure 5.30. The dispense corner and its adjacent sides were also found to be the location of the initiation of underfill to die passivation delaminations, and eventually

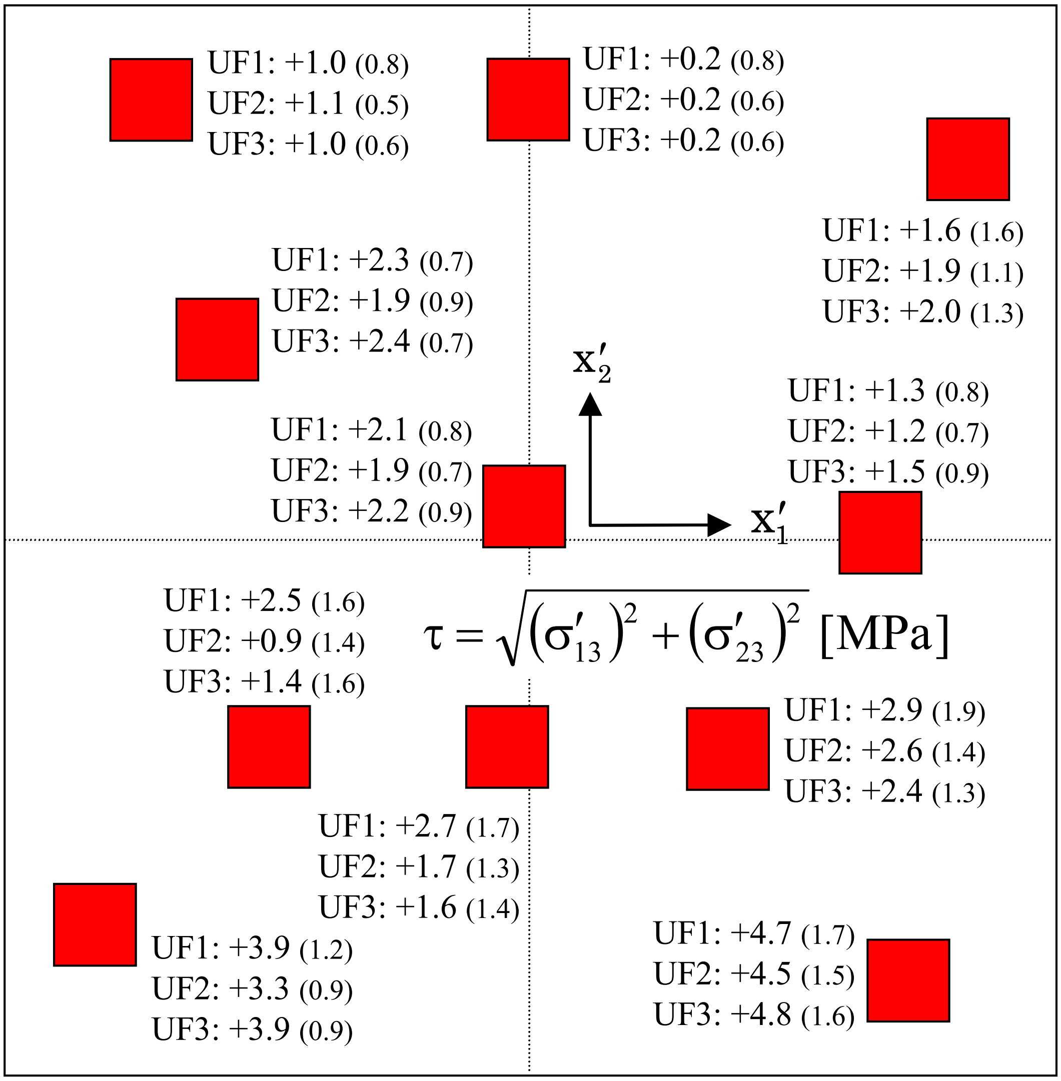

UF1: +1.0 (0.8)
UF2: +1.1 (0.5)
UF3: +1.0 (0.6)
UF1: +0.2 (0.8)
UF2: +0.2 (0.6)
UF3: +0.2 (0.6)
UF1: +1.6 (1.6)
UF2: +1.9 (1.1)
UF3: +2.0 (1.3)
UF1: +2.3 (0.7)
UF2: +1.9 (0.9)
UF3: +2.4 (0.7)
$x'_2$
UF1: +1.3 (0.8)
UF2: +1.2 (0.7)
UF3: +1.5 (0.9)
UF1: +2.1 (0.8)
UF2: +1.9 (0.7)
UF3: +2.2 (0.9)
$x'_1$
UF1: +2.5 (1.6)
UF2: +0.9 (1.4)
UF3: +1.4 (1.6)
$\tau = \sqrt{(\sigma'_{13})^2 + (\sigma'_{23})^2}$ [MPa]
UF1: +2.9 (1.9)
UF2: +2.6 (1.4)
UF3: +2.4 (1.3)
UF1: +2.7 (1.7)
UF2: +1.7 (1.3)
UF3: +1.6 (1.4)
UF1: +3.9 (1.2)
UF2: +3.3 (0.9)
UF3: +3.9 (0.9)
UF1: +4.7 (1.7)
UF2: +4.5 (1.5)
UF3: +4.8 (1.6)

Figure 5.29 - Average Interfacial Stresses after Underfill Cure

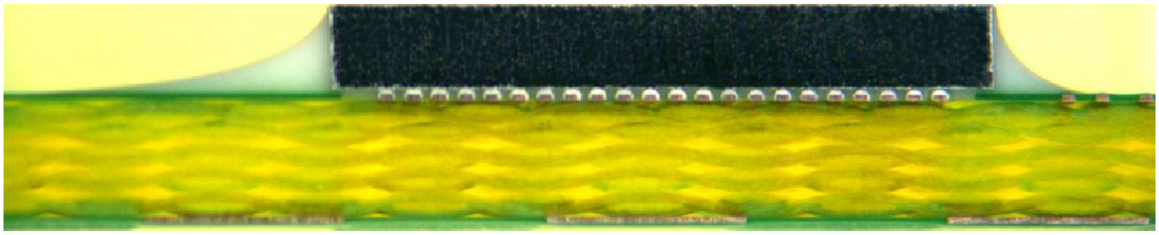


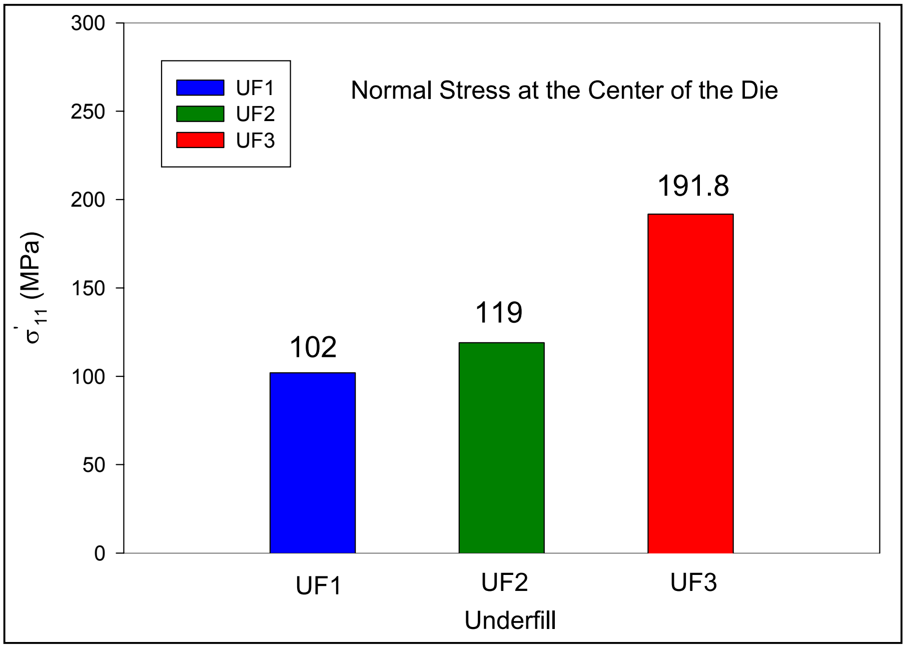
Figure 5.30 - Cross-Section Along Outside Row of Solder Balls Showing Non-Uniform Underfill Fillet (Dispense Corner is on the Left Side)

first solder ball failures [195-196]. These results illustrate the strong effects that assembly and packaging processes can have on the die stress distributions.

Figures 5.31-5.32 shows graphically the die stresses comparison for three different underfills. In these graphs, the highest die stresses at the critical location of the die have compared for underfills UF1, UF2, and UF3. It is very important to know the effects of underfill materials on die stresses as well as flip chip package reliability. Thus, the stress test chip technique is a very effective tool and efficient way to characterize and select appropriate underfill materials for flip chip technology.

## 5.6 Finite Element Correlations

The measured room temperature die stress data have been evaluated through correlation with the predictions of nonlinear three-dimensional finite element simulations of the underfill curing process. In the finite element models, the materials were modeled as linear elastic. Temperature dependent mechanical properties and large deformations (kinematic nonlinearities) were utilized. The time dependent (viscoplastic) behaviors of the underfill encapsulant and solder were neglected to simplify the analysis. The die was assumed to be stress free at the glass transition temperature of the underfill encapsulant (see Figure 5.15), and cooling from the glass transition temperature to room temperature was simulated. It should be emphasized that the experimental measurements were the main emphasis of this work. The finite element model predictions were used to show the proper signs and approximate trends of the various stress component distributions, so that the experimental data could be better understood. In addition, correlation of the finite



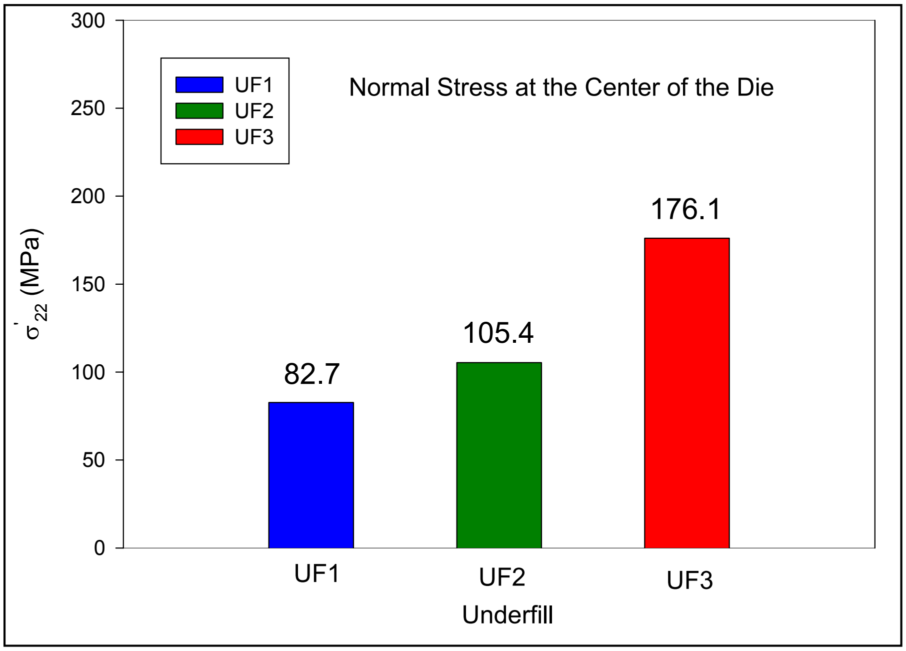


Figure 5.31 – Comparison of Normal Stresses at the Die Center for the Three Underfills

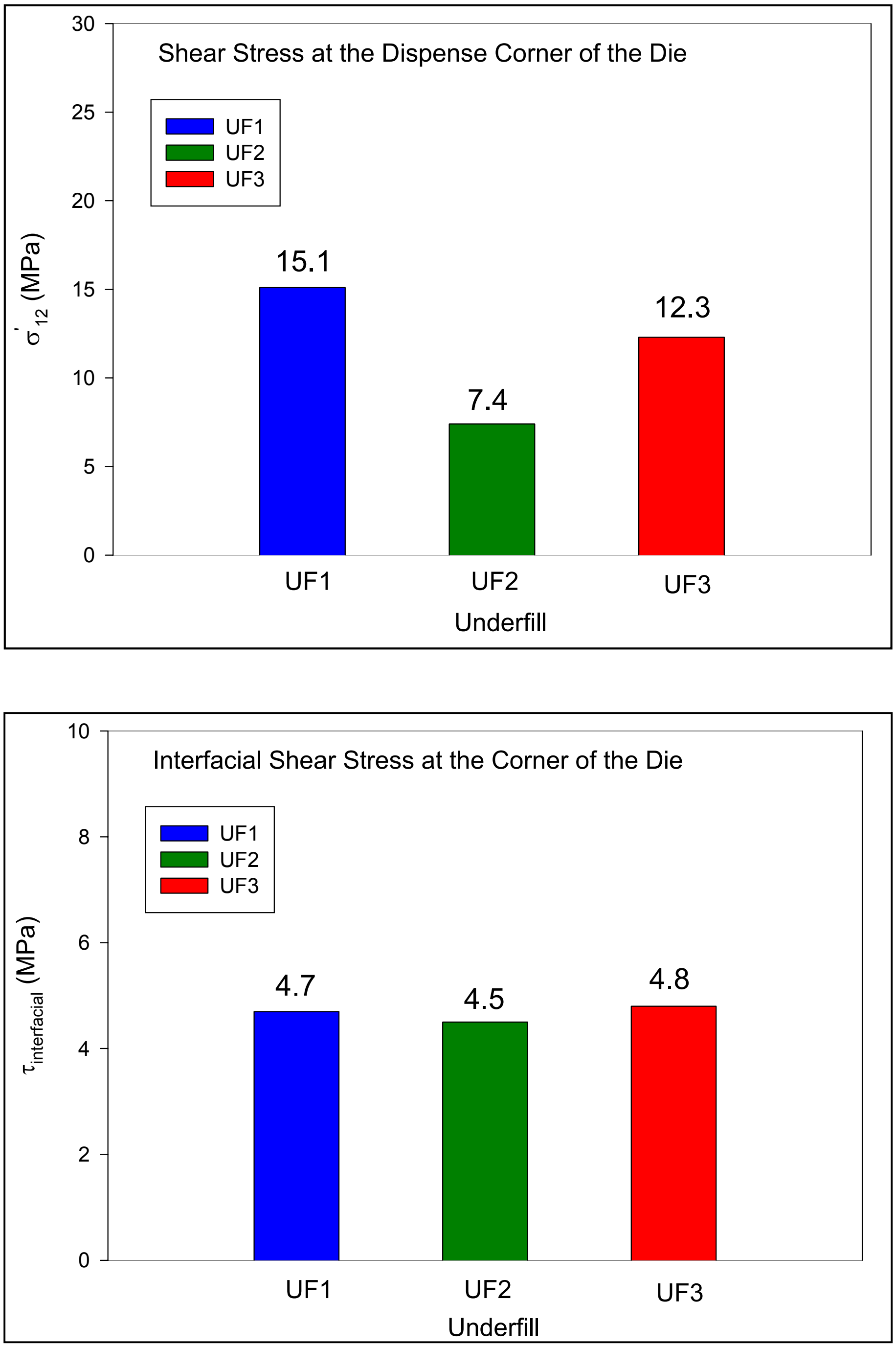


Figure 5.32 – Comparison of Shear Stresses at the Die Dispense Corner for the Three Underfills

element predictions with the test chip data allowed identification of the limitations of using an expedient but approximate engineering numerical simulation procedure that neglects encapsulant relaxation and cure/processing details.

As shown in Figure 5.33, a full model of the specimen was meshed to allow for the non-uniform underfill fillet to be accommodated (fillet for UF1 is shown). Figure 5.34 depicts the flip chip sample dimensions used in the FEM simulations. Figures 5.35-5.36 show the material properties information for underfill UF1. Stress-strain curves for underfill encapsulant UF1 are shown in Figure 5.35 for the temperature range of -75 to +125 $^{o}$C. A list of flip chip packaging material properties is shown in Figure 5.36.

Typical graphical correlations between the experimental test chip measurements and the finite element predictions for the die surface distributions are shown in Figures 5.37-5.40 for the in-plane shear stress $\sigma'_{12}$, the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$), and out-of-plane shear stresses $\sigma'_{13}$ and $\sigma'_{23}$, respectively. The illustrated results are again for underfill UF1. In these plots, the shaded contours are the room temperature stress distributions predicted by the finite element model. Each of the small squares in these diagrams locates a sensor rosette site. The color of a given square represents the average room temperature experimental value of the stress at the rosette site, when considering the results for all 25 specimens (the square is colored to the same scale/legend of the finite element contours).

It can be see that the finite element predictions are in reasonable agreement with the experimental results. The measured stresses show the same trends and numerical signs as the distributions predicted by finite element analysis. However, the finite element model over predicts the observed normal stress data due to the fact that the

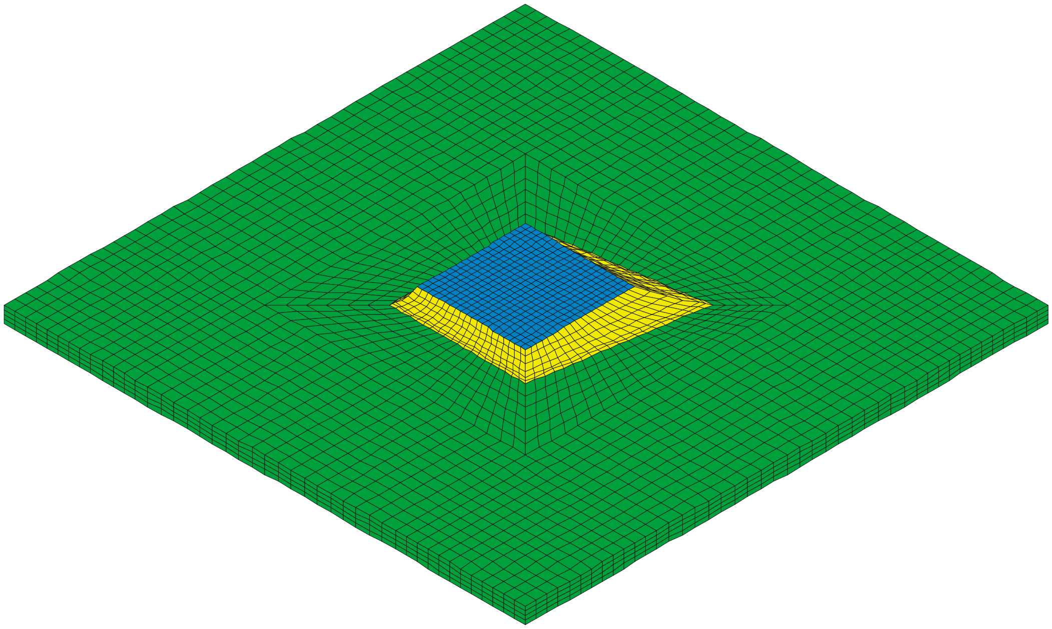


Figure 5.33 - Finite Element Mesh (UF1)

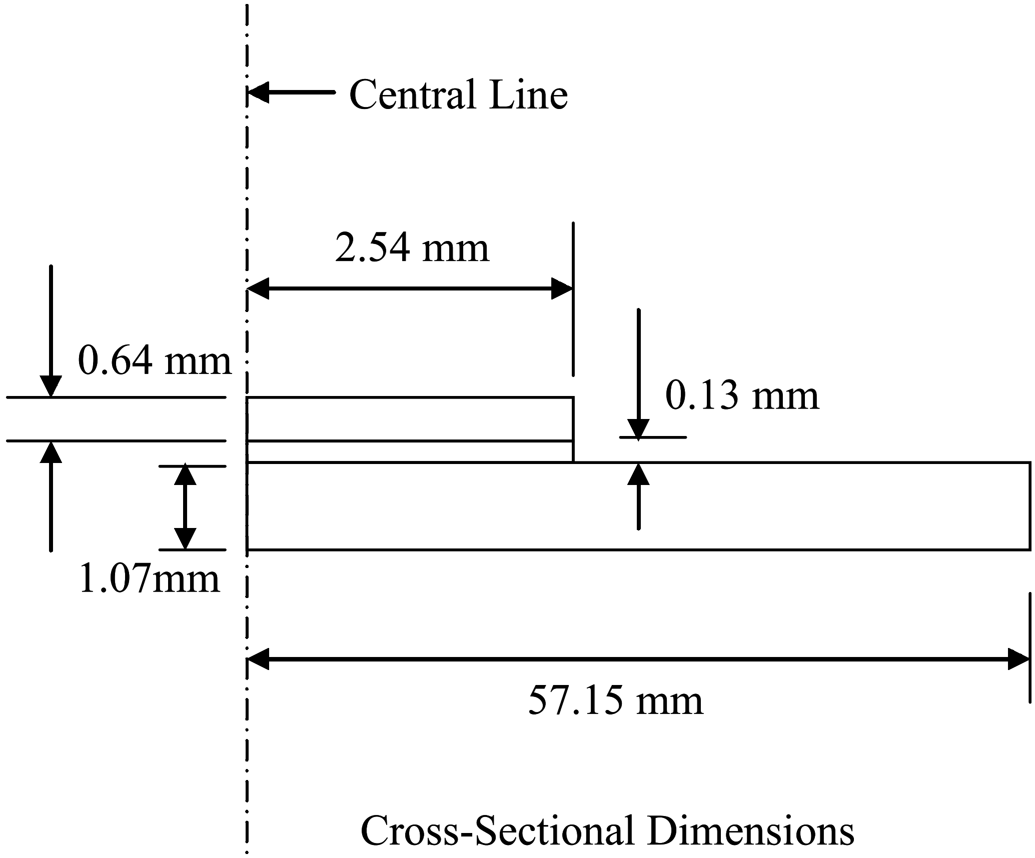

Central Line
2.54 mm
0.64 mm
0.13 mm
1.07mm
57.15 mm
Cross-Sectional Dimensions

Figure 5.34 - Dimensions of the Flip Chip on Laminate Assemblies

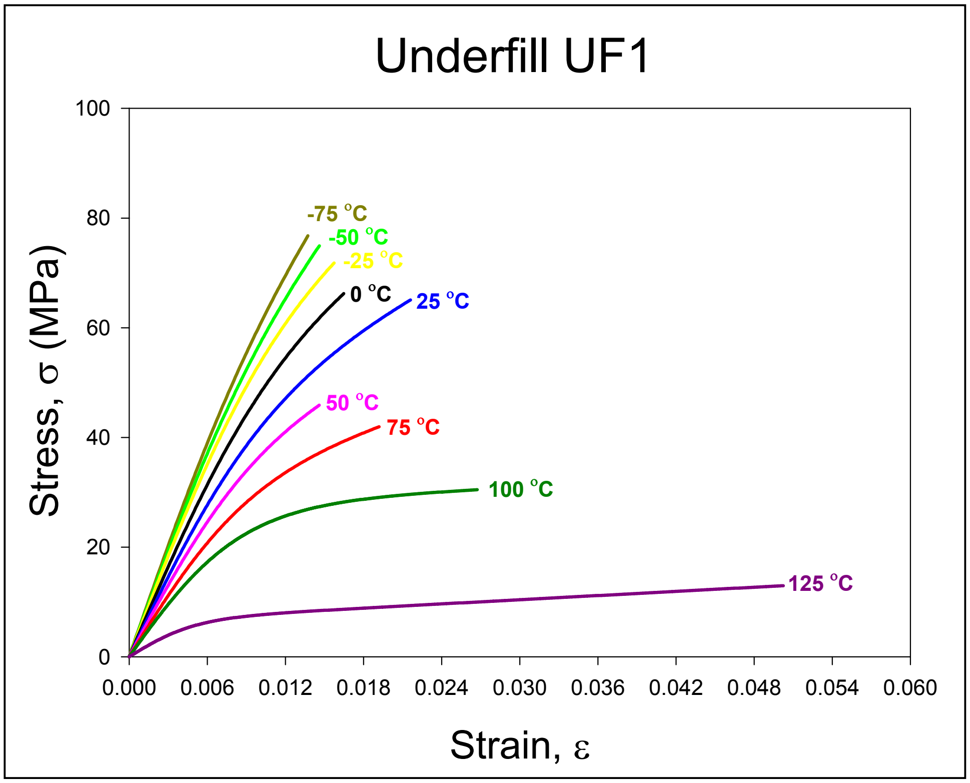


Figure 5.35 - Underfill UF1 Stress-Strain Curves (-175 to +150 °C) [144]

| Material Name | E (MPa) | ν | α (1/ °C) |
|---|---|---|---|
| PCB | $1.79 \times 10^4$ | 0.28 | $20 \times 10^{-6}$ |
| Underfill | $0.475 \times 10^4$ | 0.3 | $35 \times 10^{-6}$ |
| Silicon | $17.0 \times 10^4$ | 0.278 | $2.6 \times 10^{-6}$ |

Figure 5.36 - Packaging Material Properties for FEM Simulations

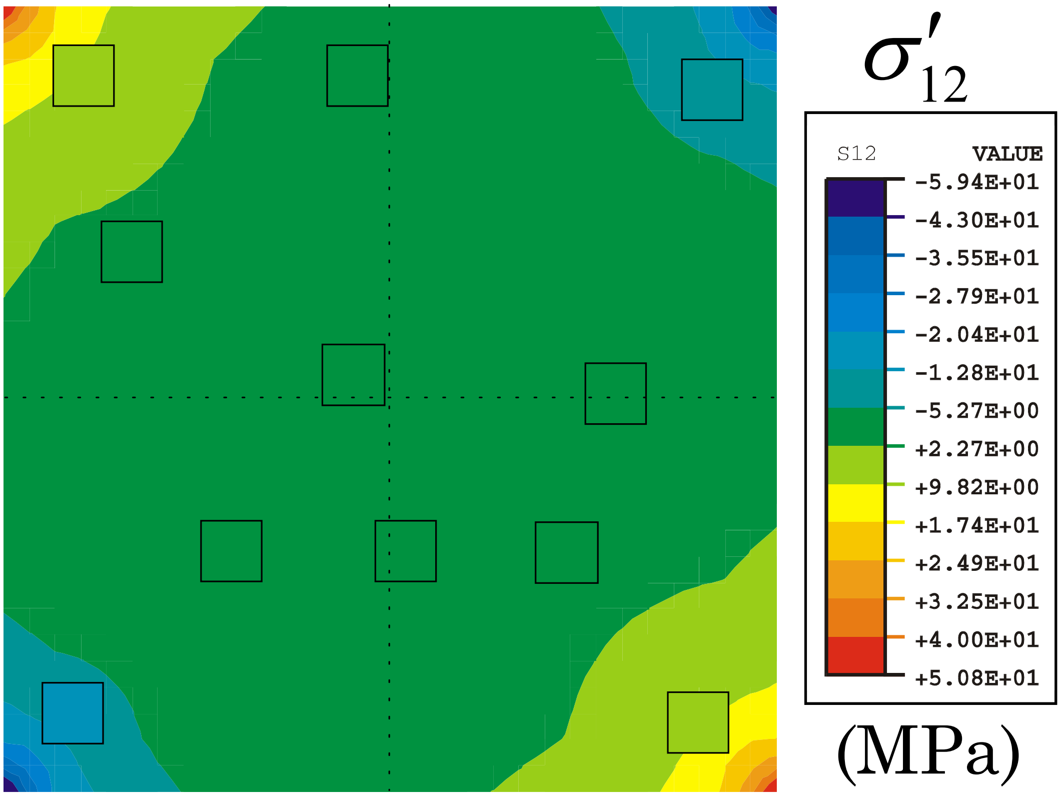


Figure 5.37 - Correlation of Test Chip Measurements with Finite Element Simulations (UF1)

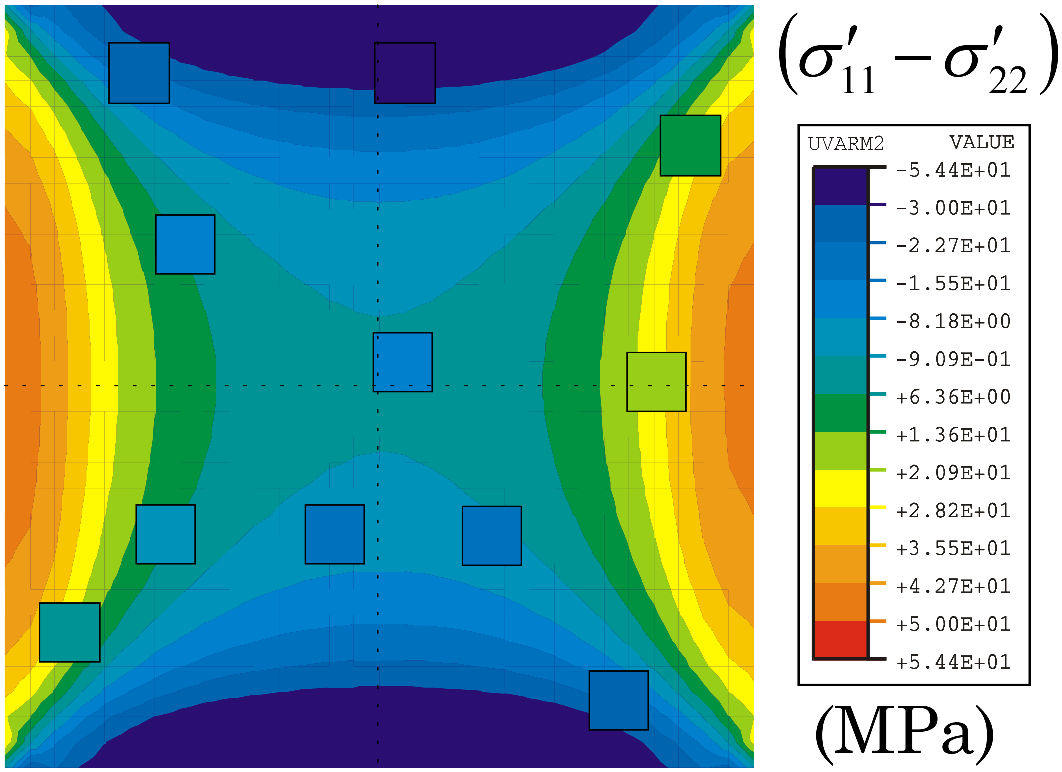


Figure 5.38 - Correlation of Test Chip Measurements with Finite Element Simulations (UF1)

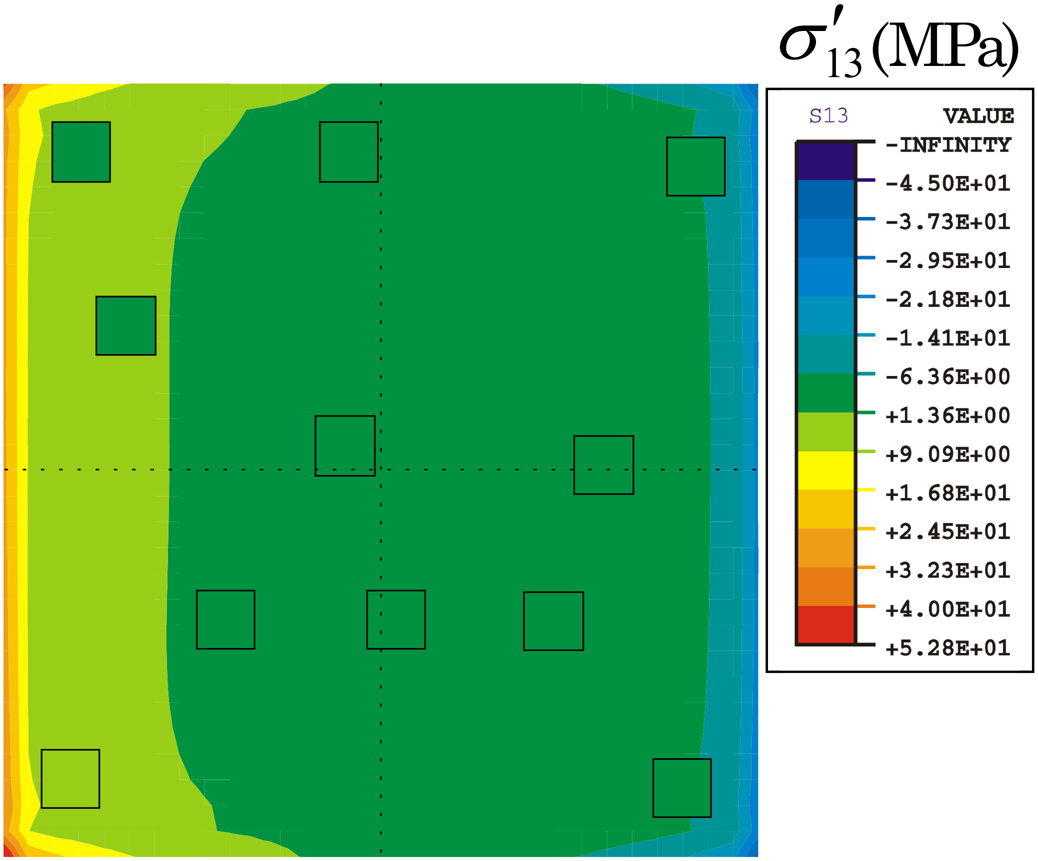


Figure 5.39 - Correlation of Test Chip Measurements with Finite Element Simulations (UF1)

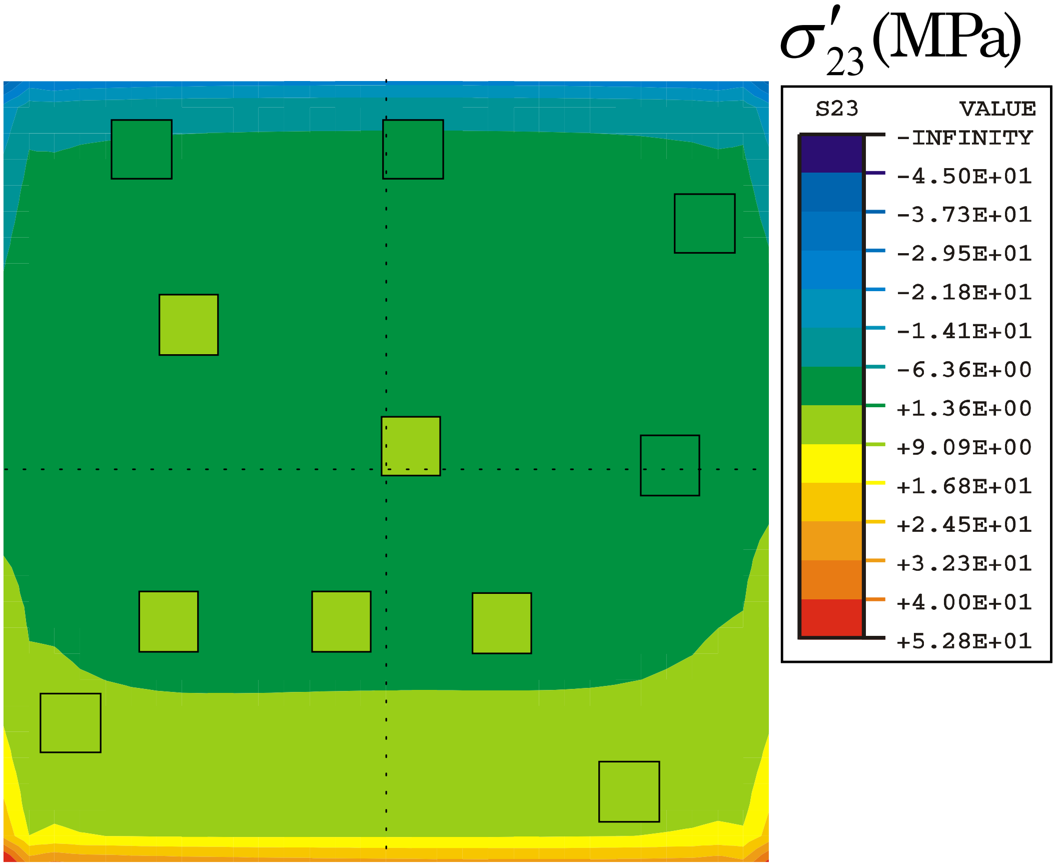


Figure 5.40 - Correlation of Test Chip Measurements with Finite Element Simulations (UF1)

viscoplastic relaxation of the composite layer of underfill encapsulant and solder was neglected. The maximum measured value if the normal stress difference was 44.3 MPa (rosette site at center of top edge of die), while the finite element prediction for the same point was 54.4 MPa.

Although it is not immediately clear from the contours in Figure 5.38, the finite element model also predicted a concentration of the in-plane shear stress in the lower right corner of the die. This fact can be seen in Figure 5.41, where the stress is plotted along the diagonal lines connecting the four corners to the center point of the die. The finite element results show essentially the same response in three of the quadrants, and a clear increase in the stress distribution in the quadrant containing the underfill dispense corner and longer underfill fillet. In addition, it is seen that a very high stress gradient is predicted to occur between the corner rosette locations and the actual corner/edge of the silicon die. The numerical correlations between the experimental shear stress values and the finite element predictions at the corner rosette sites are given in Figure 5.42. Although the finite element simulations also predicts a stress concentration is the dispense corner, the effect is not as predominant as shown by the experimental piezoresistive sensor measurements. This is likely due to several of the approximations present in the model such as the use of linear elastic material properties, neglecting any underfill flow effects through the assumed simultaneous and instantaneous underfill dispense at all locations under the chip, etc. It is clear that far more sophistication must be included in the finite element simulations to fully account for the asymmetry in the actual die stress distributions.

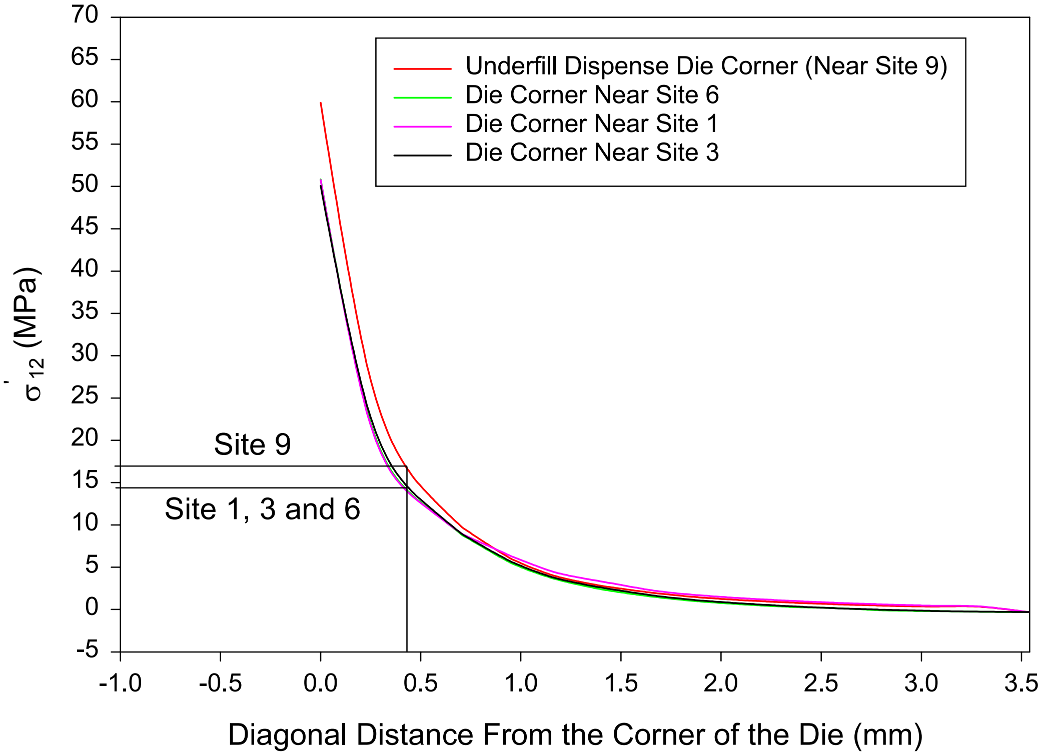


Figure 5.41 - Numerical Prediction of the In-Plane Shear Stress Distributions Along the Four Chip Diagonals

|  | $\sigma'_{12}$ (MPa) |  |  |  |
|---|---|---|---|---|
| Site # | S1 | S3 | S6 | S9 |
| Experimental | 7.3 | 7.9 | 9.6 | 15.1 |
| Finite Element | 13.5 | 13.5 | 13.5 | 16.8 |

Figure 5.42 - Correlation of the In-Plane Shear Stresses

## 5.7 Die Stress Variation with Temperature (-40 to +150 $^{o}$C)

To further illustrate the nature of the stresses induced by underfill encapsulation, several flip chip assemblies with three different underfills were subjected to slow temperature change from -40 to +150 $^{o}$C. Resistance values were monitored continuously, and the stresses were extracted as a function of temperature. When using eqs. (5.1, 5.2), it was assumed that the piezoresistive coefficients were approximately independent of temperature. Typical in-plane normal stress difference and in-plane shear stress data for underfill UF1 are shown in Figures 5.43 and 5.44, respectively. In all cases, raising the temperature from room temperature decreases the magnitude of the stress component. As the temperature approached or exceeded 165 $^{o}$C (the cure temperature of the underfill UF1) and the assembly flattens back out, the stresses approach zero. Although the normal stress difference illustrated a quite linear response with the temperature of assembly, the in-plane shear stress values began to deviate from linearity as soon as the glass transition temperature Tg = 130 $^{o}$C of underfill UF1 was exceeded. This type of behavior was illustrated at all of the corner rosette sites. It is also suspected that the individual normal stresses exhibit the same type of nonlinear behavior above the Tg, and that the nonlinear effect is cancelled out in through subtraction when the normal stress difference data that is plotted in Figure 5.43.

As the temperature is lowered; the stress levels continue to decrease. This is because the material expansion mismatch becomes worse due to the larger temperature change from the "relaxed" configuration of the package materials at approximately 165$^{o}$C. As can be seen in Figure 5.43, the die stresses can be come quite high for

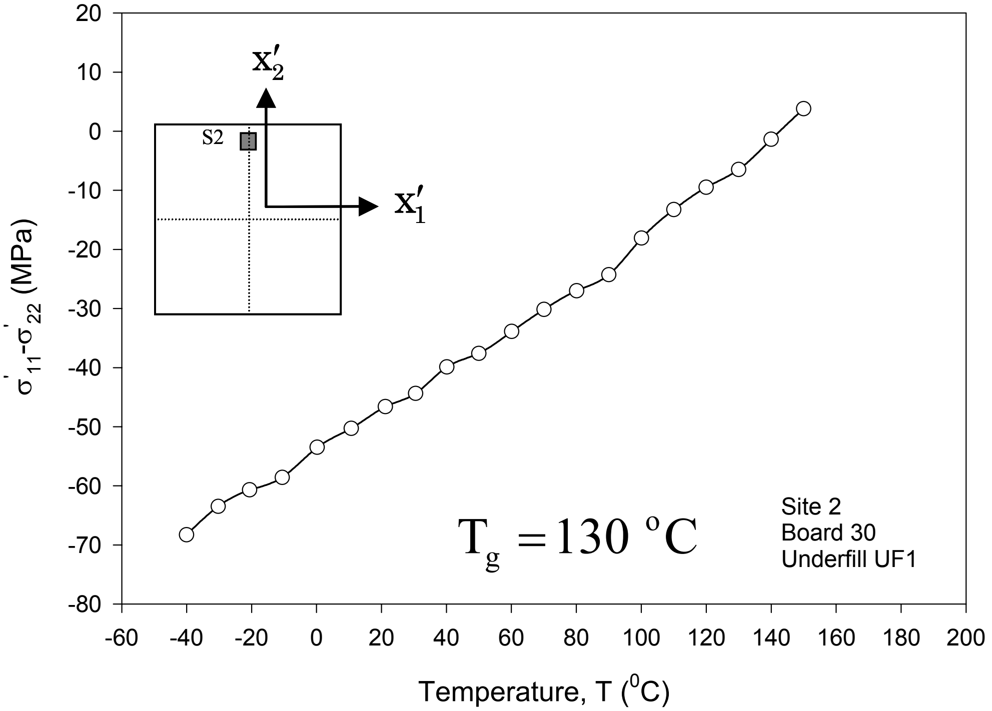


Figure 5.43 - Die Normal Stress vs. Temperature (Underfill UF1)

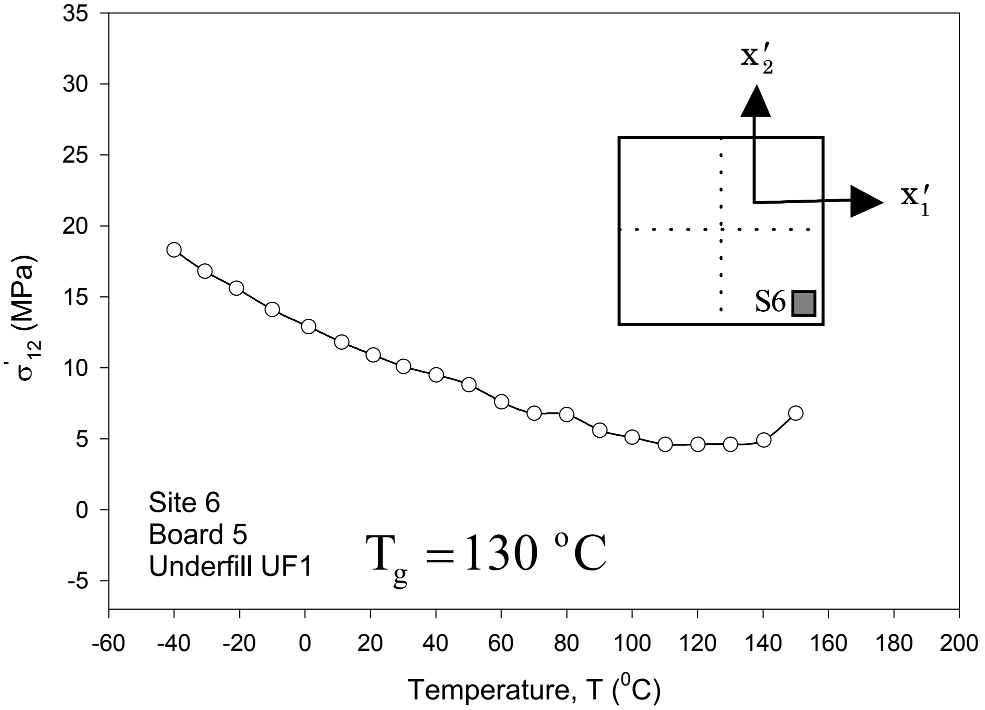


Figure 5.44 - Die Shear Stress vs. Temperature (Underfill UF1)

temperatures significantly below room temperature. Similar tests have also been performed for other two underfills materials (UF2 and UF3). Typical in-plane normal stress difference and in-plane shear stress data for underfill UF2 and UF3 are shown in Figures 5.45-5.48. The die stress variation with temperature for underfill UF2 (Figures 5.45 and 5.46) and for underfill UF3 (Figures 5.47 and 5.48) were observed and compared with underfill UF1. In all cases, analogous die stress variations with temperature were observed.

## 5.8 Summary

In this work, test chips with piezoresistive sensors have been used to measure the mechanical stresses on the silicon die device surface in flip chip on laminate assemblies. The utilized (111) silicon test chips contain an array of sensor rosettes capable measuring all of the stress components including the interfacial shear stresses. The stress chips were bumped with 200 μm (8 mil) pitch perimeter solder balls. The flip chip test die were then packaged, and die surface stresses were measured throughout the assembly process and during post-assembly environmental testing.

The observed transient stress variation during underfill cure was recorded and discussed. As noted in earlier research by the authors [142-144, 167], the majority of the final assembly stresses are developed during cooldown after the underfill snap cure oven exposure. These stresses were typically 5-10 times larger than the maximum values observed during the actual cure cycle. In addition, no stress overshoot phenomenon was observed for the device side die stresses; unlike the previous findings with the backside die stresses [142]. This supports the earlier hypothesis that die cracking and tensile stress

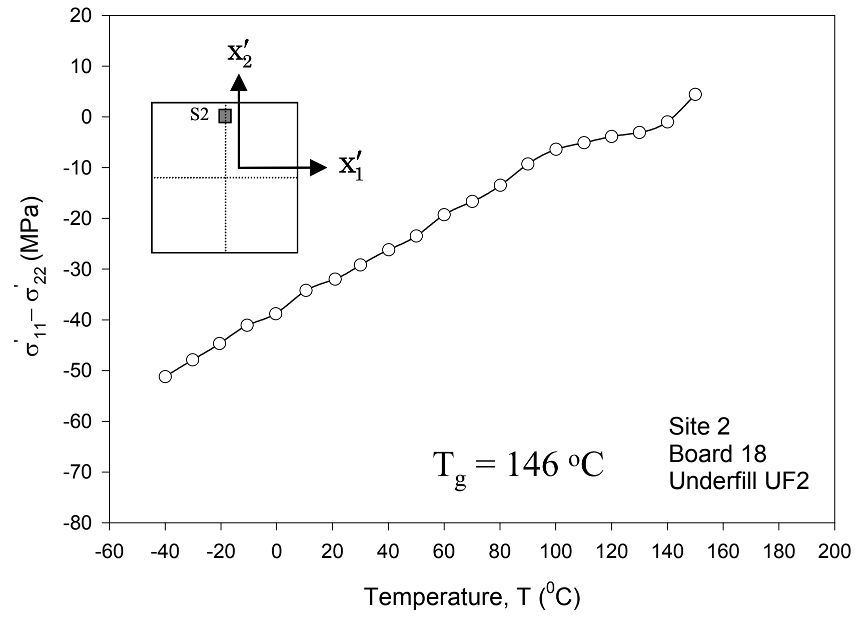


Figure 5.45 - Die Normal Stress vs. Temperature (Underfill UF2)

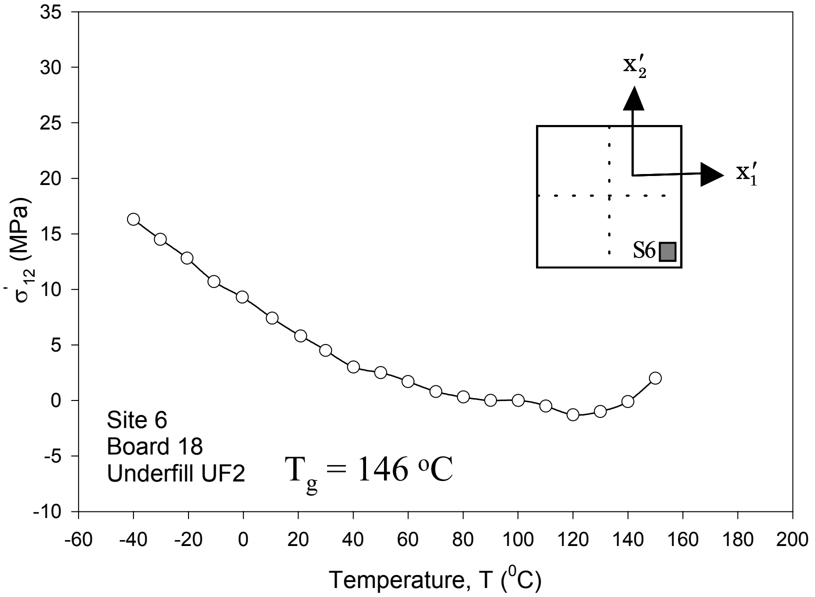


Figure 5.46 - Die Shear Stress vs. Temperature (Underfill UF2)

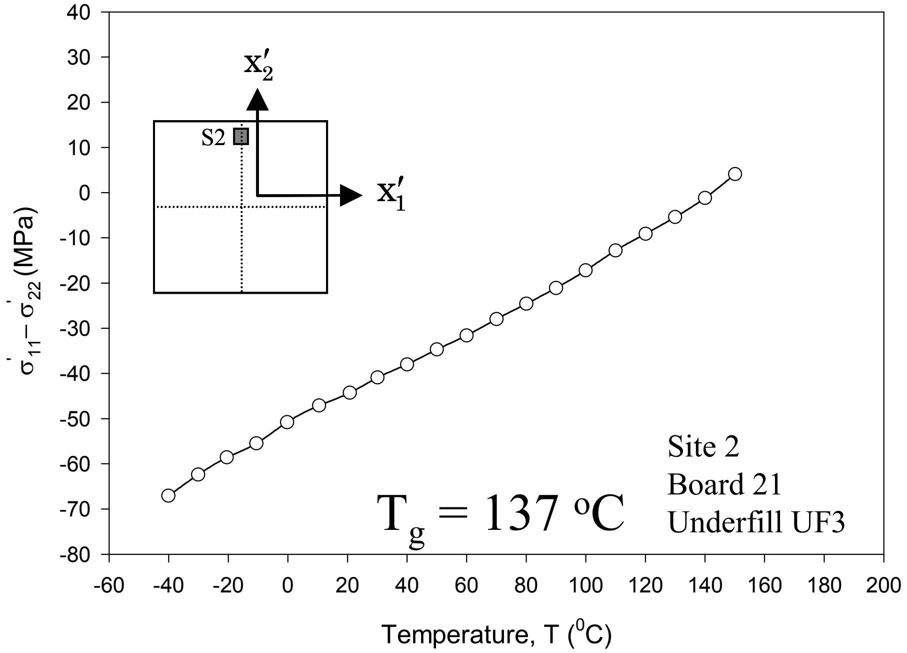


Figure 5.47 - Die Normal Stress vs. Temperature (Underfill UF3)

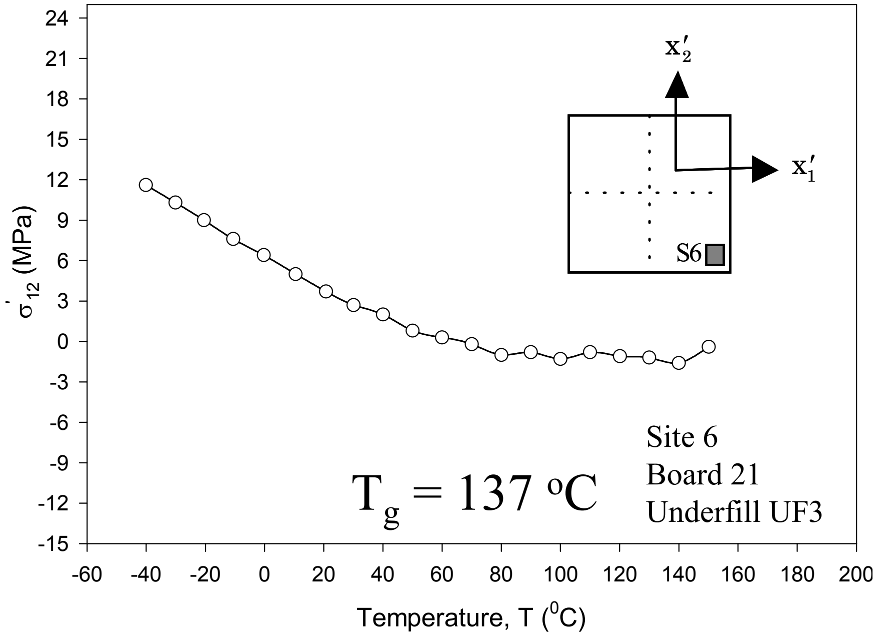


Figure 5.48 - Die Shear Stress vs. Temperature (Underfill UF3)

overshoot on the backside of the assembled flip chip die are due to differential cooling during cooldown after underfill cure.

Room temperature die stresses after assembly have been evaluated and compared for three different underfills. Minimizing these device side die stresses is especially important when multiple copper/low-k interconnect redistribution layers are present. It was found that underfill UF1 exhibited the lowest in-plane compressive stress magnitudes. For the three encapsulants under study, the in-plane compressive stresses seemed to be strongly related to both the elastic modulus and coefficient of thermal expansion of the underfills. Underfill UF2 exhibited the lowest in-plane and interfacial shear stress magnitudes. Further finite element investigations using temperature dependent elastic and viscoplastic properties of the underfill materials will be necessary before the "stress rankings" of the three underfill materials can be better understood.

The in-plane shear stress distribution was found to lack the expected symmetry present for an ideal assembly where the underfill is dispensed at all locations under the die simultaneously. The data for all three underfills indicated a concentration in the shear stress at the underfill dispense corner. The stress magnitudes in this corner were 50-100% higher than the values at the other 3 corners, and delaminations were also observed to initiate at the high stress corner during thermal cycling. These results were explained by the presence of a larger fillet and slight buildup of underfill encapsulant at the dispense corner. The current efforts in characterizing underfill delaminations have indicated that the in-plane shear stress value is an excellent prognostic indicator of delamination initiation points and delamination propagation [195-196]. Further analysis of the existing data is discussed in a later chapter in order to formulate a better understanding of underfill delamination behavior in flip chip assemblies.

Die stress variations have been monitored in the assembled flip chip die as the test boards were subjected to slow temperature changes from -40 to +150 $^{o}$C. The die stresses were maximized at extremely low temperatures, and approached zero as the assemblies neared the cure temperature of the underfill encapsulant. A fairly linear response was observed until the assembly reached the Tg of the underfill encapsulant.

# CHAPTER 6

# MEASUREMENT OF ELECTRONIC PACKAGING MATERIAL BEHAVIOR AND FLIP CHIP DIE STRESSES AT EXTREME LOW TEMPERATURES

## 6.1 Introduction

High stresses in semiconductor die and other packaging elements can be developed in electronic assemblies subjected to extremely low ambient temperatures leading to reliability concerns. Future NASA planetary missions to the Moon, Mars, Venus, and Jupiter include ambient environments ranging from -180 to 380 °C (see Figures 6.1 and 6.2). Electronic packaging reliability is largely unexplored at such extreme low temperatures, and even the most extreme harsh environment consumer and military applications are typically concerned with performance down to only -55 $^{o}$C. In addition, temperature dependent material properties of electronic packaging materials are normally not available at extreme low temperatures. This prevents the accurate application of finite element modeling for prediction of the low temperature reliability of electronic packages and assemblies.

High stresses in semiconductor die and other packaging elements can be developed in electronic assemblies subjected to extremely low ambient temperatures leading to reliability concerns. The primary mechanism for stress buildup is the mismatch in the coefficients of expansion of the various packaging materials. Electronic

| | |
|---|---|
| Consumer | 0 to 100 °C |
| Military/NASA | -55 to 125 °C |
| Automotive and Other Ground Vehicles | -40 to 125 °C |
| Well Logging (Oil and Gas) | 75 to 225 °C |
| Geothermal Walls | 200 to 350 °C |
| Gas Turbine Engines | -55 to 1200 °C |
| Surface of Mars | -120 to 20 °C |
| Atmosphere of Mars | -135 to 20 °C |
| Giant Planets | -140 to 380 °C |
| Surface of Venus | Up to 460 °C |
| Surface of Europa | Down to –160 °C |
| Surface of Titan | Down to –180 °C |
| Pluto | Down to –220 °C |
| Jupiter Multi-Probes | -180 to 380 °C |

Figure 6.1 - Typical Harsh Environment Electronics Temperature Ranges

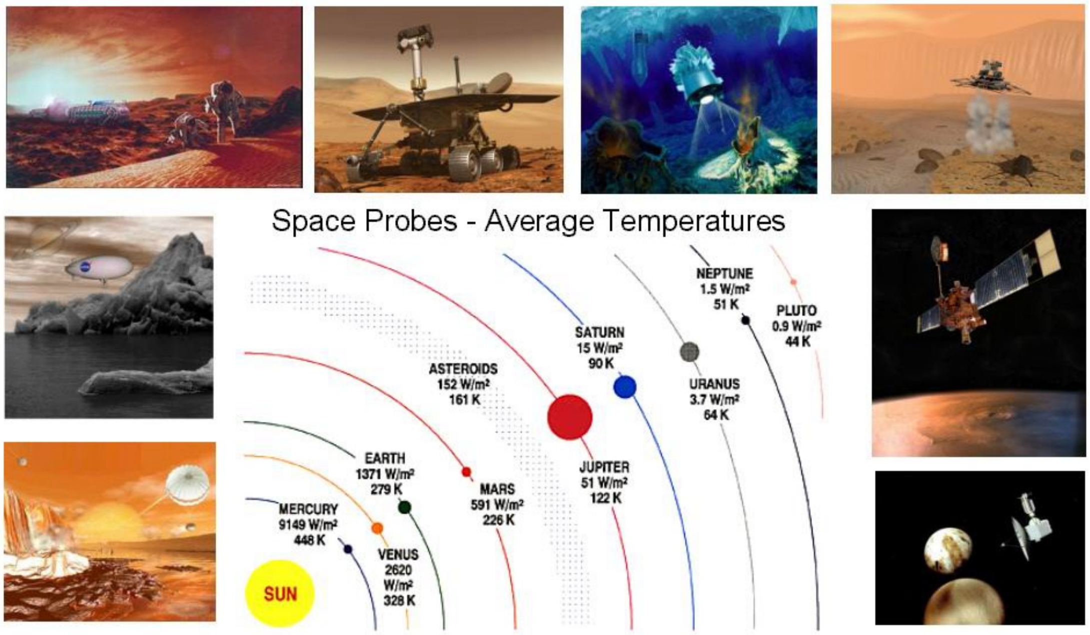

Space Probes - Average Temperatures
NEPTUNE
1.5 W/m²
51 K
PLUTO
0.9 W/m²
44 K
SATURN
15 W/m²
90 K
URANUS
3.7 W/m²
64 K
ASTEROIDS
152 W/m²
161 K
JUPITER
51 W/m²
122 K
EARTH
1371 W/m²
279 K
MARS
591 W/m²
226 K
MERCURY
9149 W/m²
448 K
VENUS
2620
W/m²
328 K
SUN

Figure 6.2 - Temperature Extremes for Planetary Missions

assemblies are approximately "stress free" near their assembly temperature, which is typically above 150 $^{o}$C when encapsulants and solders are involved. As the assemblies are cooled below room temperature, the temperature difference between ambient and "stress free" conditions becomes extremely high, and the thermal expansion mismatch induced stresses, strains, and deformations in the assembly can become very large. This phenomenon is exacerbated by the changes in material behavior that occur at low temperatures. In particular, encapsulants and solder become much more stiff/brittle, losing their typical nonlinear/inelastic stress-strain characteristics and high strains to failure.

Die stress measurements in flip chip assemblies have been performed using test chips [139, 141-144, 163]. Variations of the (100) silicon Sandia ATC04 test die have been utilized to examine device side die stresses and compare stress levels with different underfills [139, 141, 163]. In previous flip chip studies, the mechanical stresses present on the backside (top side) [142] and the device side (bottom side) [143-144] of the die at each stage of flip chip assembly process have investigated. In these investigations, (111) silicon test chips were utilized that were able to measure all of the die stress components including the interfacial shear stresses. Die stress variations were observed during underfill curing, and the room temperature die stresses in the final cured assemblies have been compared for several different underfill encapsulants. Finally, stress variations were monitored in the assembled flip chip die as the test boards were subjected to slow temperature changes from -40 to +150 $^{o}$C. No previous investigations have examined die stresses or package reliability in flip chip assemblies exposed to temperatures below -55 $^{o}$C.

In this work, the silicon die stresses occurring in flip chip assemblies at low temperatures to be found on future NASA space missions have experimentally characterized and numerically modeled. Stress measurements have been made at temperatures down to -180 °C using test chips incorporating piezoresistive sensor rosettes. The (111) silicon test chips utilized in this study are capable of measuring the complete state of stress at the die surface. The test chips were 5 x 5 mm in size, with 200-micron pitch perimeter solder bumps. Each test chip contained an array of optimized eight-element resistor rosettes for stress characterization, diodes for temperature measurement, and a sub-surface heater across the full die area.

The fabricated test chips have been utilized to measure the die stresses induced in the assembly over the temperature range of -180 to +150 °C. Using this approach, various underfills, liquid encapsulants, and solders (Sn-Pb and lead free) can be compared and ranked. The obtained stress measurement data have been correlated with the predictions of nonlinear finite element models. A microtester has been used to characterize the stress-strain behavior of the solders and encapsulants from -180 to 150 °C to aid in this modeling effort.

## 6.2 Packaging Technologies and Test Chips

A schematic of a typical flip chip on laminate assembly is shown in Figure 6.3. This configuration features a large coefficient of thermal expansion (CTE) mismatch between the silicon die and the substrate, leading to several reliability concerns including solder joint fatigue cracking during thermal cycling or die fracture at low temperatures.

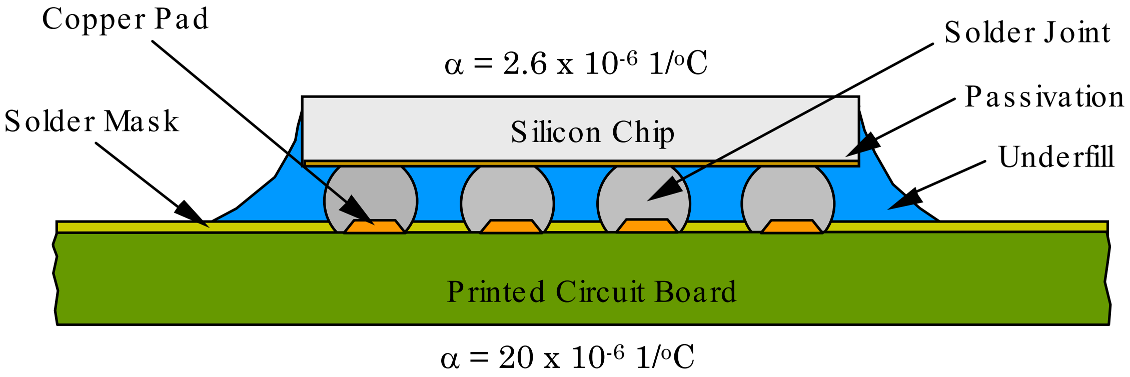

Copper Pad
Solder Joint
α = 2.6 x 10-6 1/oC
Passivation
Solder Mask
Silicon Chip
Underfill
Printed Circuit Board
α = 20 x 10-6 1/oC

Figure 6.3 - Chip on Board Assembly (Flip Chip)

The basic concept of the stress test chip approach is shown in Figure 1.1. The resistive sensors are conveniently fabricated into the surface of the die using current microelectronic technology. The sensors are not mounted on the chips. Rather, they are an integral part of the structure (chip) to be analyzed by the way of the fabrication process. In conductors such as silicon that exhibit the piezoresistive effect, the electrical resistivity changes when the material is subjected to stress or pressure, which leads to measurable resistance changes in the rosette elements. Using measured resistance changes and appropriate piezoresistive theory, piezoresistive sensors are capable of providing non-intrusive measurements of surface stress states in packaged chips. If the sensors are calibrated over a wide temperature range, thermally induced stresses can be measured. Finally, a full-field mapping of the stress distribution over the surface of a die can be obtained using specially designed test chips that incorporate an array of sensors rosettes.

The (111) silicon test chips utilized in this study contain piezoresistive sensor rosettes that are capable of measuring the complete state of stress at the die surface [35, 90, 92, 143-144]. The test chips were 5 x 5 mm in size, with 200-micron pitch perimeter solder bumps. Figure 6.4 shows a schematic of the flip chip test chip (FC200) used in this work. The FC200 wafers have a thickness of 625 μm (25 mils). In this study, wafers thinning process have not performed, so that the nominal dimensions of each test chip were 5.0 x 5.0 x 0.625 mm (200 x 200 x 25 mils). Each test chip design contains an array of optimized eight-element resistor rosettes for stress characterization (see Figure 6.5), diodes for temperature measurement, and a sub-surface heater across the full die area.

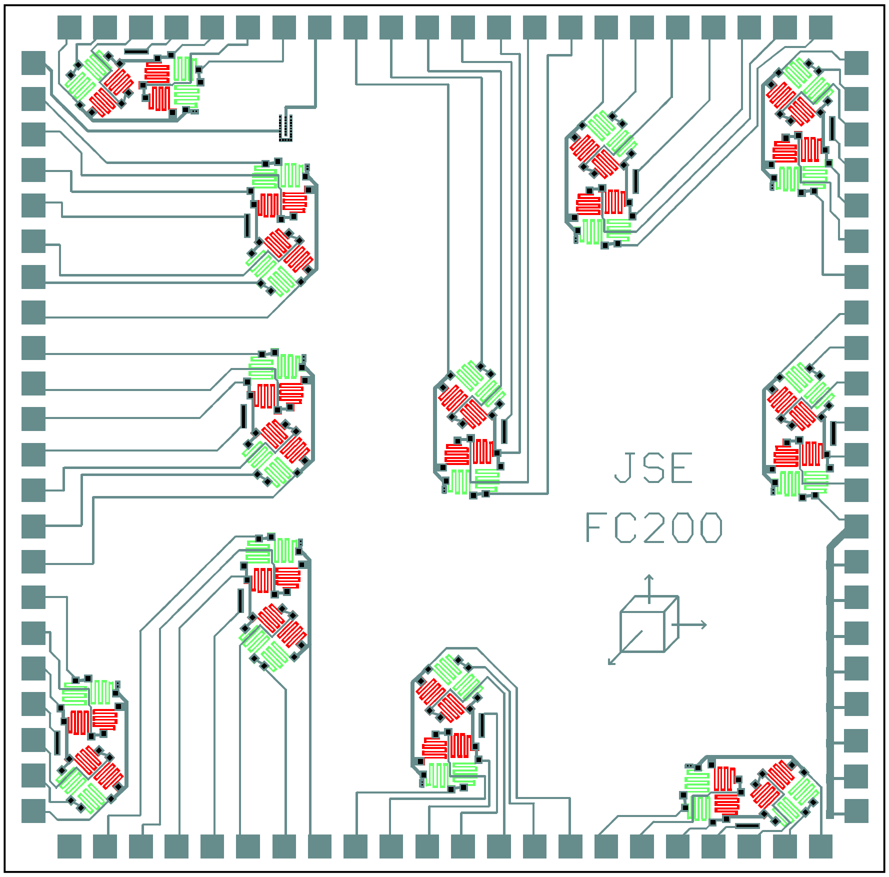


Figure 6.4 - Test Chip with Piezoresistive Sensors

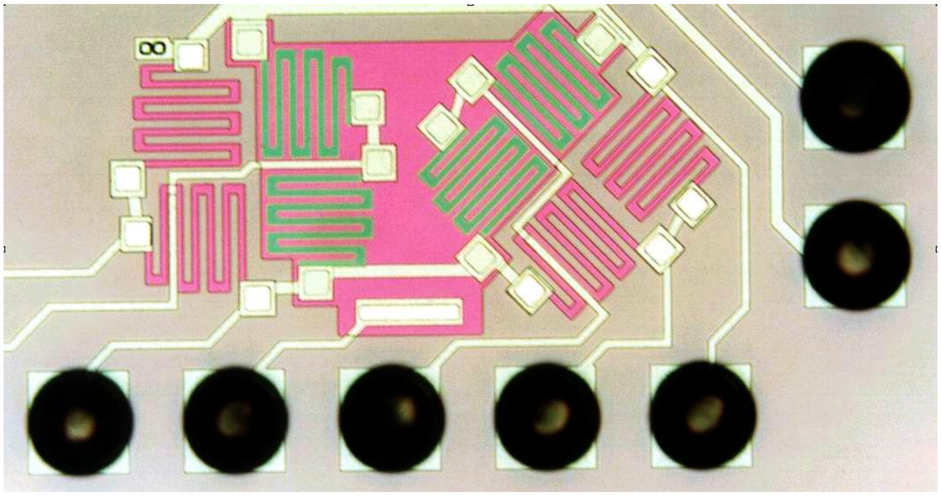


Figure 6.5 - Eight Element Piezoresistive Sensor Rosette

The eight rosette elements are routed to the die bond pads in a manner that allows them to be configured as four two-element half-bridges in order to simplify the resistor change measurements. A fully ion-implanted bipolar process has been used to balance the n- and p-type sheet resistances and resistor values, while maintaining high sensitivity to stress. Wafer bumping was performed using the Flip Chip Technologies (Kulicke and Soffa) process with an aluminum, nickel vanadium, and copper under bump metallurgy and 63Sn-37Pb solder alloy. The die pads have dimensions of 125 x 125 μm (5 x 5 mils), with a 75 μm (3 mil) spacing between pads. As shown in Figures 6.4 and 6.5, the corner bumps were not included in the perimeter arrays solder ball arrays. This intentional omission eases PCB routing challenges and removes the least reliable solder joints from the design.

When assembled in an underfilled flip chip configuration, the test chips have the piezoresistive sensors electrically accessible through the solder balls. Using the theoretical expressions in eqs. (5.1, 5.2), the stresses can be calculated from the measured resistance changes. The piezoresistive coefficients $B_1$, $B_2$ and $B_3$ present in the rosette equations were obtained for the test chips in the work using four-point bending and hydrostatic calibration methods. The average experimentally measured values are tabulated in Table 4.3. Further details on the calibration tests can be found in reference [92].

Test boards were designed and fabricated for preparation of the FC200 flip chip on laminate assemblies. Each test board was designed to accommodate a single centrally bonded FC200 stress test chip and its 88 solder bumps along the perimeter of the die.

The test board dimensions were 114 x 83 x 0.75 mm, and they were fabricated using FR4-06 prepreg, and copper traces with an Electroless Nickel Immersion Gold (ENIG) finish. Photos of an assembled test board and an underfilled FC200 stress die are shown in Figure 6.6. The soldermask opening under the chip on the test board was designed with the so-called “finger” approach, so that the ends of the PCB traces were used as bonding points for the flip chip solder balls.

The test boards were assembled at the SMT Line at Auburn University. Prior to placement, the test chip solder balls were dipped into a tacky, no-clean solder flux. The die were then aligned and placed on the test substrates using a Siemens SIPLACE $F^5$ high speed pick and place machine. Reflow was performed under a Nitrogen atmosphere in a Heller 1700 reflow oven. After solder reflow, initial sensor resistance data were measured to establish the “zero stress state” sensor resistance values. In reality, there are small stresses present in the chip due to the reflow process. In previous flip chip studies, the sensor resistances before and after reflow (die were manually probed before reflow) have measured, and then evaluated the stresses due to just the reflow process. The magnitudes of the measured die stresses due to die attachment were found to be universally small (e.g. 0-2 MPa). In this investigation, the die stresses due to solder reflow have been neglected to avoid the tedious process of probing the bumped stress chips before assembly. With this approach, the initial resistance values after reflow were assumed to be zero stress values, and all stress measurements are truly indicating the change in the die stress between the current states (where the final resistance values are measured) and the initial state (after reflow). Given the small magnitudes of the die stresses due to the reflow process, this approximation seems quite reasonable.

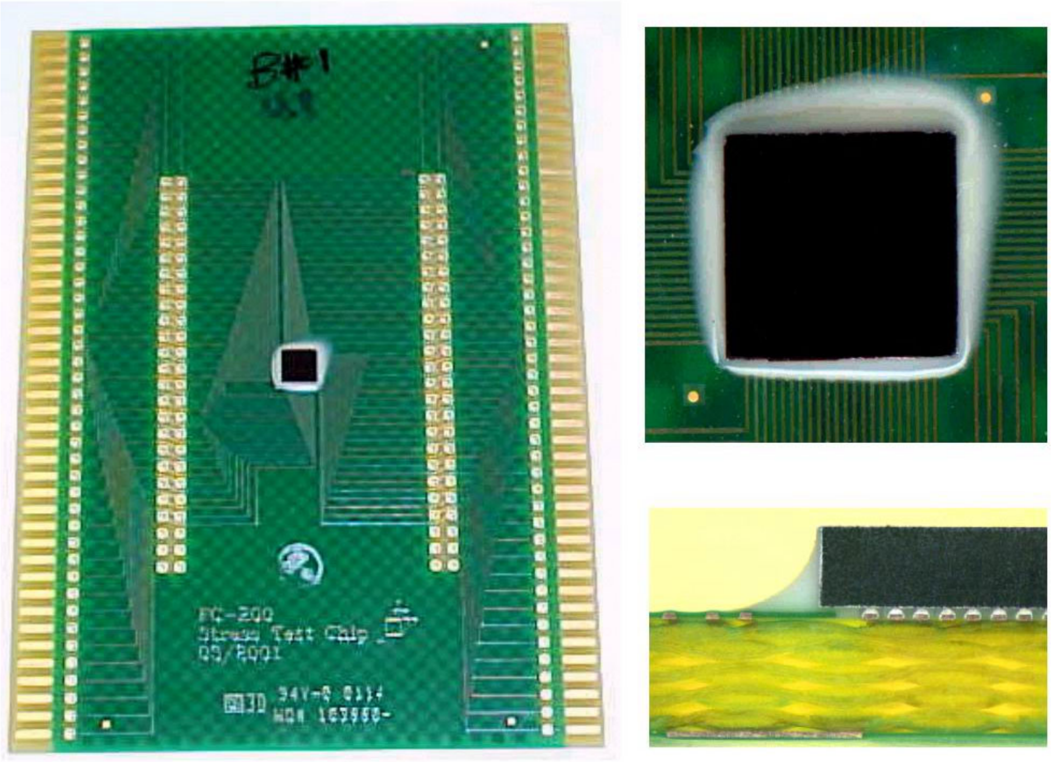

B#1
FC-200
Stress Test Chip
05/2001
94V-0

Figure 6.6 - Flip Chip Assembly Incorporating Stress Test Chip

The test board design allowed for 3 options for electrical connection to the FC200 stress sensors including edge connector, through holes for soldering individual wires, or through holes for soldering a ribbon cable connector. For both flexibility and ease of implementation in a variety of thermal environments, edge connectors were used for all connections to the test assemblies. All resistance measurements were completed using a PC-based data acquisition system incorporating a GPIB scanning system and digital multimeters.

Three different capillary flow underfill encapsulant materials from different vendors were used in the FC200 stress chip experiments. Each material was a snap/quick cure underfill requiring 5-30 minutes of high temperature curing. The glass transition temperatures, coefficients of thermal expansion, and recommended cure conditions for the three underfills are given in Table 5.2. The underfills were dispensed at near one corner of the die using a CAM/ALOT 3700 dispensing system. The work holder supporting the assemblies was heated to 95 $^{o}$C prior to underfill dispense, and the fast flow materials completely underfilled the die with one dot dispensed at the one corner. After dispense, the underfills were cured under the specified conditions in a box oven. Thermocouples were used to verify that proper durations of oven exposure were utilized and that the recommended cure temperature conditions were actually achieved within the underfill material.

A total of 5 specimens were prepared for low temperature testing with each underfill encapsulant. For each specimen and FC200 chip, the 11 rosette sites (88 resistors) were monitored as a function of temperature at each stress evaluation point. Figure 6.7 shows the rosette site designations for the resistance/stress measurements.

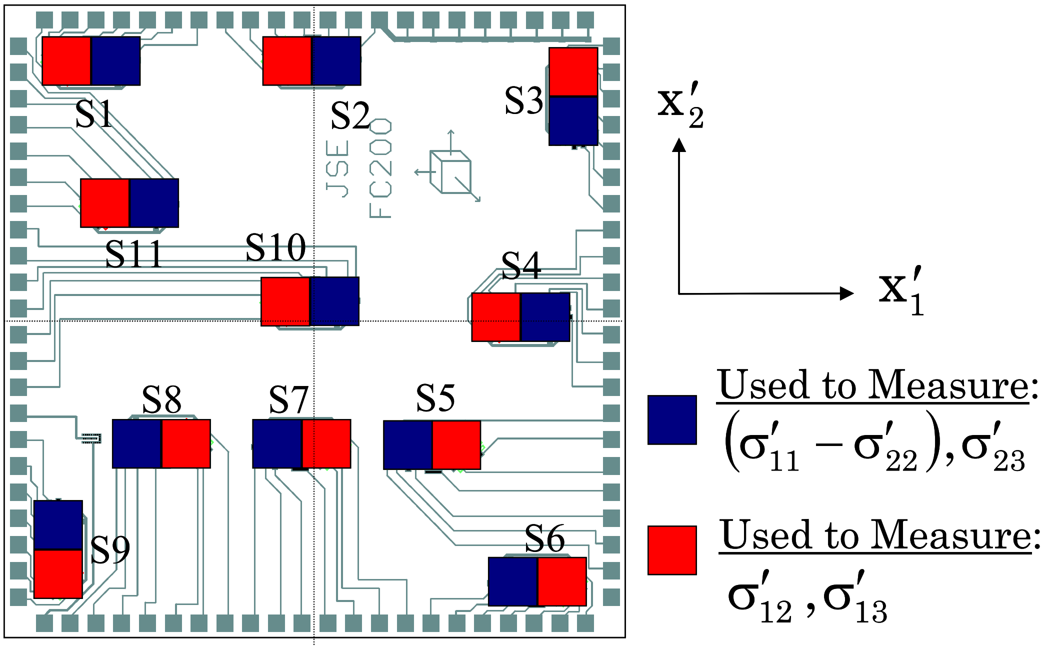

S1
S2
S3
JSE
FC200
S11
S10
S4
S8
S7
S5
S9
S6
$x_2'$
$x_1'$
🟦 Used to Measure: $(\sigma_{11}' - \sigma_{22}'), \sigma_{23}'$
🟥 Used to Measure: $\sigma_{12}', \sigma_{13}'$

Figure 6.7 - Rosette Sites for Stress Measurement

## 6.3 Test Results (-180 to +150 $^o$C)

After assembly, the resistances of the sensors were measured at room temperature (+20 $^o$C) to evaluate the initial stress state. The test samples were then subjected to slow temperature variations and the resistances of the stress sensors on the chip were further monitored. In the applied temperature profile, the assemblies were initially at room temperature, were next heated to +150 $^o$C, and then subsequently cooled to -180 $^o$C. Using the monitored sensor resistances, measurements of the various stress components at sites on the die surface were made over the entire temperature range of +20 to +150 to -180 $^o$C. For example, Figure 6.8 illustrates the variation of the in-plane shear stress in the one of the die corners in a typical flip chip assembly (UF1) during the environmental exposure. It can be seen that the magnitudes of the stress approaches zero as the assembly approaches its “stress free” state near 165 $^o$C where the underfill encapsulant UF1 was cured. As the temperature is lowered, the stress magnitudes increase, becoming very high at extreme low temperatures. In making the stress measurements shown in Figure 6.8, it has been assumed that the piezoresistive coefficients are independent of temperature. Similarly the variation of the in-plane normal stress difference $\sigma'_{11} - \sigma'_{22}$ at one of the rosette sites in one of the UF3 boards is shown in Figure 6.9.

The resistance of the doped silicon sensors exhibits a stress-free temperature dependence referred to as the temperature coefficient of resistance (TCR) effect. The piezoresistive sensors rosettes used here eliminate the need to consider these changes by using temperature compensated measurements where the TCR effect is cancelled in the stress extraction equations. However, one also needs to be careful of potential changes in

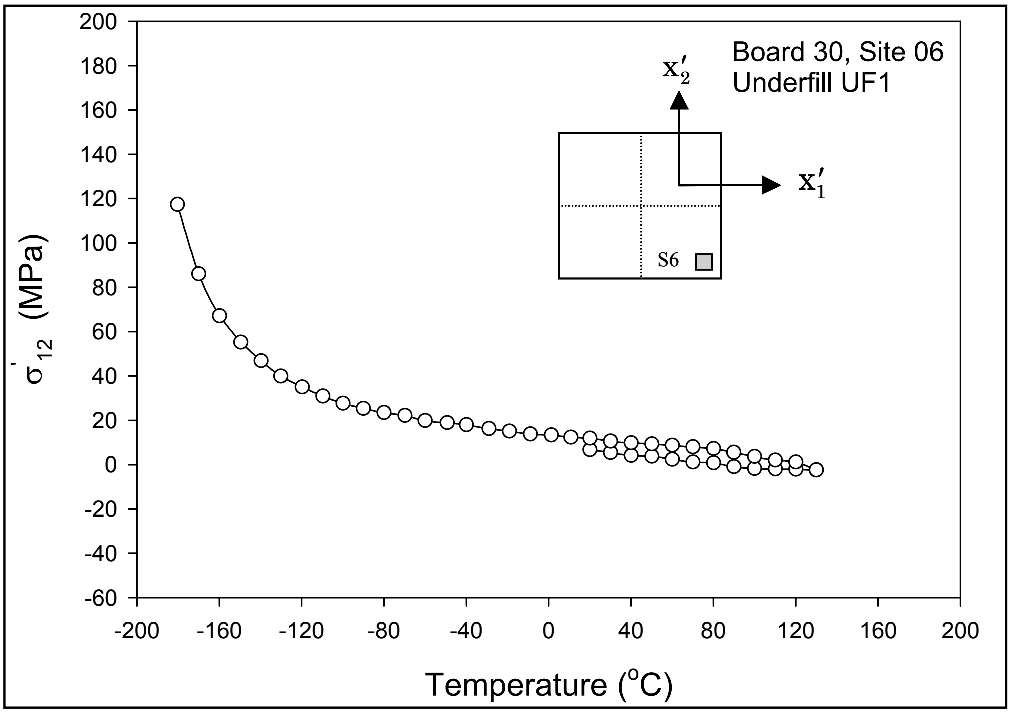


Figure 6.8 - Measured Die Stress Variation with Temperature

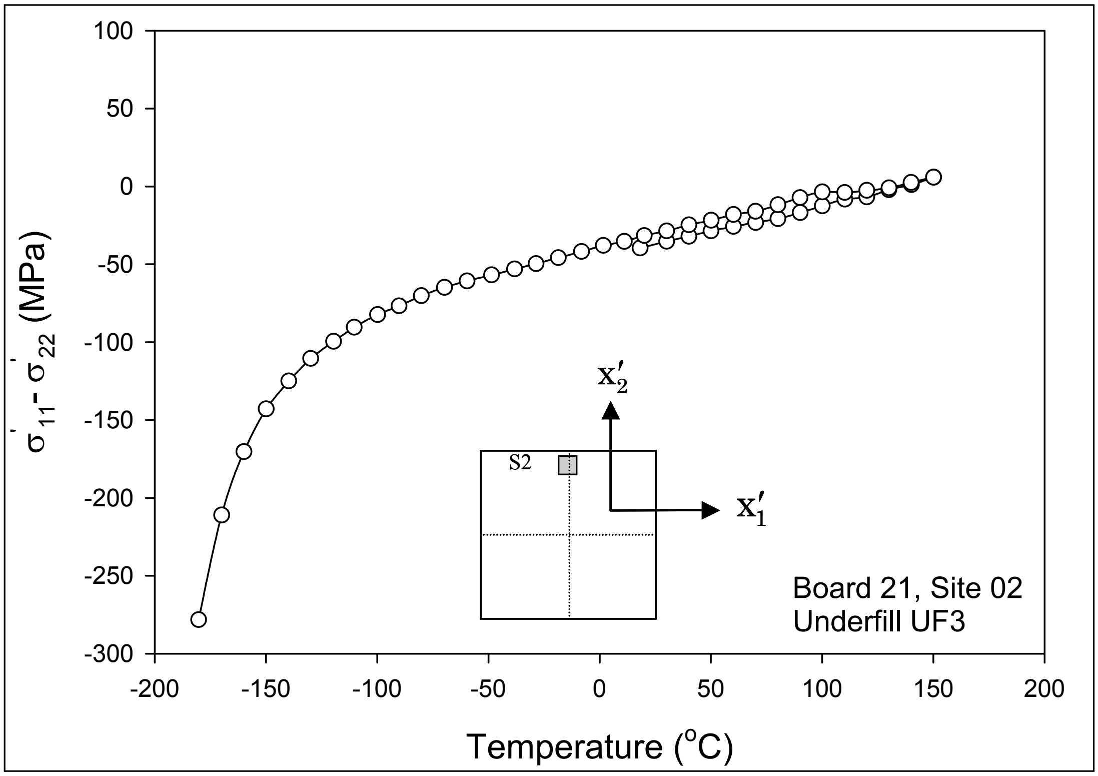


Figure 6.9 - Measured Die Stress Variation with Temperature

the governing semiconductor physics that can occur at extreme low temperatures due to "freeze out" phenomenon. Figure 6.10 and 6.11 illustrate plots of the stress-free (unpackaged) thermal behavior of the test chip sensors over the temperature range of -180 to +150 °C for n and p-type sensors, respectively. It can be seen that the heavily doped n-type resistors exhibit the expected monotonic TCR effect, while the more lightly doped p-type resistors illustrate some freeze out effects at temperatures below -50 °C.

The unusually high stress magnitudes and drastic slope changes observed in Figures 6.8-6.9 for temperatures below -50 °C are believed to be incorrect due to the freeze out effect illustrated by the p-type resistor sensors for extreme low temperatures. Since the n-type sensors do not seem to illustrate the freeze out phenomenon, we have repeated the stress measurement calculations a second time with only the n-type sensor data being used in the stress extractions. To complete such calculations, it was necessary to neglect the out of plane shear stresses $\sigma'_{13} \approx \sigma'_{23} \approx 0$. These approximations are reasonable given the magnitudes for these stress components observed in previous flip chip studies with these assemblies [144]. Using these approximations in the piezoresistive theory in eqs. (3.15 and 4.1) results in a modified set of stress extractions expressions that involve only the n-type sensor resistance changes [35, 90, 92]:

$$\begin{aligned} \sigma'_{11} - \sigma'_{22} &= \frac{1}{(B_1^n - B_2^n)}\left(\frac{\Delta R_1}{R_1} - \frac{\Delta R_3}{R_3}\right) \\ \sigma'_{12} &= \frac{1}{2\,(B_1^n - B_2^n)}\left(\frac{\Delta R_2}{R_2} - \frac{\Delta R_4}{R_4}\right) \end{aligned} \tag{6.1}$$

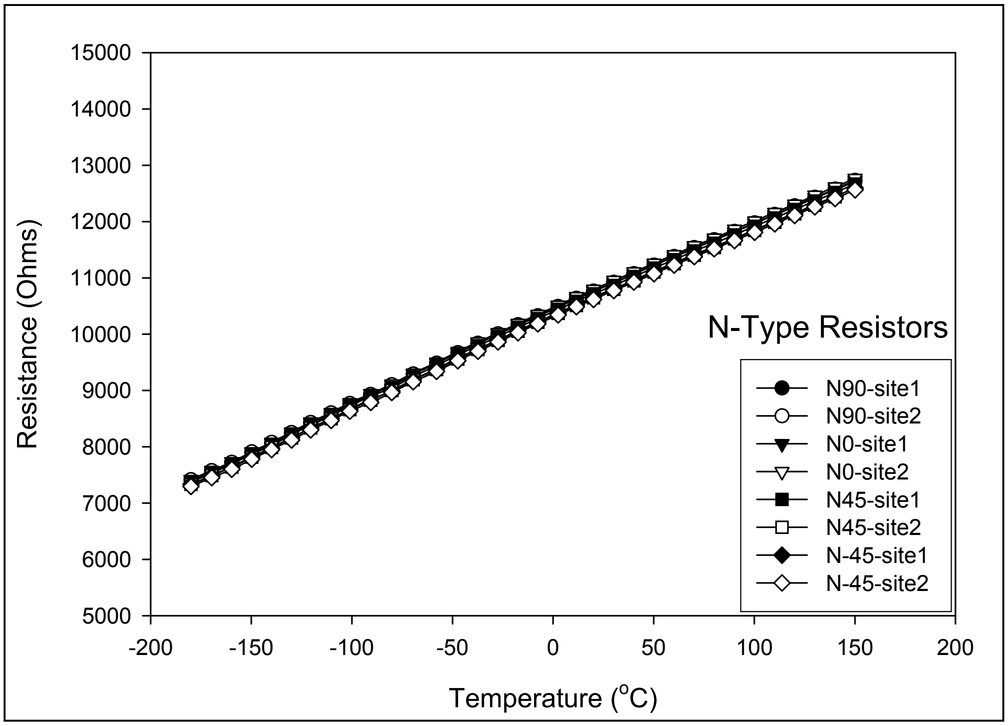


Figure 6.10 - Resistance vs. Temperature for the Resistor Sensors (Stress Free Conditions)

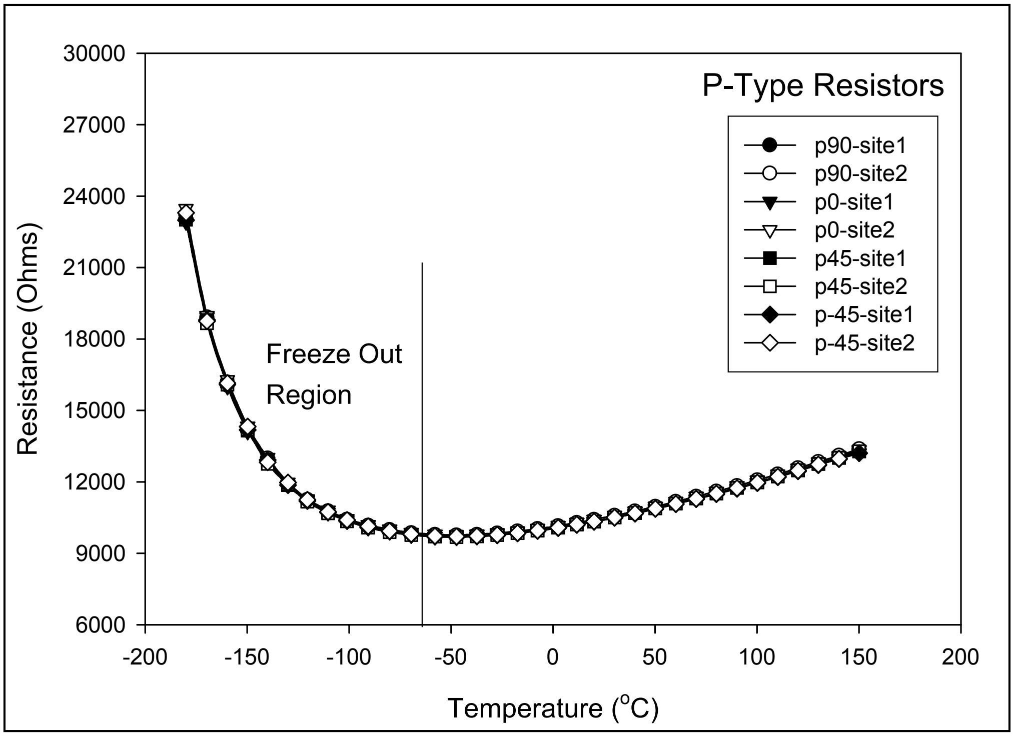


Figure 6.11 - Resistance vs. Temperature for the Resistor Sensors
(Stress Free Conditions)

With this approach, revised stress vs. temperature plots were obtained. For example, Figure 6.12 illustrates a modified version of the in-plane normal stress difference variation shown earlier in Figure 6.9. The "corrected" results in this plot better reflect the expected linear/elastic behavior of the assembly at low temperatures. We are currently developing further approaches for characterizing and calibrating the piezoresistive behavior of the sensors at extreme low temperatures where freeze out may occur. Using the stress sensor approach, various underfills and solders (Sn-Pb and lead free) for use in low temperature flip chip applications can be compared and ranked.

## 6.4 Finite Element Simulations and Low Temperature Material Characterization

The obtained stress measurement data have also been correlated with the predictions of nonlinear finite element models performed using ANSYS. The stress-strain behavior of various electronic packaging materials have been characterized from -180 to 150 $^{o}$C to aid in this modeling effort. A microscale tension-torsion test system or "microtester" with associated environmental chamber (see Figure 6.13) has been developed for temperature controlled mechanical loading of small test specimens of microelectronic packaging materials including solders (standard and lead free), encapsulants (underfills, chip on board, etc.), adhesives (die attachment, thermal interfaces), and substrates (organic, ceramic, advanced). The environmental chamber is capable of heating to 300 $^{o}$C, and can cool down to -185 $^{o}$C using recirculated cold nitrogen gas from a liquid nitrogen source.

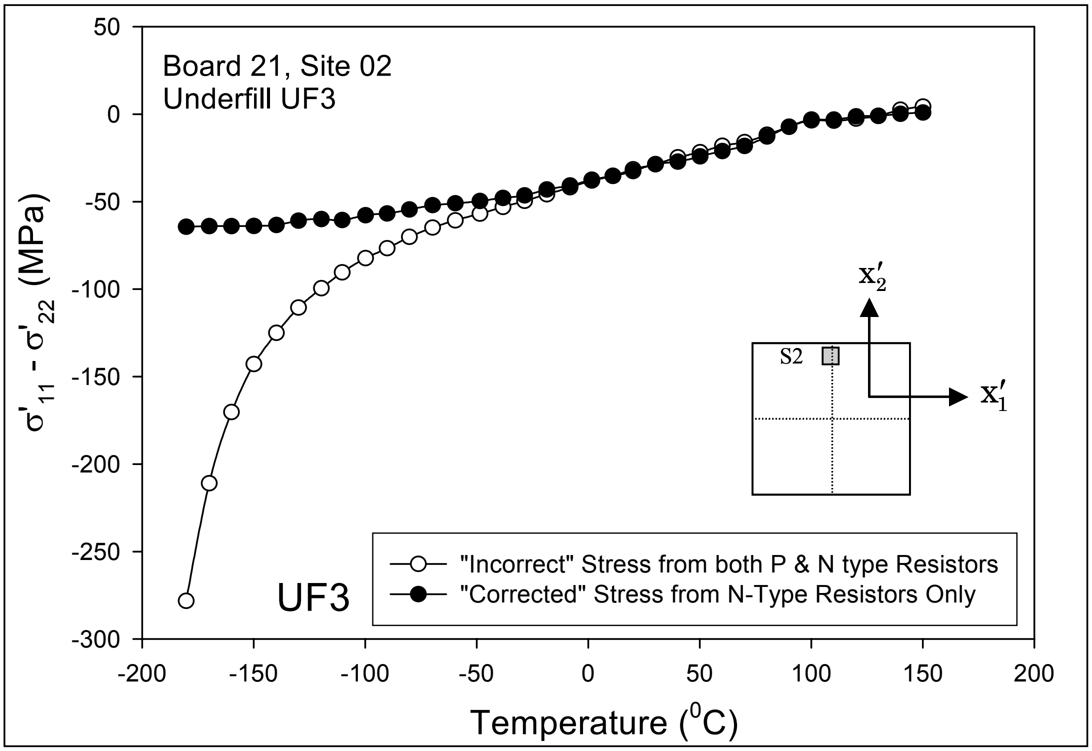
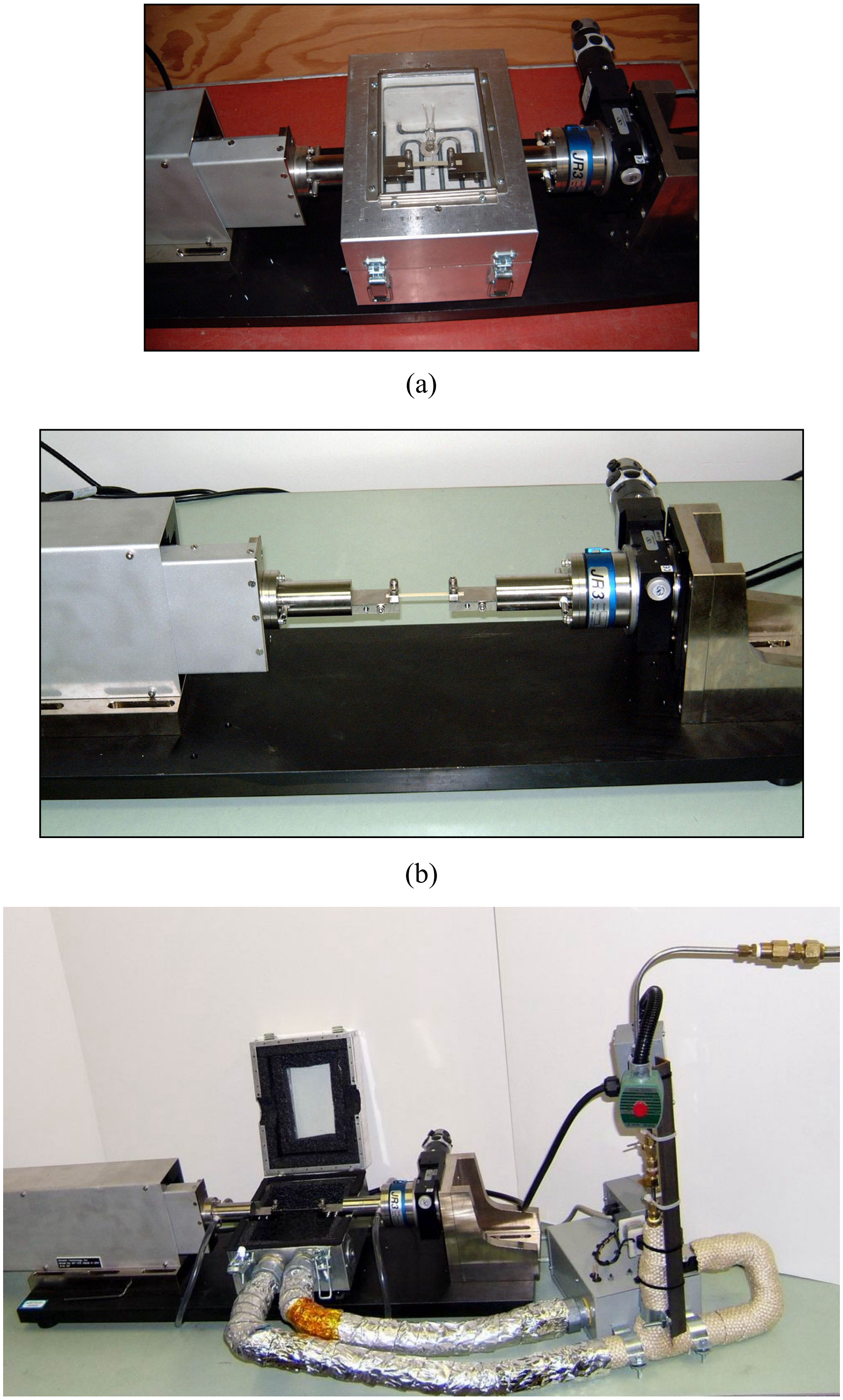


Figure 6.12 - Corrected Measurements of the Die Stress Variation with Temperature



(a)

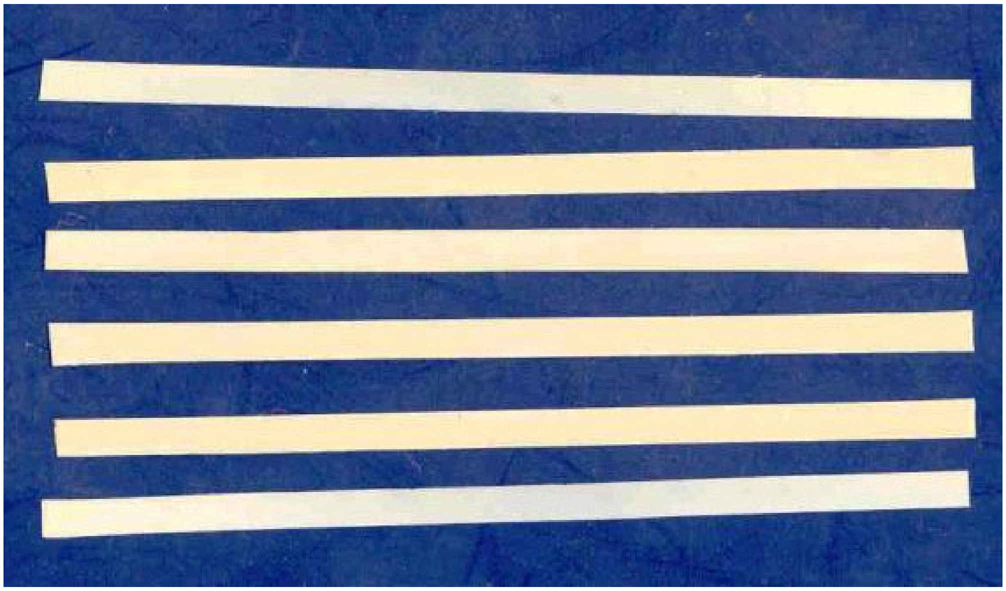
(b)

(c)

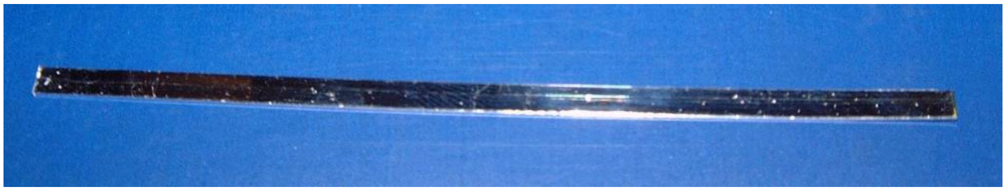
Figure 6.13 - Microtester and Associated Environmental Chamber

New specimen preparation procedures are necessary to fabricate polymer and metallic uniaxial test samples that are cured/cooled with the same temperature profiles as used in actual electronics assembly and packaging processes. Two novel preparation techniques have developed to fabricate test specimens that yield samples that truly mimic the materials present in thin encapsulant layers and real solder joints (match both composition and microstructure). In the first method, thin encapsulant samples are cast in a Teflon-coated "mold assembly" using production dispense and curing equipment [156]. In second technique, solder uniaxial test specimens are formed in rectangular cross-section glass tubes using vacuum suction and reflow processes [197]. Figure 6.14 shows example test specimens.

With the developed system, stress-strain and creep tests have been performed on microelectronic encapsulants and both tin-lead and tin-silver-copper (lead free) solder alloys over the range of -175 to +200 $^{o}$C. For example, stress-strain curves of a typical underfill encapsulant (UF3) are shown in Figure 6.15 for the temperature range of -175 to +150 $^{o}$C, and stress-strain curves for 63Sn-37Pb solder are shown in Figure 6.16 for the temperature range of -175 to +25 $^{o}$C. The measured elastic moduli of the same underfill encapsulant and solder are plotted over the temperature range -175 to +150 $^{o}$C in Figures 6.17 and 6.18, respectively. In the case of the underfill encapsulant, the material is highly viscoplastic at room temperature and above. At lower temperatures, the silica-filled epoxy encapsulating material becomes nearly linear elastic and the stiffness becomes very high. In the case of the solder, the material shows elastic-plastic tendencies at all temperatures, and the yield stress becomes very high at low temperatures as expected.



(a) Underfill Encapsulant



(b) Solder

Figure 6.14 - Test Specimens: Underfill Encapsulant and Solder

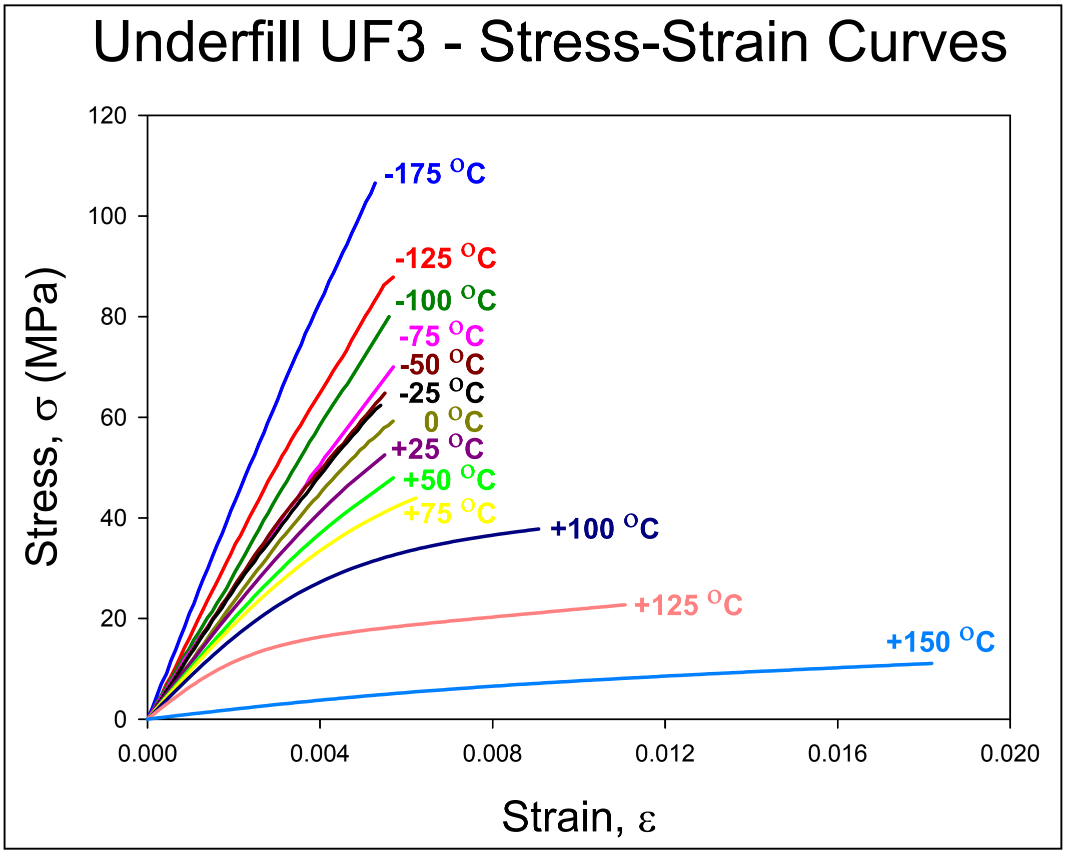


Figure 6.15 - Underfill Stress-Strain Curves (-175 to +150 °C)

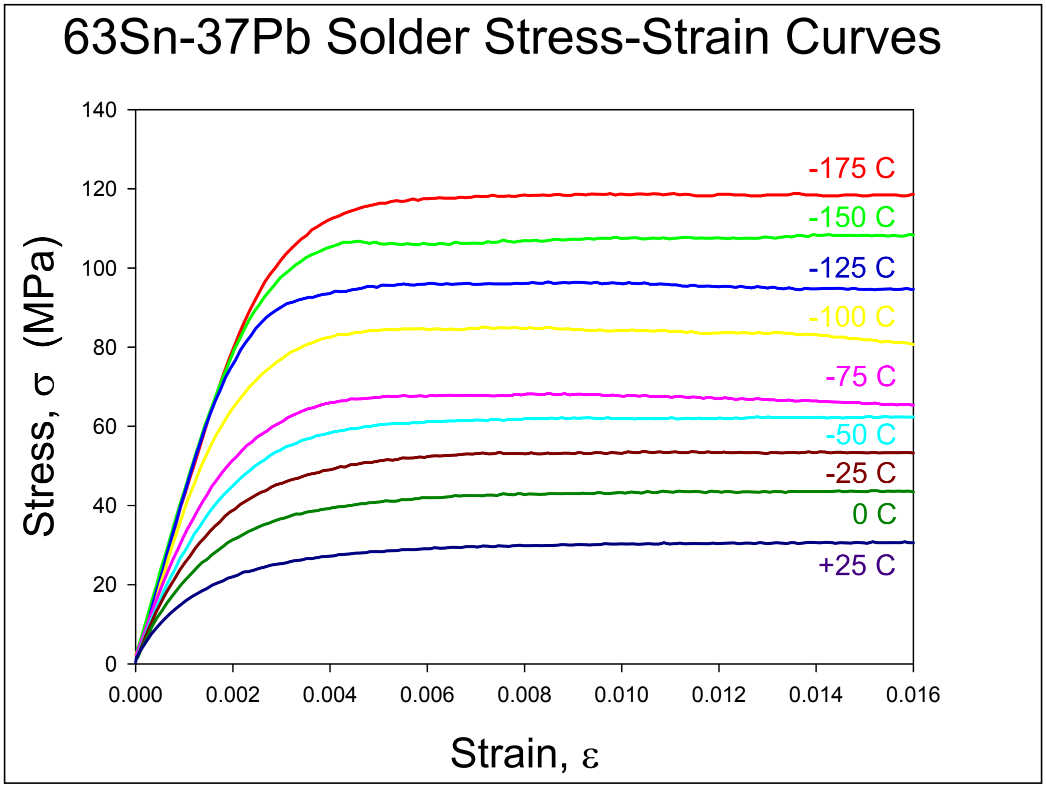


Figure 6.16 - Solder Stress-Strain Curves (-175 to +25 °C)

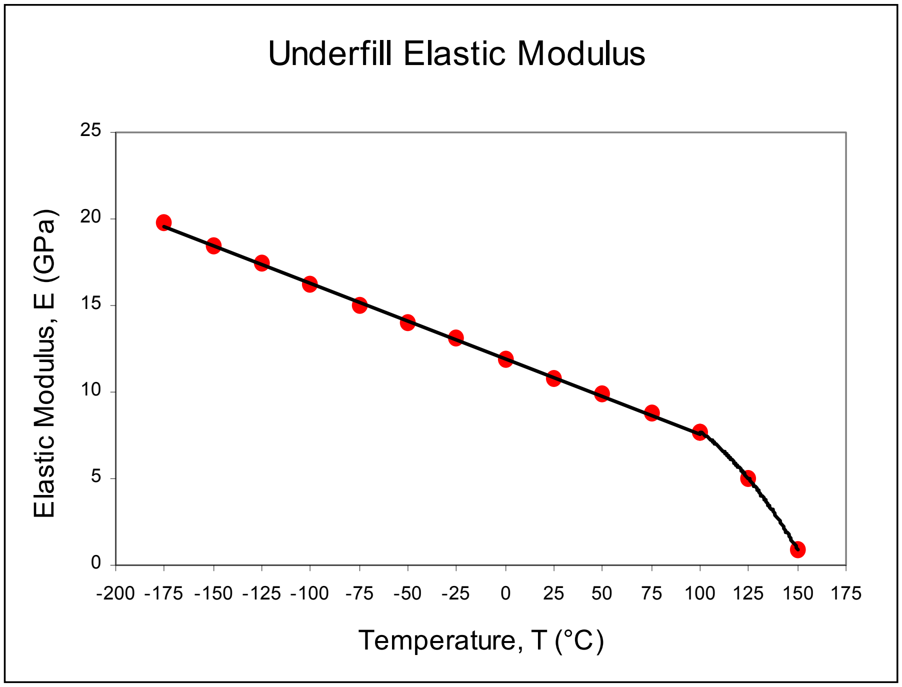


Figure 6.17 - Elastic Modulus vs. Temperature for Underfill (-175 to +150 $^o$C)

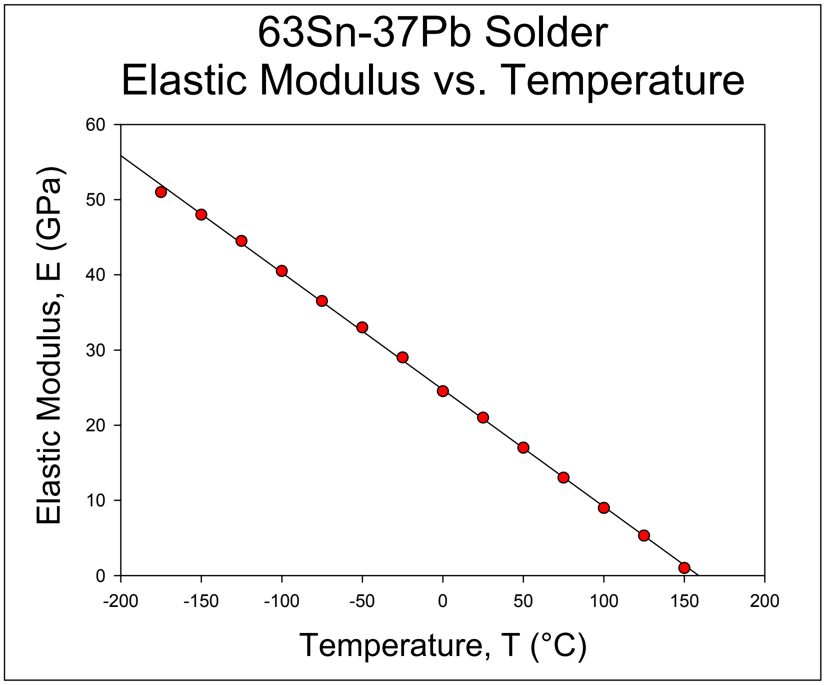


Figure 6.18 - Elastic Modulus vs. Temperature for Solder (-175 to +150 $^o$C)

In the finite element models, temperature dependent mechanical properties and large deformations (kinematic nonlinearities) were utilized. The nonlinear and elastic-plastic behaviors of the underfill encapsulant (UF3) and solder (63Sn-37Pb) were modeled using the data presented in Figures 6.15-6.16. However, the time dependent (viscoplastic) behaviors of these materials were neglected to simplify the analysis. The remainder of the assembly materials (copper, silicon, FR-4) were modeled as linear elastic. The entire assembly was assumed to be stress free at the cure temperature (165 $^{o}$C) of the underfill encapsulant, and cooling from the cure temperature to room temperature was simulated. It should be emphasized that the experimental measurements were the main emphasis of this work. The finite element model predictions were used to show the proper signs and approximate trends of the various stress component distributions, so that the experimental data could be better understood.

The mesh (quarter symmetry) utilized in the finite element simulations is shown in Figure 6.19. The finite element predictions for the temperature dependent (+150 to -180 $^{o}$C) die surface stress distributions are shown in Figures 6.20 for the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$). As expected, the stress magnitudes are nearly zero at 150 $^{o}$C, and increase as the temperature is lowered. A typical correlation between the experimental test chip measurements and the finite element predictions for the in-plane normal stress difference ($\sigma'_{11} - \sigma'_{22}$) at one of the sensor sites is shown in Figure 6.21. Good agreement was obtained with the experimental results obtained when only the n-type sensors are utilized (i.e. the corrected data in Figure 6.12).

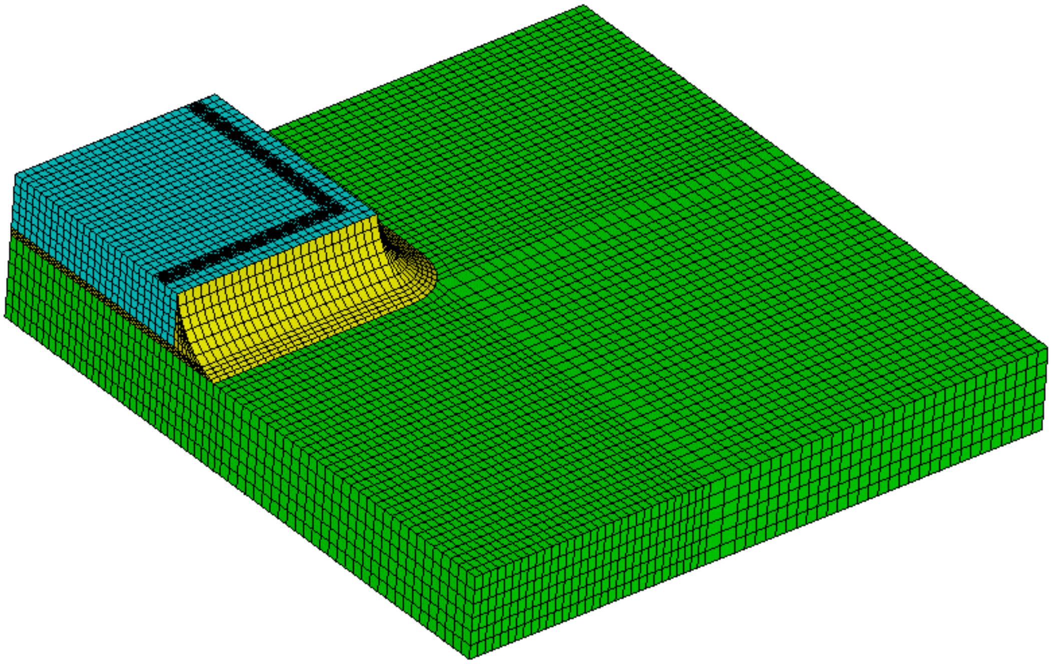


Figure 6.19 - Finite Element Mesh for the Flip Chip Test Assembly

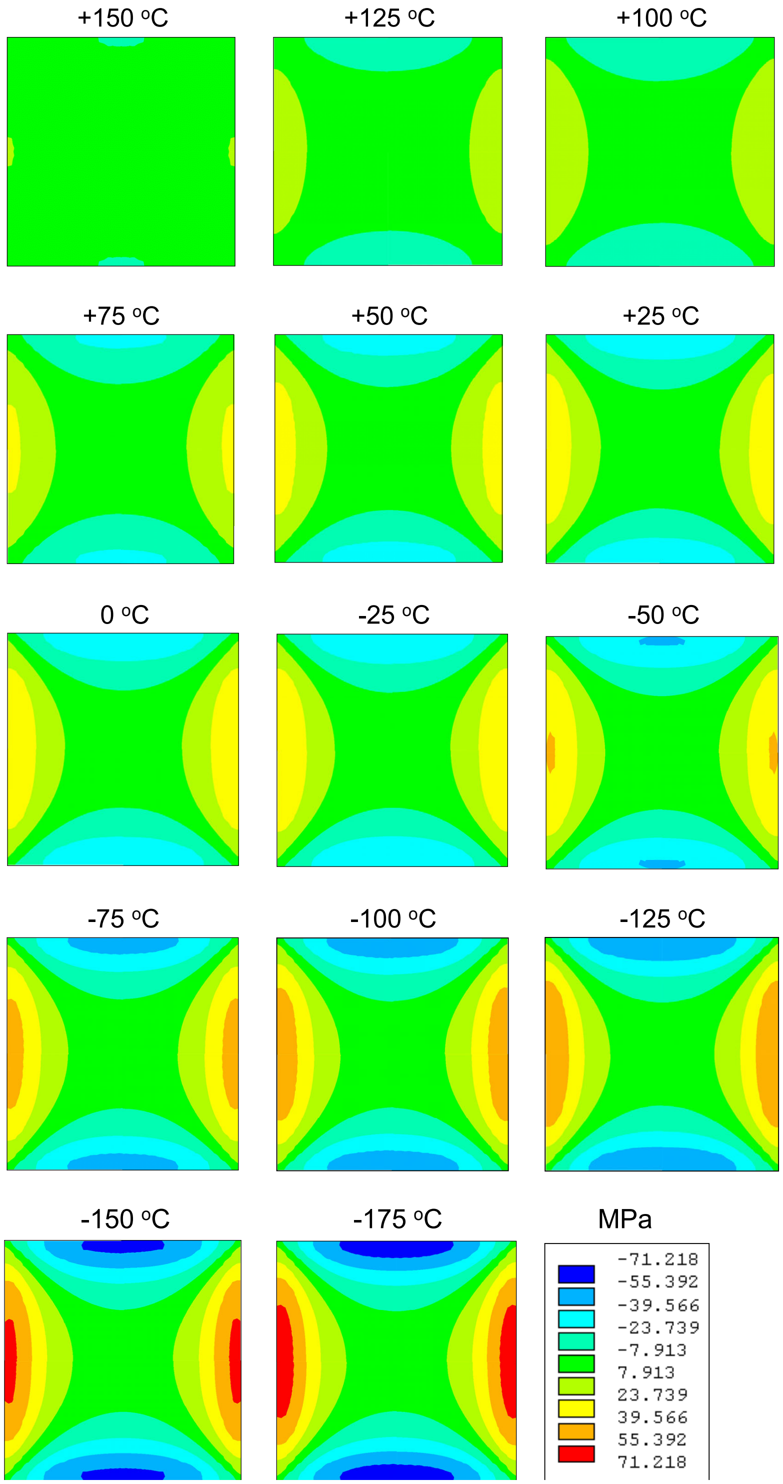


Figure 6.20 - Finite Element Predictions for the Normal Stress Difference Contours at Various Temperatures

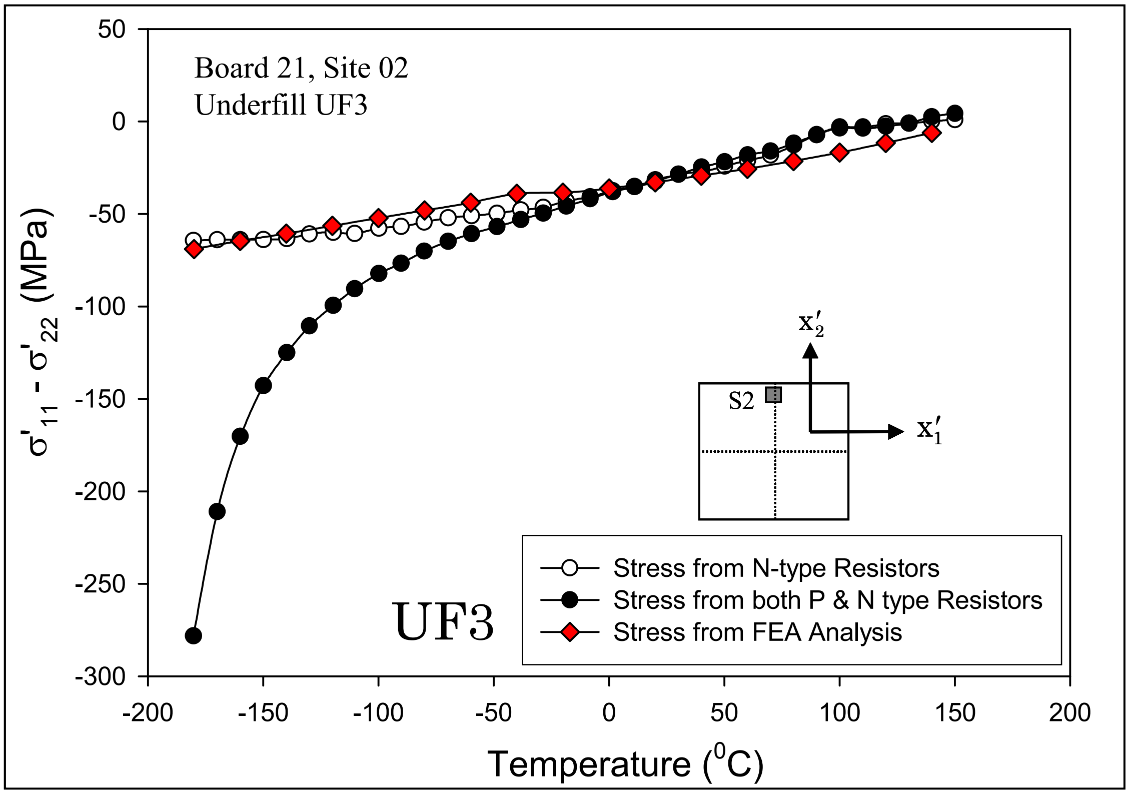


Figure 6.21 - Correlation between Finite Element Predictions and Experimental Data

## 6.5 Summary

In this work, the silicon die stresses occurring in flip chip on laminate assemblies at extreme low temperatures to be found on future NASA space missions have experimentally characterized and numerically modeled. Stress measurements have been made from -180 to +150 $^{o}$C using test chips incorporating piezoresistive sensor rosettes. The p-type resistors in the utilized test chips were found to exhibit freeze out effects at temperatures below -50 $^{o}$C, so that accurate stress measurements could only be made using the measured resistance changes exhibited by the n-type sensors. The obtained stress measurement data were then correlated with the predictions of nonlinear finite element models, and good agreement was found. The finite element models incorporated temperature dependent material property data. A microtester was used to characterize the stress-strain behavior of the solders and encapsulants from -180 to 150 $^{o}$C.

# CHAPTER 7

# FUNDAMENTALS OF DELAMINATION INITIATION AND GROWTH IN FLIP CHIP ASSEMBLIES

## 7.1 Introduction

As discussed earlier chapters, underfill encapsulation is used with flip chip die assembled to laminate substrates to distribute and minimize the solder joint strains, thus improving thermal cycling fatigue life. Any delaminations that occur at the underfill/die interface will propagate to the neighboring solder bumps and lead to solder joint fatigue and failure. The onset and propagation of delaminations in flip chip assemblies exposed to thermal cycling are governed by the cyclic stresses and damage occurring at the underfill to die interface. For this reason, underfills are optimized by increasing their adhesion strength, interfacial fracture toughness, and resistance to thermal aging.

A typical flip chip on laminate assembly is shown in Figure 5.1. Due to the large coefficient of thermal expansion (CTE) mismatch between the silicon chip and the organic laminated substrate (see in Figure 6.3), underfill encapsulation is typically used to more evenly distribute and minimize the solder joint strains, thus improving thermal cycling fatigue life. With the die coupled to the substrate through the underfill epoxy, bending of the assembly occurs and the dependence of the solder bump shear strains on the distance from the chip center (neutral point) is reduced. Delamination at the underfill/die interface becomes the primary failure mode. If interfacial cracks develop and propagate to the neighboring solder bumps, the previously described stress relief on the solder joints will be lost and the onset of solder joint fatigue cracking will be hastened. The onset and propagation of delaminations in flip chip assemblies exposed to thermal cycling are governed by the stress state at the underfill to die interface. The critical stresses have maximum values at the corners of the die. As a flip chip assembly is thermally cycled, the interfacial stresses also cycle in value and the interface is subjected to fatigue and damage. For this reason, underfills are optimized to resist delamination by increasing their adhesion strength, interfacial fracture toughness, and resistance to thermal aging.

Flip chip packages consist of multiple layers and thin film coatings. The underfill/die interface is a weak link due to imperfect adhesion and stress concentration. The initiation and growth of underfill/die interface cracks determines the reliability and performance of the flip chip packages. Therefore, study of interface delamination is crucial to the reliability prediction. Several researchers have studied delamination and interfacial stresses in flip chip assemblies [171-178]. In the majority of these efforts, the authors have investigated interface delamination and cracking of the underfill in flip chip packages under temperature cyclic loading using facture mechanics and/or finite element analysis [171-176]. Jackshick, et al. [177] have used optical microscopy to observe delamination propagation rates with glass die, while Hirohata and co-workers [178] have introduced a new mechanical fatigue test method for predicting the delamination resistance of underfill interfaces.

The primary experimental tool for study of delaminations in electronic packaging is C-Mode Scanning Acoustic Microscopy (CSAM). This technique is especially adept at revealing delaminations between silicon die and a surrounding encapsulant. For analysis, the flip chip samples are immersed in water and a sonic high frequency transducer emitting sound wave pulses is scanned over the die surface by a highly accurate translation stage. Sound energy is reflected by internal surfaces in the sample and detected by the same sonic transducer. The depth at which the reflection occurs may be estimated from the time at which the reflected sound pulse is received. Total reflection of the sound pulse occurs at the interface between solid materials and air or vacuum, for example at a void or delamination. An image is built up from the scan by gating the reflection signal from the transducer to cover the layer or layers of interest in the packages. The magnitude of the largest reflection between the gates is mapped to a grayscale value to form a pixel of the image. Because total reflection of the sound pulse occurs at the interface between solid materials and air or vacuum, voids and delamination usually cause the largest reflected signal and hence appear white within the image. When using the method on flip chip assemblies, focused acoustic waves are impinged on the die to underfill interface, and the phase and magnitude of the reflected beams are observed. The presence of phase reversals in the reflected waves signifies acoustic impedance drops resulting from the existence of an air gaps (delaminations) at the interface. By systematically scanning the entire die to underfill interface, a mapping of the delamination locations can be obtained. Although adept at identifying delaminations locations, the CSAM technique is unable to interrogate the stress state at the die to underfill interface. For this reason, it has been impossible in the past to experimentally establish the loading/stress conditions responsible for the onset of delamination or to quantify the level of damage prior to delamination initiation. In addition, little is known of the mechanisms that occur during delamination growth.

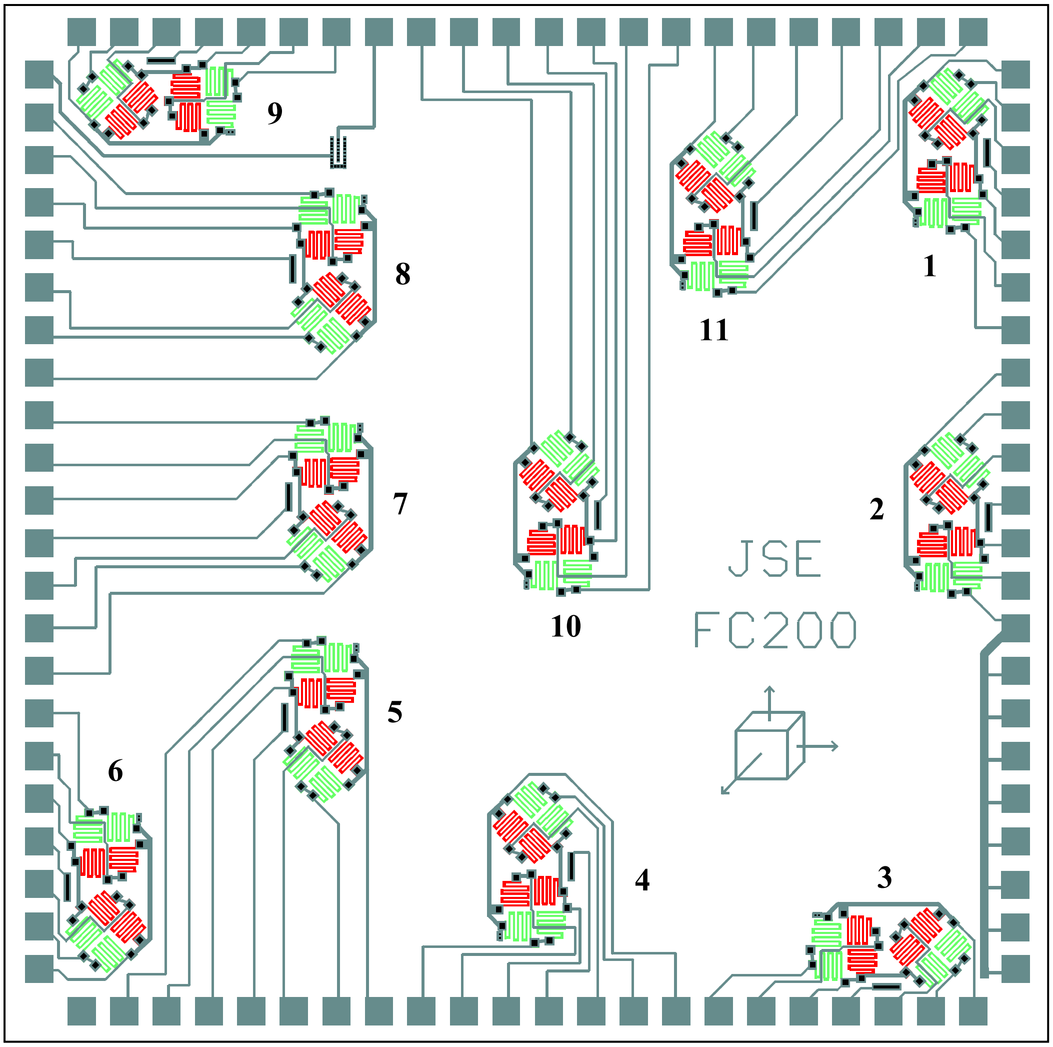
Stress sensing test chips are powerful tools for measuring in-situ stresses in electronic packages [34, 35, 90]. In prior work, variations of the (100) silicon Sandia ATC04 test die have been utilized to examine device side die stresses in flip chip on laminate assemblies [139, 141, 163]. The use of test chips fabricated in the (100) plane allow in-plane stresses to be characterized, but precludes the measurement of the interfacial (out-of-plane) shear stresses between the underfill layer and die surface. To further aid in investigation of flip chip delamination and failure phenomena, (111) silicon test chips have developed and applied that can be used to measure all of the die stress components including the interfacial shear stresses [23, 92, 142-144, 167, 169].

In this work, a fundamental understanding of delamination initiation and growth in flip chip assemblies through simultaneous characterization of the stress and delamination states at the die to underfill interface during thermal cycling have been developed. Mechanical stresses on the device side of the flip chip die have been measured using special (111) silicon stress test chips containing piezoresistive sensor rosettes that are capable of measuring the complete three-dimensional silicon surface stress state in the silicon (including the interfacial shear and normal stresses at the die to underfill interface). The fabricated flip chip test die were first assembled to FR-406 laminate substrates and encapsulated using 3 different underfills. The assemblies were then subjected to 3000 thermal cycles from -40 to 125 $^{o}$C. By continuous monitoring of the sensor resistances during the environmental testing, the die surface stresses were measured throughout the post-assembly thermal cycling exposure. With this approach, the stress distributions across the chip, and the stress variations at particular locations at the die to underfill interface have been interrogated for the entire life of the flip chip assembly. In order to correlate the stress changes at the sensor sites with delamination onset and propagation, CSAM evaluation of the test assemblies was performed after every 125 thermal cycles.

A total of 75 flip chip assemblies with 3 different underfills have been evaluated. Testing of 75 flip chip assemblies has been completed to date (1 die size x 3 underfills x 25 samples per combination). In each assembly, the complete histories of the three-dimensional die surface stresses and delamination propagation have been recorded versus the duration of -40 to 125 $^{o}$C thermal cycling. With this approach, the stress histories that lead to delamination initiation for each underfill encapsulant, and the variation of the stresses that occur before and during delamination propagation have been identified. The progressions of stress and delamination have been mapped across the entire surface of the die, and a series of stress/delamination videos have been produced. One of the most important discoveries is that the shear stresses occurring at the corners of flip chip die have been demonstrated to be a suitable proxy for prognostic determination of future delamination initiations and growth.

## 7.2 Stress Test Chips

Figure 7.1 shows the layout of the FC200 flip chip test die used in this study. The basic chip image has dimensions of 5 x 5 mm (200 x 200 mils), and contains 200 μm (8 mil) pitch perimeter solder bumps. This chip includes 11 eight-element sensor rosettes, a



9
8
7
5
6
10
4
3
11
1
2
JSE
FC200

Figure 7.1 - FC200 Flip Chip Test Die (5 x 5 mm)

diode for temperature measurement, and an eight-bit fuse style chip ID. A close up photograph of one of the FC200 sensor rosettes was shown previously in Figure 5.8. Detailed descriptions and capabilities of the FC200 test chip were also discussed in Chapter 5.

When assembled in an underfilled flip chip configuration, the test chips have the piezoresistive sensors electrically accessible through the solder balls. Using the theoretical expressions in eqs. (5.1, 5.2), the stresses can be calculated from the measured resistance changes. The piezoresistive coefficients $B_1$, $B_2$ and $B_3$ present in the rosette equations were obtained for the test chips in the work using four-point bending and hydrostatic calibration methods. The average experimentally measured values are tabulated in Table 5.1.

## 7.3 Test Board Assembly

The FC200 stress test chip wafers have a thickness of 625 μm (25 mils). In this study, wafer thinning process has not performed, so that the nominal dimensions of each test chip were 5.0 x 5.0 x 0.625 mm (200 x 200 x 25 mils). Test boards were designed and fabricated for preparation of the FC200 flip chip on laminate assemblies. Each test board was designed to accommodate a single centrally bonded FC200 stress test chip and its 88 solder bumps along the perimeter of the die. The test board dimensions were 114 x 83 x 0.75 mm, and they were fabricated using FR4-06 prepreg, and copper traces with an electroless Nickel immersion Gold finish. Photos of an assembled test board and an underfilled FC200 stress die are shown in Figure 7.2. The soldermask opening under the chip on the test board was designed with the so-called “finger” approach as shown in

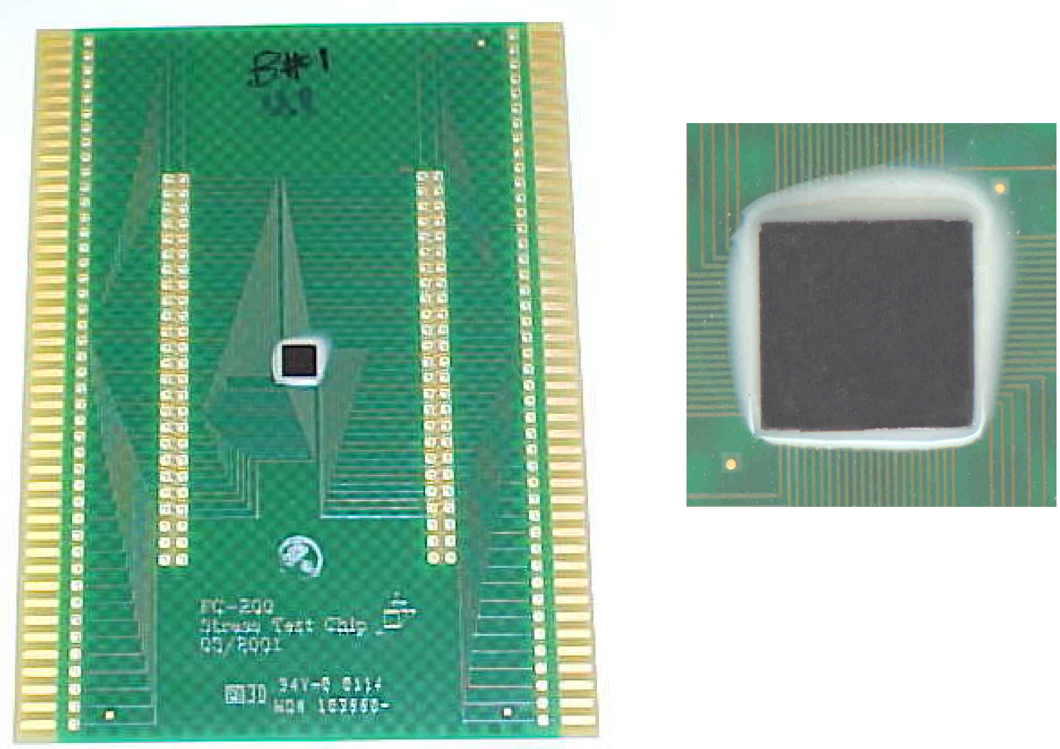

B#1
FC-200
Stress Test Chip
03/2001

Figure 7.2 - Photos of an Assembled Test Board and Test Chip

Figure 5.11, so that the ends of the PCB traces were used as bonding points for the flip chip solder balls.

The test boards were assembled at the SMT Line at Auburn University (see in Figure 5.12). Prior to placement, the test chip solder balls were dipped into a tacky, no-clean solder flux. The die were then aligned and placed on the test substrates using a Siemens SIPLACE $F^5$ high speed pick and place machine. Reflow was performed under a Nitrogen atmosphere in a Heller 1700 reflow oven.

Three different capillary flow underfill encapsulant materials from different vendors were used in the FC200 stress chip experiments (see in Figure 5.13). Each material was a snap/quick cure underfill requiring 5-30 minutes of high temperature curing. The glass transition temperatures, coefficients of thermal expansion, and recommended cure conditions for the three underfills are given in Table 5.2. The underfills were dispensed at near one corner of the die using a CAM/ALOT 3700 dispensing system. The work holder supporting the assemblies was heated to 95 $^{o}$C prior to underfill dispense, and the fast flow materials completely underfilled the die with one dot dispensed at the one corner. After dispense, the underfills were cured under the specified conditions in a box oven. Thermocouples were used to verify that proper durations of oven exposure were utilized and that the recommended cure temperature conditions were actually achieved within the underfill material.

A total of 25 specimens were prepared for each underfill encapsulant. For each specimen and FC200 chip, the 11 rosette sites (88 resistors) were monitored at each stress evaluation point. Figure 7.3 shows the rosette site designations for the resistance/stress measurements.

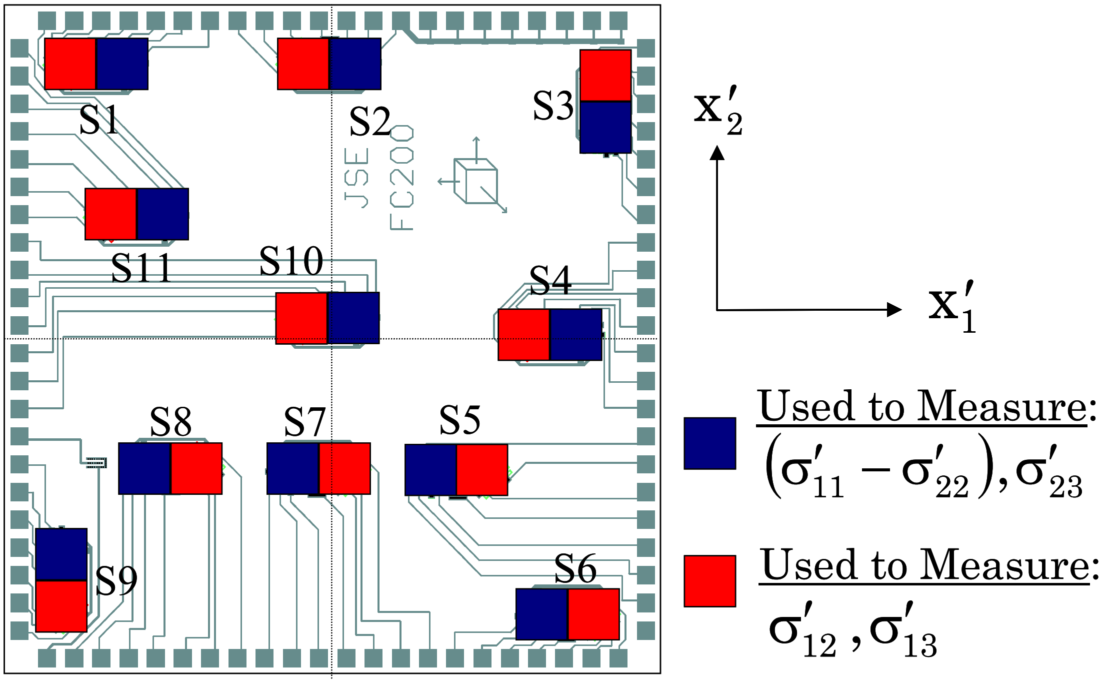

S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
JSE
FC200
$x'_2$
$x'_1$
Used to Measure:
$(\sigma'_{11} - \sigma'_{22}), \sigma'_{23}$
Used to Measure:
$\sigma'_{12}, \sigma'_{13}$

Figure 7.3 - Rosette Sites for Stress Measurement

## 7.4 Flip Chip Stress Measurements

The FC200 test chip assemblies have been utilized to measure the die stresses in flip chip on laminate assemblies throughout the assembly process and during post assembly thermal cycling environmental testing. The transient sensor resistances were first monitored during the cure cycle (see results in Chapter 5). After final assembly was completed, the sensor resistances were also measured at room temperature, as a function of temperature during a slow change from -40 to +150 $^{o}$C (see results in Chapter 5), and during repeated thermal cycling between -40 to +125 $^{o}$C. Using the measured resistance change data from each step of the assembly procedure and thermal cycling testing, the die stress variations were easily calculated using eqs. (5.1, 5.2). In previous chapters, the die stresses during underfill cure and at room temperature and as a function of temperature after cure have thoroughly discussed [142-144]. In this investigation, the observation on the changes that occur in the die stresses during post assembly thermal cycling have concentrated, and have correlated these results to underfill/die interface delamination observations made using CSAM.

## 7.5 Thermal Cycling Experiments

After the initial measurements described in Chapter 5, the variation of the flip chip die surface stresses during thermal cycling reliability testing has been explored. Such reliability qualification testing is often carried out to evaluate the capability of the flip chip on laminate assemblies and underfill encapsulants to survive harsh environments. In this work, the thermal cycling tests were performed with a temperature variation from -40 to 125 $^{o}$C. Thirty-minute dwells were utilized at the high and low temperature extremes, with a ramp rate of 5.5 °C/minute in the transition periods. Figure 7.4 illustrates the temperature profile used in the thermal cycling tests.

The assemblies were subjected to a total of 3000 thermal cycles. The thermal cycling tests were performed in a staged fashion with several different rounds of testing. Each stage consisted of either 125 or 250 cycles. After each increment of cycling was completed, room temperature stress measurements were made on all of the test boards. In addition, CSAM images of the die-to-underfill interface were also recorded for each flip chip sample. In this way, both the die stress and delamination histories of the samples were recorded as a function of the number of thermal cycles, and the variation of die stresses have been observed as delaminations have initiated and grown across the die surface. Initially, measurements were made every 250 thermal cycles. As delaminations started to initiate and grow (typically between 1000-2000 cycles for underfill UF1), the duration of cycles between sensor and CSAM measurements was reduced to 125 cycles.

### 7.5.1 Interface Delamination Initiation and Growth

A typical CSAM image of the die to underfill interface in one of the flip chip assemblies is shown in Figure 7.5. In this work, a Sonix acoustic microscopy system with 110 MHz transducer was utilized. The square image covers the die area, and small dark circles at the solder ball locations can be seen along the perimeter. In the interior of the image, dark gray areas represent the non-delaminated regions, while white areas represent regions of delamination.

As mentioned previously, CSAM images such as shown in Figure 7.5 have been recorded for each of the flip chip assemblies after set increments of thermal cycling (125 or 250 cycles). With such an approach, the initiation and progression of delamination

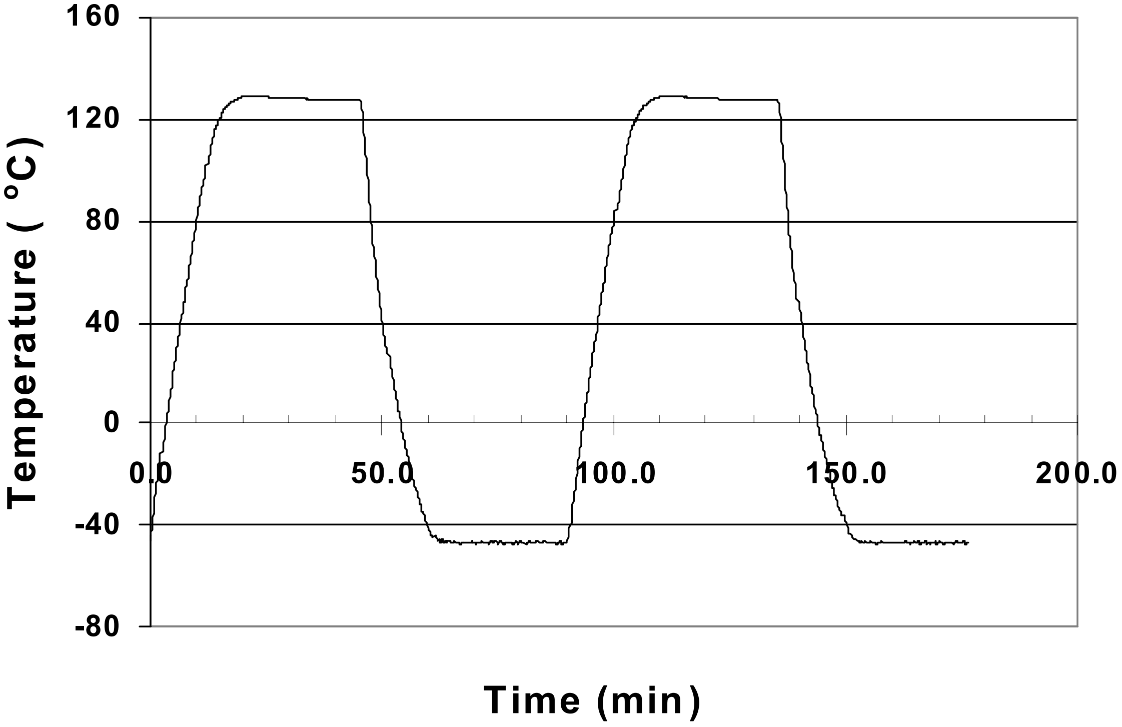


Figure 7.4 - Temperature Profile for Thermal Cycling

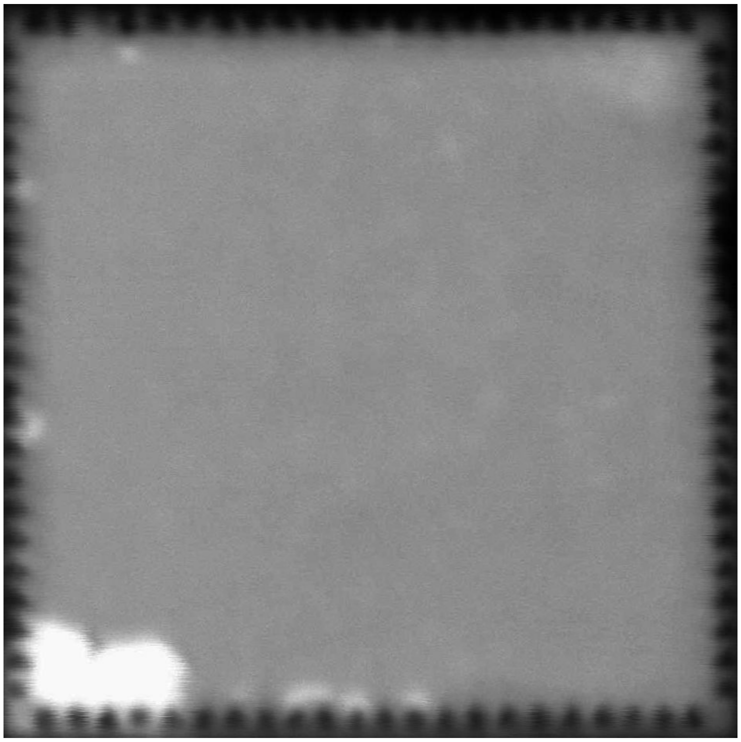


Figure 7.5 - Typical CSAM Image of the Underfill to Die Interface in a Flip Chip Assembly

have been recorded for each flip chip test assembly. Typical CSAM image histories during thermal cycling are shown in Figures 7.6, 7.7, and 7.8, for example flip chip assemblies made with underfills UF1, UF2, and UF3, respectively. From these selected specimens, it can be seen that the delamination histories where highly dependent on the underfill material. For underfill UF1, delaminations normally initiated in the lower left corner where the underfill was dispensed and there was a slight buildup in the underfill fillet. As the delaminations propagated, the delamination area remained weighted towards this corner and the two edges adjacent to it. In the case of underfill UF2, the delamination initiation sites were more random, typically near one of the four corners. As cycling continued, delaminations gradually would initiate along the entire die perimeter, eventually leading to complete delamination at the die edge. For underfill UF3, delaminations typically initiated along one of the two edges that did not intersect the dispense corner. Delamination growth was concentrated along these two edges, and even after 3000 thermal cycles were completed, delamination rarely occurred at the dispense corner itself. The observations made above are further supported by the initial and final images shown in Figures 7.9, 7.10, and 7.11 for multiple samples assembled with underfills UF1, UF2, and UF3, respectively. In this context, “initial” refers to the CSAM image recorded immediately after assembly (i.e. when no delaminations were present), and “final” refers to the CSAM image made after the same assembly had been subjected to 3000 thermal cycles from -40 to 125 $^{o}$C.

The number of thermal cycles to delamination initiation and the delamination growth rate are crucial elements to the reliability of flip chip packages. Faster initiation and growth of delamination will reduce the solder joint reliability as well as service life

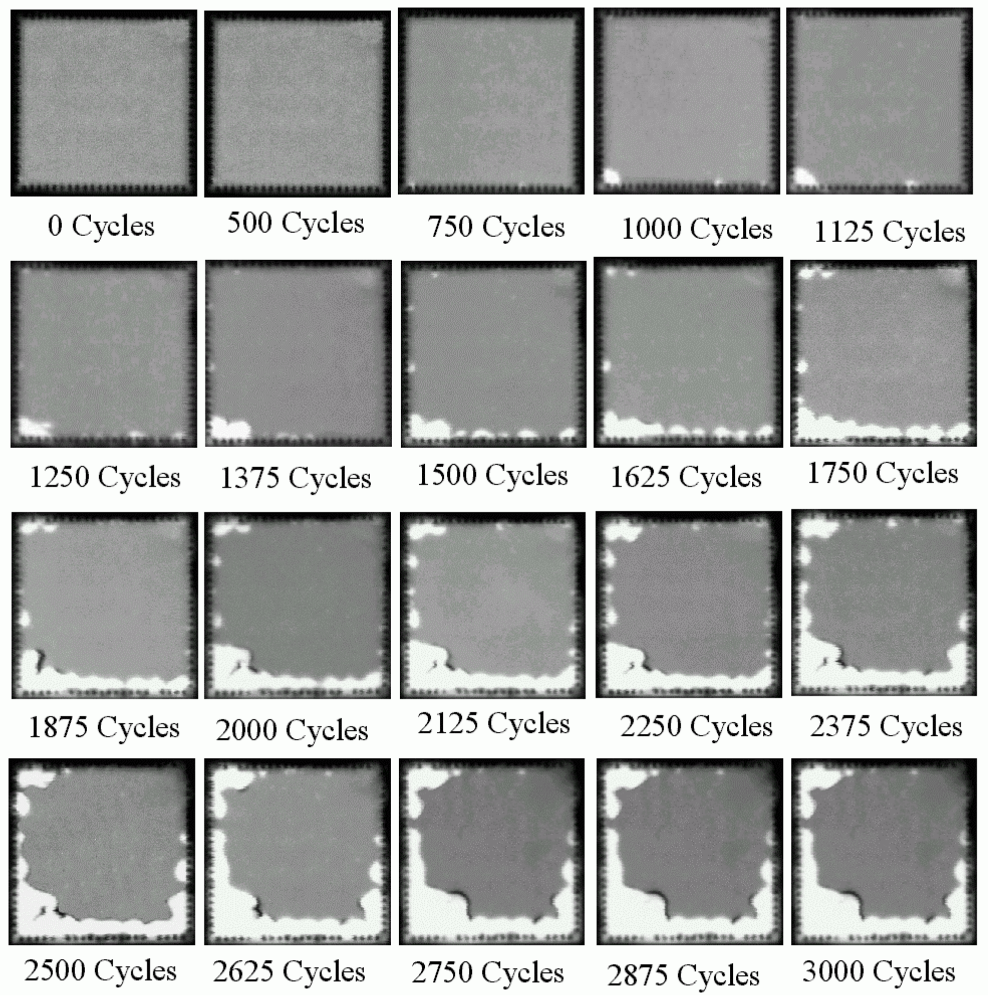
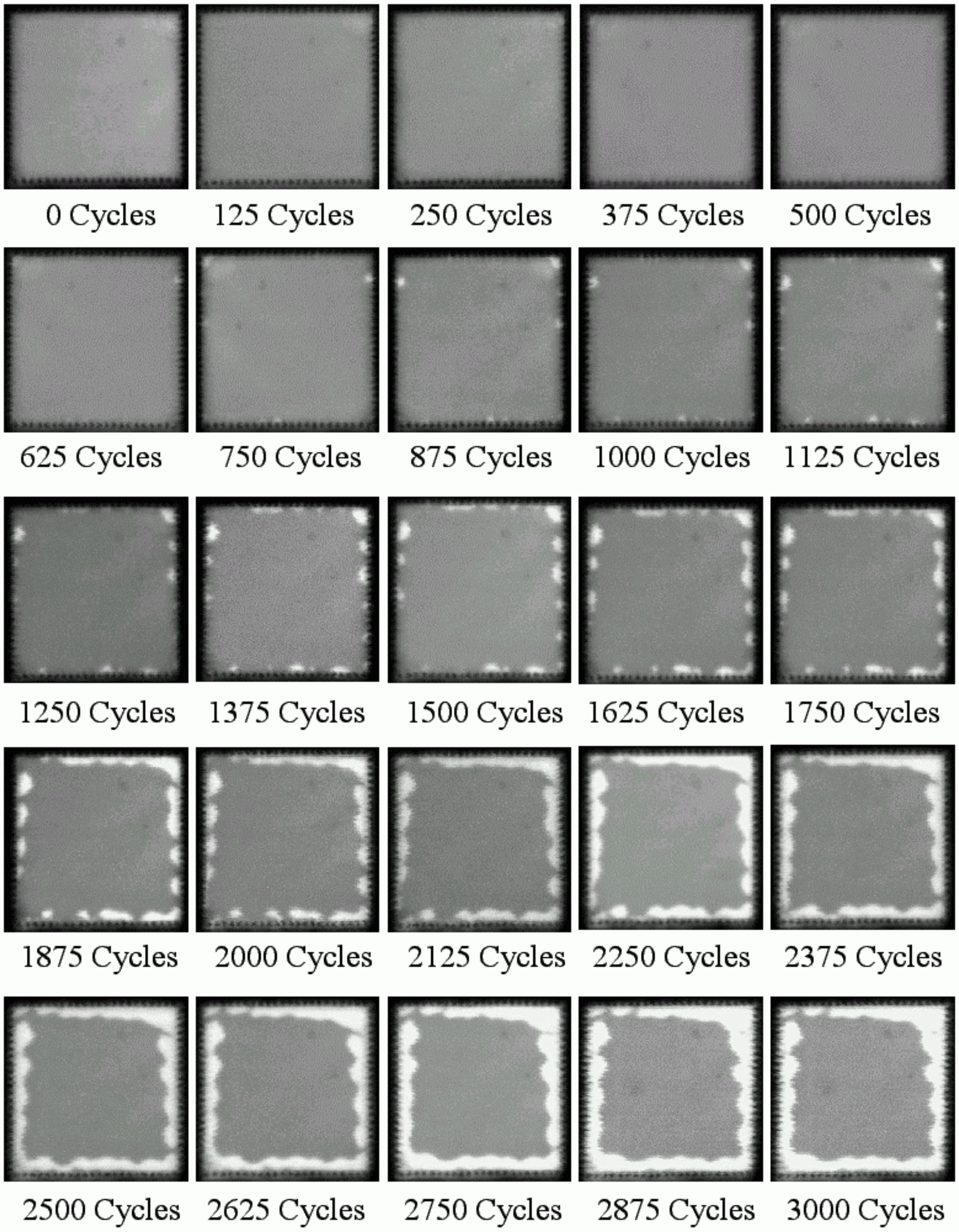

0 Cycles
500 Cycles
750 Cycles
1000 Cycles
1125 Cycles
1250 Cycles
1375 Cycles
1500 Cycles
1625 Cycles
1750 Cycles
1875 Cycles
2000 Cycles
2125 Cycles
2250 Cycles
2375 Cycles
2500 Cycles
2625 Cycles
2750 Cycles
2875 Cycles
3000 Cycles

Figure 7.6 - Typical Delamination History for a Single Flip Chip Assembly (Underfill UF1, Board 22)



0 Cycles, 125 Cycles, 250 Cycles, 375 Cycles, 500 Cycles

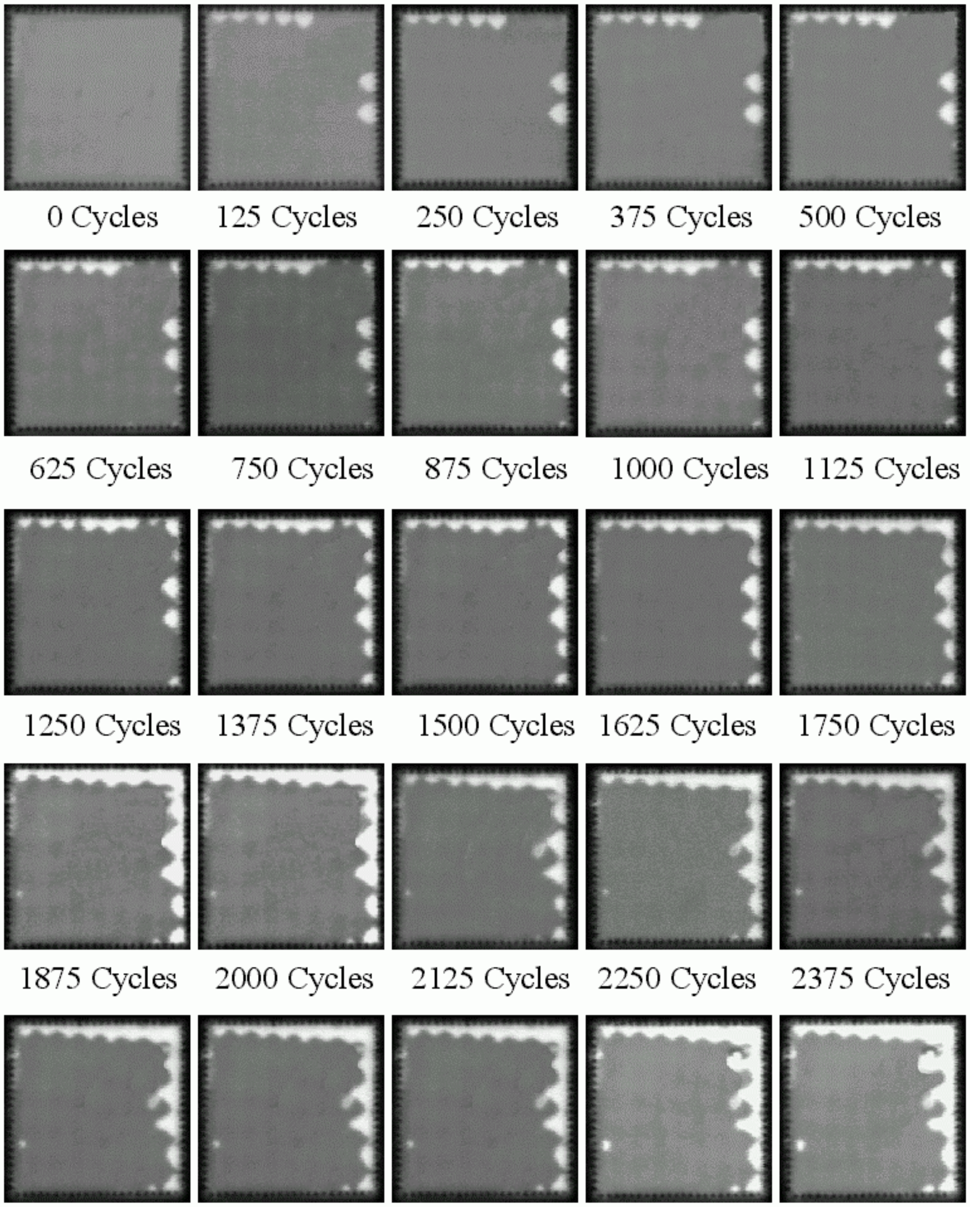
625 Cycles, 750 Cycles, 875 Cycles, 1000 Cycles, 1125 Cycles

1250 Cycles, 1375 Cycles, 1500 Cycles, 1625 Cycles, 1750 Cycles

1875 Cycles, 2000 Cycles, 2125 Cycles, 2250 Cycles, 2375 Cycles

2500 Cycles, 2625 Cycles, 2750 Cycles, 2875 Cycles, 3000 Cycles

Figure 7.7 - Typical Delamination History for a Single Flip Chip Assembly (Underfill UF2, Board 10)



0 Cycles 125 Cycles 250 Cycles 375 Cycles 500 Cycles

625 Cycles 750 Cycles 875 Cycles 1000 Cycles 1125 Cycles

1250 Cycles 1375 Cycles 1500 Cycles 1625 Cycles 1750 Cycles

1875 Cycles 2000 Cycles 2125 Cycles 2250 Cycles 2375 Cycles

2500 Cycles 2625 Cycles 2750 Cycles 2875 Cycles 3000 Cycles

Figure 7.8 - Typical Delamination History for a Single Flip Chip Assembly (Underfill UF3, Board 16)

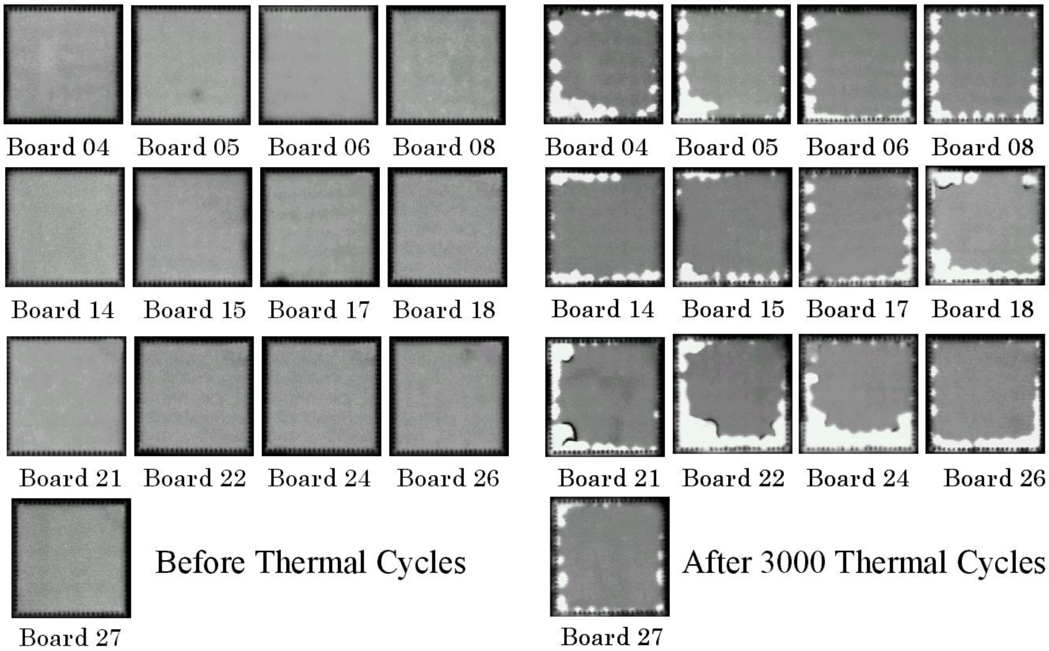

Board 04
Board 05
Board 06
Board 08
Board 14
Board 15
Board 17
Board 18
Board 21
Board 22
Board 24
Board 26
Board 27
Before Thermal Cycles
Board 04
Board 05
Board 06
Board 08
Board 14
Board 15
Board 17
Board 18
Board 21
Board 22
Board 24
Board 26
Board 27
After 3000 Thermal Cycles

Figure 7.9 - Initial and Final CSAM Images for the Flip Chip Assemblies with Underfill UF1

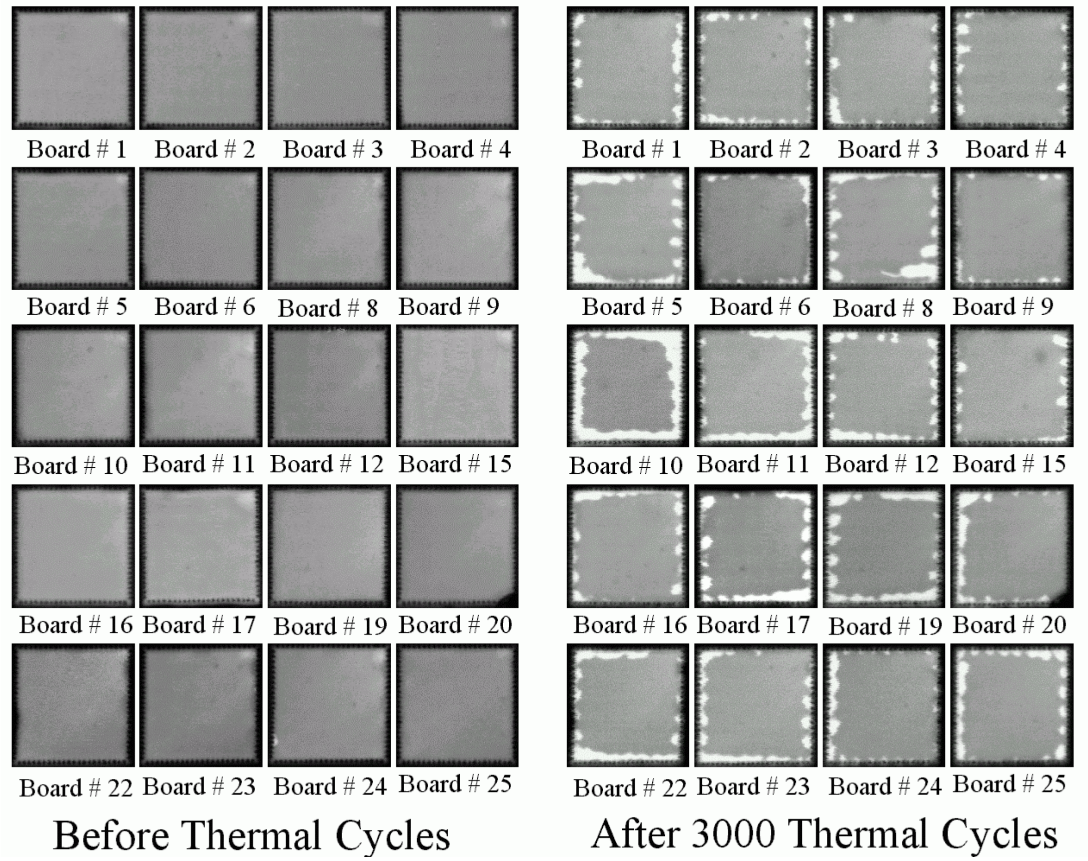
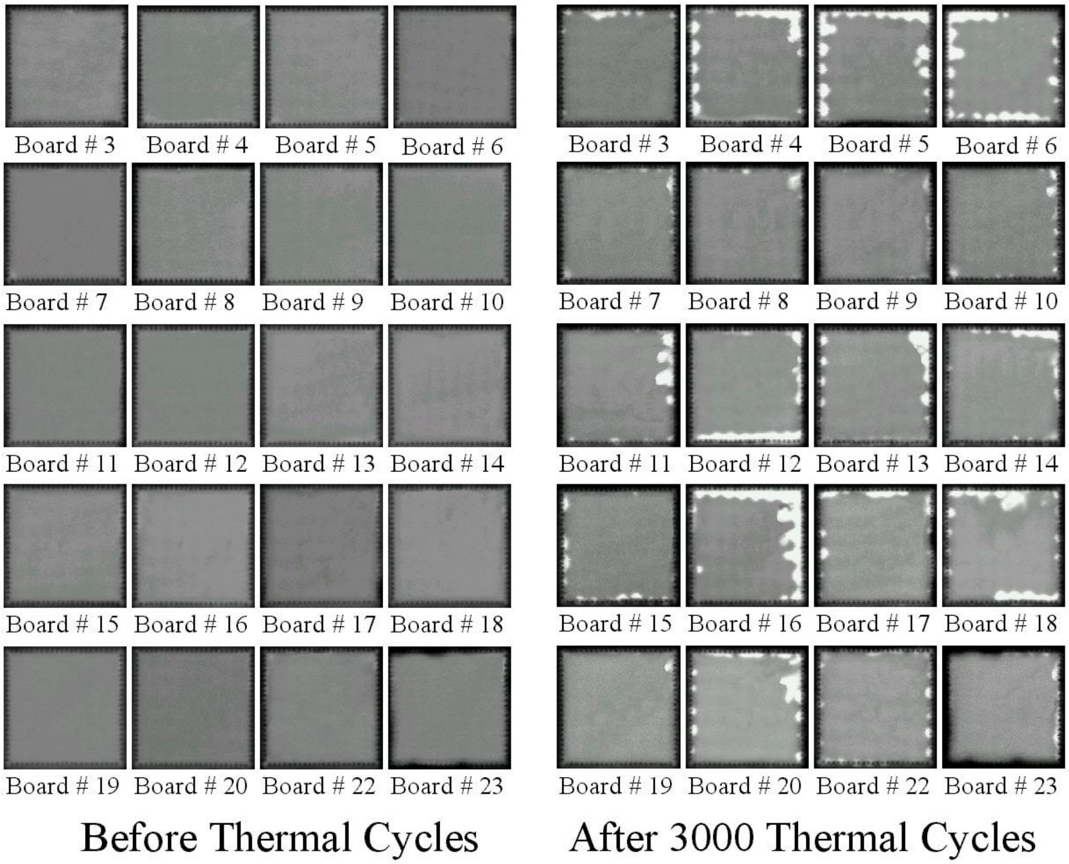

Board # 1
Board # 2
Board # 3
Board # 4
Board # 5
Board # 6
Board # 8
Board # 9
Board # 10
Board # 11
Board # 12
Board # 15
Board # 16
Board # 17
Board # 19
Board # 20
Board # 22
Board # 23
Board # 24
Board # 25
Before Thermal Cycles
Board # 1
Board # 2
Board # 3
Board # 4
Board # 5
Board # 6
Board # 8
Board # 9
Board # 10
Board # 11
Board # 12
Board # 15
Board # 16
Board # 17
Board # 19
Board # 20
Board # 22
Board # 23
Board # 24
Board # 25
After 3000 Thermal Cycles

Figure 7.10 - Initial and Final CSAM Images for the Flip Chip Assemblies with Underfill UF2


Board # 3
Board # 4
Board # 5
Board # 6
Board # 7
Board # 8
Board # 9
Board # 10
Board # 11
Board # 12
Board # 13
Board # 14
Board # 15
Board # 16
Board # 17
Board # 18
Board # 19
Board # 20
Board # 22
Board # 23
Board # 3
Board # 4
Board # 5
Board # 6
Board # 7
Board # 8
Board # 9
Board # 10
Board # 11
Board # 12
Board # 13
Board # 14
Board # 15
Board # 16
Board # 17
Board # 18
Board # 19
Board # 20
Board # 22
Board # 23

Before Thermal Cycles

After 3000 Thermal Cycles

Figure 7.11 - Initial and Final CSAM Images for the Flip Chip Assemblies with Underfill UF3

of flip chip assemblies. It should be noted that the delaminations seen in Figure 7.8 occurred at an unusually low level of thermal cycling. For the majority of the other underfill UF3 samples, the delamination initiations occurred after (at higher cycle count) than those for the samples manufactured with underfills UF1 and UF2. In addition, delaminations generally occurred earliest (lowest cycle count) for the samples manufactured with underfill UF1. Thus, the generally observed ranking of the number of cycles to delamination initiation was $N_{\text{Initiation-UF1}} < N_{\text{Initiation-UF2}} < N_{\text{Initiation-UF3}}$. The precise number of cycles to initiation of in any given sample could not be determined because CSAM images were only recorded at set increments of thermal cycling (e.g. every 125 cycles). In addition, the number of cycles required for delamination initiation typically had a fairly large spread (over 1000 cycles) when considering all of the samples for each material. Nearly all of the assemblies showed some delamination by the end of thermal cycling (3000 cycles), with underfill UF3 typically showing the slowest delamination growth rates and smallest final delamination areas.

### 7.5.2 Stress Variation During Thermal Cycling

Presentation of the “average” stress measurement results from the thermal cycling testing becomes more problematic relative to the final assembly stress data shown in the previous section. As delaminations form in the samples, the stress distributions were observed to vary drastically as interfacial cracks initiate and propagate at the underfill to die passivation interface. Also, as mentioned previously, the number of thermal cycles to delamination initiation and the subsequent spreading of the delamination crack patterns have been found to show significant variance across the specimen sets. For example, delamination initiations were observed in some assemblies at around 1000 cycles, while others survived in excess of 2000 cycles with no delaminations. In addition, any solder joint failures in the delaminated regions make resistance measurements impossible due to loss of electrical access to the sensors. Finally, the piezoresistive surface sensors are often physically destroyed as the delamination front propagates across the rosette location. For all of the above reasons, we have chosen to present the “average” sensor data during thermal cycling for only the specimens that have not delaminated at the sensor site being discussed. With such an approach, the number of samples with stresses being averaged will drop as the thermal cycling proceeds.

The variations in the average values of stresses $\sigma'_{11}$, $\sigma'_{11} - \sigma'_{22}$, $\sigma'_{12}$, and $\tau_{\text{Interfacial}}$ with thermal cycling duration for non-delaminated samples with underfills UF1, UF2 and UF3 are tabulated in Figures 7.12-7.15, respectively. In these figures, we have chosen to simplify the presentation by only listing the data for the sensor rosette sites with the highest/maximum values for the given stress components. Also, only the magnitudes (absolute values) of the stresses are given. It is clear from these illustrations that significant variations occur in the stress magnitudes as thermal cycling proceeds, even if there is no delamination at the sensor site. In particular, the individual die normal stresses and their difference (temperature compensated) in Figure 7.12 and 7.13 are seen to decrease by at least 78% and 25% for underfill UF1, while the die shear stresses in Figures 7.14 and 7.15 are seen to decrease by up to 90% and 60%, respectively. The large 90% drop in the in-plane shear stress occurred at site S9 in the lower left corner of the die (underfill dispense corner) after 2750 thermal cycles. After 2750 cycles, the sensor (S9) at the dispense corner of flip chip assemblies with underfill UF1 were all electrically failed (most likely due to solder joint failure). At the same time the corner

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 102.0 | 119.0 | 191.8 |
| 250 | 92.6 | 98.1 | 111.2 |
| 500 | 87.4 | 93.6 | 105.6 |
| 750 | 75.2 | 85.2 | 100.9 |
| 1000 | 73.0 | 83.3 | 99.8 |
| 1250 | 69.5 | 75.8 | 95.2 |
| 1375 | 67.4 | 75.0 | 92.5 |
| 1500 | 58.1 | 73.6 | 90.4 |
| 1625 | 56.5 | 72.5 | 86.7 |
| 1750 | 50.1 | 68.1 | 85.9 |
| 1875 | 47.4 | 64.3 | 77.9 |
| 2000 | 44.8 | 58.0 | 69.1 |
| 2125 | 41.9 | 48.3 | 69.7 |
| 2250 | 40.7 | 46.2 | 66.4 |
| 2375 | 31.3 | 45.0 | 55.8 |
| 2500 | 28.2 | 32.2 | 54.5 |
| 2625 | 28.8 | 32.4 | 55.0 |
| 2750 | 25.1 | 31.4 | 43.2 |
| 2875 | 25.3 | 30.4 | 27.3 |
| 3000 | 22.3 | 19.4 | 25.9 |

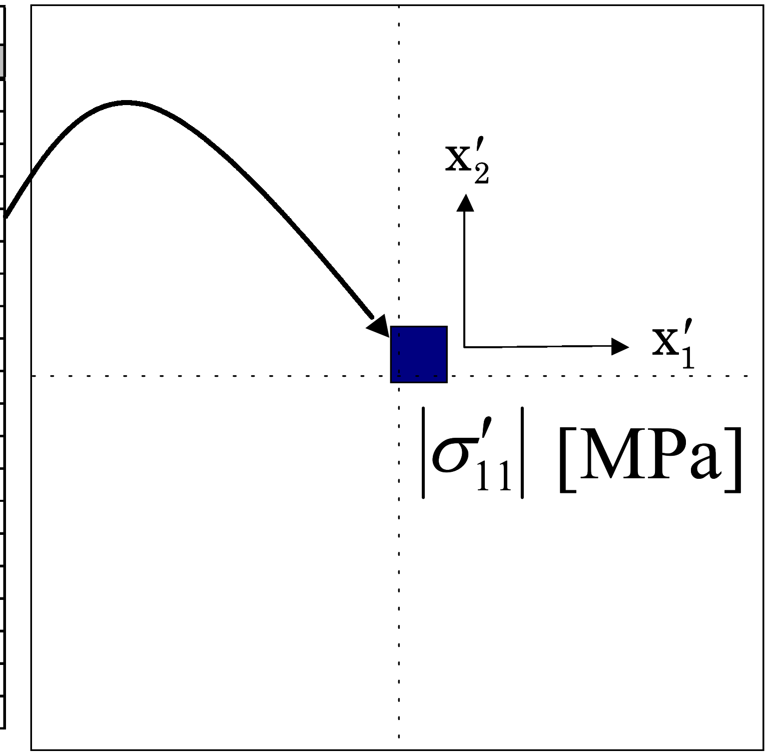


Figure 7.12 - Average Stress Variation with Thermal Cycling

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 40.5 | 39.5 | 44.3 |
| 250 | 40.5 | 29.0 | 37.8 |
| 500 | 40.4 | 28.8 | 36.7 |
| 750 | 39.3 | 30.3 | 36.5 |
| 1000 | 38.3 | 30.4 | 35.7 |
| 1250 | 38.0 | 30.1 | 35.0 |
| 1375 | 38.3 | 30.2 | 34.9 |
| 1500 | 37.6 | 29.7 | 34.7 |
| 1625 | 37.9 | 29.4 | 34.2 |
| 1750 | 34.8 | 28.8 | 33.5 |
| 1875 | 35.0 | 27.2 | 32.2 |
| 2000 | 29.8 | 27.0 | 31.5 |
| 2125 | 30.7 | 26.6 | 30.3 |
| 2250 | 32.5 | 26.1 | 30.6 |
| 2375 | 30.4 | 25.8 | 33.6 |
| 2500 | 30.0 | 25.2 | 32.1 |
| 2625 | 27.6 | 21.6 | 31.2 |
| 2750 | 25.7 | 22.1 | 31.0 |
| 2875 | 25.5 | 21.2 | 33.3 |
| 3000 | 22.5 | 21.7 | 33.7 |

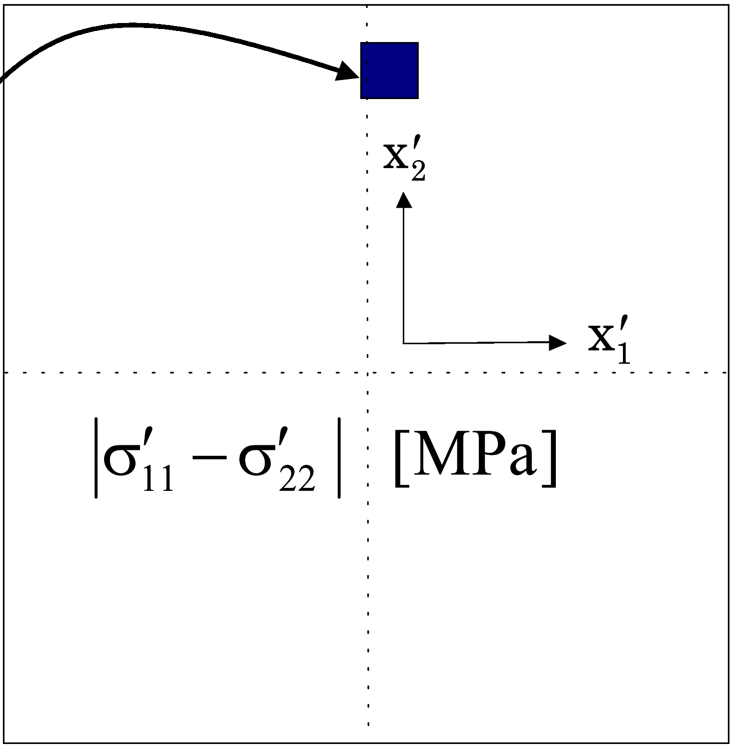
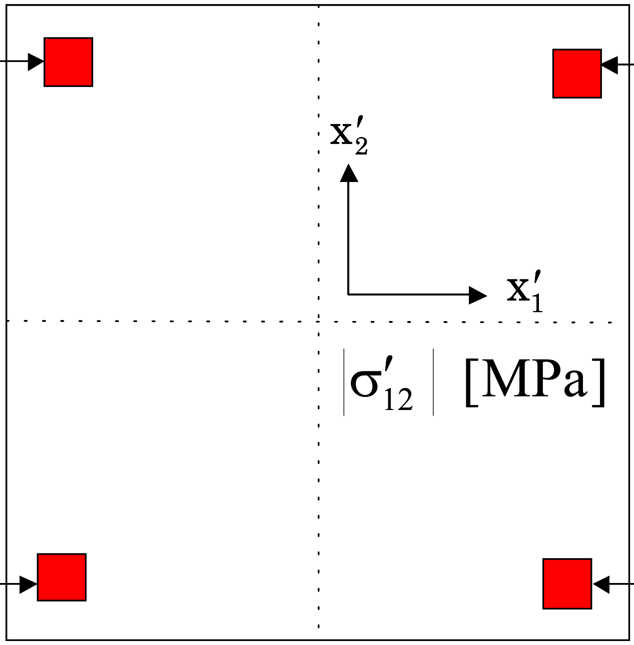


Figure 7.13 - Average Stress Variation with Thermal Cycling

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
|  | Stress | Stress | Stress |
| 0 | 7.3 | 4.2 | 4.2 |
| 250 | 9.8 | 1.4 | 3.2 |
| 500 | 9.3 | 2.9 | 2.5 |
| 750 | 9.1 | 3.4 | 2.0 |
| 1000 | 6.8 | 3.5 | 1.8 |
| 1250 | 5.8 | 3.2 | 2.1 |
| 1375 | 6.8 | 2.8 | 2.0 |
| 1500 | 6.1 | 2.8 | 2.1 |
| 1625 | 4.8 | 2.5 | 2.0 |
| 1750 | 4.2 | 2.0 | 1.9 |
| 1875 | 3.4 | 2.6 | 2.0 |
| 2000 | 2.7 | 2.8 | 2.0 |
| 2125 | 2.9 | 3.8 | 2.4 |
| 2250 | 2.6 | 5.2 | 3.6 |
| 2375 | 1.4 | 5.8 | 4.0 |
| 2500 | 1.0 | 5.3 | 4.2 |
| 2625 | 1.9 | 5.1 | 4.7 |
| 2750 | 3.8 | 4.7 | 4.5 |
| 2875 | 2.6 | 4.0 | 4.5 |
| 3000 | 2.8 | 3.9 | 4.9 |

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 7.9 | 4.1 | 6.2 |
| 250 | 6.8 | 2.9 | 3.7 |
| 500 | 6.5 | 2.6 | 3.4 |
| 750 | 6.6 | 2.8 | 3.1 |
| 1000 | 6.6 | 2.8 | 2.8 |
| 1250 | 5.6 | 2.7 | 2.8 |
| 1375 | 7.4 | 2.8 | 2.7 |
| 1500 | 7.5 | 2.9 | 2.5 |
| 1625 | 7.1 | 3.0 | 2.6 |
| 1750 | 6.0 | 3.1 | 2.7 |
| 1875 | 5.6 | 3.2 | 2.7 |
| 2000 | 4.3 | 3.3 | 2.6 |
| 2125 | 6.5 | 3.3 | 2.3 |
| 2250 | 6.7 | 4.1 | 2.4 |
| 2375 | 4.5 | 5.2 | 3.6 |
| 2500 | 4.2 | 4.7 | 4.1 |
| 2625 | 3.6 | 4.9 | 4.3 |
| 2750 | 3.1 | 5.2 | 4.4 |
| 2875 | 2.7 | 5.7 | 4.7 |
| 3000 | 2.2 | 6.4 | 4.8 |

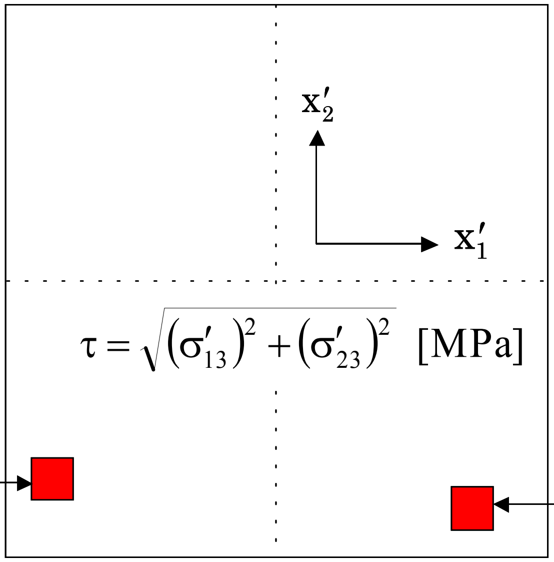


|  | UF1 | UF2 | UF3 |
|---|---|---|---|
|  | Stress | Stress | Stress |
| 0 | 15.1 | 7.4 | 12.3 |
| 250 | 14.2 | 4.8 | 8.1 |
| 500 | 13.8 | 4.3 | 7.3 |
| 750 | 13.2 | 5.3 | 7.0 |
| 1000 | 12.0 | 4.7 | 6.1 |
| 1250 | 8.7 | 4.2 | 5.6 |
| 1375 | 7.9 | 4.4 | 5.4 |
| 1500 | 7.7 | 4.4 | 5.6 |
| 1625 | 7.1 | 4.6 | 5.7 |
| 1750 | 5.0 | 4.1 | 5.8 |
| 1875 | 4.6 | 3.6 | 5.7 |
| 2000 | 4.6 | 3.3 | 5.7 |
| 2125 | 4.2 | 4.0 | 5.8 |
| 2250 | 3.3 | 5.2 | 9.6 |
| 2375 | 2.0 | 4.2 | 11.5 |
| 2500 | 1.7 | 5.0 | 12.3 |
| 2625 | 1.3 | 5.6 | 13.2 |
| 2750 | 1.2 | 5.2 | 12.5 |
| 2875 | ## | 5.3 | 10.9 |
| 3000 | ## | 4.4 | 9.8 |

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 9.6 | 5.4 | 5.2 |
| 250 | 10 | 1.8 | 4.7 |
| 500 | 10.1 | 4.0 | 4.3 |
| 750 | 10.1 | 4.8 | 4.4 |
| 1000 | 8.5 | 4.4 | 4.0 |
| 1250 | 7.6 | 3.4 | 3.7 |
| 1375 | 8.1 | 3.2 | 3.3 |
| 1500 | 7.5 | 3.6 | 3.3 |
| 1625 | 6.1 | 3.9 | 3.4 |
| 1750 | 5.3 | 4.2 | 3.0 |
| 1875 | 5.5 | 3.9 | 2.7 |
| 2000 | 3.4 | 3.7 | 2.5 |
| 2125 | 6.5 | 4.0 | 2.7 |
| 2250 | 5.8 | 5.3 | 2.9 |
| 2375 | 3.8 | 5.7 | 3.6 |
| 2500 | 2.3 | 5.1 | 4.1 |
| 2625 | 3.6 | 4.6 | 5.7 |
| 2750 | 4.9 | 4.4 | 6.2 |
| 2875 | 5.6 | 4.1 | 6.8 |
| 3000 | 3.7 | 3.8 | 6.0 |

Figure 7.14 - Average Stress Variation with Thermal Cycling

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 3.9 | 3.4 | 3.9 |
| 250 | 3.7 | 2.2 | 3.3 |
| 500 | 4.1 | 2.9 | 3.3 |
| 750 | 3.7 | 3.2 | 3.2 |
| 1000 | 3.2 | 3.0 | 3.1 |
| 1250 | 3.2 | 2.9 | 3.1 |
| 1375 | 3.0 | 2.8 | 2.8 |
| 1500 | 3.1 | 2.5 | 2.9 |
| 1625 | 2.8 | 2.7 | 2.7 |
| 1750 | 2.2 | 2.3 | 2.9 |
| 1875 | 2.5 | 2.0 | 3.0 |
| 2000 | 2.4 | 1.9 | 3.0 |
| 2125 | 3.0 | 1.8 | 2.4 |
| 2250 | 2.7 | 3.1 | 3.1 |
| 2375 | 2.7 | 2.7 | 3.4 |
| 2500 | 2.5 | 1.9 | 3.5 |
| 2625 | 2.6 | 2.1 | 3.6 |
| 2750 | 1.6 | 2.3 | 3.6 |
| 2875 | ## | 2.6 | 3.6 |
| 3000 | ## | 2.8 | 3.3 |



$$\tau = \sqrt{\left(\sigma'_{13}\right)^2 + \left(\sigma'_{23}\right)^2} \quad [\mathrm{MPa}]$$

|  | UF1 | UF2 | UF3 |
|---|---|---|---|
| N | Stress | Stress | Stress |
| 0 | 4.7 | 4.5 | 4.8 |
| 250 | 4.8 | 3.3 | 4.5 |
| 500 | 4.2 | 3.4 | 4.4 |
| 750 | 4.4 | 3.9 | 4.7 |
| 1000 | 4.3 | 3.6 | 4.7 |
| 1250 | 4.3 | 3.4 | 4.3 |
| 1375 | 4.3 | 3.7 | 4.2 |
| 1500 | 4.1 | 3.4 | 4.1 |
| 1625 | 4.2 | 3.3 | 4.1 |
| 1750 | 3.9 | 3.6 | 3.9 |
| 1875 | 4.5 | 3.0 | 3.5 |
| 2000 | 3.6 | 3.4 | 3.4 |
| 2125 | 4.4 | 2.9 | 4.2 |
| 2250 | 4.6 | 4.4 | 4.6 |
| 2375 | 4.6 | 4.2 | 4.7 |
| 2500 | 4.3 | 4.0 | 5.0 |
| 2625 | 4.0 | 3.9 | 5.3 |
| 2750 | 4.0 | 3.1 | 5.2 |
| 2875 | 3.6 | 3.2 | 5.4 |
| 3000 | 3.0 | 2.8 | 5.4 |

Figure 7.15 - Average Stress Variation with Thermal Cycling

sensors of assemblies with underfill UF2 and UF3 typically survived 3000 thermal cycles. As was observed earlier, this corner was the location of the majority of the delamination initiations in the samples with underfill UF1.

Graphical plots of the extreme reductions of the average normal stress magnitudes (listed in Figure 7.12) with thermal cycling are shown in Figure 7.16. Such behavior is most likely due to a combination of several effects including change in the underfill and solder material properties (e.g. elastic modulus E, coefficient of expansion $\alpha$, etc.) with thermal cycling, viscoplastic deformations in the underfill and solder joints during thermal cycling, and damage (without delamination) to the underfill to die passivation interface during thermal cycling. Given that the majority of the initial assembly die stresses were produced during underfill cure cooldown and not solder joint reflow, we feel that changes in the underfill are the most likely reason. Although such effects are almost universally ignored or simplified in finite element simulations for flip chip on laminate reliability, it is clear from these measurements that the effect is dramatic.

### 7.5.3 Leading Indicators-of-Failure

To more fully understand the effects of delamination initiation and delamination growth on the die stress distributions, it is necessary to look at correlation between the stress and CSAM measurements for individual test assemblies. Given that we have 25 assemblies for each of 3 underfills, and that there are 11 sensor rosettes in each assembly measuring up to 6 stress components, the amount of data available for this purpose is staggering. Here, concentration is made on the shear stress data for three underfill materials. The stress variations are examined at site S9, where delaminations initiated in most of the UF1 assemblies.

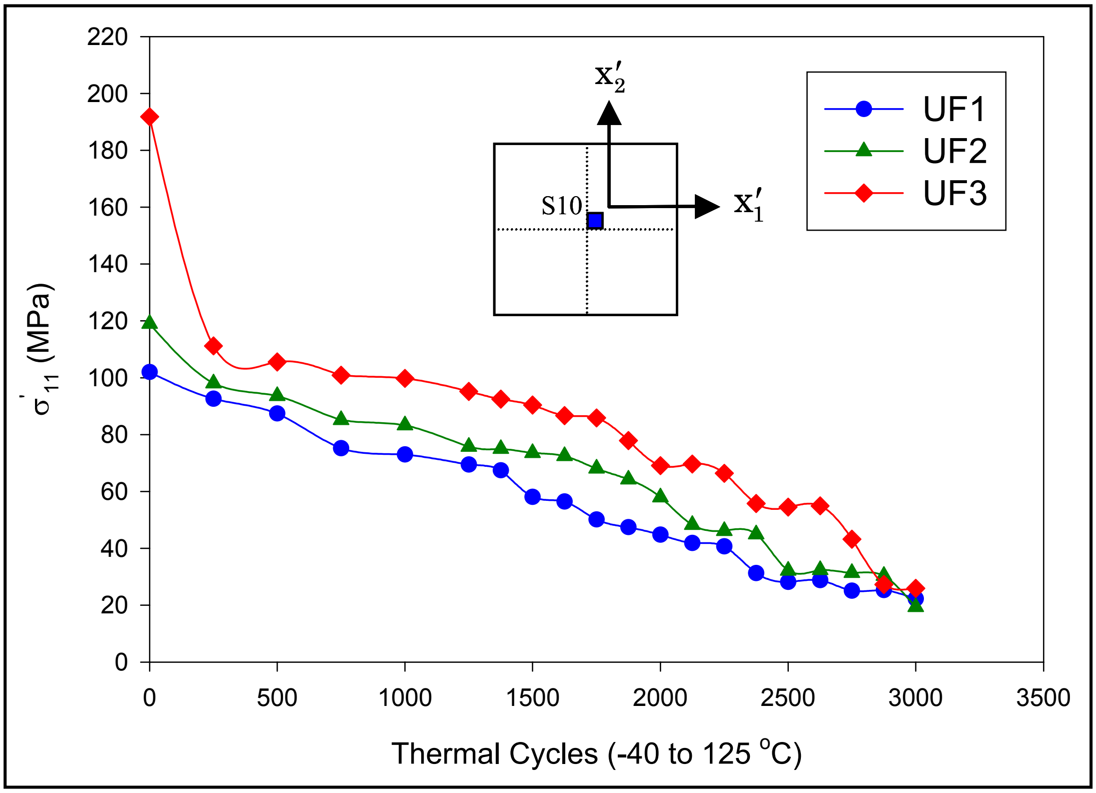


Figure 7.16 - Normal Stress Variation with Thermal Cycling

Figure 7.6 illustrated the delamination growth at the underfill to die passivation interface measured in one of the UF1 flip chip assemblies (board 22) at several levels of thermal cycling. The delaminations at the die device surface are seen to initiate at approximately 750 thermal cycles at the corner where the underfill was dispensed and where the measured high in-plane and interfacial shear stresses were observed (see Figures 7.14 and 7.15). At a little over 1000 thermal cycles, the delamination front had passed through the sensor rosette at site S9, nearest to the lower left hand corner of the chip. The measured shear stress histories at site S9 for this assembly are shown in Figure 7.17. From these data, it can be seen that the interfacial shear stress remains fairly constant until delamination occurs. At the point of delamination at the sensor site, the interfacial shear stress becomes approximately zero since the tractions between the underfill and die are released. On the contrary, the in-plane shear stress is observed to have changed dramatically, even before delaminations were detected using CSAM. The value was found to first suddenly increase, and then decrease gradually until delamination occurred. At the point of delamination, either the sensors themselves or their associated solder joints were damaged, so that the rosette no longer functioned.

From the stress variations observed in Figure 7.17, it appears that the in-plane shear stress magnitude may be a leading "early warning" indicator for impending delaminations. It was expected that the interfacial shear stress would also exhibit this characteristic as in previous work on delaminations in plastic quad flat packs [23]. However, the current data do not support this hypothesis.

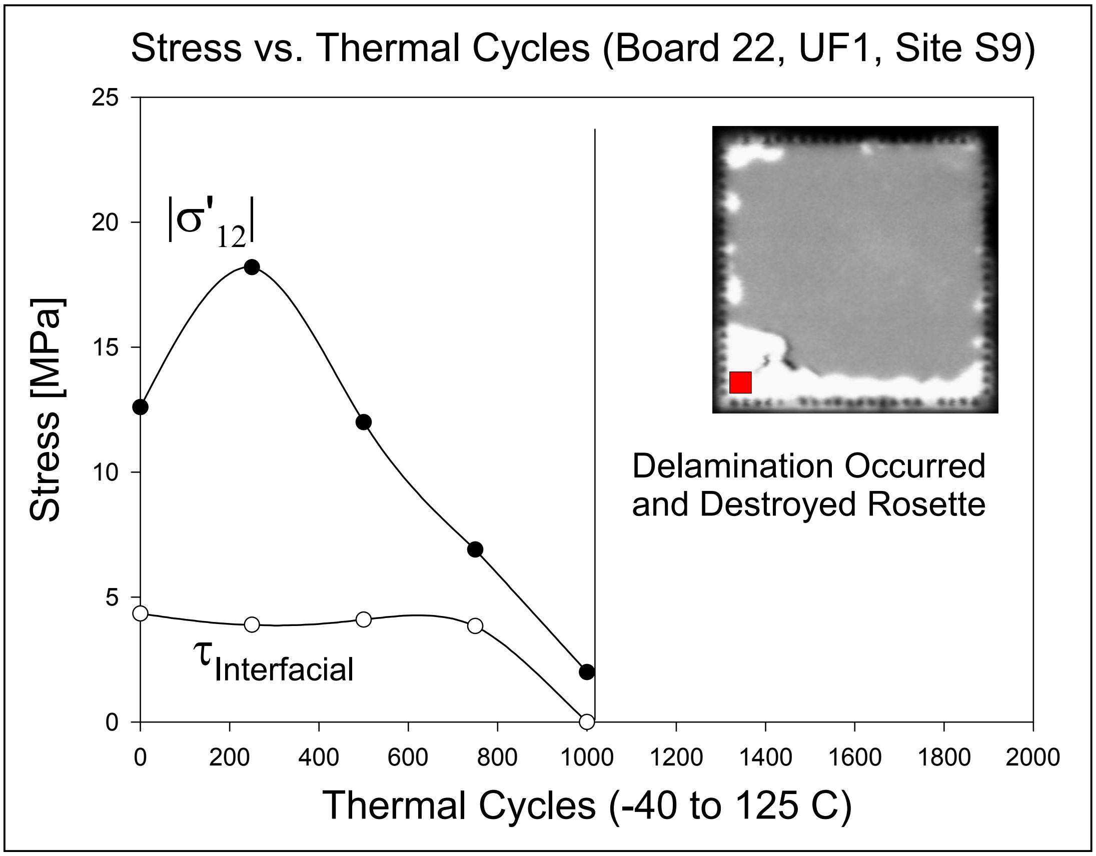


Figure 7.17 - Stress History at Site S9 (Lower Left Corner)

Measurements on other assemblies have shown the same trends as exhibited in Figures 7.6 and 7.17. For example, Figure 7.18 shows the CSAM delamination and shear stress histories for another one of the test boards (board 21). In this case, the delaminations initiated at approximately 1250 thermal cycles at the corner where the underfill was dispensed, and the delamination front passed through the sensor rosette at site S9 at approximately 1500 thermal cycles. Analogous behaviors of the in-plane and interfacial shear stresses were observed.

The die shear stress variations at non-delaminated corner locations in the flip chip assemblies have also been observed. For example, Figures 7.19 and 7.20 show the CSAM image and die in-plane shear stress variations at the delaminated and the non-delaminated corners of the same assembly (UF2). In these Figures, the stress value at the delaminated corner (lower left) was found to first suddenly increase, and then decrease gradually until delamination occurred. However, the corresponding responses at the non-delaminated corners illustrated monotonic gradual declines as cycling progressed. Similar phenomenon was also observed for other two underfills materials. Figures 7.21 and 7.22 show another example (UF1) where the CSAM image and die in-plane shear stress variations are given at the delaminated and the non-delaminated corners of the same assembly. Another example for underfill UF3 is shown in Figures 7.23 and 7.24. Further examples of this phenomenon are shown for multiple assemblies for underfill UF1 in Figures 7.25 and 7.26 for non-delaminated and delaminated corners, respectively. Similar results were also observed for underfill UF2 (shown in Figures 7.27 and 7.28), and underfill UF3 (shown in Figures 7.29 and 7.30).

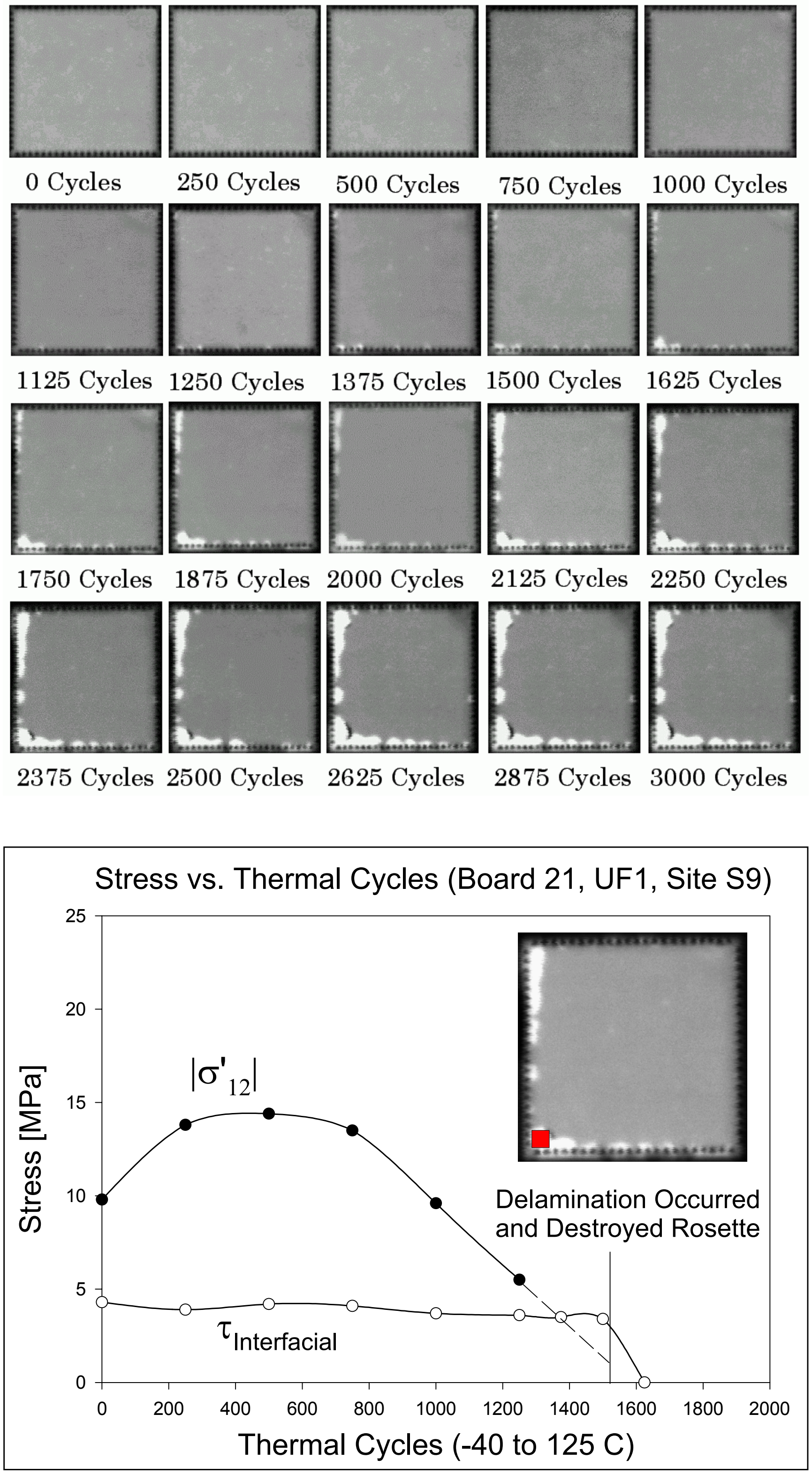


Figure 7.18 - Stress History at Site S9 (Lower Left Corner)

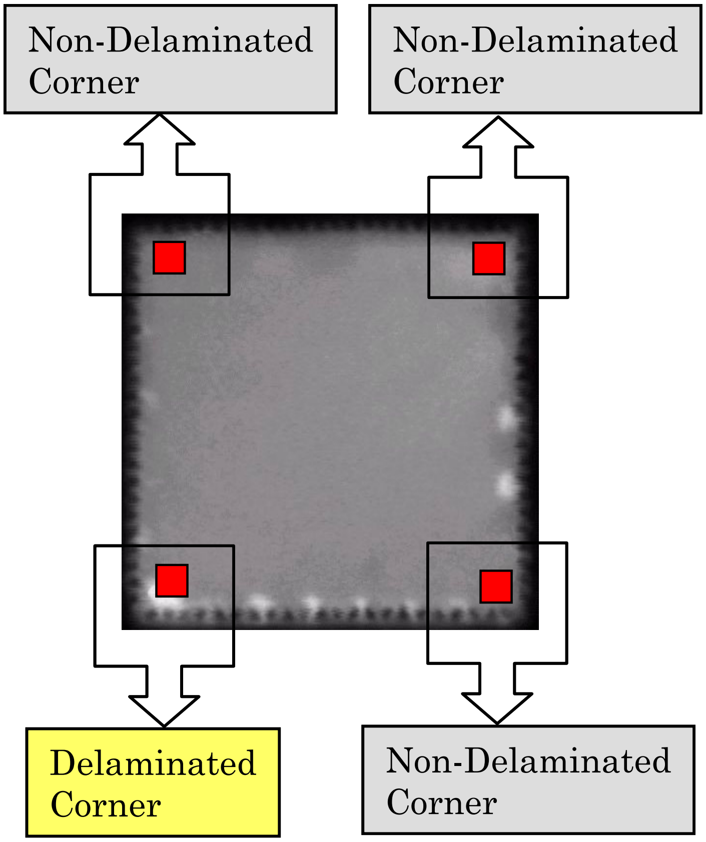

Non-Delaminated Corner
Non-Delaminated Corner
Delaminated Corner
Non-Delaminated Corner

Figure 7.19 - Corner Delamination Status (UF2, Board 3)

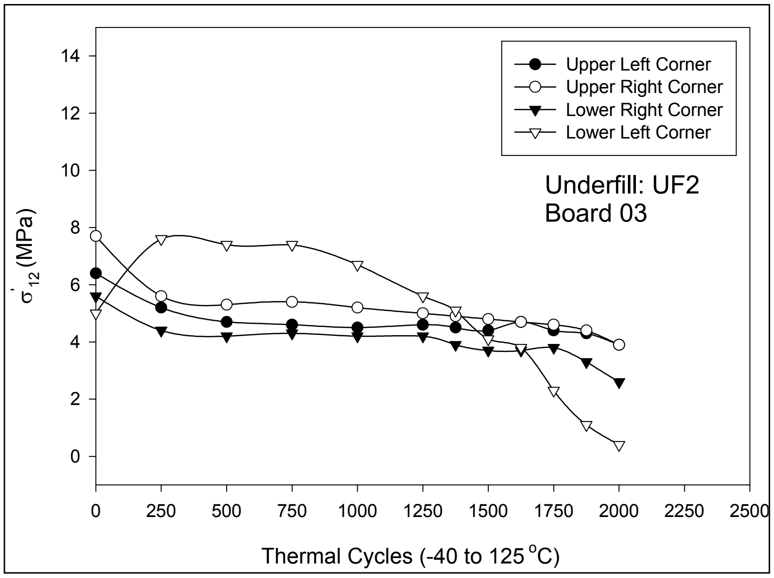


Figure 7.20 - Stress Histories at Corner Sites (UF2, Board 3)

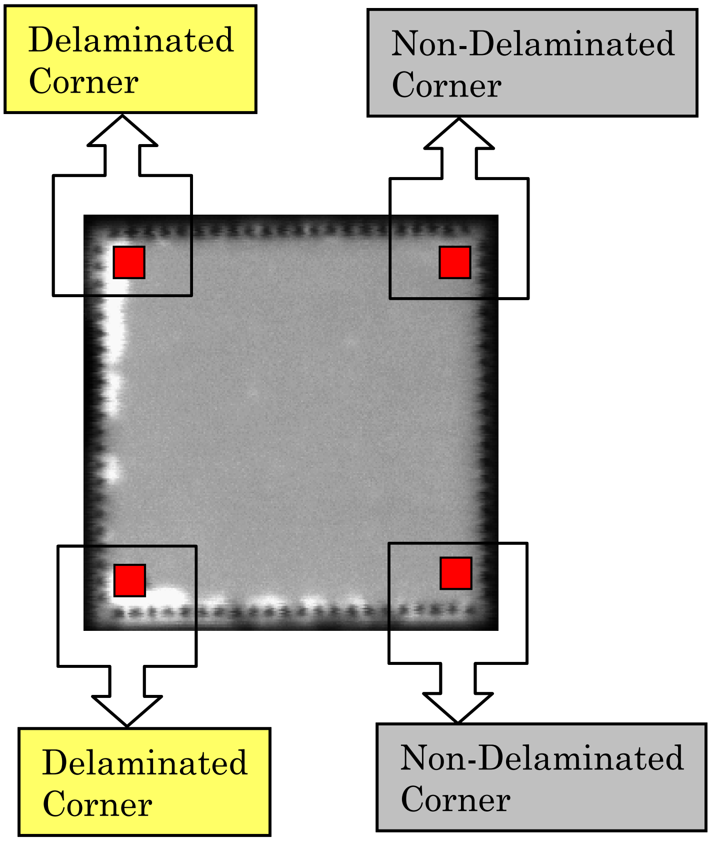

Delaminated Corner
Non-Delaminated Corner
Delaminated Corner
Non-Delaminated Corner

Figure 7.21 - Corner Delamination Status (UF1, Board 21)

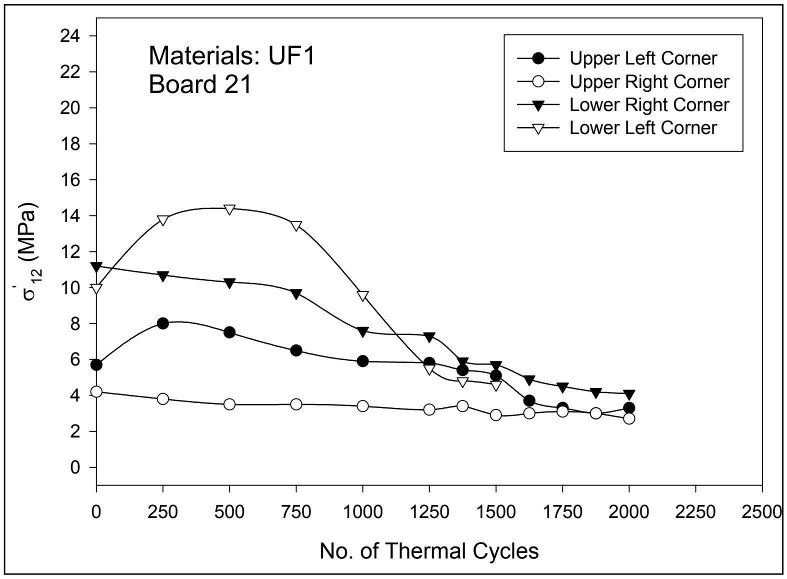


Figure 7.22 - Stress Histories at Corner Sites (UF1, Board 21)

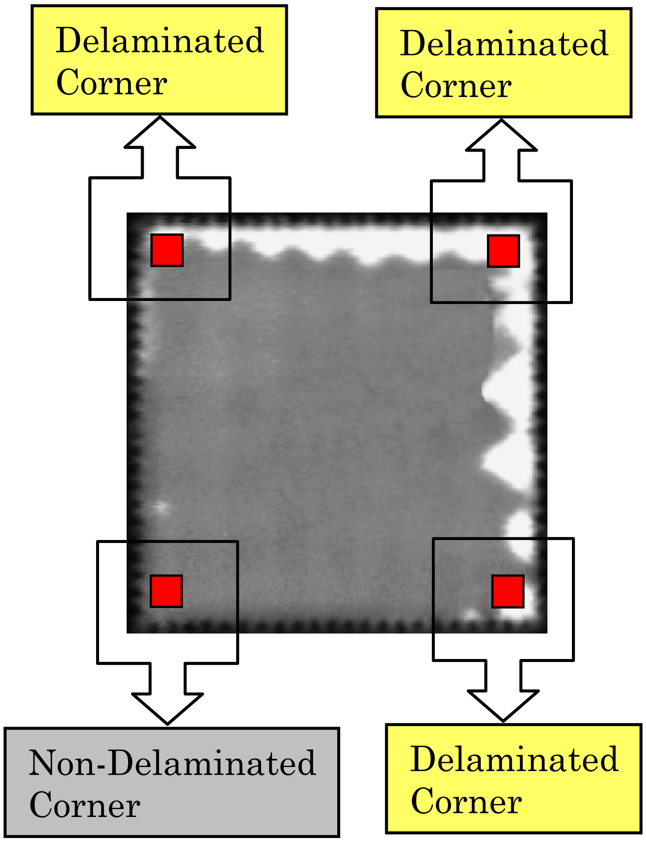

Delaminated Corner
Delaminated Corner
Non-Delaminated Corner
Delaminated Corner

Figure 7.23 - Corner Delamination Status (UF3, Board 16)

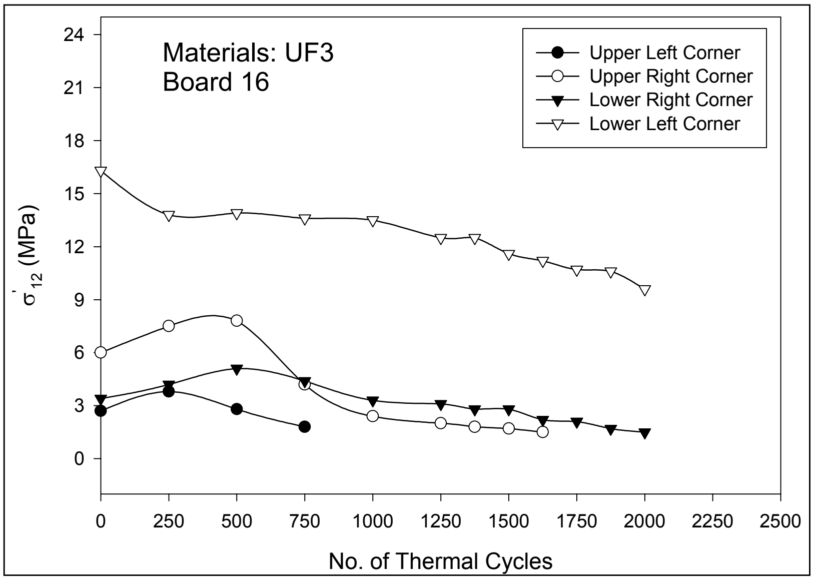
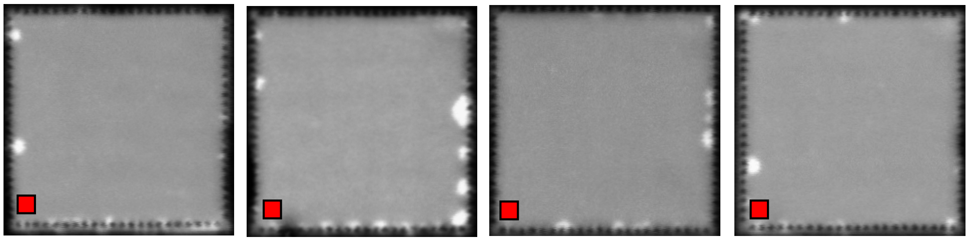


Figure 7.24 - Stress Histories at Corner Sites (UF3, Board 16)



Board 06 Board 17 Board 26 Board 27

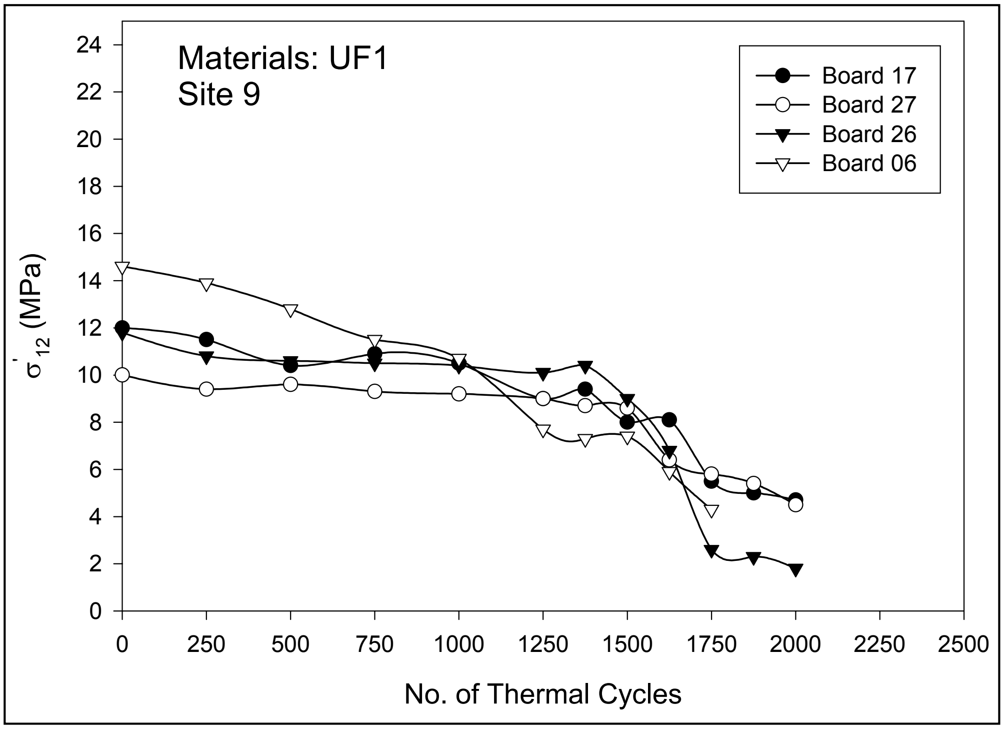


Figure 7.25 - Stress Variation at Non-Delaminated Corners (Underfill UF1)

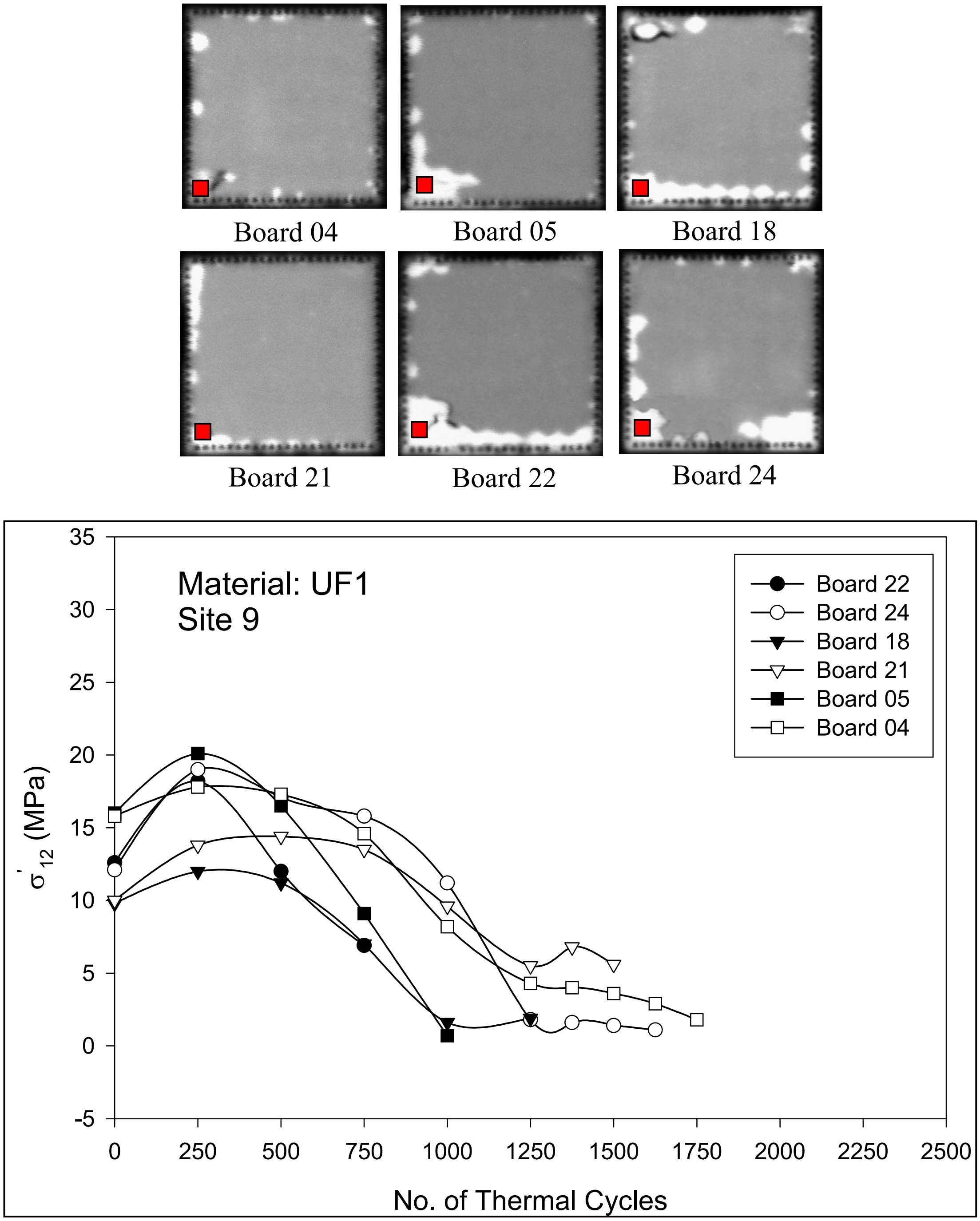


Figure 7.26 - Stress Variation at Delaminated Corners (Underfill UF1)

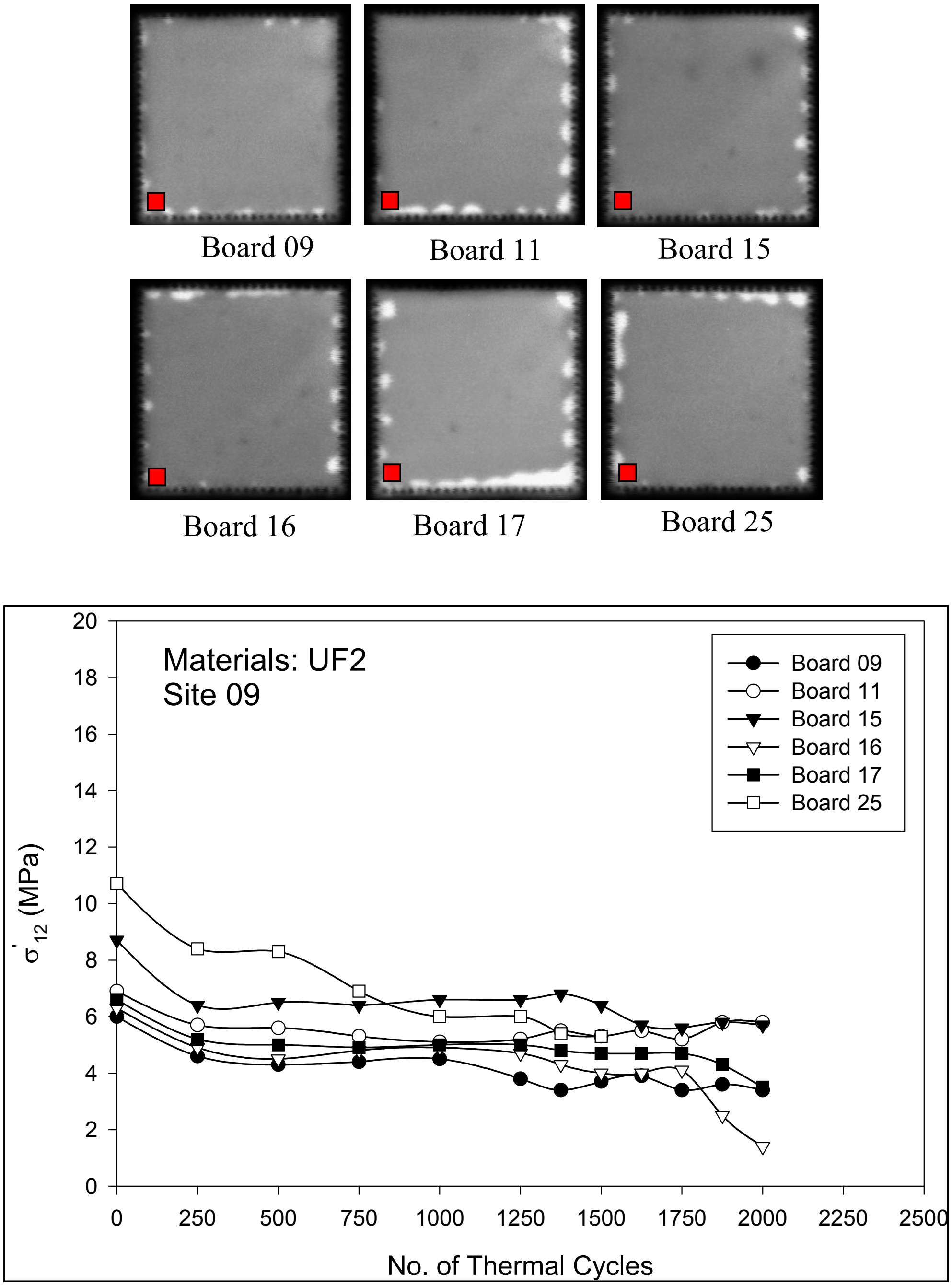
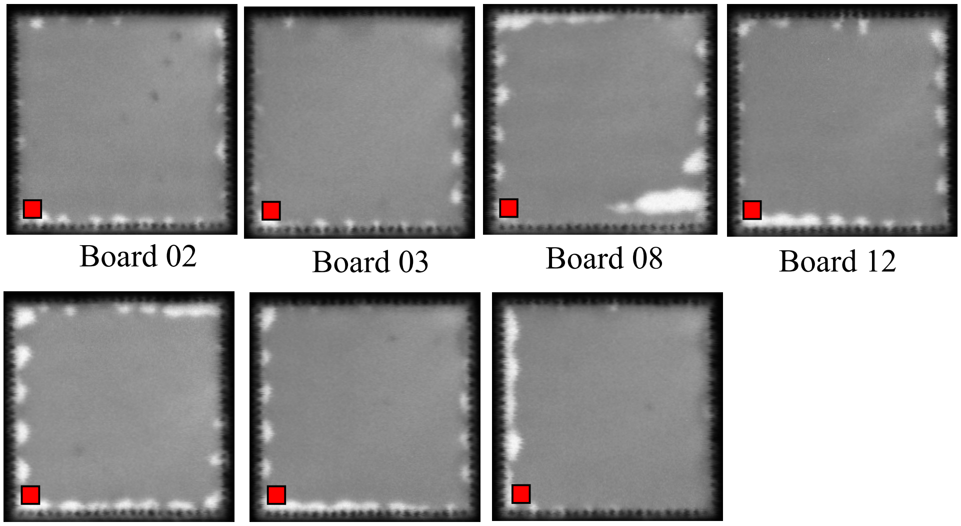


Figure 7.27 - Stress Variation at Non-Delaminated Corners (Underfill UF2)


Board 02 Board 03 Board 08 Board 12

Board 19 Board 23 Board 24

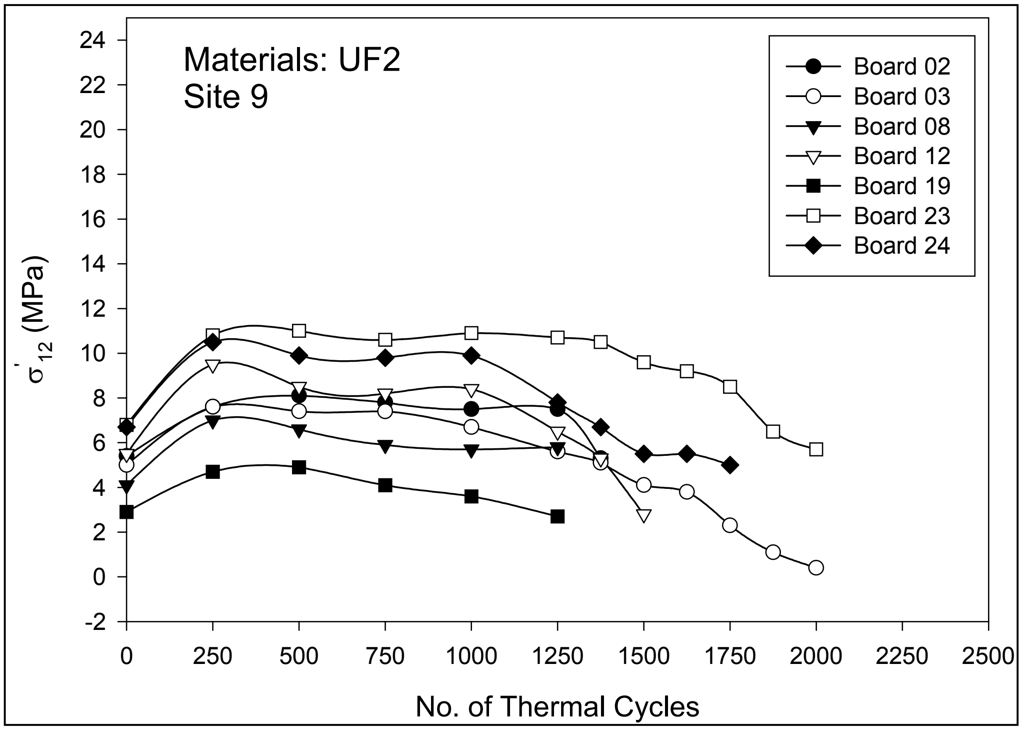


Figure 7.28 - Stress Variation at Delaminated Corners (Underfill UF2)

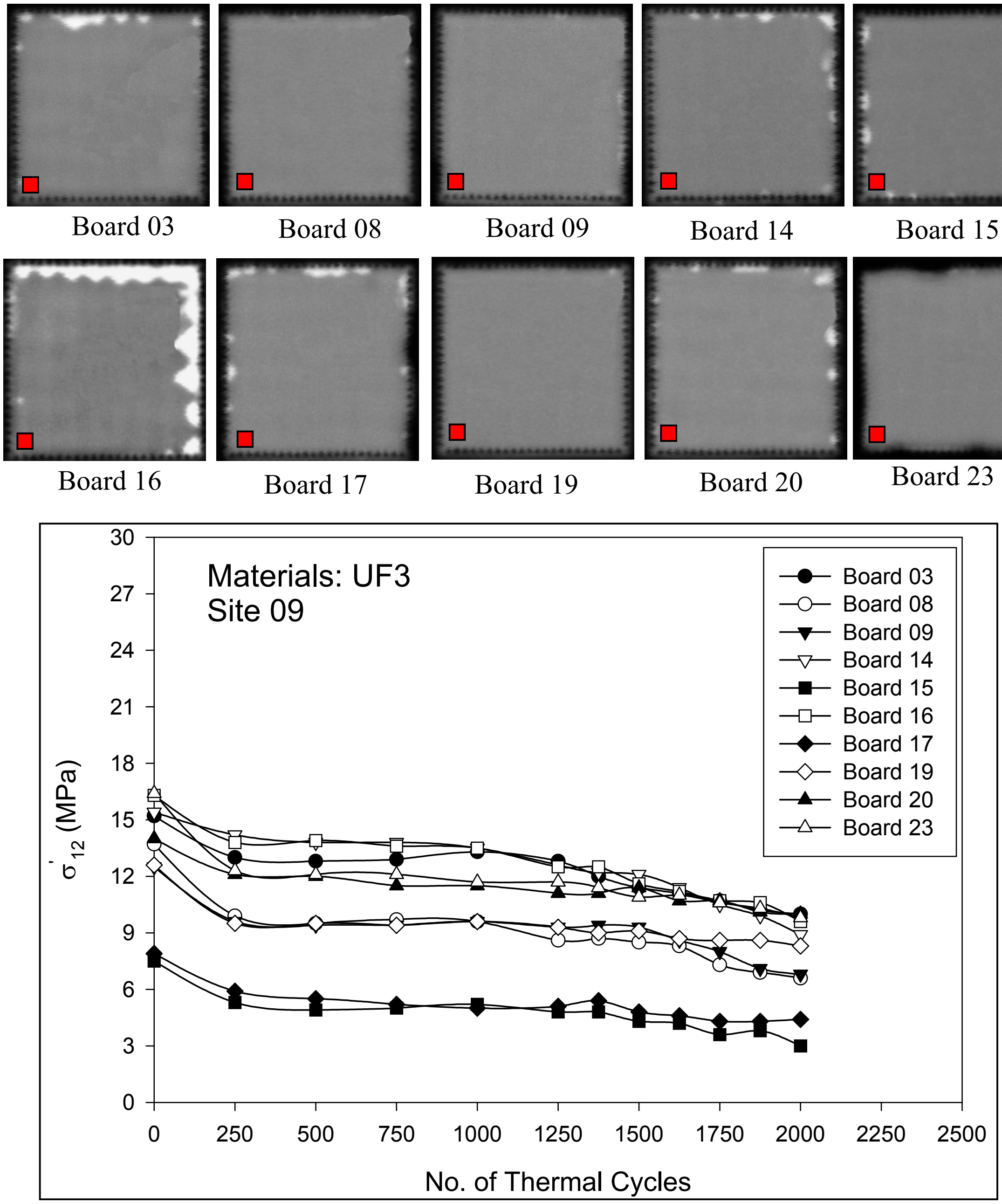


Figure 7.29 - Stress Variation at Non-Delaminated Corners (Underfill UF3)

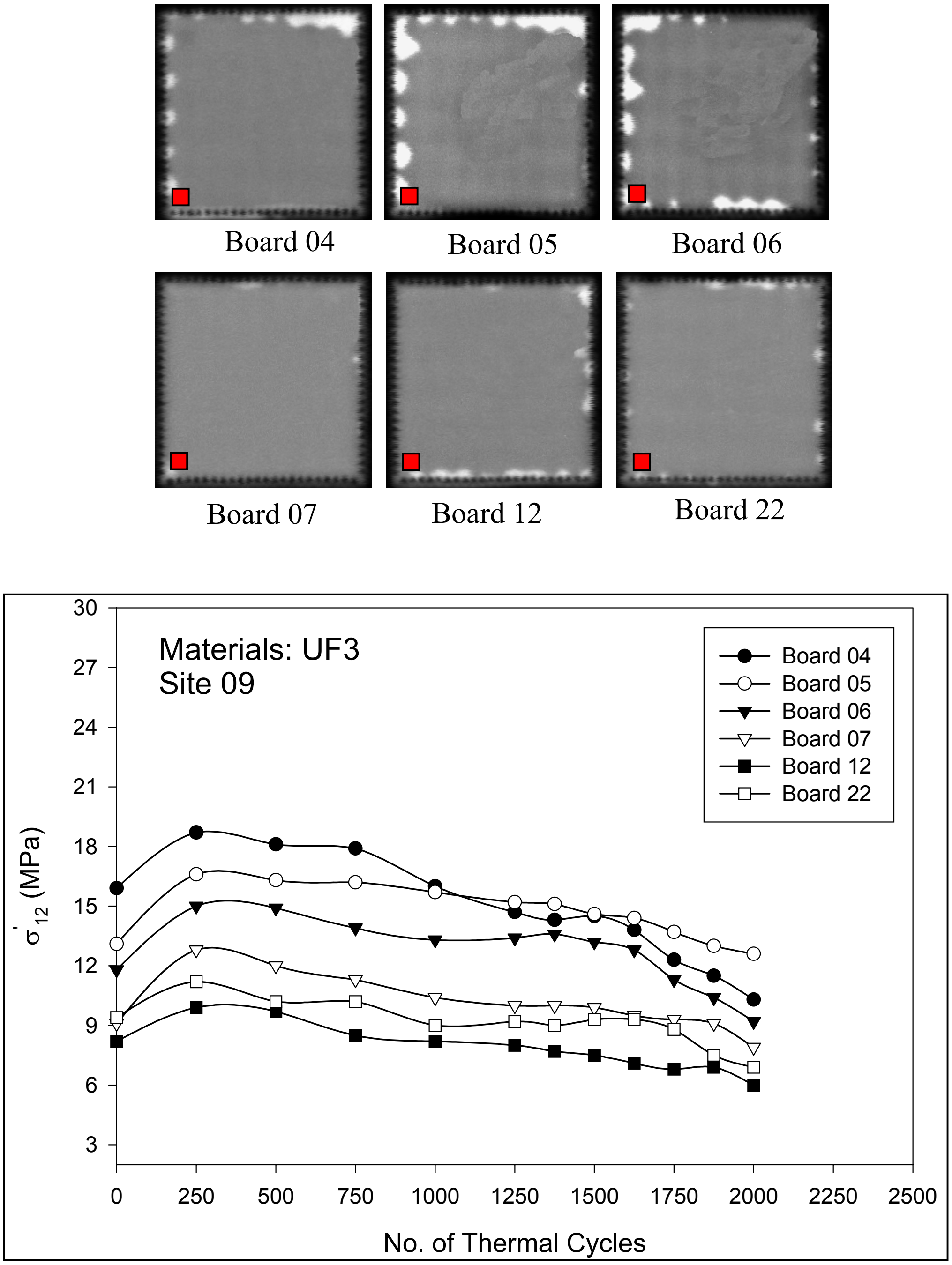


Figure 7.30 - Stress Variation at Delaminated Corners (Underfill UF3)

In this study, we found that all delaminations initiated at the corners or at the edges of the assemblies. Most of the assemblies remained non-delaminated at the die center after 3000 thermal cycles. Figure 7.31 shows the in-plane normal stresses variations at the center of one of the flip chip assemblies (Board 10, Underfill UF2). In this case, the underfill/die interface was still non-delaminated at the die center after 3000 thermal cycles, where at the same time the corners and edges of the assembly was fully delaminated. The extensive relaxation in the normal stresses in a single assembly well reflects the average stress behavior plotted in Figure 7.16. Clearly, extensive relaxation and material changes have occurred. Similar trends were observed for others two underfills materials. The in-plane normal stresses variations at the center of one of the flip chip assemblies for underfill UF1 and underfill UF3 are shown in Figures 7.32 and 7.33, respectively.

## 7.6 Summary

In this work, a fundamental understanding of delamination initiation and growth in flip chip assemblies has been developed through simultaneous characterization of the stress and delamination states at the die to underfill interface during thermal cycling. Mechanical stresses on the device side of the flip chip die have been measured using special (111) silicon stress test chips containing piezoresistive sensor rosettes that are capable of measuring the complete three-dimensional silicon surface stress state in the silicon (including the interfacial shear and normal stresses at the die to underfill interface). The fabricated flip chip test die were assembled to FR-406 laminate substrates. Room temperature die stresses after assembly have been evaluated and

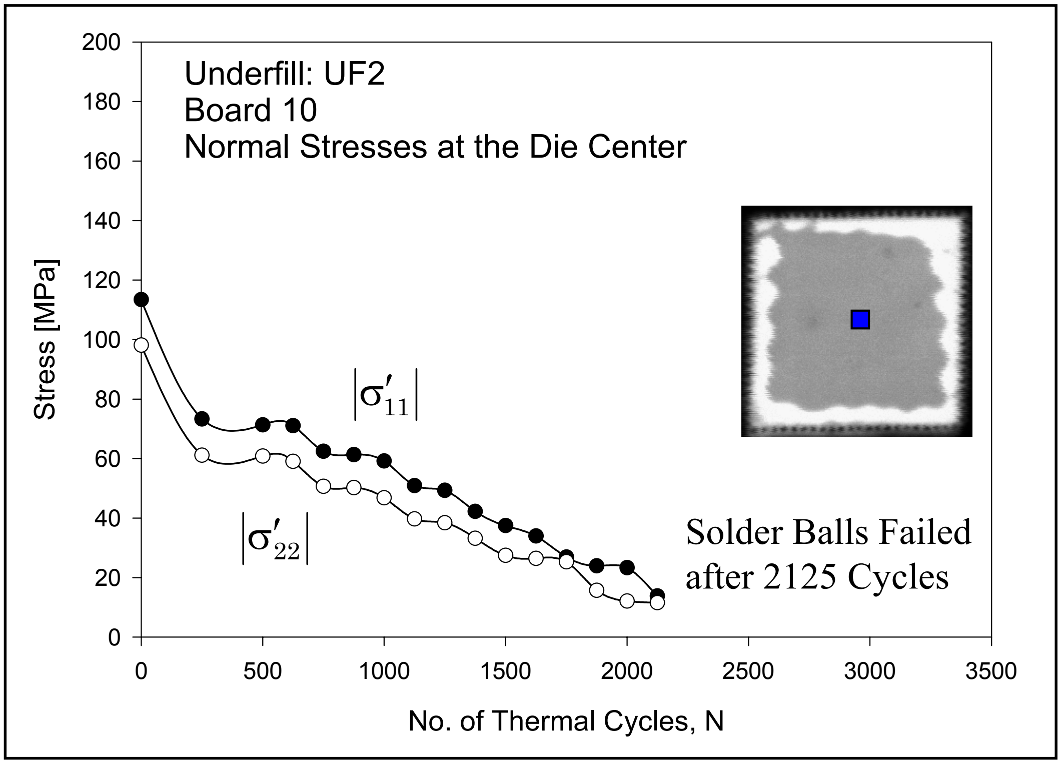


Figure 7.31 - Typical Normal Stress History at the Center of the Die in An Example Flip Chip Assembly (Underfill UF2)

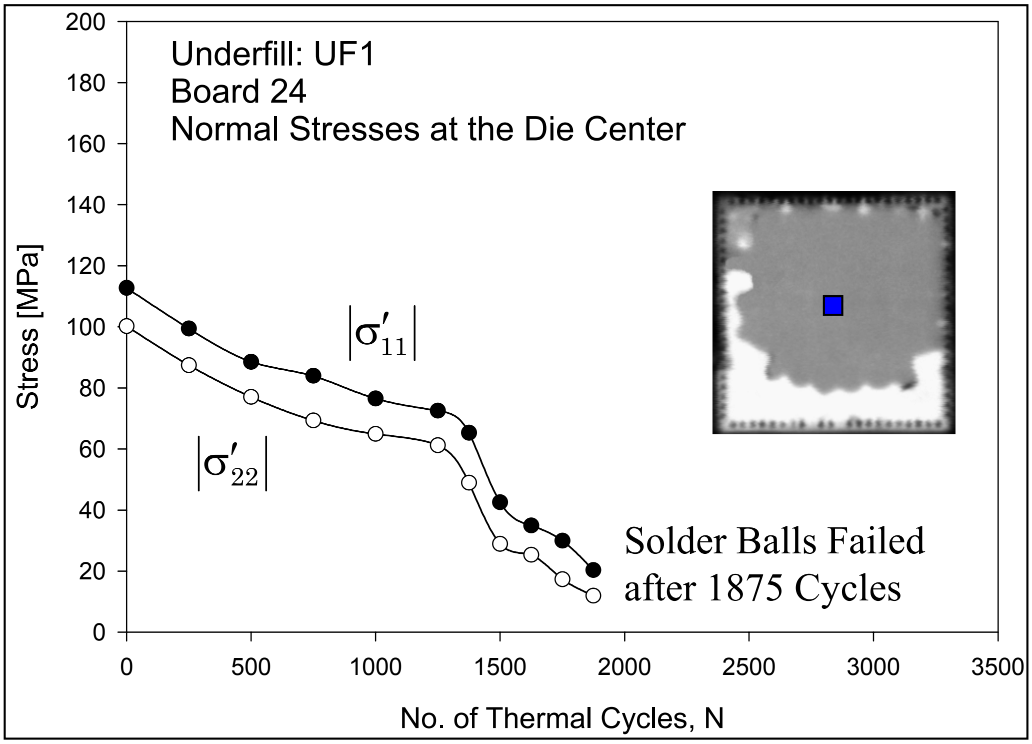


Figure 7.32 - Typical Normal Stress History at the Center of the Die in An Example Flip Chip Assembly (Underfill UF1)

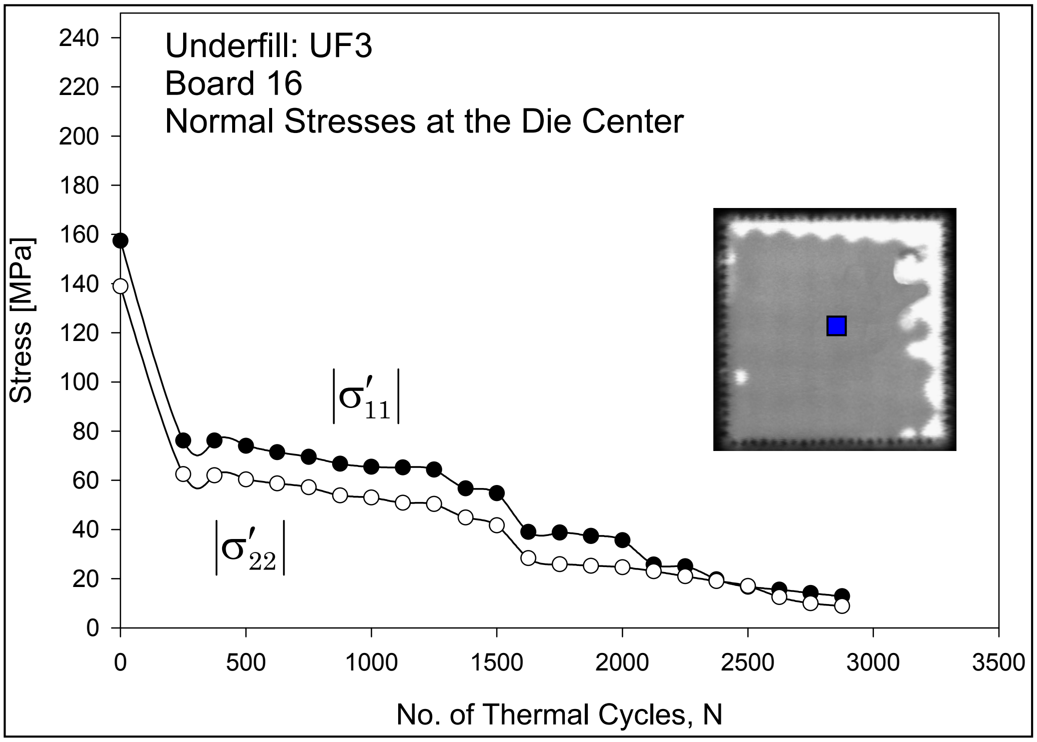


Figure 7.33 - Typical Normal Stress History at the Center of the Die in An Example Flip Chip Assembly (Underfill UF3)

compared for three different underfills. Minimizing these device side die stresses is especially important when multiple copper/low-k interconnect redistribution layers are present. The in-plane shear stress distribution was found to lack the expected symmetry present for an ideal assembly where the underfill is dispensed at all locations under the die simultaneously. The data for all three underfills indicated a concentration in the shear stress at the underfill dispense corner. The stress magnitudes in this corner were 50-100% higher than the values at the other 3 corners, and delaminations were found to initiate at this high stress corner during thermal cycling assemblies underfilled with encapsulant UF1.

The assemblies were then subjected to 3000 thermal cycles from -40 to 125 $^{o}$C. By continuous monitoring of the sensor resistances during the environmental testing, the die surface stresses were measured throughout the post-assembly thermal cycling exposure. These measurements have been correlated with the delaminations occurring at the die passivation to underfill interface measured using C-mode Scanning Acoustic Microscopy (CSAM). Significant variations were found to occur in the magnitudes of the average stresses, even if there was no delamination in the flip chip assembly as thermal cycling proceeds. Such behavior is most likely due to a combination of several effects including changes that occur in the underfill material and adhesion properties, and the viscoplastic deformations that occur during thermal cycling.

Testing of 75 flip chip assemblies has been completed to date (1 die size x 3 underfills x 25 samples per combination). In each assembly, the complete histories of three-dimensional die surface stresses, delamination propagation have been recorded versus the duration of -40 to 125 $^{o}$C thermal cycling. One of the most important discoveries is that the shear stresses occurring at the corners of flip chip die have been demonstrated to be a suitable proxy for prognostic determination of future delamination initiations and growth. Thus, shear stress sensors have great potential as health-monitoring devices in flip chip packaging. The transient die stress variation during delamination is clearly a very complex phenomenon.

# CHAPTER 8

# LOW EXPANSION PCB FOR MINIMIZING DIE STRESSES IN FLIP CHIP ON LAMINATE ASSEMBLIES

## 8.1 Introduction

Coefficient of thermal expansion mismatches between packaging materials is a major cause of die stresses in flip chip on laminate assemblies. With the die is coupled to the substrate through the underfill epoxy, bending or curvature of the assembly is produced upon changes of temperature (Figure 5.5). This leads to a greatly reduced dependence of the solder bump shear strains on the distance from the chip center (neutral point).

In addition to the use of underfill encapsulants, further improvements in the reliability of flip chip on laminate assemblies can be obtained by reducing the coefficient of thermal expansion (CTE) of the substrate material. A novel approach for obtaining laminated substrates with extremely low thermal expansion coefficients (similar to silicon) has been established by ThermalWorks, Inc. and marketed using the trade name STABLCOR®. In the developed approach, hybrid laminates are formed that include a combination of standard glass fiber reinforced resin layers with carbon fiber reinforced resin layers. With both fiber systems, processing techniques have been developed to utilize standard epoxy resins (FR-402, FR-406, etc.), as well as polyimide and Cyanate ester resins.

The utilized laminate features a sandwich construction that contains standard FR-406 outer layers surrounding a low expansion high thermal conductivity carbon fiber-reinforced composite core (STABLCOR). A simple example of the hybrid PCB composite laminate approach is shown in Figure 8.1. The carbon fiber based central core features both high stiffness and high thermal conductivity, as well as near zero thermal expansion coefficient. The outer top and bottom regions are typical glass fiber reinforced FR-4 lay-ups, which can contain multiple layers with patterned copper traces. Because of the extremely low expansion coefficient of the carbon fiber core and the bonded nature of the laminate, the surface CTE of the hybrid laminate PCB stack-up is typically in the range of 2.0-4.0 ppm/$^{o}$C over the temperature range of -55 to 150 $^{o}$C, which is much lower than the typical 13.0-20.0 ppm/$^{o}$C seen with standard FR-406 based laminates. In addition, the high stiffness of the carbon fiber based core can help reduce PCB warpage issues, as well as vastly improve the net heat conduction characteristics of the PCB substrate [198-199].

In this work, die stresses have been characterized in flip chip assemblies made with conventional FR-406 substrates and enhanced substrates with FR-406 outer layers and carbon fiber cores. The flip chip test die were packaged with both substrate technologies, and die surface stresses were measured throughout the assembly process. Transient die stresses during underfill cure, and the room temperature die stresses in final cured assemblies have been measured and compared.

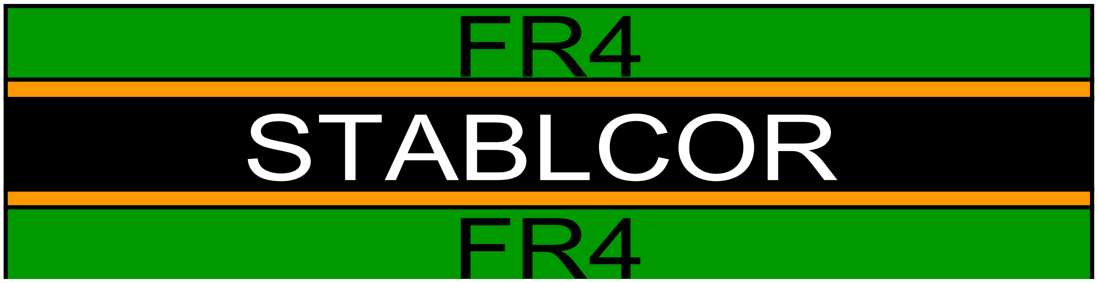

FR4
STABLCOR
FR4

Figure 8.1 - Example Hybrid PCB Laminate Incorporating Low CTE Carbon Fiber Based Core (STABLCOR)

## 8.2 Packaging Technology and Test Chips

A schematic of a flip chip assembly with the carbon fiber core hybrid laminate construction is shown in Figures 8.2. In this work, the FC200 test chip described in previous chapters has been utilized. The test chips have been assembled to substrates manufactured from standard laminate substrates featuring glass fibers in a high Tg epoxy matrix (FR-406), and to hybrid laminate substrates featuring a carbon fiber based core material (STABLCOR) surrounded by standard glass fiber reinforced FR-406 layers. These two laminate material combinations are listed in Table 8.1. To simplify further discussions in this chapter, they will be referred to with the shorthand laminate designations of FR-406 and STABLCOR. Therefore, the terminology STABLCOR laminate is intended to imply the hybrid composite laminate formed with glass-epoxy (FR-406) outer layers surrounding a carbon fiber based core (unless specifically mentioned otherwise). Figure 8.3 shows various views of one of the STABLCOR flip chip assemblies containing a 5 x 5 mm stress test chip. Underfill UF3 (see Table 5.2) was used to develop the STABLCOR flip chip test assemblies.

| Laminate Designation | Outer Layers | | |
|---|---|---|---|
| | Resin | Fiber | Core |
| FR-406 | FR-406 | Glass | None |
| STABLCOR | FR-406 | Glass | STABLCOR®<br>(ST500P) |

Table 8.1 - Laminate Types for Test Boards

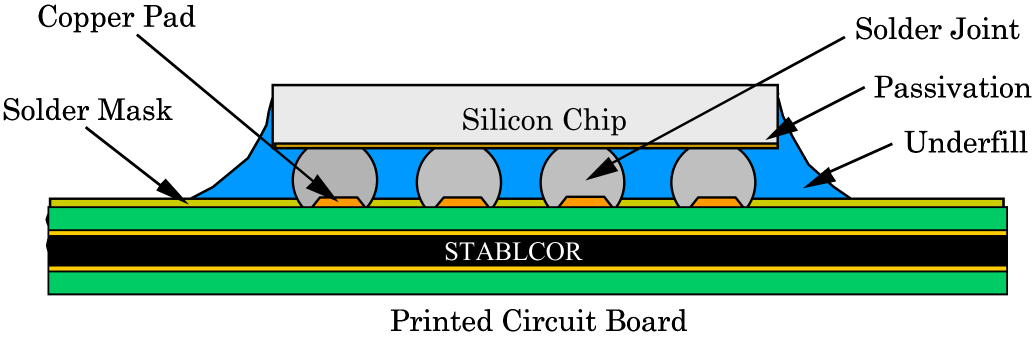

Copper Pad
Solder Mask
Silicon Chip
Solder Joint
Passivation
Underfill
STABLCOR
Printed Circuit Board

Figure 8.2 – Flip Chip Assembly on Low CTE Carbon Fiber Based Core (STABLCOR)

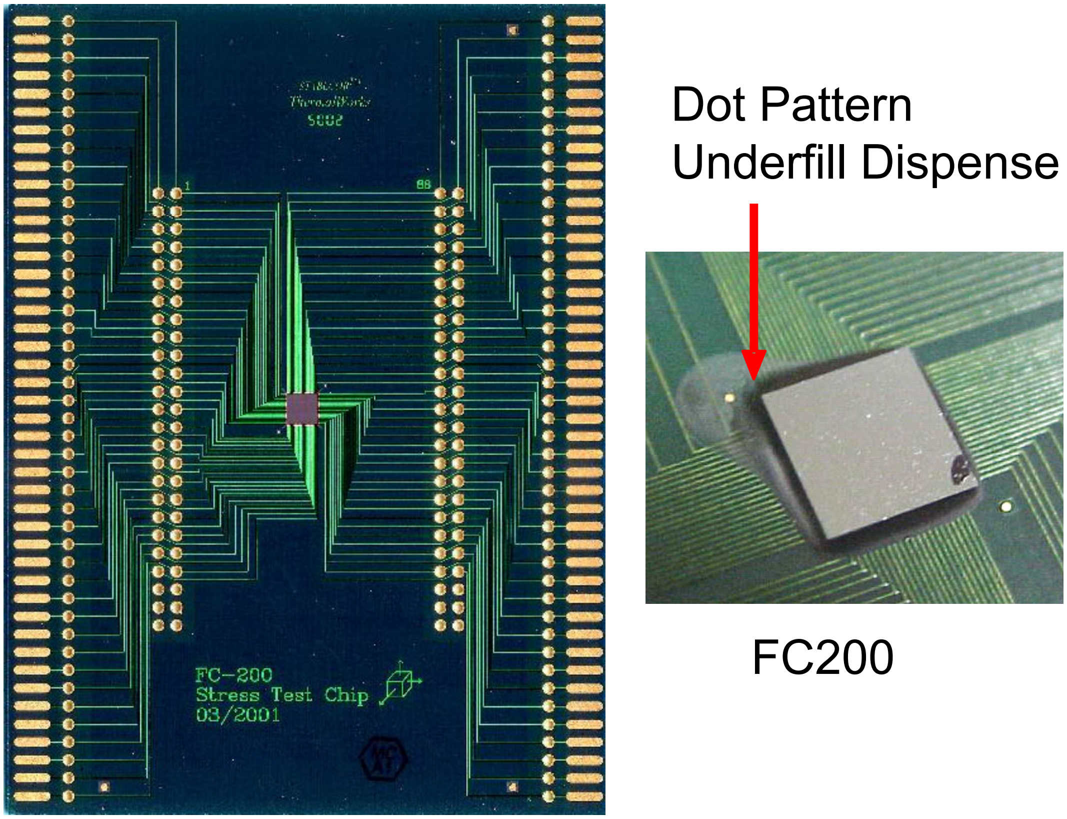

Dot Pattern
Underfill Dispense
FC200
1
88
FC-200
Stress Test Chip
03/2001

Figure 8.3 – STABLCOR  Flip Chip Assembly Incorporating Stress Test Chip

## 8.3 Comparison of Test Results with FR-406 Flip Chip Assembly

The FC200 test chip assemblies have been utilized to measure the die stresses in flip chip on laminate assemblies throughout the assembly process. The transient die stresses were monitored during the cure cycle. After final assembly was completed, the die stresses were also measured at room temperature, and as a function of temperature during a slow change from -55 to +150 $^{o}$C. The measured stresses for the two substrate technologies were then compared. Figure 8.4 shows the rosette site designations for the resistance/stress measurements.

### 8.3.1 Stress Variation During Underfill Cure

As mentioned previously, transient sensor resistances were monitored during the entire underfill encapsulant cure process. In Chapter 5, the die stresses during underfill cure and at room temperature and as a function of temperature after cure have thoroughly discussed [143-144]. The comparison of the in-plane normal stress difference and shear stress variation with time for example STABLCOR and FR-406 assemblies are shown in Figures 8.5 and 8.6, respectively. When comparing the results in the plots in Figures 8.5-8.6 for the FR-406 and STABLCOR laminates (FC200, 5 x 5 mm die size), it can be seen that the final die in-plane shear stress magnitudes are 4-8X smaller in the assemblies using the STABLCOR hybrid laminates.

### 8.3.2 Stresses After Underfill Encapsulation

After underfill cure and cooldown, the final assembly room temperature die stresses for the two substrate technologies were characterized and compared. In this case, the initial and final sensor resistance measurements used to evaluate the stresses were both made at room temperature (23 $^{o}$C). Thus, all thermal errors in application of the

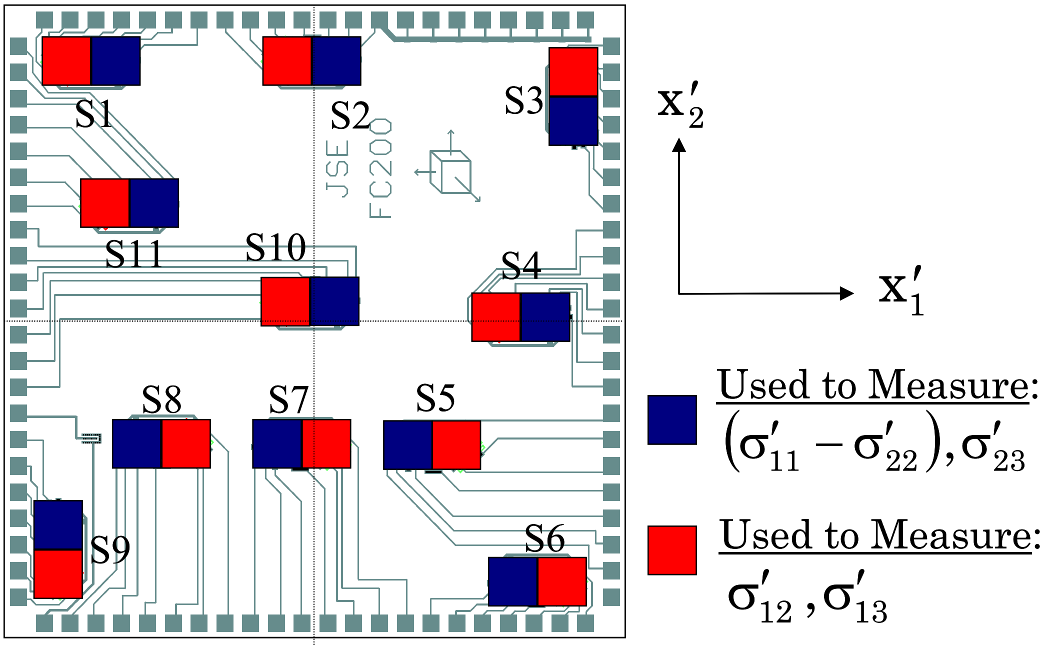

S1
S2
S3
JSE
FC200
$x_2'$
S11
S10
S4
$x_1'$
S8
S7
S5
S9
S6
🟦 Used to Measure: $\left(\sigma_{11}' - \sigma_{22}'\right), \sigma_{23}'$
🟥 Used to Measure: $\sigma_{12}', \sigma_{13}'$

Figure 8.4 - Rosette Sites for Stress Measurement

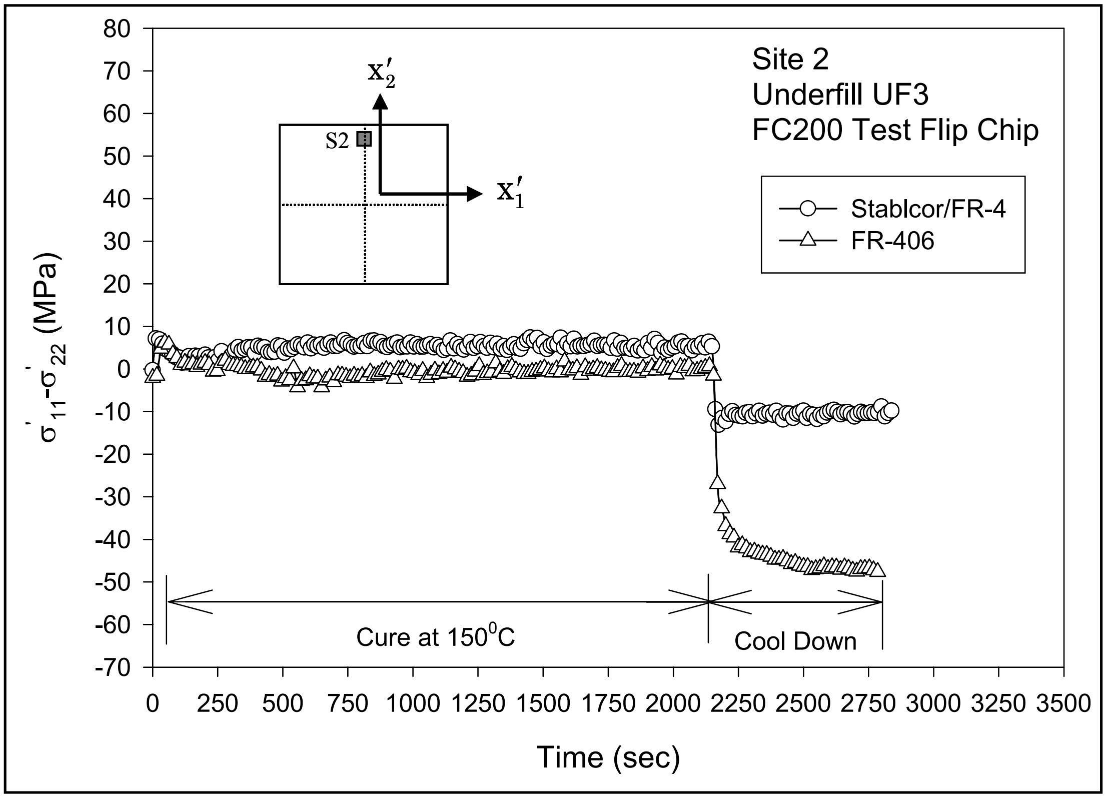


Figure 8.5 - In-Plane Normal Stress Difference Variation During Underfill Cure for Different Substrate Configurations (FR-406 and STABLCOR)

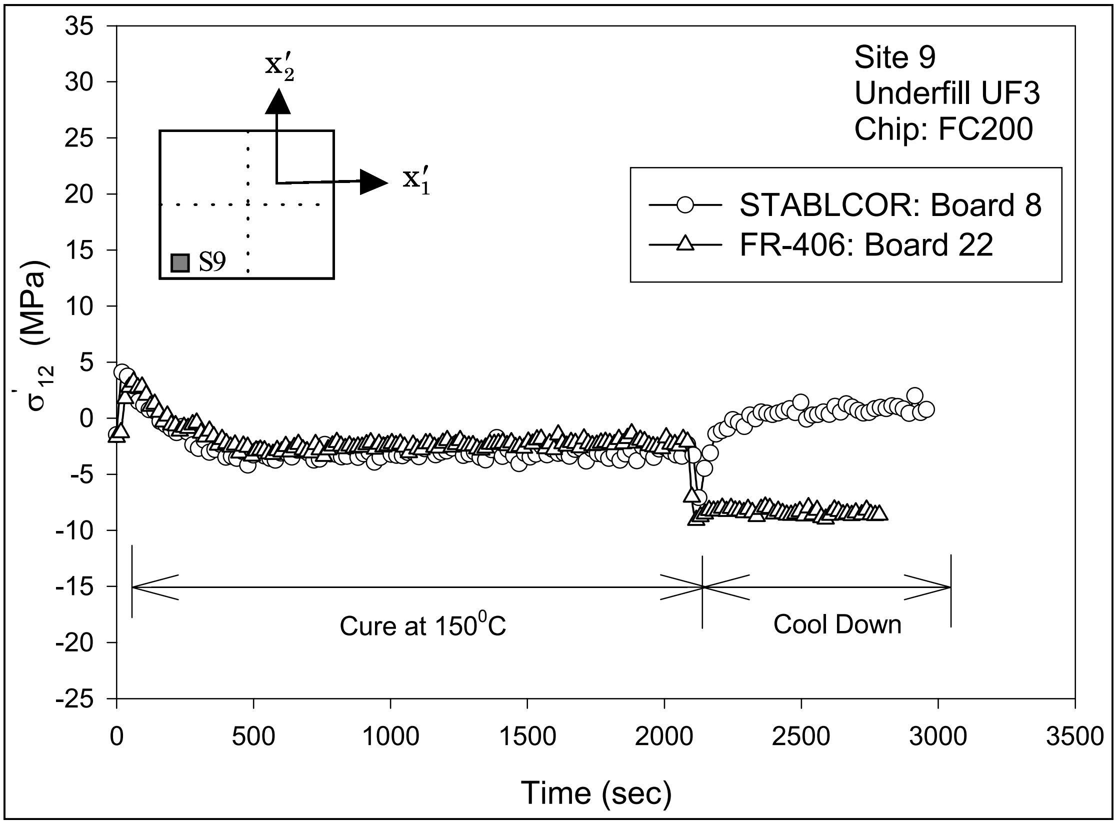


Figure 8.6 - In-Plane Shear Stress Variation During Underfill Cure for Different Substrate Configurations (FR-406 and STABLCOR)

sensors will be minimized (T = 0). Figures 8.7-8.10 show the comparison of measured data for the in-plane normal stresses $\sigma'_{11}$ and in-plane normal stress difference $(\sigma'_{11} - \sigma'_{22})$, in-plane shear stress $\sigma'_{12}$, and interfacial shear stresses $\tau_{\text{Interfacial}}$, respectively. At every rosette site in these plots, results are given for the two different substrates. The values beside each rosette site indicate the average and standard deviation from the 25 specimens used for each substrate technology.

For the in-plane normal stresses in the FC200 die, it can be seem that large reductions in the die stress magnitudes are realized when using the low CTE STABLCOR substrates. For stress $\sigma'_{11}$, the stress magnitudes in the FR-406 assemblies were typically 8-12X larger than the corresponding stresses in the STABLCOR assemblies. Similar large reductions in the FC200 die stresses are seen for the in-plane shear stress $\sigma'_{12}$, and total out-of-plane (interfacial) shear stress $\tau_{\text{Interfacial}}$. Figures 8.11-8.12 show graphically the die stresses comparison for two different PCB substrates. In these graphs, the highest die stresses at the critical location of the die have compared.

### 8.3.3 Temperature Dependent Stress Measurements

To further illustrate the nature of the stresses induced by underfill encapsulation, several flip chip assemblies were subjected to slow temperature change from -55 to +150 $^{o}$C. Resistance values were monitored continuously, and the stresses were extracted as a function of temperature. Typical in-plane normal stress difference and in-plane shear stress data are shown in Figures 8.13 and 8.14, respectively.

In all cases, raising the temperature from room temperature decreases the magnitude of the stress component. As the temperature approached or exceeded 150 $^{o}$C

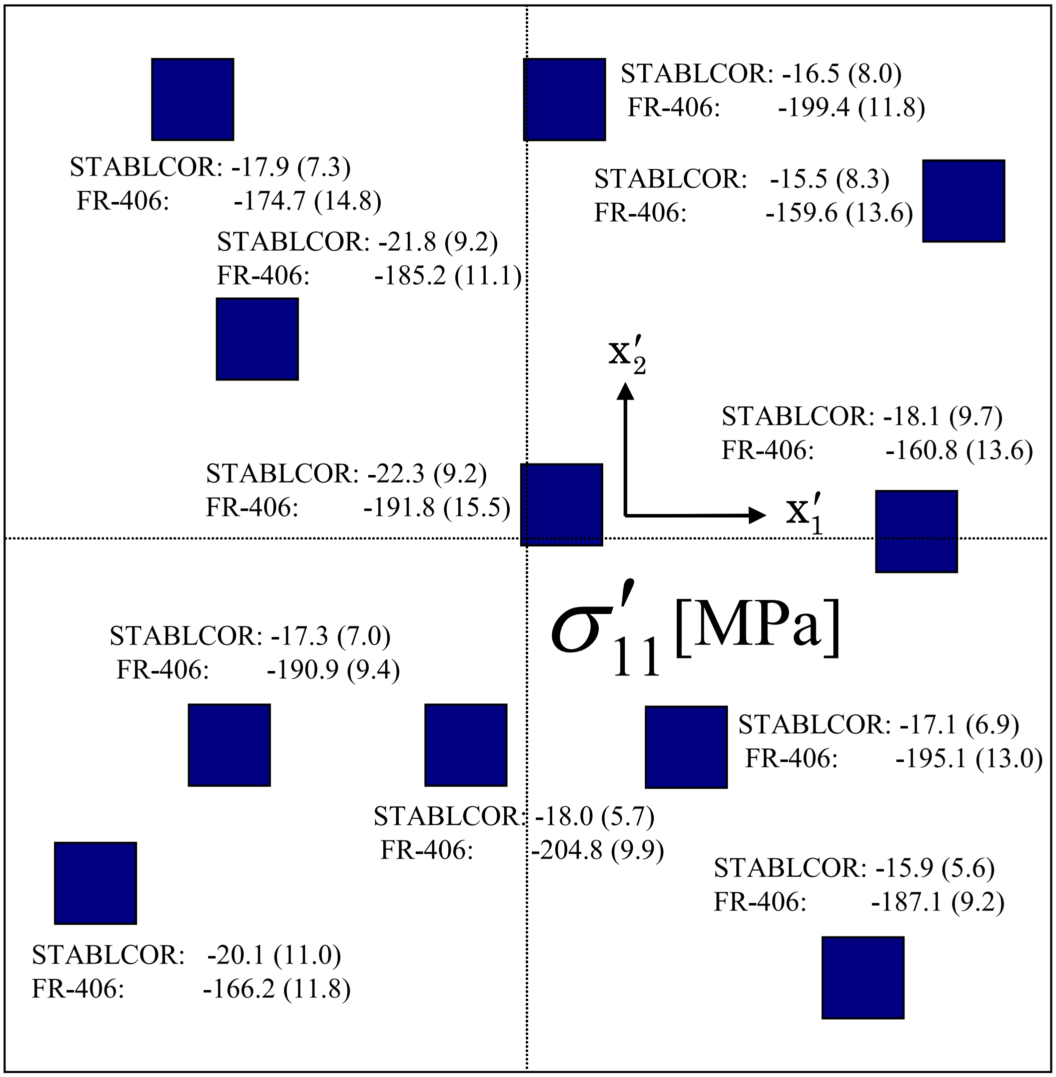

STABLCOR: -16.5 (8.0)
FR-406: -199.4 (11.8)
STABLCOR: -17.9 (7.3)
FR-406: -174.7 (14.8)
STABLCOR: -15.5 (8.3)
FR-406: -159.6 (13.6)
STABLCOR: -21.8 (9.2)
FR-406: -185.2 (11.1)
$x_2'$
STABLCOR: -18.1 (9.7)
FR-406: -160.8 (13.6)
STABLCOR: -22.3 (9.2)
FR-406: -191.8 (15.5)
$x_1'$
$\sigma_{11}'$ [MPa]
STABLCOR: -17.3 (7.0)
FR-406: -190.9 (9.4)
STABLCOR: -17.1 (6.9)
FR-406: -195.1 (13.0)
STABLCOR: -18.0 (5.7)
FR-406: -204.8 (9.9)
STABLCOR: -15.9 (5.6)
FR-406: -187.1 (9.2)
STABLCOR: -20.1 (11.0)
FR-406: -166.2 (11.8)

Figure 8.7 – Average In-Plane Normal Stress After Cure for Different Substrate Configurations (FR-406 and STABLCOR)

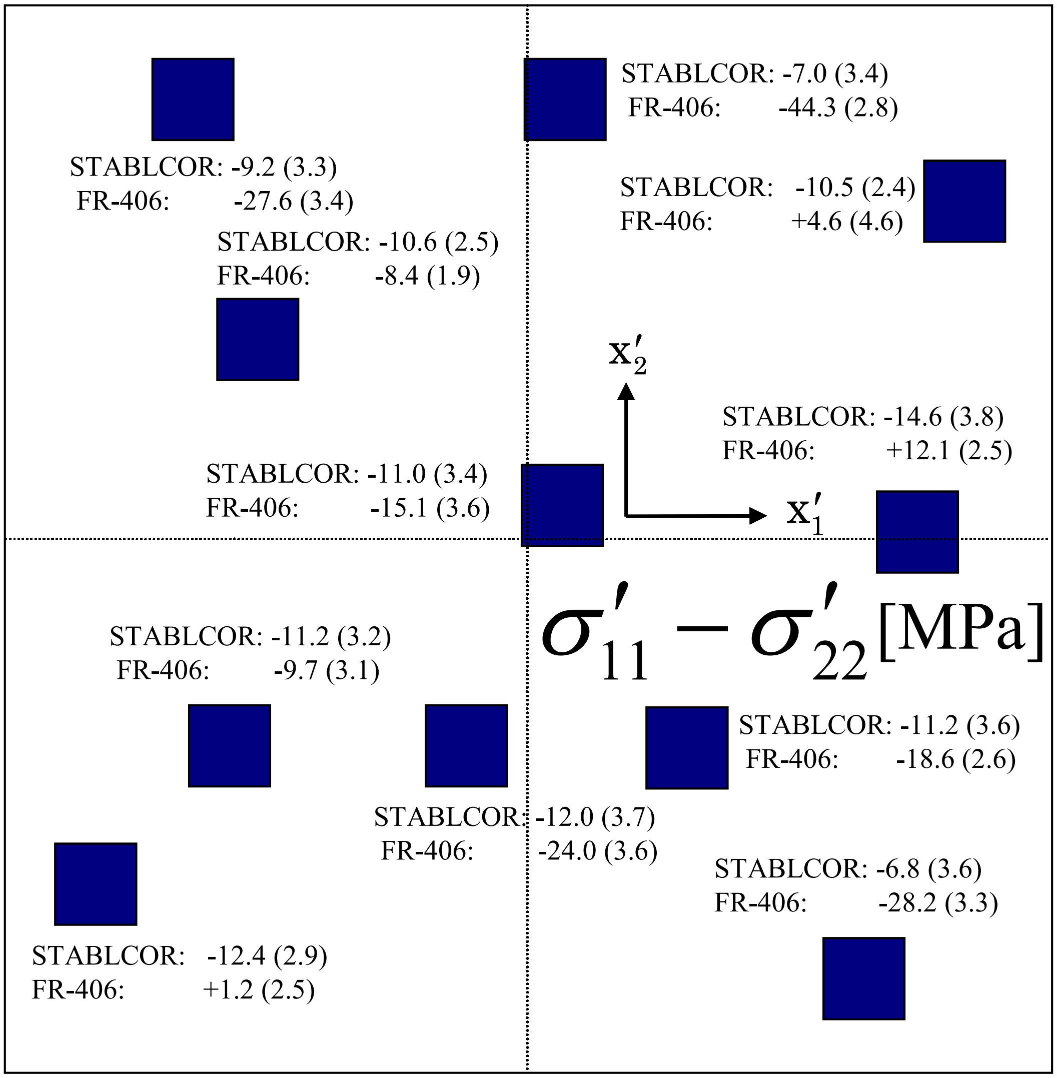

STABLCOR: -7.0 (3.4)
FR-406: -44.3 (2.8)
STABLCOR: -9.2 (3.3)
FR-406: -27.6 (3.4)
STABLCOR: -10.5 (2.4)
FR-406: +4.6 (4.6)
STABLCOR: -10.6 (2.5)
FR-406: -8.4 (1.9)
$x_2'$
STABLCOR: -14.6 (3.8)
FR-406: +12.1 (2.5)
STABLCOR: -11.0 (3.4)
FR-406: -15.1 (3.6)
$x_1'$
$\sigma_{11}' - \sigma_{22}'$ [MPa]
STABLCOR: -11.2 (3.2)
FR-406: -9.7 (3.1)
STABLCOR: -11.2 (3.6)
FR-406: -18.6 (2.6)
STABLCOR: -12.0 (3.7)
FR-406: -24.0 (3.6)
STABLCOR: -6.8 (3.6)
FR-406: -28.2 (3.3)
STABLCOR: -12.4 (2.9)
FR-406: +1.2 (2.5)

Figure 8.8 – Average In-Plane Normal Stress Difference After Cure for Different Substrate Configurations (FR-406 and STABLCOR)

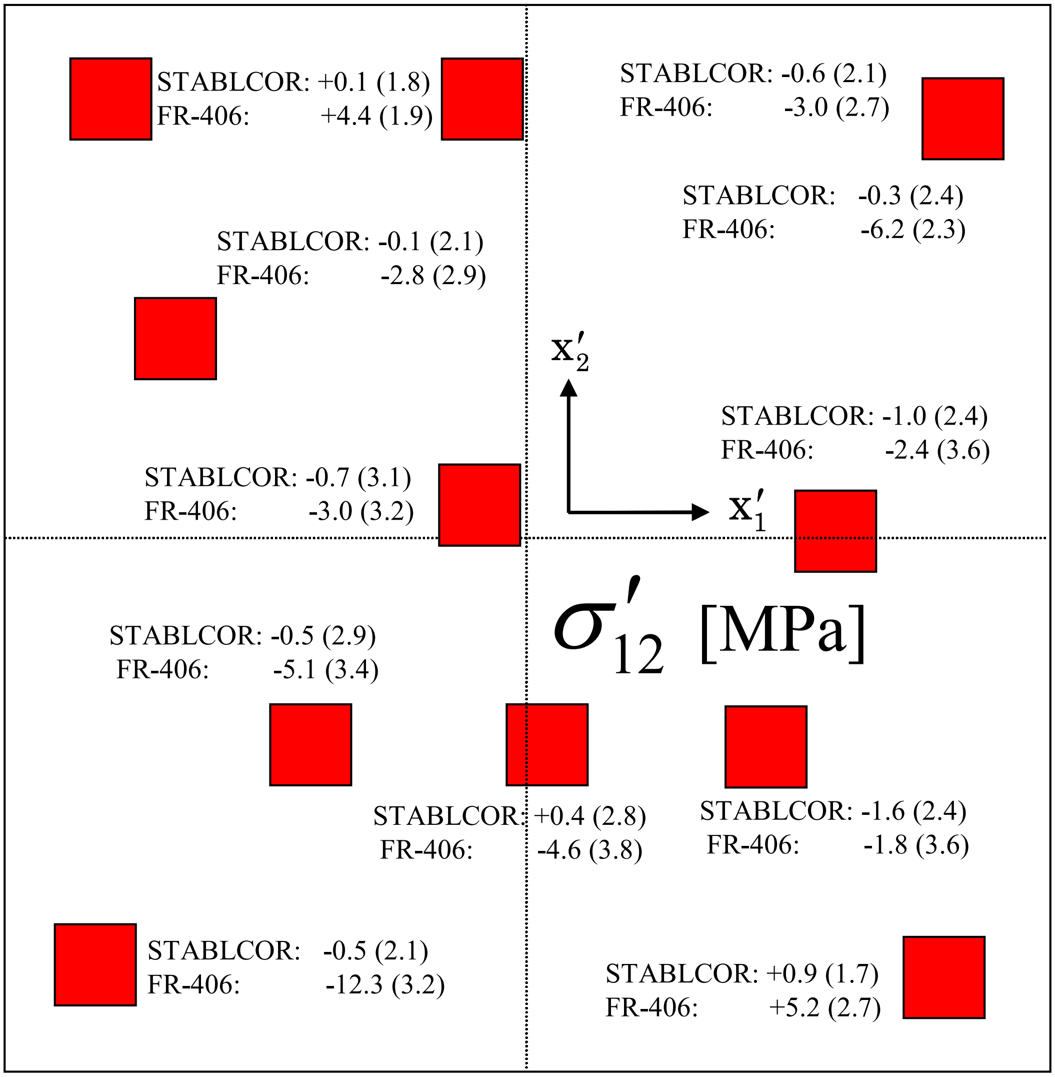

STABLCOR: +0.1 (1.8)
FR-406: +4.4 (1.9)
STABLCOR: -0.6 (2.1)
FR-406: -3.0 (2.7)
STABLCOR: -0.3 (2.4)
FR-406: -6.2 (2.3)
STABLCOR: -0.1 (2.1)
FR-406: -2.8 (2.9)
$x_2'$
STABLCOR: -1.0 (2.4)
FR-406: -2.4 (3.6)
STABLCOR: -0.7 (3.1)
FR-406: -3.0 (3.2)
$x_1'$
$\sigma_{12}'$ [MPa]
STABLCOR: -0.5 (2.9)
FR-406: -5.1 (3.4)
STABLCOR: +0.4 (2.8)
FR-406: -4.6 (3.8)
STABLCOR: -1.6 (2.4)
FR-406: -1.8 (3.6)
STABLCOR: -0.5 (2.1)
FR-406: -12.3 (3.2)
STABLCOR: +0.9 (1.7)
FR-406: +5.2 (2.7)

Figure 8.9 – Average In-Plane Shear Stress After Cure for Different Substrate Configurations (FR-406 and STABLCOR)

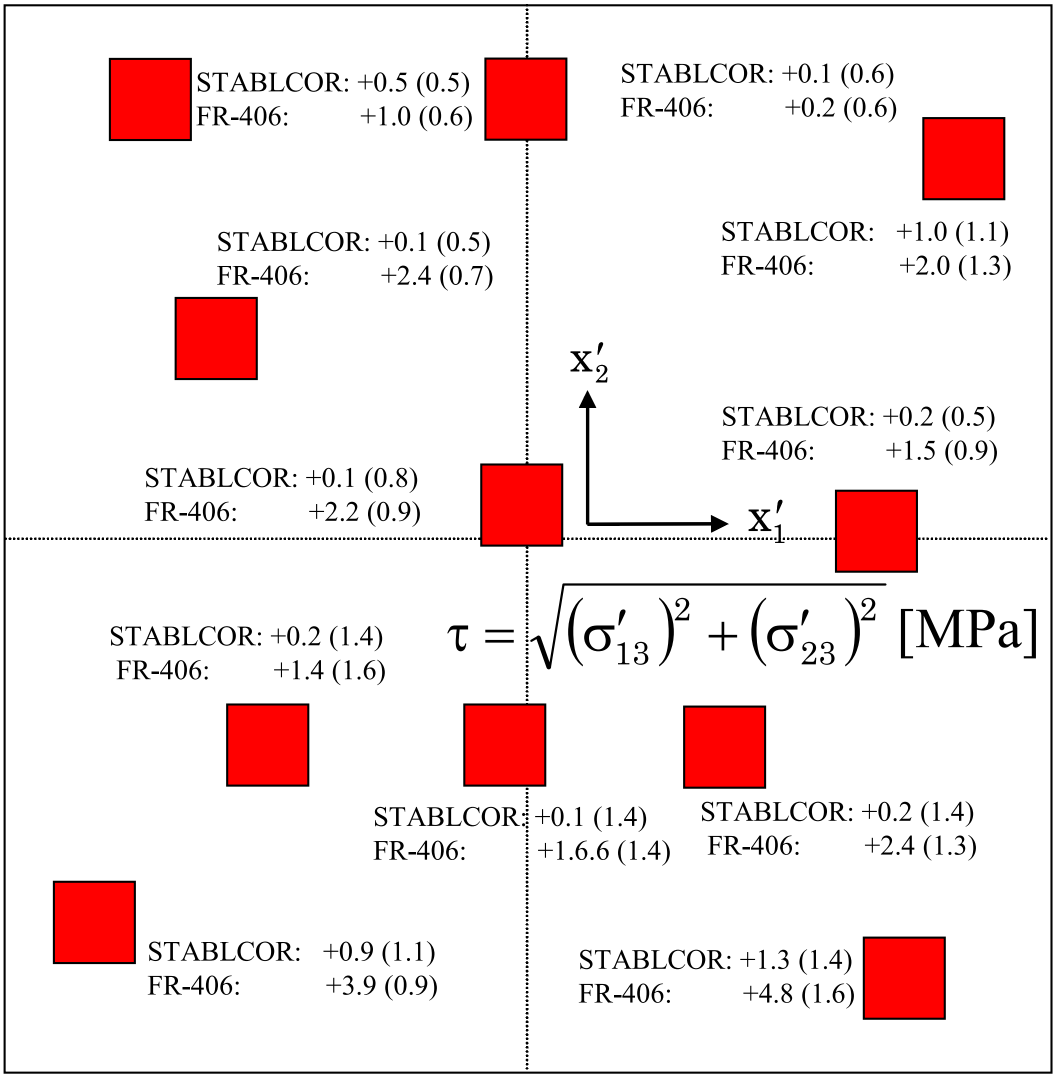

STABLCOR: +0.5 (0.5)
FR-406: +1.0 (0.6)
STABLCOR: +0.1 (0.6)
FR-406: +0.2 (0.6)
STABLCOR: +0.1 (0.5)
FR-406: +2.4 (0.7)
STABLCOR: +1.0 (1.1)
FR-406: +2.0 (1.3)
$x'_2$
STABLCOR: +0.2 (0.5)
FR-406: +1.5 (0.9)
STABLCOR: +0.1 (0.8)
FR-406: +2.2 (0.9)
$x'_1$
$\tau = \sqrt{(\sigma'_{13})^2 + (\sigma'_{23})^2}$ [MPa]
STABLCOR: +0.2 (1.4)
FR-406: +1.4 (1.6)
STABLCOR: +0.1 (1.4)
FR-406: +1.6.6 (1.4)
STABLCOR: +0.2 (1.4)
FR-406: +2.4 (1.3)
STABLCOR: +0.9 (1.1)
FR-406: +3.9 (0.9)
STABLCOR: +1.3 (1.4)
FR-406: +4.8 (1.6)

Figure 8.10 – Average Interfacial Shear Stress After Cure for Different Substrate Configurations (FR-406 and STABLCOR)

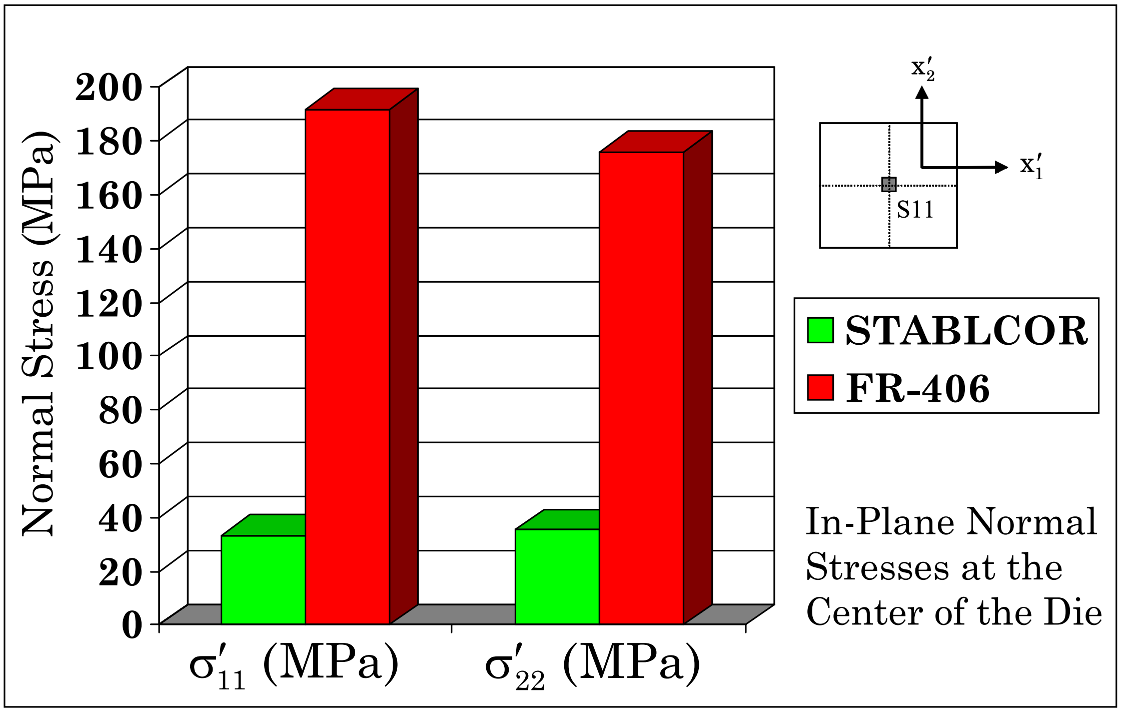


Figure 8.11 – Comparison of Average In-Plane Normal Stress for Different Substrate Configurations (FR-406 and STABLCOR)

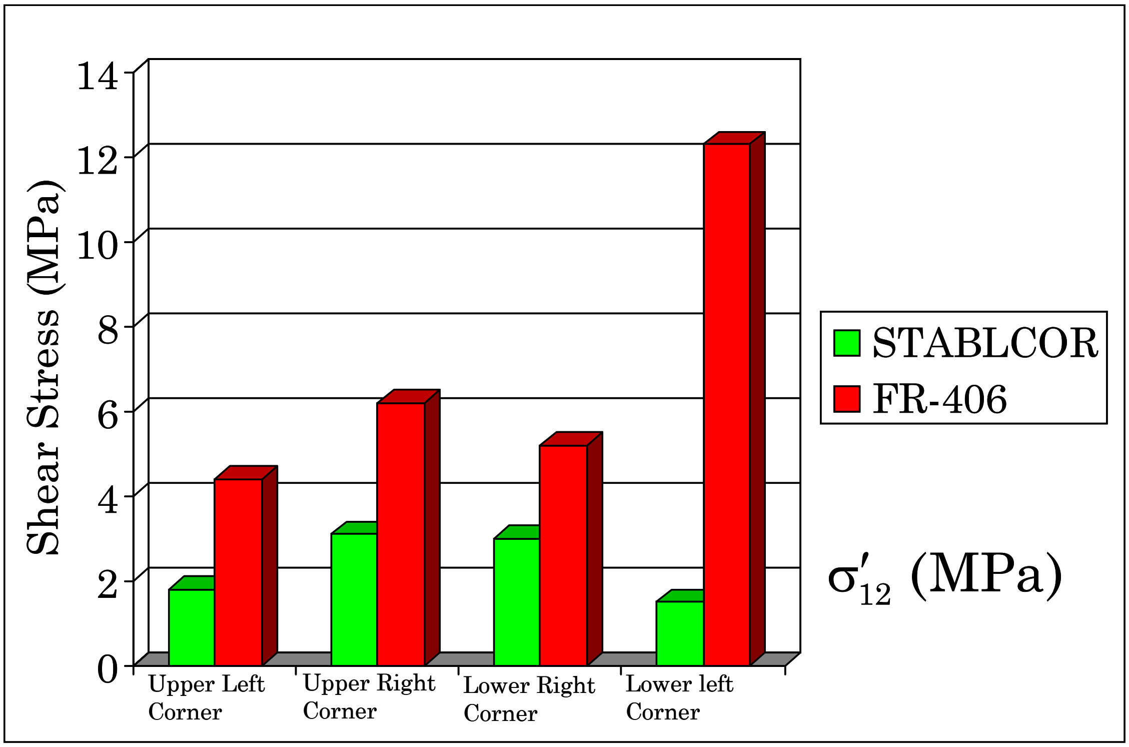


Figure 8.12 – Comparison of Average In-Plane Shear Stress for Different Substrate Configurations (FR-406 and STABLCOR)

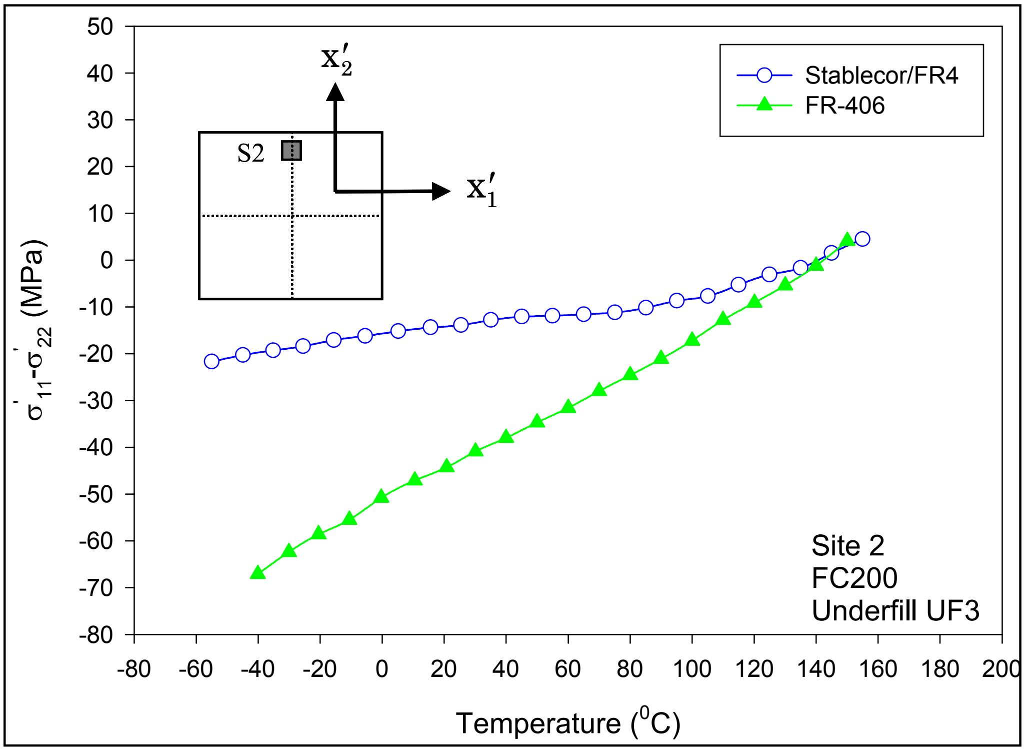


Figure 8.13 – Comparison of In-Plane Normal Stress Difference Variation with Temperature for Different Substrate Configurations (FR-406 and STABLCOR)

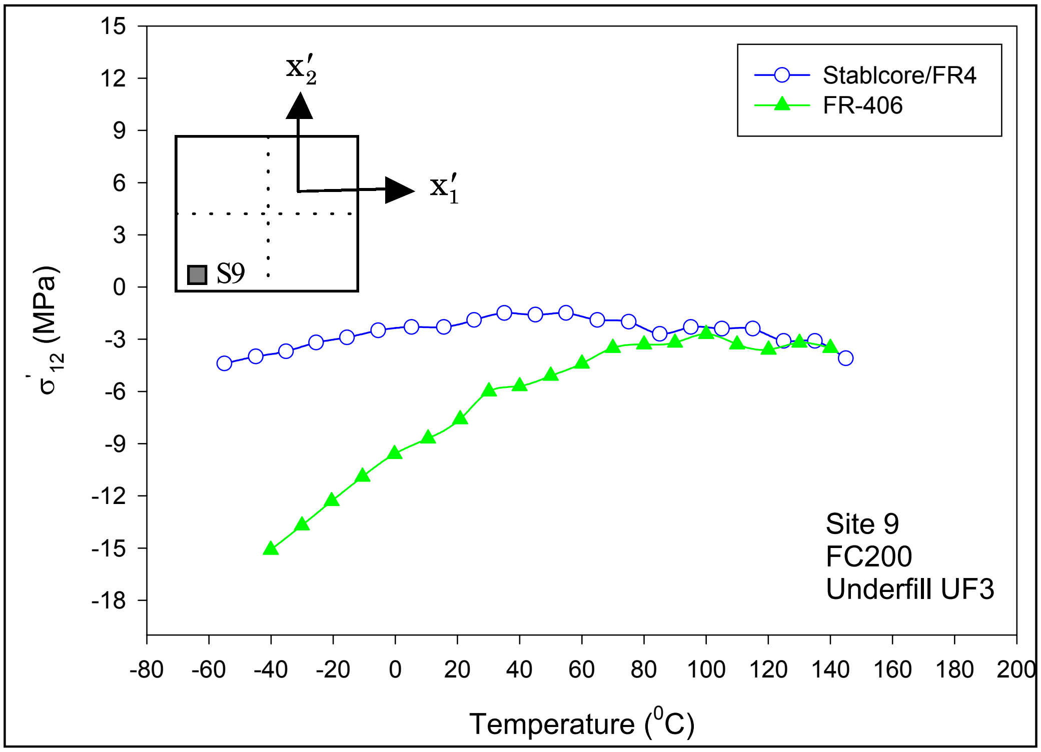


Figure 8.14 – Comparison of In-Plane Shear Stress Variation with Temperature for Different Substrate Configurations (FR-406 and STABLCOR)

(the cure temperature of the underfill) and the assembly flattens back out, the normal stress difference approached zero. Although the normal stress difference illustrated a somewhat linear response with the temperature of assembly, the in-plane shear stress values began to deviate from linearity when the temperature came near the glass transition temperature of the underfill encapsulant. This type of behavior was illustrated at all of the corner rosette sites. It is suspected that the individual normal stresses exhibit the same type of nonlinear behavior around the Tg, and that the effect is cancelled out through subtraction when the normal stress difference data is plotted. When the temperature is lowered; the stress levels continue to increase. This is because the material expansion mismatch becomes worse due to the larger temperature change from the "relaxed" configuration of the package materials at approximately 150 $^oC$. As can be seen in these figures, the die stresses can become quite high for temperatures significantly below room temperature. In addition, the advantages of the low expansion coefficient STABLCOR substrate become readily apparent.

## 8.4 Summary

In this work, Die stresses were characterized and compared for flip chip on laminate assemblies employing a novel low expansion, high stiffness, and relatively low cost laminate substrate material that virtually eliminates CTE mismatches between the silicon die and top layer PCB interconnect. The enhanced substrate is a hybrid composite laminate PCB, which features a sandwich construction that contains standard FR-406 outer layers surrounding a low expansion high thermal conductivity carbon fiber-reinforced core (STABLCOR). Measurements of the die stresses in 5 x 5 mm flip chip die attached to the low expansion laminates have been made using test chips with piezoresistive sensors. The findings of this work indicate that a significant reduction in the die normal and shear stresses magnitude occurs relative to those present in conventional FR-406 substrate assemblies.

# CHAPTER 9

# SUMMARY AND CONCLUSIONS

In this work, (111) silicon test chips containing an array of optimized piezoresistive stress sensor rosettes, have been successfully applied within flip chip packaging configurations. Calibrated and characterized (111) FC200 test chips were encapsulated in the flip chip packages and the post packaging resistances of the sensors were then recorded. The sensor resistances were monitored at room temperature, as a function of temperature excursion, and during a long term packaging reliability qualification tests (thermal cycling). The stresses on the die surface were calculated using the measured resistance changes and the appropriate theoretical equations. For comparison purpose, three-dimensional nonlinear finite element simulations of the packaging configurations were also performed, and the stress predictions were correlated with the experimental test chip data.

In the flip chip study, test chips with piezoresistive sensors have been used to measure the mechanical stresses on the silicon die device surface in flip chip on laminate assemblies. The utilized (111) silicon test chips contain an array of sensor rosettes capable measuring all of the stress components including the interfacial shear stresses. The stress chips were bumped with 200 μm (8 mil) pitch perimeter solder balls. The flip chip test die were then packaged, and die surface stresses were measured throughout the assembly process and during post-assembly environmental testing.

The observed transient stress variation during underfill cure was recorded and discussed. As noted in earlier research by the authors [142-144, 167], the majority of the final assembly stresses are developed during cooldown after the underfill snap cure oven exposure. These stresses were typically 5-10 times larger than the maximum values observed during the actual cure cycle. In addition, no stress overshoot phenomenon was observed for the device side die stresses; unlike the previous findings with the backside die stresses [142]. This supports the earlier hypothesis that die cracking and tensile stress overshoot on the backside of the assembled flip chip die are due to differential cooling during cooldown after underfill cure.

Room temperature die stresses after assembly have been evaluated and compared for three different underfills. Minimizing these device side die stresses is especially important when multiple copper/low-k interconnect redistribution layers are present. It was found that underfill UF1 exhibited the lowest in-plane compressive stress magnitudes. For the three encapsulants under study, the in-plane compressive stresses seemed to be strongly related to both the elastic modulus and coefficient of thermal expansion of the underfills. Underfill UF2 exhibited the lowest in-plane and interfacial shear stress magnitudes. Further finite element investigations using temperature dependent elastic and viscoplastic properties of the underfill materials will be necessary before the “stress rankings” of the three underfill materials can be better understood.

The in-plane shear stress distribution was found to lack the expected symmetry present for an ideal assembly where the underfill is dispensed at all locations under the die simultaneously. The data for all three underfills indicated a concentration in the shear stress at the underfill dispense corner. The stress magnitudes in this corner were 50-100% higher than the values at the other 3 corners, and delaminations were also observed to initiate at the high stress corner during thermal cycling. These results were explained by the presence of a larger fillet and slight buildup of underfill encapsulant at the dispense corner. The current efforts in characterizing underfill delaminations have indicated that the in-plane shear stress value is an excellent prognostic indicator of delamination initiation points and delamination propagation [195-196].

In the low temperature packaging study, the silicon die stresses occurring in chip on board assemblies have experimentally characterized and numerically modeled at extreme low temperatures to be found on future NASA space missions. Stress measurements have been made from -180 to +150 $^{o}$C using test chips incorporating piezoresistive sensor rosettes. The p-type resistors in the utilized test chips were found to exhibit freeze out effects at temperatures below –50 $^{o}$C, so that accurate stress measurements could only be made using the measured resistance changes exhibited by the n-type sensors. The obtained stress measurement data were then correlated with the predictions of nonlinear finite element models, and good agreement was found. The finite element models incorporated temperature dependent material property data. A microtester was used to characterize the stress-strain behavior of the solders and encapsulants from -180 to 150 $^{o}$C.

In the flip chip delamination study, a fundamental understanding of delamination initiation and growth in flip chip assemblies through simultaneous characterization of the stress and delamination states at the die to underfill interface during thermal cycling have been developed. Mechanical stresses on the device side of the flip chip die have been measured using special (111) silicon stress test chips containing piezoresistive sensor rosettes that are capable of measuring the complete three-dimensional silicon surface stress state in the silicon (including the interfacial shear and normal stresses at the die to underfill interface). The fabricated flip chip test die were assembled to FR-406 laminate substrates. Room temperature die stresses after assembly have been evaluated and compared for three different underfills. The in-plane shear stress distribution was found to lack the expected symmetry present for an ideal assembly where the underfill is dispensed at all locations under the die simultaneously. The data for all three underfills indicated a concentration in the shear stress at the underfill dispense corner. The stress magnitudes in this corner were 50-100% higher than the values at the other 3 corners, and delaminations were found to initiate at this high stress corner during thermal cycling assemblies underfilled with encapsulant UF1.

The assemblies were then subjected to 3000 thermal cycles from -40 to 125 $^{o}$C. By continuous monitoring of the sensor resistances during the environmental testing, the die surface stresses were measured throughout the post-assembly thermal cycling exposure. These measurements have been correlated with the delaminations occurring at the die passivation to underfill interface measured using C-mode Scanning Acoustic Microscopy (CSAM). Significant variations were found to occur in the magnitudes of the average stresses, even if there was no delamination in the flip chip assembly as thermal cycling proceeds. Such behavior is most likely due to a combination of several effects including changes that occur in the underfill material and adhesion properties, and the viscoplastic deformations that occur during thermal cycling.

Testing of 75 flip chip assemblies has been completed to date (1 die size x 3 underfills x 25 samples per combination). In each assembly, the complete histories of three-dimensional die surface stresses, delamination propagation have been recorded versus the duration of -40 to 125 $^{o}$C thermal cycling. One of the most important discoveries is that the shear stresses occurring at the corners of flip chip die have been demonstrated to be a suitable proxy for prognostic determination of future delamination initiations and growth. Thus, shear stress sensors have great potential as health-monitoring devices in flip chip packaging. The transient die stress variation during delamination is clearly a very complex phenomenon.

In the flip chip assembly with STABLCOR laminate configuration study, Die stresses were characterized and compared for flip chip on laminate assemblies employing a novel low expansion, high stiffness, and relatively low cost laminate substrate material that virtually eliminates CTE mismatches between the silicon die and top layer PCB interconnect. The enhanced substrate is a hybrid composite laminate PCB, which features a sandwich construction that contains standard FR-406 outer layers surrounding a low expansion high thermal conductivity carbon fiber-reinforced core (STABLCOR®). The findings of this work indicate that a significant reduction in the die normal and shear stresses magnitude occurs relative to those present in conventional FR-406 substrate assemblies.

There are several opportunities for future work on flip chip assemblies. In addition, including more realistic material properties and assumptions for interfaces of dissimilar materials will give improved FEM predictions and better correlation with the experimental data. Further investigations of the delaminations at the interface of the larger silicon die and encapsulant are also needed.

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