INVESTIGATIONS ON DAMAGE MECHANICS AND LIFE PREDICTION OF FINE-PITCH ELECTRONICS IN HARSH ENVIRONMENTS

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INVESTIGATIONS ON DAMAGE MECHANICS AND LIFE PREDICTION OF FINE-PITCH ELECTRONICS IN HARSH ENVIRONMENTS

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Mohd Nokibul Islam, son of Late Mohd Nurul Islam and Raggia Islam, was born on April 08, 1972, at Chuadanga, Bangladesh. He Graduated from Victoria Jubilee High School, Chuadanga, Bangladesh, in 1987. He attended Chuadanga Government College, Chuadanga, Bangladesh, for his Higher Secondary School Certificate Program. In 1991 he entered Bangladesh University of Engineering & Technology (BUET), Dhaka, Bangladesh and received a Bachelor of Science in Mechanical Engineering in 1996. In September, 1998, he continued his education by entering the Graduate School, Auburn University, Alabama, USA, and received his M.S in Mechanical Engineering in 2001. In 2001 he continued his education in the department of mechanical engineering at Auburn University, to pursue the degree of Doctor of Philosophy in mechanical engineering. He was married to Najrin Nahid in December 2000, and blessed by a daughter Nabeeha Islam in September 2004.

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Increased use of sensors and controls in automotive applications has resulted in significant emphasis on the deployment of electronics directly mounted on the engine and transmission. Increased shock, vibration, and higher temperatures necessitate the fundamental understanding of damage mechanisms which will be active in these environments. Electronics typical of office benign environments uses FR-4 printed circuit boards.

In this dissertation, damage mechanics and prognostication techniques for thermo-mechanical reliability of fine-pitch electronics in harsh environments have been studied. The research encompasses investigations on 63Sn37Pb, 62Sn36Pb2Ag leaded and 95.5Sn4Ag0.5Cu leadfree solder alloy systems in conjunction with high T_g metal-backed laminate assemblies. Damage relationships have been developed on plastic packages,

with predominantly NSMD pads. The focus on lead free solder alloys (95.5Sn4.0Ag0.5Cu) is motivated by legislation that mandates the banning of lead in electronics, due to environmental and health concerns.

In addition, electronic-system prognostication methodologies have been developed and demonstrated with data on leading indicators of failure for accurate assessment of product damage significantly prior to appearance of any macro-indicators of damage. The focus of prognostication techniques and models is thermo-mechanical loads typical of automotive underhood applications. The current state-of-art in managing system reliability is geared towards the development of predictive models for un-aged pristine materials. The research is targeted at need for methods and processes that will allow interrogation of complex systems and sub-systems to determine the remaining useful life prior to repair or replacement. Damage proxies have been correlated to measures of damage progression.

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CHAPTER 1

INTRODUCTION

1.1 Background of Fine Pitch Packages

One of the most fascinating, dynamic, and demanding industries in the world is the electronics industry. Creation of electronic products consists of chip design, assembly, and packaging. The electronic packaging industry is the part of the electronics industry concerned with electrical interconnection, heat removal, physical design, and structural integrity.

A major trend in the electronics industry is to make products smaller, lighter, and faster, while at the same time, to make them powerful, functional, reliable, and inexpensive. The minimization of the product size has made surface mount technology (SMT) more popular and advantageous than traditional through-hole technology. Furthermore, SMT provides better overall electrical performance relative to insertion mount components. Miniaturization continues to accelerate for portable consumer electronics. Today, cellular phones are nearly 100 times smaller in volume than they were 20 years ago. Although the pace of miniaturization has slowed down in the past few years, challenge remains as how to increase functionality. This market dynamic has accelerated the development and use of finer pitch products, both at the integrated circuit (IC) and IC package. Cellular phones, personal digital assistants (PDA), notebook PCs, digital still cameras (DSC) and MP3 players are all beneficiaries of the technologies enabling product miniaturization. The driving force in product miniaturization primarily comes from consumers who constantly seek more features and functionalities, although for lower cost. Finer geometries coupled with increased functionalities equal to finer bond pad pitch and smaller bond pad openings on the device itself. Wire bond and flip chip technologies and related processes are keeping relatively good pace in providing appropriate cost-effective interconnection between the device and IC package. However, it is where the IC package connects to the PCB that presents some of the greatest challenges. Nowhere is this challenge greater than on chip scale packages (CSP) and fine-pitch ball grid array (FBGA) packages.

With the increasing need for high interconnection density, use of fine pitch Ball Grid Array (BGA) components has become a major trend in surface mount technology. BGA packaging technology offers many advantages over more conventional fine pitch leaded surface mount components (e. g. Quad Flat Packs). These benefits include the ability to reduce component size, cost and weight; to greatly simplify manufacturing and assembly process; and to obtain higher I/O count for a given substrate area. In addition, better electrical performance can be achieved, and extension to multichip modules is easier.

1.2 Fine Pitch Packages in Harsh Environment

In the automotive under-the-hood environment, electronic packages are subjected to various types of loadings including solder joint strains caused by uneven thermal deformations of the various assembly parts due to mismatches in the coefficient of thermal expansion of the different materials, thermally induced assembly warpage, and dynamic mechanical loadings and vibration. For automotive applications, conventional leaded devices (PLCC and QFP) are less desirable as the pin count increases because of manufacturing concerns and yield loss. For this reason, PBGA packages are often considered as the best replacements for conventional leaded packages. For lead counts exceeding 200, PBGA packages offer size and manufacturability advantageous over gull-wing-leaded devices.

Eutectic 63Sn-37Pb solder is widely used due to low melting point, softness and excellent wettability. Most BGA solder joint failures can be attributed to thermal cycling induced fatigue caused by coefficient of thermal expansion (CTE) mismatch between the PBGA structure and its PCB attachment surface. Although the thermal deformations of the solder balls are often plastic (yielding has occurred), creep behavior is typically the most harmful mechanism as observed by Akay et al. [1]. Some important parameters that affect solder joint integrity are now described.

The standoff height of the solder bump can enhance its thermal cycling reliability. Standoff height depends on the size and weight of the PBGA, amount of solder paste printed during assembly, pad size, solder spheres, etc. Reduced standoff height will lead to increased shear strains in thermally cycled solder joints (Lu, et al. [2]). Increased standoff height provides better compliance and better reliability in automotive applications.

The low coefficient of thermal expansion (CTE) of the silicon die contributes greatly to the failures of the solder balls in the PBGA package as demonstrated by Wang, et al. [3]. The BT substrate actually serves as a shield between the silicon die and solder.

Thus, increases in the BT substrate thickness lead to decreases in the total inelastic strains, and hence ultimately to increases in the fatigue life of the PBGA solder joints.

The exposed copper areas on the PCB where an interconnection is to be made must be protected from the environment to prevent oxidation. This is because solder doesn't bond with oxidized copper very well and bad bonding may produce defective solder joints. Both organic and inorganic coatings are used to preserve copper solderability. Hot air solder leveling (HASL), flash gold, immersion gold, immersion silver, nickel, palladium, and palladium-nickel have been used successfully as inorganic coatings and OSP as organic coatings by the electronics industry.

There are two soldermask design strategies that are commonly used with PBGAs are referred to as solder mask defined (SMD) and non-solder mask defined (NSMD). Each design has advantages and disadvantages in use. Pad size is typically better defined with SMD pads. This is because soldermask size definition is typically better than copper pad definition; as copper depends on etch control while the soldermask is photo imaged. Another important advantage of SMD is that the larger copper pad enhances the copper adhesion to the epoxy/glass laminate surface. One main disadvantage of SMD is the sharp edges formed in the solder balls where stress concentrations can occur during thermal cycling as shown by Mawer, et al. [4]. With NSMD pads, HASL surface finish with better uniformity and coverage can usually be achieved.

Underfill is a glass-filled epoxy material that can be used to fill the air gaps around the solder balls and between the BT substrate and the PCB. In non-underfilled PBGAs solder joint is the only material connecting the BT substrate to the PCB. Use of underfill can help reduce thermal fatigue failures by lowering the shearing deformations in the solder joints. The most significant properties of underfill materials are CTE and elastic modulus (stiffness).

Several methodologies are employed in testing electronic packages depending on the characteristics of the package being evaluated. Many of the tests with accelerated stress conditions are designed to qualify electronic packages for application in practical environments. Thermal cycling is one of the standard methods for accelerated testing, and it is used for packages exposed to different temperatures during application. The test vehicles are designed to reflect the fabrication and process limits of a given technology. Typical industry requirements for components used in under-the-hood automotive controllers include the ability to survive over 2500 thermal cycles from -40 to 125 ^{o}C (study has been done at CAVE, Auburn University).

In this work, the solder joint reliability of several PBGA packages has been evaluated in the automotive thermal cycling environment. Various methods of enhancing reliability have been explored including increased BT substrate thickness, the utilization of NSMD pads on the BGA component, alternative PCB plating finishes, and the use of underfill encapsulants. A set of test boards was assembled with several 15, 17, 23, and 27 mm body size BGA components from two different vendors. In addition to non-underfilled parts, the enhancements achieved with four different underfill encapsulants have been explored. The assembled test vehicles have been subjected to over 6000 thermal cycles in the range of –40 to 125 ^{o}C, and the daisy-chain resistances of the various components were monitored throughout the testing. Logged failures have been statistically analyzed using two parameter Weibull models. The analysis results have allowed the board level reliabilities of the examined BGA components to be compared and ranked, and the reliability enhancements achieved with various underfills to be accessed. Detailed failure analyses have also been performed to find the locations of solder joint fatigue crack growth, and to identify other failure modes occurring in underfilled parts.

1.3 Models for Fine Pitch Packages Reliability in Harsh Environment

Fine-pitch ball grid array (BGA) and underfills have been used in benign office environments and wireless applications for a number of years, however their reliability in automotive underhood environment is not well understood. In this study, the reliability of fine-pitch plastic ball grid array (PBGA) packages has been evaluated in the automotive underhood environment. Experimental studies indicate that the coefficient of thermal expansion (CTE) as measured by thermo mechanical analyzer (TMA) typically starts to change at 10-15°C lower temperature than the T_g specified by differential scanning calorimetry (DSC) potentially extending the change in CTE well into the accelerated test envelope in the neighborhood of 125°C. High T_g substrates with glass-transition temperatures much higher than the 125°C high temperature limit are therefore not subject to the effect of high coefficient of thermal expansion close to the high temperature of the accelerated test. Darveaux's damage relationships [5-7] were derived on ceramic ball grid array (CBGA) assemblies, with predominantly solder mask defined (SMD) pads and 62Sn36Pb2Ag solder. In addition to significant differences in the crack propagation paths for the two pad constructions, SMD pads fail significantly faster than the non solder mask defined (NSMD) pads in thermal fatigue. The thermal mismatch on CBGA's is much larger than PBGA assemblies. Crack propagation in CBGA's is often observed predominantly on the package side as opposed to both package and board side for PBGAs. In the present study, crack propagation data has been acquired on assemblies with 15 mm, 17 mm, and 23 mm size plastic BGAs with NSMD pads and 63Sn37Pb on high-T_g printed circuit boards. The data has been benchmarked against Darveaux's data on CBGA assemblies. Experimental matrix also encompasses the effect of bis-maleimide triazine (BT) substrate thickness on reliability. Damage constants have been developed and compared against existing Darveaux Constants. Prediction error has been quantified for both sets of constants.

1.4 Damage Mechanics on Metal-Backed Substrates in Harsh Environments

Electronic modules for harsh environment applications face challenging issues for future designs. These modules must adapt to the shrinking packaging envelopes while managing higher power dissipation due to increased feature content and higher processor clock frequencies. For automotive electronic controllers, these issues are often compounded with higher ambient operating temperatures. In addition, the high-volume, low-cost issues facing automotive electronics manufacturers provide added burden for system designers.

The research described herein investigates the use of metal-backed organic laminate substrate technology to provide a reliable low-cost solution for high-temperature powertrain vehicle electronics. In particular, the research investigates the thermal performance and solders joint reliability of metal-backed PCBs intended for next generation powertrain products. This research also investigates the potential for substrate delamination, as well as the impact of conformal coating on component reliability.

In this study, the effect of metal-backed boards on the interconnect reliability has been evaluated. Previous studies on electronic reliability for automotive environments have addressed the damage mechanics of solder joints in plastic ball-grid arrays on non-metal backed substrates [4, 8-10] and ceramic BGAs on non-metal backed substrates [5-7]. Other failure mechanisms investigated include – delamination of PCB from metal backing.

Increased use of sensors and controls in automotive applications has resulted in significant emphasis on the deployment of electronics directly mounted on the engine and transmission. Increased shock, vibration, and higher temperatures necessitate the fundamental understanding of damage mechanisms which will be active in these environments. Electronics typical of office benign environments uses FR-4 printed circuit boards. Automotive application typically use high glass-transition temperature laminates such as FR4-06 glass/epoxy laminate material (T_g = 164.9°C in this study, but some of the cases T_g varies between 140 to 170^oC). In application environments, metal-backing of printed circuits boards is being targeted for thermal dissipation, mechanical stability and interconnections reliability.

The test vehicle is a metal backed FR4-06 laminate. The printed circuit board has an aluminum metal backing, attached with pressure sensitive adhesive (PSA). Component architectures tested include – plastic ball grid array devices, C2BGA devices, QFN, and discrete resistors. Reliability of the component architectures has been evaluated for HASL.

Crack propagation and intermetallic thickness data has been acquired as a function of cycle count. Reliability data has been acquired on all these architectures. Material constitutive behavior of PSA has been measured using uni-axial test samples. The measured constitutive behavior has been incorporated into non-linear finite element simulations. Predictive models have been developed for the dominant failure mechanisms for all the component architectures tested.

1.5 Impact of Modeling Methodology on Accelerated Life Correlation of Thermal Fatigue Component Failures

In recent years there are so many solder (Sn63/Pb37) fatigue life prediction models for thermal cycle conditions have been developed. Few publications have reported the impact of modeling methodology on accuracy of predicted life. Generally in the BGA, the highest strain solder ball is used for estimation of solder fatigue life. The peak plastic work levels predicted in finite element analysis usually depend on mesh density, due to singular points in the model. Convergence, and error estimation of field quantity (plastic work) with the mesh discretization has been analyzed. To compensate the mesh density effect, a volume averaging technique is used to average the results over the damage volume elements. Selection of the damage volume plays a very significant role for solder fatigue life prediction. The optimal damage volume of the solder is the choice of few elements selected from the highest strain solder ball. The number of elements and the thickness of the elements are very important in calculating the damage volume.

The main objective of this study is to find an optimal damage volume for estimation of solder joint fatigue life under thermal cycle conditions. In this study the damage volume has been optimized by different types of BGA packages from different vendors. The amount of strain energy induced per thermal cycle is calculated to measure the damage of the material. A correlation between the simulated strain energy density and experimentally tested 1% solder joint reliability results in an empirical equation. The accuracy of each type of damage volume has been defined by the accuracy of the fitting

(R-square) value. An accurate empirical relationship has been built for the optimal damage volume. Finally the empirical model constants for different damage volumes have been normalized with the previous study model constant

1.6 Prognostication of Electronics and MEMS Packaging

The capability of determination of material or system state is called “prognosis”. Prognostics methodologies can be very valuable in development of field-life correlations and derivation of acceleration transforms. A scarce understanding of damage in field environments stems from limitations on quantification of prior stress histories for products. Most analytical tools, address damage estimation for known stress histories imposed on pristine materials. The field environment is often complicated and random based on usage profile and ambient environment. In absence of macro-indicators of damage, there are no means for evaluation of percentage useful life consumed or estimation of the residual life for electronics subjected to unknown prior stress histories.

In this work, a methodology for prognosis-of-electronics has been demonstrated with data of leading indicators of failure for accurate assessment of product damage significantly prior to appearance of any macro-indicators of damage. Proxies for leading indicators of failure have been developed including – micro-structural evolution characterized by average phase size and intermetallic growth rate in solder (leaded and lead free) interconnects. Structures examined include – electronics package, MEMS packages and interconnections on a metal backed printed circuit board typical of electronics deployed in harsh environments. Since, an aged material knows its state the research presented in this paper focuses on enhancing the understanding of material damage to facilitate proper interrogation of material state. Mathematical relationship has been developed between phase growth rate and time-to-1-percent failure to enable the computation of damage manifested and a forward estimate of residual life.

1.7 Reliability of Lead Free Electronics

The tin–lead (Sn–Pb) solder alloy has been widely used as interconnection material in electronic packaging due to its low melting temperatures and good wetting behavior on several substrates such as Cu, Ag, Pd and Au. Legislation that mandates the banning of lead in electronics for environmental and health concerns has been actively pursued in several countries during the past 15 years. Although the covered products and implementation deadlines continue to evolve, it is clear that laws requiring conversion to lead-free electronics are becoming a reality. Other factors that are affecting the push towards the elimination of lead in electronics are the market differentiation and advantage being realized by companies producing so-called "green" products that are lead-free. A large number of research studies have been performed and are currently underway in the lead-free solder area. Detailed reports on multi-year studies have been published by the National Center for Manufacturing Sciences (NCMS) and the National Electronics Manufacturing Initiative (NEMI), as well as other consortia. Although no "drop in" replacement has been identified for all applications; Sn-Ag, Sn-Ag-Cu (SAC), and other alloys involving elements such as Sn, Ag, Cu, Bi, In, and Zn have been identified as promising replacements for standard 63Sn/37Pb eutectic solder.

The electronic industry is making substantial progress toward a full transition to Pb-free soldering in the near future. At present, the leading candidate Pb-free solders are near-ternary eutectic Sn-Ag-Cu alloys. The electronic industry has begun to study both the processing behaviors and the thermo-mechanical fatigue properties of these alloys in detail in order to understand their applicability in context of current electronic card reliability requirements. In the present study, thermal fatigue behavior of PBGA and Chip resistors solder joints was investigated in thermal cycling conditions. Extensive failure analysis was conducted with thermal-cycled solder joints to understand the failure mechanisms operating during the accelerated thermal cycling (ATC) tests. Prognostication study has also been carried out for Sn-Ag-Cu solder alloys.

CHAPTER 2

LITERATURE REVIEW

Since its origin in the 1960's within the aerospace and defense industries, surface mount technology (SMT) has become the defacto standard in the electronics industry. In older generations of automotive electronics based on surface mount technology and laminated substrates; packaging of microprocessor and ASIC chips was typically performed using Quad Flat Packs (QFPs) and Plastic Leaded Chip Carriers (PLCCs). With their superior packaging densities, circuit performance, automation efficiency, and assembly costs, Plastic Ball Grid Array (PBGA) components have become desirable for use in automotive powertrain (engine and transmission) controllers modules.

To determine the reliability of fine pitch packages for the automotive industry, thermal cycle testing is often performed from -40 to 125 ^{o}C. When a mounted fine pitch package goes through thermal cycling, the differential expansions of silicon die and package substrate results in stresses and strains on the solder joints. The repetitions of these thermal excursions can lead to fatigue failure of the fine pitch package solder balls.

Increase in pin counts past 160, have made Plastic Ball Grid Array (PBGA) components more desirable for use in automotive powertrain (engine and transmission) controller modules. Such modules are exposed to the under-hood environment, and typical reliability specifications include the ability to survive a certain number of –40 to

125 °C thermal cycles (e.g. 2000 cycles with no failure, or 2500 cycles with less than 1% failure rate).

In an early investigation by Lindley [14], it was suggested that PBGA packages would fail to meet the reliability requirements for use in the automotive environment. However, -40 to 125 ^{o}C thermal cycling tests performed recently by several investigators [4, 9] have demonstrated the properly designed larger BGAs (e.g. 23, 27, and 35 mm body sizes) can be robust performers and meet the solder joint reliability design requirements for under-hood controllers. Syed [9] tested 23 mm components, and examined several parameters including BT substrate thickness, solder pad size, perimeter vs. full arrays, and solder ball pitch, and found that BGAs with perimeter arrays and thicker (0.76 mm) BT substrates could comfortably satisfy automotive reliability specifications. Mawer, et al. [4] examined several 23 and 27 mm BGA configurations, and found that most satisfied automotive reliability requirements. Most of their work focused on 27 mm BGA parts with a .56 mm BT substrate thickness, 1.27 mm ball pitch, and Solder Mask Defined (SMD) pads. In a limited number of exploratory experiments, they demonstrated that improved reliability could be realized with Non Solder Mask Defined (NSMD) pads on the BT substrate, and that a more fine pitch 17 mm BGA could also meet most automotive requirements, although with minimal margin.

Evans, Newberry, Bosley, and coworkers [10] at DaimlerChrysler Huntsville Electronics (DCHE), made the first production use of a PBGA in the under-hood environment. In that application, a large Multichip Module (MCM) BGA was utilized as the digital core of a transmission controller. As that product evolved to incorporate additional features, the need for smaller single-chip BGAs became apparent.

Transition to smaller BGAs and Chip Scale Package (CSP) technology is desirable in future under-hood controllers to aid in product footprint miniaturization, weight savings, and cost reduction. However, such components pose several reliability concerns in the harsh automotive environment. In some applications thin packages are required to make the product small in size (e.g. cellular phones). In those cases, polyimide tape is often used as the BGA substrate to reduce the overall package size. Thompson, et al. [15] observed that a thin polyimide tape substrate provided better reliability than a BT resin substrate. Several investigations have also showed that solder pad size plays a big role in solder joint reliability. Yee, et al. [16] observed the influence of pad geometry on BGA solder joint reliability. Amagai, et al. [17] presented the effect of the copper core size on the response of the viscoplastic deformation in the PBGA. Mercado, et al. [18] found that the effect of pad size is so significant that will override the effect of substrate thickness, especially in flip chip PBGA packages. Moreover, larger solder pads enhance BGA life significantly due to better adhesion with the solder. In particular, reduced solder joint fatigue life is known to occur in smaller body size BGAs due to their smaller ball size and pitch, reduced standoff (solder ball height), and the closer proximity of the perimeter (signal) solder balls to the edge of the semiconductor die. Solder joint geometry is also an important parameter for thermal fatigue life.

The bare copper interconnection pads on a PCB need to be protected from the environment to prevent oxidation, which causes poor adhesion with the solder, and hence reduces solder joint life. Both organic and inorganic coatings are used to preserve copper solderability. Two common methods to preserve copper solderability in use in the electronics industry are Palladium plating, and Hot air solder leveling (HASL) using Sn-

Pb solder. Palladium plating is used only in special cases, and is not widespread as HASL. However, the electroless palladium finish can meet some of the challenging feature size specifications required of today's high-density SMT printed circuit boards. HASL finish PCB boards yield very good reliability as demonstrated by Langan, et al. [19]. In another investigation, Bradley, et al. [20] examined the solderability of Organic Protective Coatings (OPC) and various metallic plating chemistries as alternatives to traditional HASL. Several experiments showed that OPC resulted in better reliability than HASL.

Enhancements of BGA solder joint reliability by using underfill encapsulants have been previously explored by Young [21], and Burnette, et al. [22-23]. It has been shown experimentally through thermal cycling tests that significant increases in solder joint reliability can be obtained in large CBGA, PBGA, and Super-BGA components using properly selected underfills [21-23]. In addition, underfill also greatly enhanced the measured thermal cycling board level reliability of smaller flexBGAs (12 and 16 mm body sizes) [23]. However, the finite element predictions (3D slice approach) performed by Burnette and co-workers [22-23] gave results that contradicted the measured thermal cycling data (e.g. the non-underfilled parts were predicted to be more reliable than some of the underfilled parts). Such results were also predicted by Pyland, et al. [24] using two-dimensional finite element models. In their work, it was suggested that underfills with certain mechanical and thermal expansion properties would actually decrease the solder joint reliability of the studied SuperBGA components.

Thermal fatigue life prediction of fine pitch packages is a major concern for the electronic packaging industry which has driven research efforts to develop effective models that are capable of predicting failure initiation and propagation under thermal fatigue loads. Typically, the reliability problem has been approached using a combination of experimental measurements and numerical simulation.

In under-hood environments, solder joints failure modes depends on several factors. In most cases, failures occur as crack initiations followed by propagation through the bulk of the solder joint. Experimental progressive crack growth measurements are conducted by slicing the fine pitch packages at some particular level of cycling for crack initiation and speed of propagation in solder joints. Both primary and secondary crack growth data has been captured in the solder joints. Numerical simulation models were created for the packages used in experimental measurements and loaded with thermal loads similar to those applied experimentally. Finally, failure prediction models were developed by correlating experimental measurements with numerical simulation. The inelastic behavior of solder is captured in ANSYS using Anand's constitutive model [25]. The modeling methodology utilizes finite element analysis to calculate the viscoplastic strain energy density accumulated per cycle during thermal or power cycling. The strain energy density is then utilized with crack growth data to calculate the number of cycles to initiate a crack, and the number of cycles for the crack to propagate across a solder joints diameter.

Several finite element based analysis methodologies have been proposed which predict solder joint fatigue life (e.g. Engelmaier [26]; Shine and Fox [27]; Wong et al. [28]; Yamada [29]; Subrahmanyan et al. [30]; Dasgupta et al. [31]; Pao [32]; Clech et al. [33]; Syed [34]; Darveaux et al. [6]; and Darveaux [7]). It should be noted that there is a material limitation inherent to many of these methodologies since they assume the utilization of eutectic 63Sn/37Pb solder or some similar combination of solder materials (i.e. 62Sn/36Pb/2Ag). Darveaux's damage relationships [5-7] were derived on ceramic ball grid array (CBGA) assemblies, with predominantly solder mask defined (SMD) pads and 62Sn36Pb2Ag solder. It is a strain energy based approach, where the work term consists of time-dependent creep and time independent plasticity. In addition to significant differences in the crack propagation paths for the two pad constructions, SMD pads fail significantly faster than the non solder mask defined (NSMD) pads in thermal fatigue. The thermal mismatch on CBGA's is much larger than PBGA assemblies. Crack propagation in CBGA's is often observed predominantly on the package side as opposed to both package and board side for PBGAs.

Increasing automotive engine controller functionality, plus smaller and hotter engine compartment are placing greater demands on the thermal design of engine control modules. The traditional method of adding the heat sinks with the component (e.g. transistors) on the printed circuit board (PCB) is very costly and provides significant thermal resistance to the surroundings. The thermal requirements have been met with improved heat-sink design, and thermal attachment materials promoting thermal conductivity between the electronics and the module casing. Traditional module using double sided reflowed components and thermally conductive pads to thermally connect the substrate and the metal housing. This design increases the material cost of the module by adding the thermal enhancing material and creates an added manufacturing process for attaching the thermal pad to the housing. While this design meets the thermal and reliability requirements for the module, the system design is not optimal.

Metal-backed substrates are attractive alternative from the thermal point of view. An alternative to the previous design involves, structurally attaching the metal directly to the substrate providing a direct thermal path. This design has the added advantage of allowing the metal to act as a module "cover" and employs a single-path manufacturing process. Utilizing this design significantly reduces the module system cost, and improves product quality by limiting the assembly to single-pass reflow exposure. However, attaching the metal directly to the substrate (FR-4) increases the assembly's effective coefficient of thermal expansion (CTE).

Metal backed printed circuit board's disadvantage of high coefficient of thermal expansion relative to bare FR4-06, leads to increased susceptibility to solder joint fatigue failure due to thermal cycling. Some research in this field has been done at CAVE. The focus of this research is to evaluate the system-level issues related to metal-backed substrate interconnections reliability, damage mechanism, provide modeling techniques to further investigate design alternatives, reliability prediction, and to provide recommendations to automotive system designers. In this work, the effect of metal-backed boards on the interconnect reliabilities are evaluated.

During the soldering process when solder is in the molten stage, the formation of intermetallic compounds between tin-based solders and substrates is inevitable and then it continues to grow during solid-state aging. Intermetallic growth was monitored as a function of cycle count. Intermetallic growth, which generally starts right after the solder reflow, is fairly thin prior to thermal fatigue damage. Studies on intermetallic growth of Cu-Sn compounds [35-37] showed that two types of intermetallic compounds are generated namely Cu_3Sn on the copper pad side and Cu_6Sn_5 on the eutectic solder side.

The metal backed samples in this study exhibited formation of thicker intermetallic layers. The loss of Sn resulting from its diffusion with Cu results in further localized coarsening of the eutectic solder microstructure where Pb-rich regions are observed adjacent to the Cu_6Sn_5 intermetallic layer.

The peak plastic work levels predicted in finite element analysis usually depend on mesh density, due to singular points in the model. To compensate the mesh density effect, a volume averaging technique is used to average the results over the damage volume elements. Selection of the damage volume plays a very significant role for solder fatigue life prediction in electronic packaging filed. The optimal damage volume of the solder is the choice of few elements selected from the highest strain solder ball. The number of elements and the thickness of the elements are very important in calculating the damage volume.

Generally the simplification of the 2D plane and 3D slice model gives inaccurate behavior [38]. In some cases it is sufficient to study the trends of the packages with the simplified material properties. To study the actual behavior of the packages, 3D model with fine mesh and accurate materials nonlinearity must include in the modeling. Wong [39] reported that predicted finite element strains or stress are heavily dependent on finite element mesh size as well as the geometry of the packages. The smaller the element size, the higher the result strains. The finite element mesh size dependency is primarily due to stress/strain singularity at the edge of bi-materials [40-43]. Hence, the calculated strain energy density increases as the number of element in the solder joint decreases. Kay et al. [44] reported that the stress singularity can be overcome by local elements (very fine mesh) with the global elements (very coarse mesh) by submodeling approach. Syed [45] studied the substructuring technique to overcome the stress singularity issue in the model. The negative effect of stress singularities in the simulation are reported by Stock et al. [46]. He investigated the effect of different level of mesh refinement for damage accumulation. To compensate the mesh refinement effect, a volume averaging technique [41] is used to compute the average results over the damage volume elements. Now these days' researchers [7, 48-49] have been using this technique to minimize the mesh dependency effect in finite element results.

The current state-of-art in managing system reliability is geared towards the development of life-prediction models for un-aged pristine materials under known loading conditions based on relationships such as the Paris's Power Law [11-12], Coffin-Manson Relationship [13] and the S-N Diagram. There is need for methods and processes that will allow interrogation of complex systems and sub-systems to determine the remaining useful life prior to repair or replacement. This capability of determination of material or system state is called "prognosis". There is scarcity of methodologies which enable determination of damage state, when the prior stress histories are not accurately known or quantified. Leading indicators-of-failure, which enable interrogation of material state and determination of residual life, can provide a framework for successful prognostication and health monitoring of electronic systems.

The solder microstructure and the growth of intermetallic due to thermal fatigue has been reported previously by several researchers. Morris, Jr., et al. [35] reported that the thermal fatigue of Sn63/Pb37 solder was characterized by microstructural coarsening in the fatigue damaged region. Pang et al. [50] reported that the microstructural and intermetallic development due to thermal cycling aging had a major impact on the fatigue strength of solder joint. Solder joint fatigue life degrades with microstructure changes during thermal aging. Frear, et al. [51] analytically studied the microstructural evolution of solder and suggested that solder grain size could be used as an important parameter for thermal fatigue life prediction. Sayama, et al. [52] examined the changes in microstructure occurring in the Sn63/Pb37 chip resistor solder joints during thermal cycling. In previous studies, the use of phase growth as the evolution parameter for thermal fatigue life time of solder joint has been investigated. A power law relation has also been investigated between the number of cycles to crack initiation and the average increase in the α-Pb phase growth parameter. Frear, et. al. [53] reported that microstructure of solder changes under thermo-mechanical fatigue. Frear, et al. [51] analytically studied the microstructural evolution of solder and suggested that solder grain size could be used as an important parameter for thermal fatigue life prediction. Bangs and Beal [54], Wolverton [55], and Tribula, et al. [56] have shown that during thermal fatigue of eutectic and high lead solders grain coarsening happened and the fatigue failure initiates in the coarsened region. The grain growth rate (per unit time) is found to increase with increasing strain rate. Callister [57] found that after recrystallization is complete, the strain-free phases will continue to grow if the metal specimen is stored at an elevated temperature. The process of the particle growth induced by volume diffusion was theoretically analyzed by Lifshitz, et al. [58]. Ardell [59] and Speight [60] studied independently and proposed a phase diffusion theory, which states that when phase boundary diffusion dominates, then average phase size to the fourth power increases proportional to time. Senkov and Myshlev [61] extended the theory the phase growth process of a superplastic alloy and validated the theory in that of Zn/Al eutectic alloy.

Legislation that mandates the banning of lead in electronics for environmental and health concerns has been actively pursued in several countries during the past 15 years. Although the covered products and implementation deadlines continue to evolve, it is clear that laws requiring conversion to lead-free electronics are becoming a reality. Other factors that are affecting the push towards the elimination of lead in electronics are the market differentiation and advantage being realized by companies producing so-called “green” products that are lead-free.

Lead-free solders have received a lot of attention recently. Detailed multi-year studies have been published by the National Center for Manufacturing Sciences (NCMS) and the National Electronics Manufacturing Initiative (NEMI), as well as other consortia. There have been many reports that solder joint reliability can actually be increased for a given application by using a lead-free replacement alloy such as of Sn-Ag-Cu instead of conventional Sn-Pb. However, this conclusion is not universal, and the degree of reliability improvement/degradation is package/design and environment dependent. In thermal cycling environments, Sn-Ag-Cu alloys appear to often outperform Sn-Pb when used in solder joints in more compliant package-board assemblies such as with leaded components (e.g. QFPs) and Plastic Ball Grid Array (PBGA) applications. However, for very stiff components with high CTE mismatch with the substrate (e.g. CBGA on FR-4, and non-underfilled flip chip on laminate), the solder joint reliability is typically poorer for lead-free Sn-Ag-Cu alloys in thermal cycling tests with large swings between the temperature extremes [62-63]. The reliability of Sn-Ag-Cu solder joints has been a major research in electronic industry and a number of researchers have published data showing Sn-Ag-Cu performs better or worse than Sn-Pb solder, depending on the components tested and test conditions. Bartelo et al. [64] reported that thermo-mechanical fatigue behavior of Sn-3.8Ag-0.7Cu is much more sensitive to the choice of ATC temperature range and peak test temperature than eutectic Sn-Pb solder. He found that the peak temperature is a critical factor in reducing the fatigue life of Sn-3.8Ag-0.7Cu for a given temperature range.

Recently, a number of papers have been published on the constitutive equation for creep deformation for Sn-Ag-Cu alloy for different compositions. Wiese et al [65] studied the creep behavior of bulk, PCB sample, and Flip Chip solder joint samples of Sn-4.0Ag-0.5Cu solder and identified two mechanisms for steady state creep deformation for the bulk and PCB samples. They attributed these to climb controlled (low stress) and combined glide/climb (high stress) behavior and represented steady state creep behavior using double power law model. Schubert et al [63] combined data from various sources and from their own testing on different compositions of Sn-Ag-Cu solder (Sn-3.8Ag-0.7Cu, Sn-3.5Ag-0.75Cu, Sn-3.5Ag-0.5Cu, and Castin™). They also identified two regions for stress-strain rate behavior like Wiese et al., but claimed the high stress region as power law break-down region, and chose hyperbolic sine function to represent creep data. Zhang et al [66] studied on single lap shear specimen of Sn-3.9Ag-0.6Cu solder alloy. They generated data on the test results and modeled the steady state creep behavior using hyperbolic sine function claiming power law break-down at high values of stress. Similar study has been done by Morris et al [67], using double power law constitutive model to represent creep data on single lap shear specimens of Sn-3.0Ag-0.5Cu solder joints. A rate-dependent plasticity and the strength of solders with a variety of plating materials such as Cu, Ni, were characterized for lead-free solders by Amagai [68]. Similar type of study for leaded and lead free solder viscoplastic constitutive model (Anands Model) has been carried out by Wang et al. [69]. Zhang et al. [70] found the total creep is composed of primary (transient) creep, which can be observed at low stress level, and secondary steady-state creep normally occurred at high stress for lead free solder. They recommended to include both primary and secondary creep in the constitutive model.

The mechanical properties of lead free solder are highly dependent on temperature and strain rates. John et al. [71] found that mechanical properties of Sn-3.8Ag-0.7Cu solder alloy will decrease with an increase in temperature and with lower strain rate. He investigated both the microstructure and mechanical properties for 95.5Sn-3.8Ag-0.7Cu bulk solders. Sayama, et al. [72] has recently examined the changes in microstructure occurring in Sn-Ag-Cu solder joints during thermal cycling. A power law relation was established between the number of cycles to crack initiation and the average increase in the Ag-Sn phase growth parameter. Dutta et. al. [73] investigated the dislocation creep model incorporating the effect of in-situ second phase particle coarsening applicable to lead-free solder alloys is presented. It is shown that dispersed intermetallic particles in Sn-based lead-free solders may undergo substantial strain-enhanced as well as static coarsening, and are subject to a commensurately increasing creep rate during thermo-mechanical cycling.

The solder joints, especially the Sn-Ag-Cu joints, have higher tendencies to break at the interface due to the formation of brittle intermetallic layer in the impact test than the shear test investigated by Date et al [74]. As a consequence of aging, they found that the properties of the solder changes from ductile-to-brittle transitions. The growth of intermetallic also depends on the PCB plating. Lee et al. [75] investigated the growth of intermetallic on OSP and Au/Ni plating condition. He noticed that the thickness of intermetallics in Au/Ni plating varies a lot while OSP plating has a consistent intermetallic thickness. Peng et al. [76] reported that increase in solder volume and the UBM size can enhance the solder bump strength by suppressing the effect of intermetallic compound growth rate.

CHAPTER 3

RELIABILITY OF SMALL BGAs IN THE AUTOMOTIVE ENVIRONMENT

3.1 Introduction

Earlier, thermal cycle testing of both 23 and 27 mm body size BGAs revealed that both packages exceeded the reliability requirements specified for under-hood packaging technology. In later DCHE production implementations, such components have been successfully utilized, as illustrated in the current generation automotive controller module board pictured in Figure 3.1.

Transition to smaller BGAs and Chip Scale Package (CSP) technology is desirable in future under-hood controllers to aid in product footprint miniaturization, weight savings, and cost reduction. However, such components pose several reliability concerns in the harsh automotive thermal cycling environment. In particular, reduced solder joint fatigue life is known to occur relative to larger BGAs due to their smaller ball size and pitch, reduced standoff (solder ball height), and the closer proximity of the perimeter (signal) solder balls to the edge of the semiconductor die. In addition, future automotive electronics product designs will face additional constraints in terms of poor mounting orientations, reduced airflows, and increased ambient temperatures. Thus, it is likely that design and/or assembly modifications will be necessary to achieve adequate thermal cycling reliability when using small BGAs (e.g. 15 and 17 mm body sizes) in automotive controller modules.

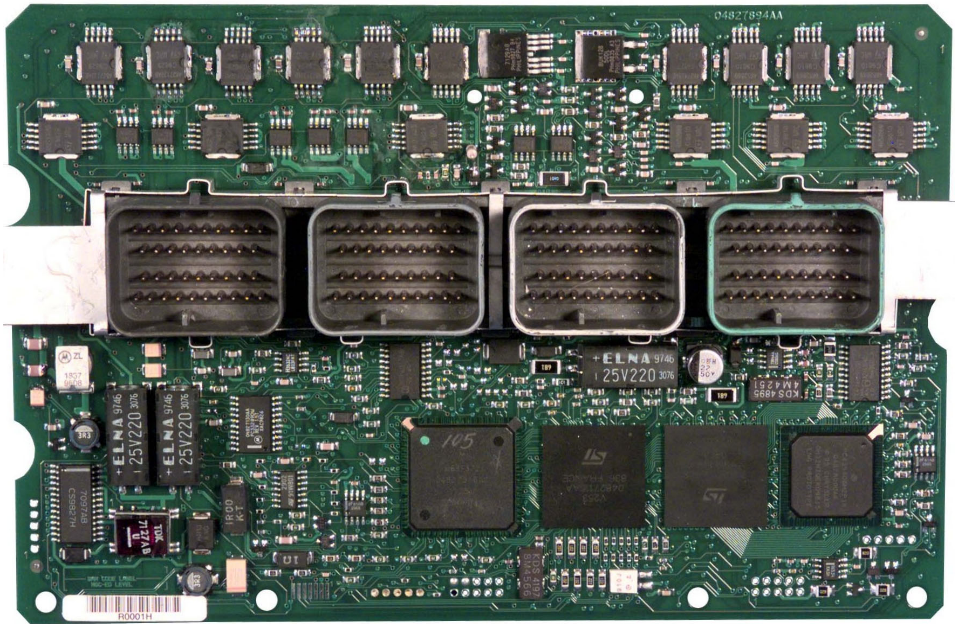


Figure 3.1 - Current Generation Automotive Control Module Board with 23 and 27 mm PBGA Components

In this work, the under-the-hood reliability of smaller PBGA packages (15 and 17 mm body sizes) has been evaluated in the automotive thermal cycling environment. Various methods of enhancing reliability have been explored including increased BT substrate thickness, the utilization of NSMD pads on the BGA component, alternative PCB plating finishes, and the use of underfill encapsulants. A set of test boards was assembled with several 15, 17, and 23 mm body size BGA components from two different vendors (see Table 3.1). In addition to non-underfilled parts, the enhancements achieved with four different underfill encapsulants have been explored. The assembled test vehicles have been subjected to 6000 thermal cycles over the range -40 to 125 ^{o}C, and the daisy-chain resistances of the various components were monitored throughout the testing. Logged failures have been statistically analyzed using two parameter Weibull models. The analysis results have allowed the board level reliabilities of the examined BGA components to be compared and ranked, and the reliability enhancements achieved with various underfills to be accessed. Detailed failure analyses have also been performed to find the locations of solder joint fatigue crack growth, and to identify other failure modes occurring in underfilled parts.

Vendor	Body Size (mm)	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	BT Thickness (mm)	BT Pad Diameter (mm)	BT Pad Type	Ball Diameter (mm)
V1	15	132	1	None	8.6 x 8.6 x 0.37	.38	.4	NSMD	.60
V1	15	132	1	None	8.6 x 8.6 x 0.37	.56	.4	NSMD	.60
V1	17	172	1	16 (4x4)	8.6 x 8.6 x 0.37	.38	.4	NSMD	.54
V1	23	168	1.27	None	8.6 x 8.6 x 0.37	.56	.6	NSMD	.76
V2	17	208	1	16 (4x4)	8 x 8 x 0.35	.38	.5	SMD	.60
V2	23	217	1.27	9 (3x3)	10 x 10 x 0.35	.56	.6	SMD	.70

Table 3.1 - Table of Tested BGA Configurations

3.2 Preliminary Work

Prior to initiation of testing performed in this work, a set of preliminary thermal shock and thermal cycling tests were performed to evaluate the feasibility of using smaller BGA components in the automotive thermal cycling environment. The test vehicles in these early experiments involved a range of 15 to 27 mm body size PBGA components, with only limited samples in each leg of the test matrix. These tests verified that while the larger components (23 and 27 mm) meet the reliability specifications for under-hood applications, the small 15 and 17 mm packages appear to be marginal or miss design targets. It was also found that BGA parts using NSMD pads demonstrate improved thermal cycle performance as compared to BGAs using SMD pads. Small 15 mm BGAs with increased thickness in their BT substrate indicated much improved performance over those with a thinner substrate.

To evaluate PCB plating finishes, test boards with both palladium and HASL finishes were included. In general, it was found that test assemblies prepared with palladium PCBs had much poorer reliabilities relative to the HASL boards, for all BGA component sizes. Failure analysis indicated a large number of voids near the top of the reflowed solder joints in the assemblies prepared with palladium plated test boards.

Finally, two underfills were evaluated as candidate materials for extending the thermal cycling solder joint reliability of the smaller BGAs. It was found that both materials greatly extended the solder joint fatigue life of the 15, 17, and 23 mm parts assembled with underfill. These experiments verified the potential of 15 and 17 mm PBGA packages with underfill to meet the under-the-hood design requirements of the automotive industry, and thus motivated the further experiments presented in this work.

3.3 Test Vehicle Description

3.3.1 PBGA Configurations

The BGA parts included in the current study are tabulated in Table 3.1. Several 15, 17, and 23 mm body size BGA components from two different vendors were included in the test matrix. The major obvious design difference in the parts from the two vendors was the choice of SMD or NSMD pads on the BT substrate. The 23 mm components have been previously qualified for under-hood applications without the use of underfill, and are already in production use in the automotive industry (e.g. Figure 3.1). They were included here as a reference/control in the experiments, as were a set of 0805 chip resistors. The utilized small BGAs (15 and 17 mm) all featured perimeter arrays of smaller diameter solder balls on a 1 mm pitch. In the 15 mm component size, both .38 and .56 mm BT substrate thicknesses were evaluated. The 17 mm parts from both vendors included a 4 x 4 central array of thermal solder balls used to enhance heat transfer. As indicated, the die sizes in the various PBGA parts were quite similar.

3.3.2 Test Boards

All of the BGA parts described above were built with daisy-chain routing on the BT substrates. The designed test board included complementary daisy-chain routing, and brought out the signals to a connector on the edge of the PCB for resistance monitoring during the thermal cycling tests. For parts with thermal balls, the resistances of the perimeter and thermal daisy chain nets were monitored separately. The fabricated test boards included four metal layers, FR-406 glass/epoxy laminate material, copper traces with HASL finish, and a thickness of 1.57 mm. The specified copper diameter of the NSMD test board pads was .50 mm for the 1.27 mm pitch large BGA parts, and .30 mm for the 1.0 mm pitch smaller BGA components. A photograph of a fully assembled test board is contained in Figure 3.2.

3.3.3 Underfills

In addition to measuring the reliability of standard non-underfilled parts, the enhancements achieved with four different underfill encapsulants from three different vendors have been explored. As a result of the confidentiality agreements required by the vendors submitting candidate BGA underfill materials, the identity of the underfills has been coded as UF1, UF2, UF3, and UF4. The recommended curing conditions for the evaluated materials are listed in Table 3.2, along with the final processing conditions developed for the 15 mm BGA components.

Since the volume of underfill that must be dispensed for BGA packages is significantly larger than is required for flip chip applications, several issues have been investigated in formation, dehydration requirements, and the effect of voids on reliability. In addition, while underfill offers increased thermal cycling reliability, unfortunate side effects include additional capital expense, manufacturing processes, and cycle-time increases. The added process steps include underfill dispense, underfill flow, and cure.

Underfill Material	Dispense Time (sec)	Stage Temp (^oC)	Flow Time (sec)	Recommended Cure Conditions
UF1	4.0	100	45	165 ^oC / 7 min
UF2	4.0	105	19	165 ^oC / 5 min
UF3	4.5	100	45	150 ^oC / 30 min
UF4	5.0	105	23	165 ^oC / 5 min

Table 3.2 - Table of Underfill Processing Results (15 mm BGA)

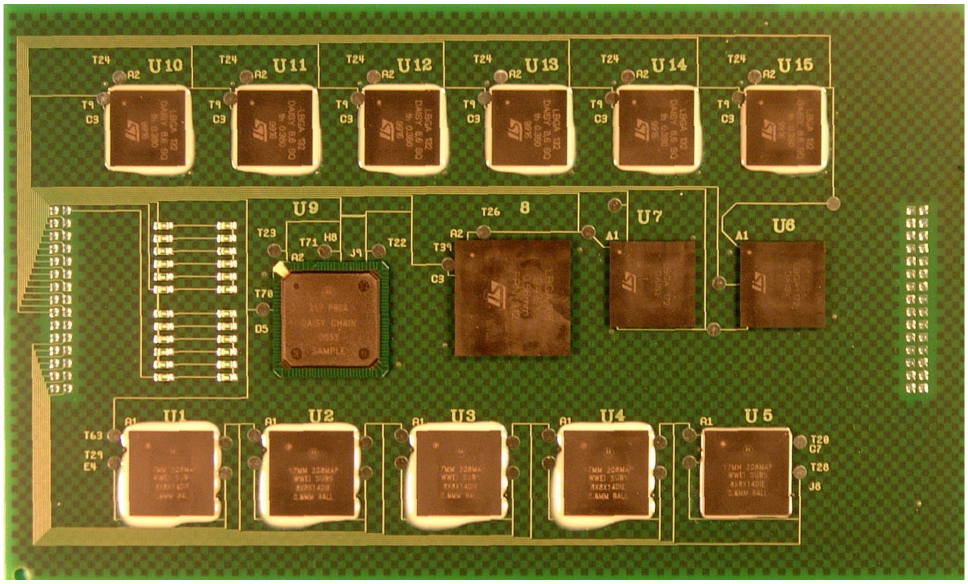


Figure 3.2 - BGA Test Vehicle

The flow time is a function of the substrate (stage) temperature. Increasing the temperature lowers the underfill viscosity, improving the flow speed. Increasing temperature also leads to underfill gelling that impedes proper flow. To achieve a balance between these competing situations, the dispense pattern and stage temperature were optimized for each underfill. If subsequent heating elements are placed in-line after the dispense step, the underfill can continue to flow as the board moves down the assembly line. Alternately, with in-line curing the underfill can flow under the BGA during the ramp to the cure temperature to minimize the impact of the underfill process on cycle time.

Flat sections (the board was polished away) and cross sections were examined for voids to determine the best dispense process. With the proper selection of dispense pattern, no dispense pattern related voids were observed. However, some voids near the base of the solder balls were observed. These are due to the presence of flux residues. This situation was previously observed when underfilling BGAs. In a typical flip-chip assembly, the solder balls are dipped into a thin layer of flux. The resulting volume of residue after reflow is very small. However, with BGAs, solder paste is printed. Solder paste is typically fifty percent flux by volume, and thirty to forty percent of the original flux volume remains as residue (fifteen to twenty percent of the original solder paste volume). With BGAs, there is quite a significant volume of flux residue.

The performed flat sectioning indicated that to an extent the flux residue dissolved into the liquid underfill, but not entirely. This was observed by a color variation in the underfill near the base of the solder ball with light colored underfills. The extent of dissolution varies by underfill material. The residues can also impede the flow of underfill around the base of the solder ball resulting in voids. During thermal shock or cycling, solder will extrude into the void and may this lead to early failures. Additional work is required to understand flux residue/underfill compatibility to establish a robust process.

3.4 Reliability Testing

Thermal cycling (-40 to +125 ^{o}C) of the assembled test boards was performed in a Blue-M environmental chamber, and 6000 cycles were completed before the testing was terminated. The thermal cycle duration was 90 minutes, with 20 minutes at each extreme. Thermocouple results from under a component on one of the test boards are illustrated in Figure 3.3. Enough boards were assembled so that the various legs of the test matrix had from 24-70 samples. The boards were placed vertically in the chamber, and the wiring passed through access ports to the developed data acquisition system. Monitoring of the various daisy chain networks was performed throughout the cycling using a high accuracy digital multimeter coupled with a high performance switching system controlled by LabView software. Failure of a daisy-chain network was defined as the point when the resistance became 300 Ω or higher.

3.5 Thermal Cycling Results

For those components with sufficient failures after 6000 cycles, the resulting failure data were statistically analyzed using two parameter Weibull models. The standard parameters in such an approach are the Weibull Slope β, and the Characteristic Life η, which is the number of cycles required to fail 63.2% of the samples from a particular leg of the test matrix. From these values for a particular PBGA configuration, the cumulative failures (percent) after any number of thermal cycles can be predicted. When comparing the various component reliabilities in this study, we have used the value of $N_{1\%}$, the number of cycles necessary to cause 1% of the parts in a sample set to fail. For electronic

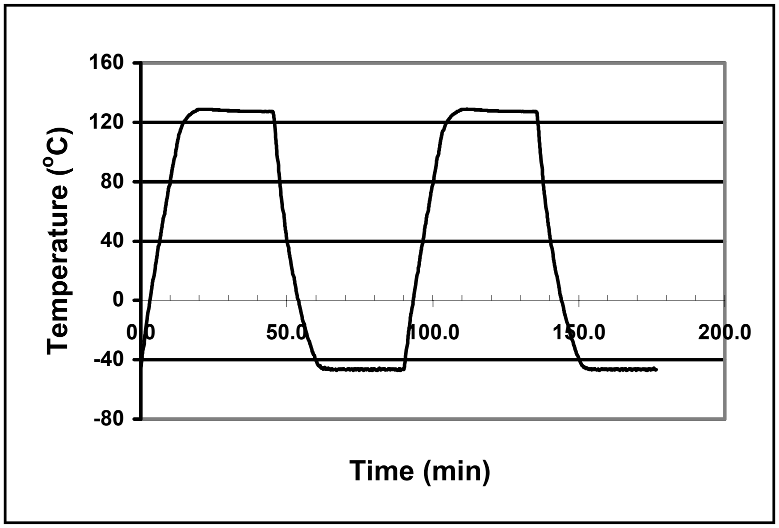


Figure 3.3 - Test Board Thermal Cycle

component thermal cycling failure phenomenon governed by the Weibull distribution, the percentage of failed components is given by:

$$F(N) = 1 - e^{-\left[\frac{N}{\eta}\right]^{\beta}} \qquad \text{(eq. 3.1)}$$

Where F(N) is the fraction of parts failing (CDF), N is the number of thermal cycles (time), η is the Weibull characteristic life or scale parameter, and β is the Weibull slope or shape parameter. This relation can be inverted to solve for the number of thermal cycles in terms of the failure fraction:

$$N = \eta \left[\ln\left(\frac{1}{1 - F(N)} \right) \right]^{1/\beta} \qquad \text{(eq. 3.2)}$$

When comparing the various component reliabilities in this study, the value of $N_{1\%}$ (number of cycles necessary to cause 1% of the parts in a sample set to fail) has been utilized. For 1% failure (F = .01), eq. (3.2) becomes

$$N_{1\%} = \eta \left[.0100503 \right]^{1/\beta} \qquad \text{(eq. 3.3)}$$

The measured failure data for each leg of the test matrix have been analyzed and plotted using WinSmith Weibull commercial software, which calculates the best-fit values of η and β for a set of failure data. Equation (eq. 3.3) was then used to calculate the $N_{1\%}$ values.

Weibull plots for the various BGA parts are shown in Figures 3.4-3.9, and the calculated Weibull parameters are tabulated in Tables 3.3-3.4. The Weibull failure plot for the non-underfilled BGA components from vendor V1 is shown in Figure 3.4. From these data, it can be seen that the relative reliability of the various components is strongly related to the package body size. As expected, the smaller 15 and 17 mm packages are less reliable than the established 23 mm components, and the first failures begin at a level significantly under the 2000 thermal cycle mark typically specified for automotive under-hood electronics. The 15 and 17 mm BGAs with .38 mm thick BT substrates had nearly identical reliability behavior under the -40 to 125 ^{o}C thermal cycling exposure. In addition, use of the thicker .56 mm BT substrate in the 15 mm component gave significantly improved reliability relative to the 15 and 17 mm parts with thinner .38 mm thick BT substrates. The effect of substrate thickness on the reliability of the 15 mm BGA parts from vendor V1 is plotted directly in Figure 3.5.

The Weibull failure plot for the non-underfilled 17 and 23 mm BGAs from vendor V2 are shown in Figure 3.6. Both thermal and perimeter daisy chains were successfully monitored for three different components (17 mm V1, 17 and 23 mm components of V2). Comparison of the reliabilities of the perimeter and thermal balls for 17 mm non-underfilled BGAs from vendor V1 is shown in Figures 3.7. In this case thermal ball reliability exceeds perimeter ball reliability. Due to the use of NSMD pads on the BT substrate, it was expected that the reliabilities of the parts from vendor V2 would be less than the analogous sized components from vendor V1. As shown numerically by the $N_{1\%}$ values in Table 3.3, this was indeed the case. However, the reliability performances of the vendor V2 parts were much less than expected. Even the 23 mm part experienced initial failures at a level significantly under the 2000 thermal cycle mark typically specified for automotive under-hood electronics. This contradicted our experiences with the same component from vendor V2 in previous thermal cycling tests. Our failure analysis of the vendor V2 components indicated the expected solder joint cracking along the top of the ball (near the BT substrate). However, there were also instances where smooth separations developed at the nickel-copper interface on the pads on the BT laminate. Therefore, we believe that there were plating issues on the BGA substrates from vendor V2 that reduced the reliability levels below expected normal levels. This phenomenon was further exacerbated with the presence of underfill, because the thermal expansion of the underfill material tended to lift off the component from the PCB. A photograph of a top view of a smooth separation failure of one of the vendor V2 solder balls is shown in Figure 3.10.

The reliability enhancements realized when using underfill with the 15 mm BGAs from vendor V1 are illustrated in Figures 3.8 and 3.9, for the .38 and .56 mm thick BT substrates, respectively. As is evident from these plots, the failures that occurred with underfilled 15 mm parts began at levels above 2000 thermal cycles. Even more remarkable is that there were no failures of any kind throughout the entire 6000 thermal cycles when using underfills UF1 and UF3 with the 15 mm (.38) BGA parts. Likewise, no failures occurred with underfill UF1 and the 15 mm (.56) components. Finally, there were no failures of any underfilled 17 mm BGAs from vendor V1 (all four underfills) within the 6000 thermal cycles of the reliability testing. Numerical comparisons of the reliabilities of the small BGA (15 and 17 mm) parts from vendor V1, with and without underfill, are given in Table 3.4. If the ratio is taken of the $N_{1\%}$ cycle value with underfill over the $N_{1\%}$ cycle value without underfill for a specific component, a "reliability gain" can be calculated for each underfill/component combination.

Such numbers are tabulated in Table 3.4. If no failures had occurred for a particular underfill and component with the duration of the testing (6000 thermal cycles), then $N_{1\%}$ was set equal to 6000. It can be seen that the reliability enhancements with underfill ranged from 1.5X to greater than 4.4X.

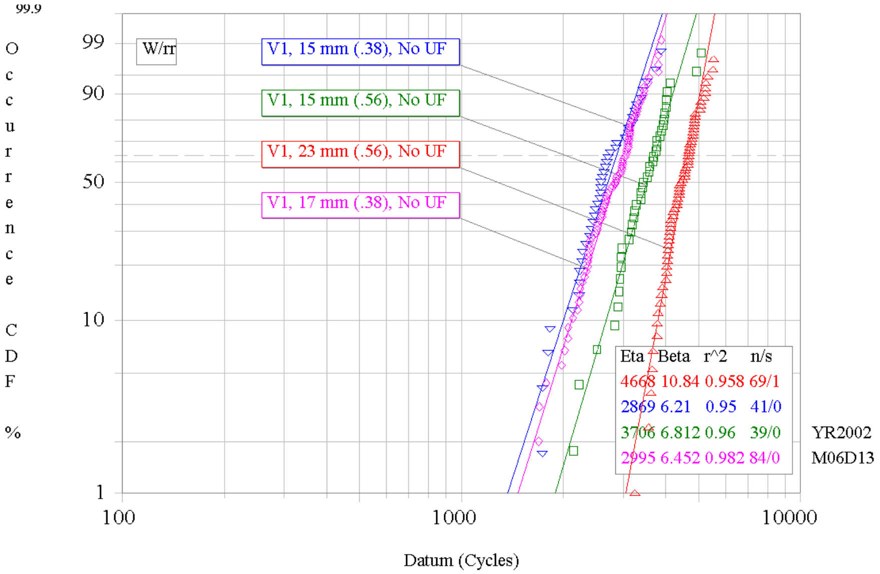


Figure 3.4 – Weibull Plot for Non-Underfilled PBGA Components from Vendor V1

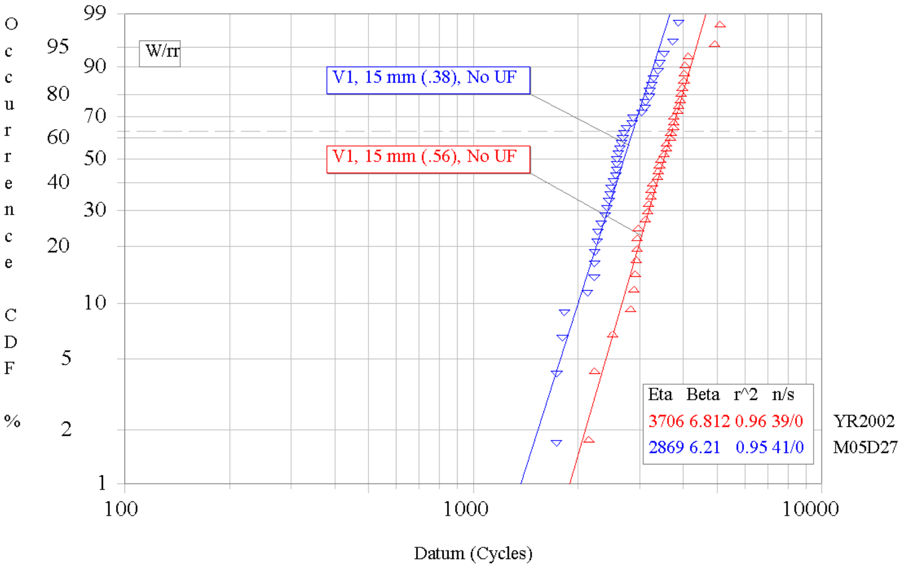


Figure 3.5 – Weibull Plot for Non-Underfilled 15 mm PBGA Components Illustrating the Effect of BT Substrate Thickness

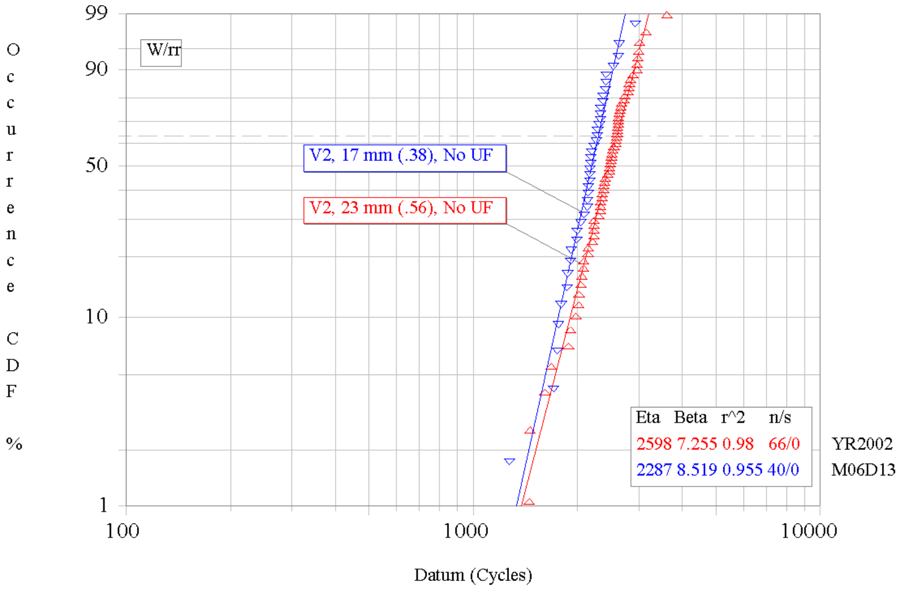


Figure 3.6 – Weibull Plot for Non-Underfilled PBGA Components from Vendor V2

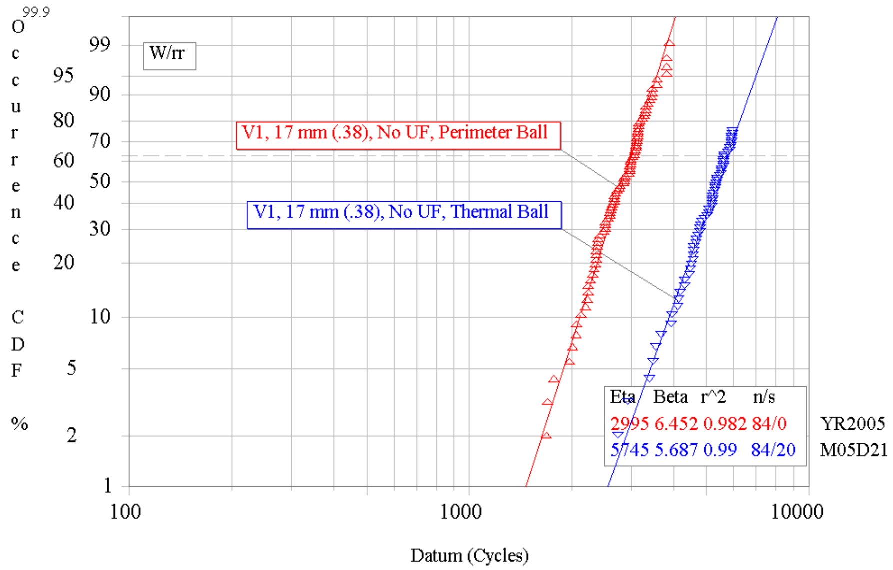


Figure 3.7 – Weibull Plot for Reliabilities of Perimeter and Thermal Balls for Non-Underfilled PBGA Components from Vendor V1

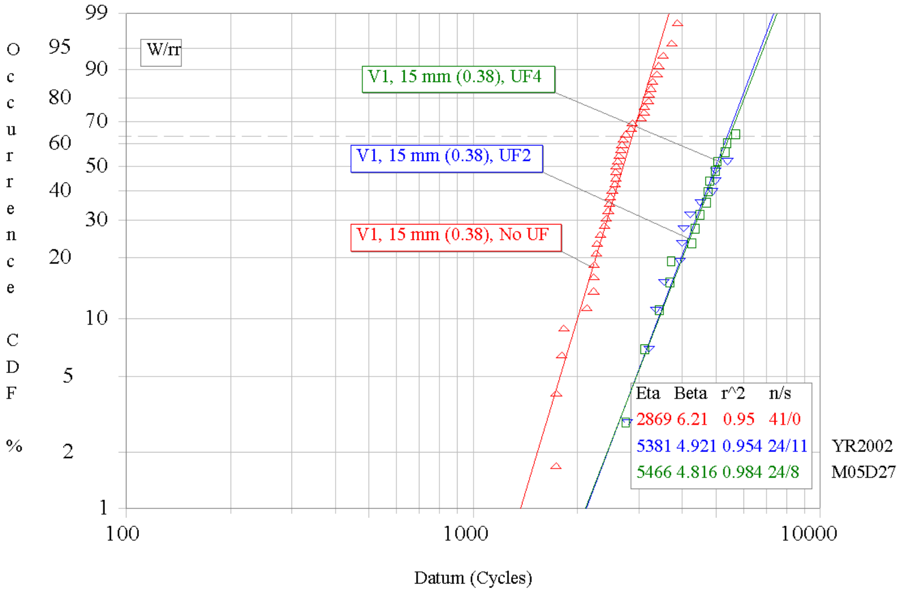


Figure 3.8 - Weibull Plot for Non-Underfilled and Underfilled 15 mm (.38) PBGA s

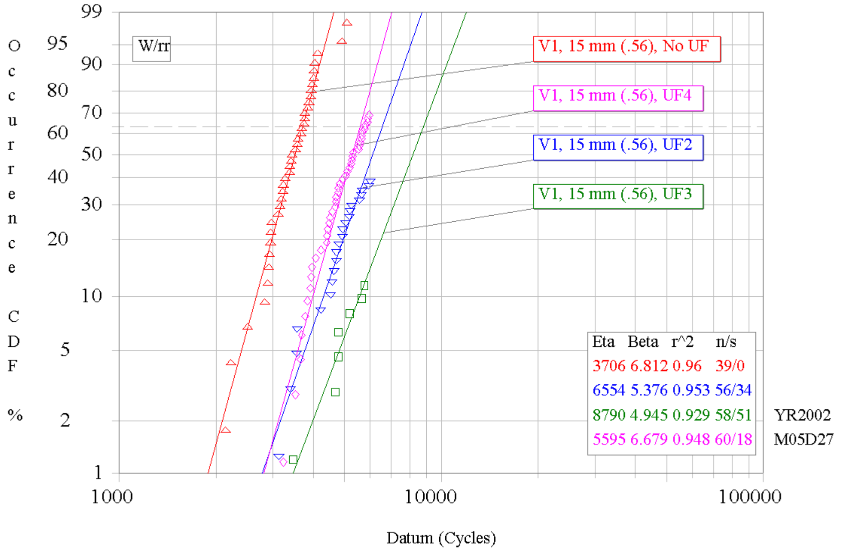


Figure 3.9 - Weibull Plot for Non-Underfilled and Underfilled 15 mm (.56) PBGA s

BGA Component	Weibull Slope, β	Characteristic Life, η	Number of Cycles at 1% Failure Rate, $N_{1\%}$
V1, 15 mm (.38)	6.210	2869	1368
V1, 15 mm (.56)	6.812	3706	1886
V1, 17 mm	6.452	2995	1468
V1, 23 mm	10.84	4668	3054
V2, 17 mm	8.519	2287	1333
V2, 23 mm	7.255	2598	1378

Table 3.3 – Weibull Parameters for the Non-Underfilled PBGA Components

BGA Component	Underfill	Weibull Slope, β	Characteristic Life, η	Number of Cycles at 1% Failure Rate, $N_{1\%}$	Reliability Gain
V1, 15 mm (.38)	None	6.210	2869	1368	
	UF1	-	-	>6000	>4.4X
	UF2	4.921	5381	2113	1.5X
	UF3	-	-	>6000	>4.4X
	UF4	4.816	5466	2103	1.5X
V1, 15 mm (.56)	None	6.812	3706	1886	
	UF1	-	-	>6000	>3.2X
	UF2	5.376	6554	2785	1.5X
	UF3	4.945	8790	3467	1.8X
	UF4	6.679	5595	2810	1.5X
V1, 17 mm	None	6.452	2995	1468	
	UF1	-	-	>6000	>4.1X
	UF2	-	-	>6000	>4.1X
	UF3	-	-	>6000	>4.1X
	UF4	-	-	>6000	>4.1X

Table 3.4 – Weibull Parameters for the Underfilled PBGA Components from Vendor V1

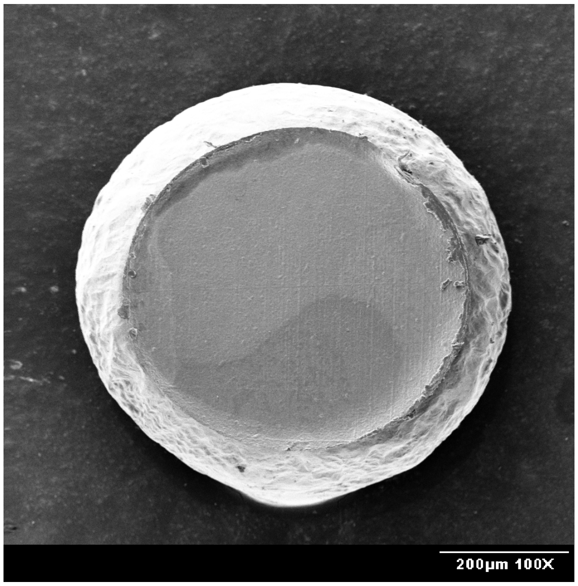


Figure 3.10 - Smooth Failure at the Nickel-Copper Interface on the BT laminate Pads

3.5 Failure Analysis

Extensive failure analysis has been performed on the 15 and 17 mm BGA solder joints, and only the highlights will be presented in this paper. Dedicated specimens for cross sectioning (not part of the electrically monitored test matrix) were removed from the cycling chamber after every 500 or 1000 thermal cycles. Typical solder joint failures in non-underfilled components are illustrated in Figures 3.11 and 3.12. Thermal cycling fatigue cracks were typically found to initiate at the top of the solder joint (BT side), in the high strain regions in the corners at the edges of the NSMD pads. Crack growth would then proceed across the entire joint, near but not at the BT pad interface (intermetallic regions). In some cases, solder joint cracking occurred simultaneously at both the top and bottom of the solder joint (e.g. Figure 3.12). However, only rarely were cracks observed to form only at the bottom of the joint.

Using all of the cross-sectional samples for a particular component type, solder joint grain growth (coarsening) and crack initiations could be observed as shown in Figure 3.13. The observed grain coarsening levels were similar for the various 15 and 17 mm BGA components, with and without underfill. This would indicate that the change in grain structure is predominantly caused by time at temperature and not thermal cycling induced strains. We are in the process of examining these results further and correlating them with finite element predictions and grain growth models.

Underfilled components failed through a variety of mechanisms including solder joint cracking, substrate cracking with solder extrusion causing a short circuit to the neighboring joint, underfill cracking with solder solder extrusion causing a short circuit to the neighboring joint, and cracking/delamination between the soldermask and copper traces. Filler separation has been observed in one of the underfill (UF1), causing more solder extrusion, and bridging. Examples of these failure modes are illustrated in Figures 3.14-3.19.

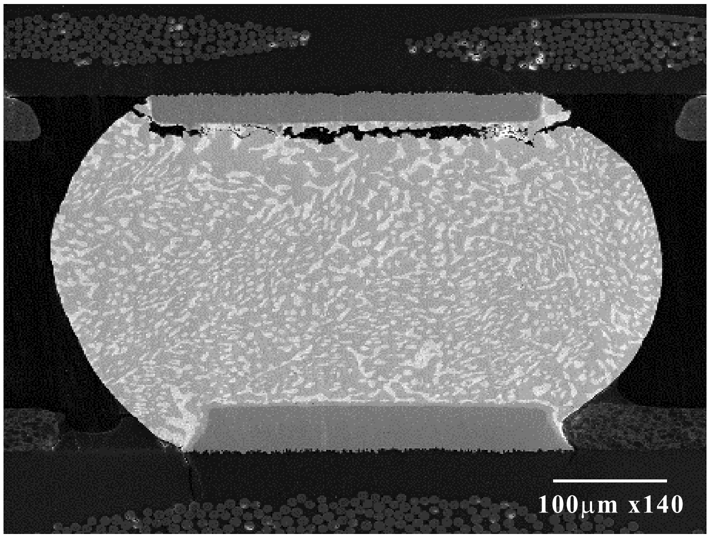


Figure 3.11 - Typical Solder Joint Fatigue Failure, 17 mm BGA, Vendor V1

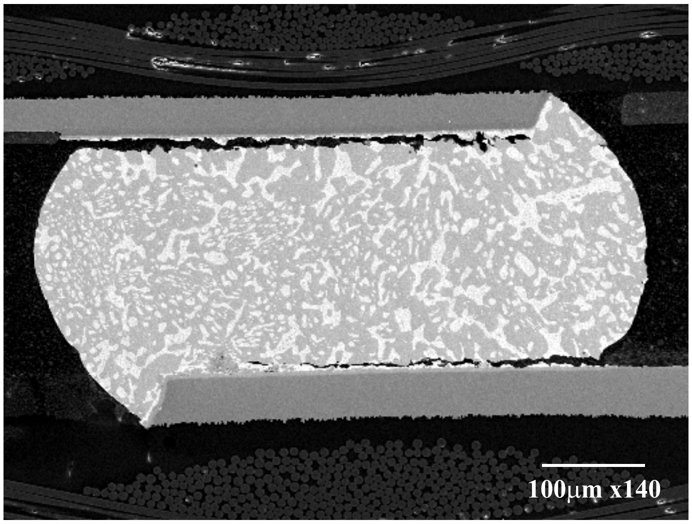


Figure 3.12 - Typical Solder Joint Fatigue Failure, 15 mm BGA, Vendor V1

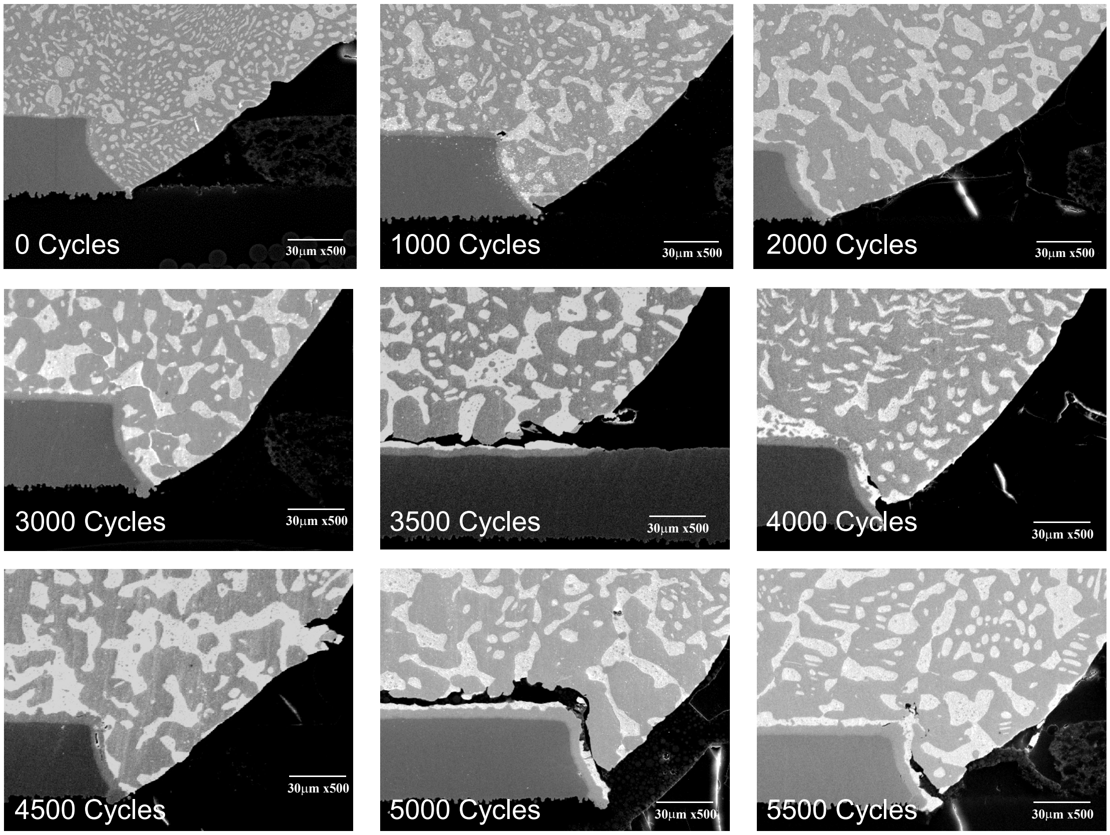


Figure 3.13 - Typical Solder Joint Grain Coarsening, 23 mm BGA, Vendor V1

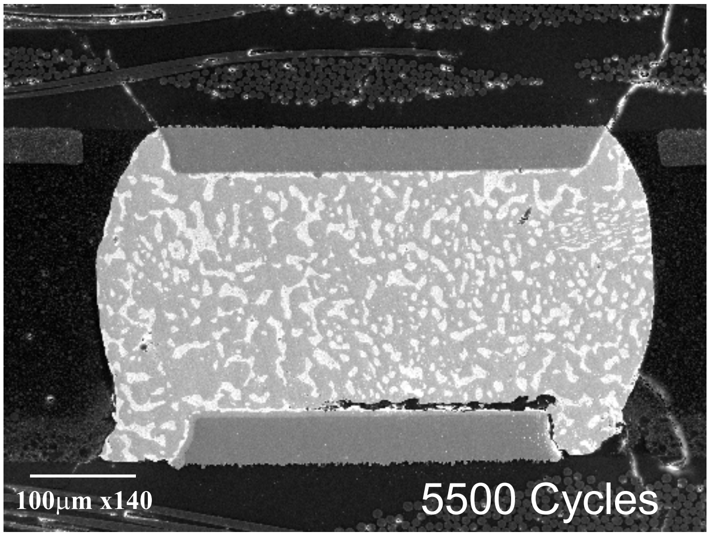


Figure 3.14 - Failure Mode for Underfilled BGA Solder Joint Fatigue Cracking

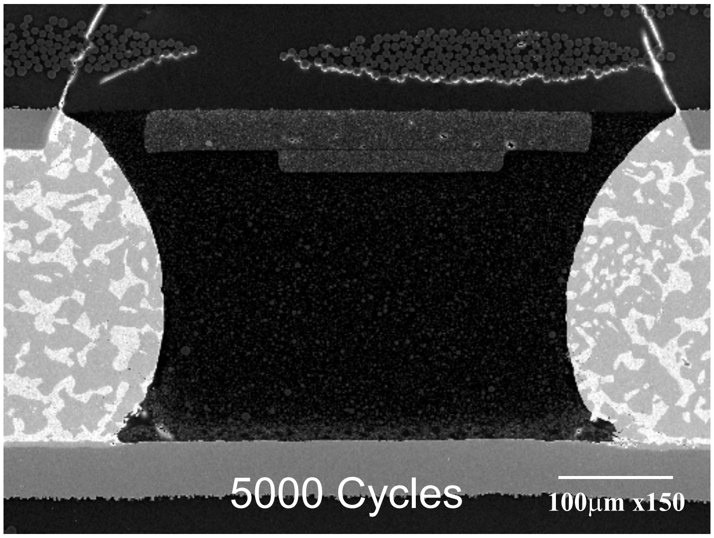


Figure 3.15 - Failure Mode for Underfilled BGA Substrate Cracking
with Solder Extrusion to Cause Shorting

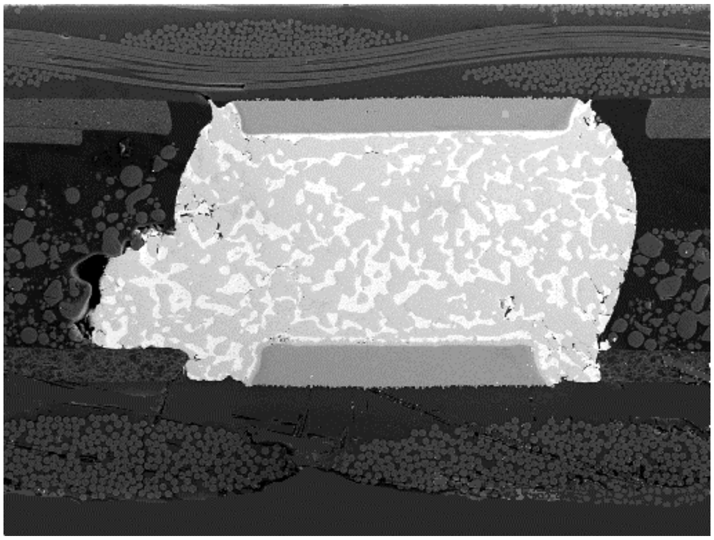


Figure 3.16 - Failure Mode for Underfilled (UF1) BGA Solder Extrusion with Filler Separation in the Underfill

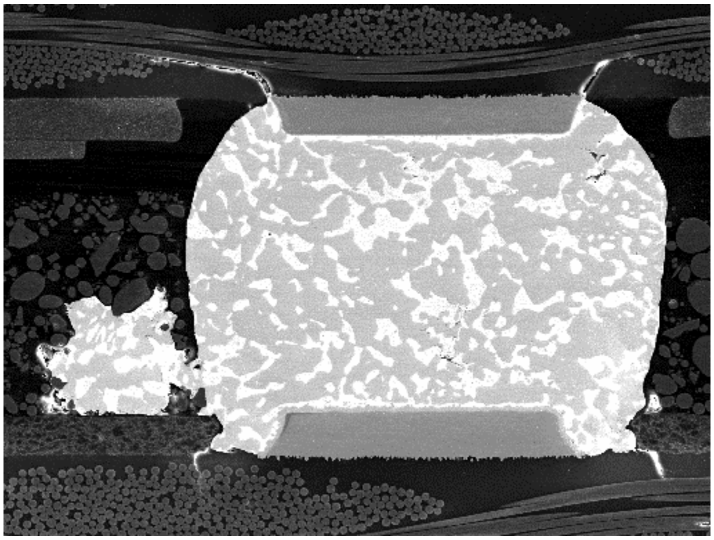


Figure 3.17 - Failure Mode for Underfilled (UF1) BGA Solder Extrusion to Cause Shorting with Filler Separation in the Underfill

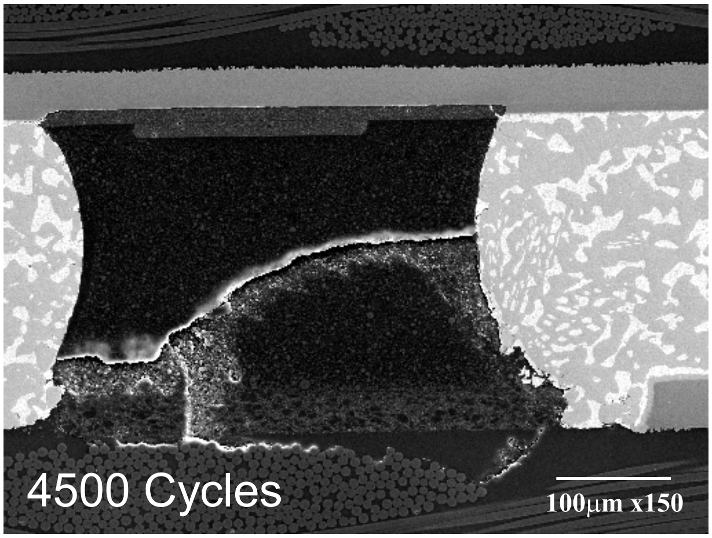


Figure 3.18 - Failure Mode for Underfilled BGA Underfill Cracking with Solder Extrusion to Cause Shorting

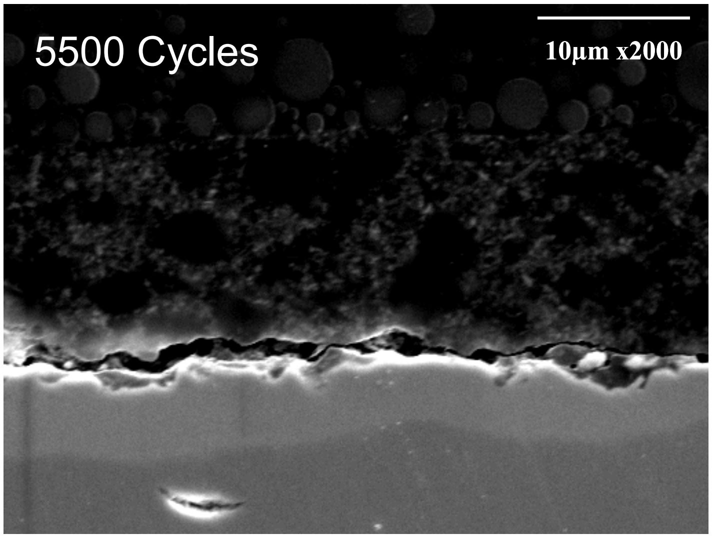


Figure 3.19 - Failure Mode for Underfilled BGA Cracking/Delamination between the Soldermask and Copper Traces

3.6 Summary and Conclusions

In this work, the under-the-hood reliability of smaller PBGA packages (15 and 17 mm body sizes) has been evaluated in the automotive thermal cycling environment. Various methods of enhancing reliability have been explored including increased BT substrate thickness, the utilization of NSMD pads on the BGA component, alternative PCB plating finishes, and the use of underfill encapsulants. A set of test boards was assembled with several 15, 17, and 23 mm body size BGA components from two different vendors. The 23 mm components have been previously qualified for under-hood applications without the use of underfill, and are already in production use in the automotive industry. They were included here as a reference/control in the experiments.

In addition to non-underfilled parts, the enhancements achieved with four different underfill encapsulants have been explored. The assembled test vehicles have been subjected to 6000 thermal cycles over the range -40 to 125 ^{o}C, and the daisy-chain resistances of the various components were monitored throughout the testing. Logged failures have been statistically analyzed using two parameter Weibull models. The analysis results have allowed the board level reliabilities of the examined BGA components to be compared and ranked, and the reliability enhancements achieved with various underfills to be accessed. When used without underfill, it was found that the smaller 15 and 17 mm BGA components do not meet typical automotive thermal cycling requirements. However, for each of the small BGA configurations from vendor V1, certain underfills were found that yielded no thermal cycling failures within the 6000 cycles completed in this investigation. For one underfill identified in this study (UF1), no failures were observed for any of the small BGA components. Overall, the reliability enhancements with underfill ranged from 1.5X to greater than 4.4X, relative to the non-underfilled BGAs.

CHAPTER 4

MODEL FOR BGA AND CSP RELIABILITY IN AUTOMOTIVE UNDERHOOD APPLICATIONS

4.1 Introduction

In this section, results of investigation of fine-pitch ball grid array (BGA) reliability in automotive underhood environment have been reported. The effect of temperature cycling on the reliability of microelectronic packages is the topic of much research. Because of the difference in thermal expansion of various materials involved in the electronic packages, temperatures variations create thermal mismatch resulting in solder joint stress. Solder joint failure occurs due to the repeated application of the stress, which is termed as low cycle fatigue. The thermo-mechanical reliability of these packages is a concern for the electronic industry. The board level reliability of solder joint is one of the most critical issues for successful application of BGA.

4.2 Glass Transition Effect on Reliability Data

For most laminates with T_g in the range of 130 to 140°C, using a –55 to 125°C, liquid to liquid thermal shock (LLTS) may be inappropriate in many cases. The basic reason being that the vendor specified T_g values are typically calculated from DMA or DSC which tend to be typically 10°C – 25°C higher than those determined from TMA. In actuality, for a material with a T_g of 140°C, the Z-axis CTE begins to increase in the neighborhood of 115-130°C. Figure 4.1 shows the difference between glass transition temperature from DMA and TMA for six-different printed circuit board (PCB) designs from double-sided to six-layer configurations. Thermal fatigue reliability of solder joints is impacted by the glass transition temperature measured from TMA. Figure 4.2 shows the glass transition temperature of 121°C measured by TMA, for a low T_g glass-epoxy laminate. The CTE of most glass epoxy laminates increases 3X to 5X above the glass transition temperature (Figure 4.2). If the accelerated test extreme occurs above the CTE transition zone, the CTE is not constant during test.

Similar difference in the glass-transition temperature from TMA and DSC exists in the high-T_g laminates also. Table 4.1 shows the values of glass transition temperature for the NELCO N4000-13 material [77] from TMA, DSC, and DMA measured as per IPC-TM-650. However, high-T_g laminates commonly used in automotive applications, have glass transition temperature in the neighborhood of 160-200°C well beyond the high-temperature threshold of 125°C commonly used in accelerated tests.

Thus, high T_g laminates may behave like low T_g laminates only in a subset of the applications. The predictions of Darveaux's damage relationships have been verified by several researchers for portable applications, which regularly require accelerated tests of –55 to 125°C or –40 to 125°C on low T_g FR4 boards. Will the correlation of state-of-art damage relationships with accelerated test data improve or degrade for Plastic BGAs soldered on high T_g printed circuit boards? Damage relationships for crack initiation and propagation have been developed for 15 mm, 17 mm, and 23 mm size plastic BGAs on

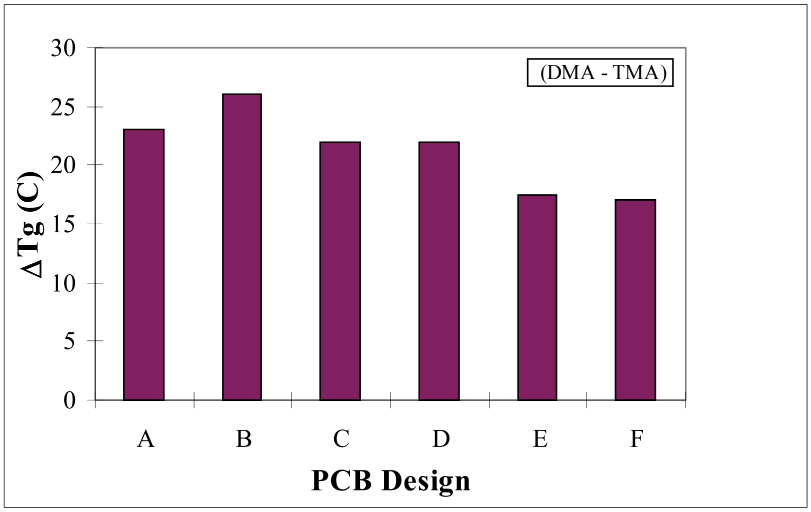


Figure 4.1: Difference in glass transition temperature of PCB from DMA and TMA for six-board designs constructed from low-T_g laminates.

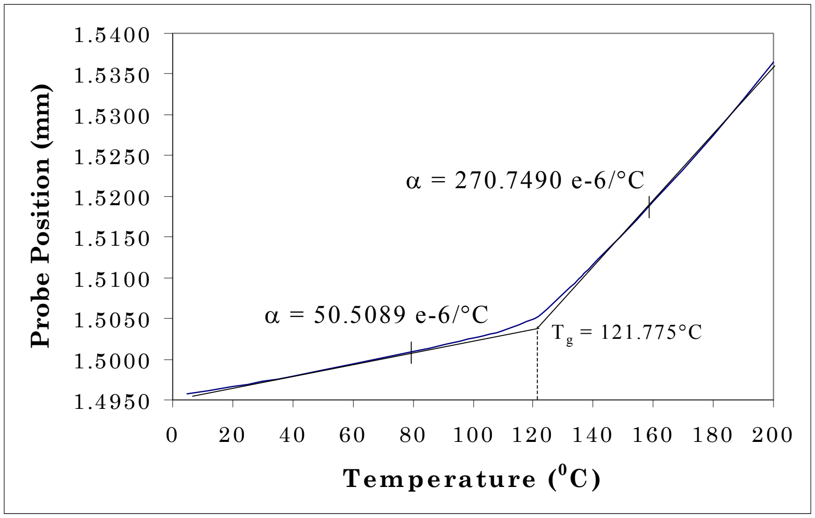


Figure 4.2: Change in Z-CTE with temperature. [78]

high-T_g printed circuit boards. The data has been benchmarked against the previously published Darveaux's Data for both crack initiation and propagation [5-7].

4.3 Pad Geometry, Solder Composition and IC Package

Benchmark of the package deformation between CBGAs and PBGAs from finite element analysis indicates significant differences in the deformation field which may contribute to differences in crack propagation. Major part of the deformation in the Ceramic BGAs is in the board since the ceramic is much stiffer than the PCB. Crack propagation measurements reported in [6] are predominantly on the package side. The crack propagation measurements reported in this study are both on the package and the board side. Major portion of the crack propagation data in [7, 14] is on 62Sn36Pb2Ag solder. Under identical conditions, 60Sn40Pb solder has about 6 to 25% higher crack growth rate than 62Sn36Pb2Ag solder. The present study uses 63Sn37Pb solder.

The damage relationships in [5-7] were predominantly derived for SMD pads. The present study uses NSMD pads for measuring crack propagation Data. Several researchers have shown that SMD pads fail significantly faster than NSMD pads in thermal fatigue due to a different solder joint shape which produces a 90° angle of the solder joint with respect to the copper pad.

4.4 Test Vehicle

A set of test boards was assembled with several 15, 17, and 23 mm body size BGA components. The fabricated test boards included four metal layers, FR-406 glass/epoxy laminate material (T_g = 164.9°C), copper traces with hot air solder level (HASL) finish, and a thickness of 1.57 mm. (Figure 4.3). The BGA package parameters

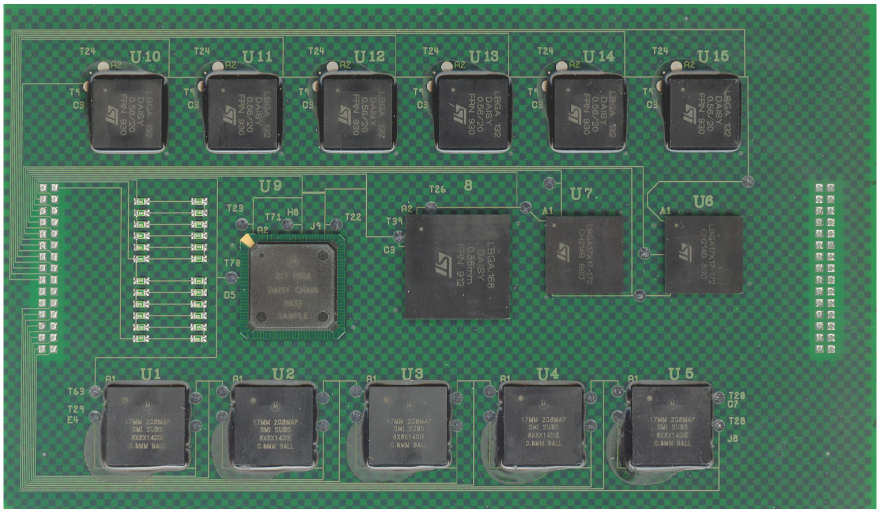


Figure 4.3: BGA Test Vehicle.

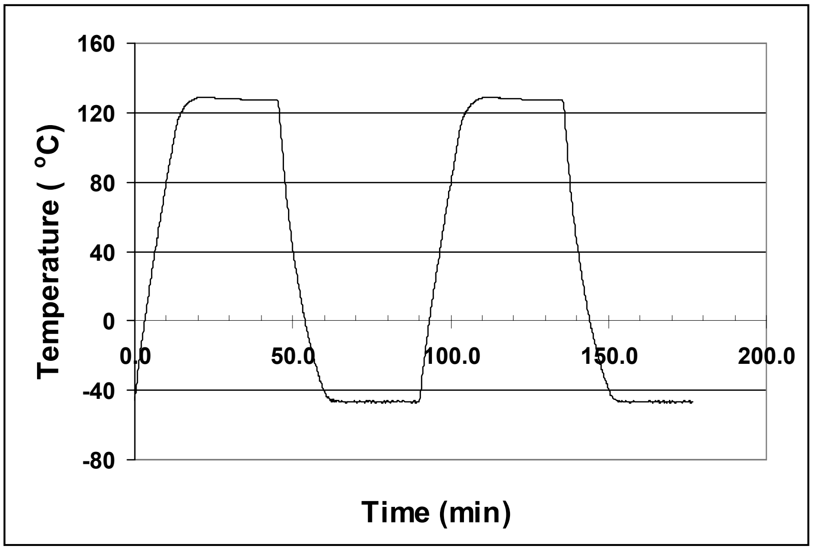


Figure 4.4: Typical Thermal Cycle (-40 to 125^{0}C) Profile

included in the current study are tabulated in Table 4.2. The test vehicles have been subjected to air-to-air temperature cycle. The thermal cycle duration is 90 minutes with 15 minutes ramps between temperature extremes and 30 minutes dwells at each temperature extreme. The thermal cycle profile parameter is shown in Table 4.3. The graphical form of thermal cycling profile for this study has been shown in Figure 4.4.

	Glass-Transition Temperature (°C)	
DSC	210°C	IPC-TM-650.2.4.25c
TMA	200°C	IPC-TM-650.2.4.25c
DMA	240°C	IPC-TM-650.2.4.24.3

Table 4.1: T_g for NELCO N4000-13 laminate material [Park Nelco 2003]

Vendor	Body Size (mm)	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	BT Thickness (mm)	BT Pad Diameter (mm)	BT Pad Type	PCB Pad	Ball Diameter (mm)
V1	15	132	1	None	8.6 x 8.6 x 0.37	.38	.4	NSMD	NSMD	.60
V1	15	132	1	None	8.6 x 8.6 x 0.37	.56	.4	NSMD	NSMD	.60
V1	17	172	1	16 (4x4)	8.6 x 8.6 x 0.37	.38	.4	NSMD	NSMD	.54
V1	23	168	1.27	None	8.6 x 8.6 x 0.37	.56	.6	NSMD	NSMD	.76

Table 4.2: Package Parameters

Low Temp	High Temp	Ramp Up Time (sec)	Dwell Time High (sec)	Ramp Down Time (sec)	Dwell Time Low (sec)
-40	125	900	1800	900	1800

Table 4.3: Profile for Temperature Cycle Chamber

4.5 Materials Model

Linear and non-linear, elastic, plastic, creep, temperature and time dependent and time-independent material properties have been incorporated in the finite element models. It is well known that solder is above half its melting point at room temperature that's why time-dependent creep phenomena dominate solder joint fatigue. Most of the package materials are considered as linear elastic with temperature independent and dependent except solder. The details thermo mechanical properties of those materials are displayed in Table 4.4.

The thermal fatigue failure of electronic packages is associated with combined plastic-deformation and creep of solder joints. The Anand Viscoplasticity model, a standard material in ANSYS, which has been used by several researchers to model the constitutive behavior of solder – has been used in this study. This constitutive law has been used by Darveaux [5-7, 79] in development of damage relationships. The constitutive behavior model has therefore been kept the same to enable benchmark of damage relationships. Anand's model [25] is split into a flow equation and three evolution equations that describe the strain hardening or softening of the materials (Table 4.5).

Flow Equation

$$\frac{d\varepsilon_p}{dt} = A\left(\sinh(\xi\sigma/s_0)\right)^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \qquad \text{(eq. 4.1)}$$

Evolution Equations

$$\frac{ds_0}{dt} = \left\{h_0\left(|B|\right)^a \frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt} \qquad \text{(eq. 4.2)}$$

$$B = 1 - \frac{s_0}{s^*} \qquad \text{(eq. 4.3)} \qquad s^* = s\hat{}\left[\frac{\frac{d\varepsilon_p}{dt}}{A}\exp\left(\frac{Q}{kT}\right)\right]^n \qquad \text{(eq. 4.4)}$$

The nomenclature of the equation 4.1 through 4.4 is explained in Table 4.4 and 4.5.

Materials Name	Elastic Modulus (MPa)	Shear Modulus (MPa)	Poisson's Ratio	CTE (1/K)
PCB	27924-37T (XY) 12204-16T (Z)	12600-16.7T (XY) 5500-7.3T (YZ & XZ)	.39 (XZ & YZ) .11 (XY)	14.5E-6 (XY) 67.2E-6 (Z)
Solder Mask	3100	--	.3	30E-6
Copper	129000	--	.34	16.3E-6
Solder	75842-152T	--	.35	24E-6
BT	17890 (XY) 7846 (Z)	8061 (XY) 2822 (YZ & XZ)	.39 (XZ & YZ) .11 (XY)	12.42E-6 (XY) 57E-6 (Z)
Die Adhesive	6769	--	.35	52E-6
Silicon	163000	--	.28	2.5E-6
Mold Compound	23520	--	.3	15E-6

T=Temperature in Kelvin

Table 4.4: Mechanical Properties of Package Materials

Parameter	Value	Definition
S_0 (MPa)	12.41	Initial Value of Deformation Resistance
Q/k (1/K)	9400	Activation Energy/ Boltzmann's Constant
A (1/sec)	4.0E6	Pre-Exponential Factor
ξ (dimensionless)	1.5	Multiplier of Stress
m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
h_0 (MPa)	1378.95	Hardening Constant
s^ (MPa)	13.79	Coefficient of Deformation Resistance Saturation Value
n (dimensionless)	0.07	Strain Rate Sensitivity of Saturation (Deformation Resistance) Value
a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

Table 4.5: Values of Anand Constants used for Simulation.

4.6 Crack Growth Measurement

Extensive failure analysis has been performed on the 15, 17, and 23 mm BGA solder joints, and only the highlights will be presented in this paper. Dedicated specimens for cross sectioning (not part of the electrically monitored test matrix) were removed from the cycling chamber after every 500 thermal cycles. The samples were polished to match the measured pad diameter with the intended pad diameter before any crack measurements were taken.

Cross section measurements were validated by prying-off some of the samples. Typical solder joint failures in 17 mm components are illustrated in Figure 4.5. In most of the cases the crack initiates in the corner solder ball of the packages. Thermal cycling fatigue cracks were typically found to initiate at the top of the solder joint (BT side), in the high strain regions in the corners at the edges of the NSMD pads. Crack growth typically proceeds across the entire joint, near intermetallic layer close to the BT pad interface. In most cases, solder joint cracking occurred simultaneously at both the top and bottom of the solder joint (Figure 4.6). In almost all cases, the primary crack initiated at the package interface and later a secondary crack initiated at the board interface. Once the primary crack initiated it progressed to other edges of the joint, and caused complete failure.

Solder joint cracks have been measured at each temperature cycling data-interval. An average value of crack length across samples has been calculated for each set and cycle-count. The crack growth data in this study indicates that characteristic crack growth rate stays fairly uniform during the thermal cycle tests. The primary and secondary crack lengths are plotted with the number of thermal cycles for the test condition shown in Figure 4.7. Table 4.6 shows the crack initiation and crack propagation rates for each of the data sets.

The number of crack initiation cycles has been found by solving the regression fit of the data for a crack length of zero. Primary and secondary cracks for 15, 17, and 23 mm packages have been summed up for analysis. It is seen that the crack initiation only accounts for about 14% of the fatigue life (Figure 4.8). This correlates well with the 10% initiation life estimate measured by Darveaux [6-7] on CBGA assemblies.

4.7 Crack Growth Correlations

ANSYS 6.1 was used to simulate the thermal cycle experiments. The quarter symmetry model was used with mapped finite element mesh that varied from approximately 25,000 nodes and 23,000 elements to 52,000 nodes and 50,000 elements depending on the complexity of the geometry and the number of solder balls. Solder ball materials were meshed with VISCO 107 elements, and all other package materials were meshed with SOLID 45 elements.

The quarter model has a symmetry boundary condition along the symmetry line of the full package and vertical movement is free along the corner edge (centerline) of the package. A typical 3D finite element mesh of a quarter symmetry package is shown in the Figure 9. The element thickness has been chosen to be 1.5 mils for the correlation.

A volume averaging technique was used to reduce this sensitivity to meshing. The volume of the element normalizes the strain energy value at each element.

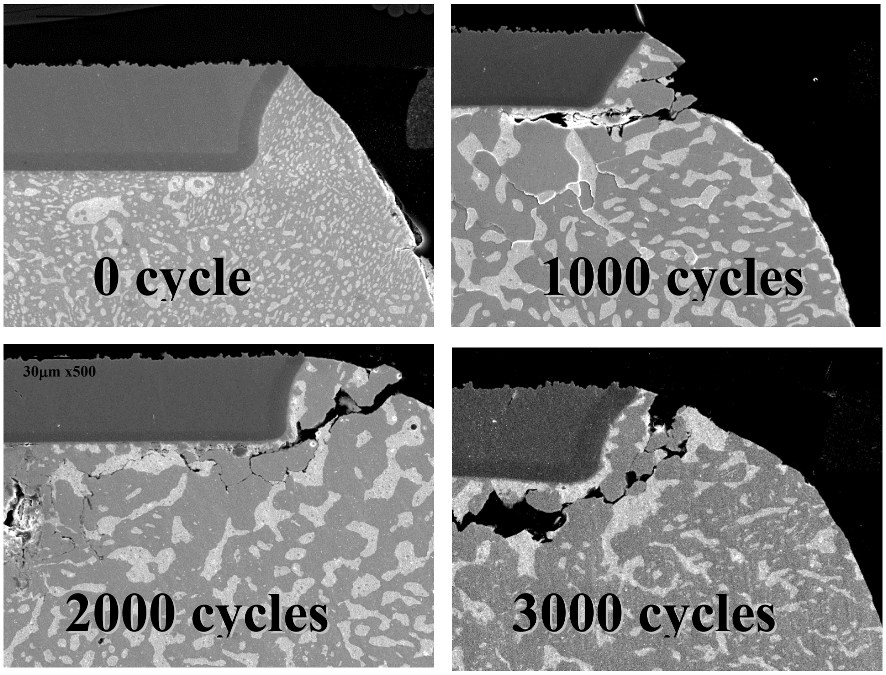


Figure 4.5: Solder Joint Progressive Crack 17mm BGA, V1

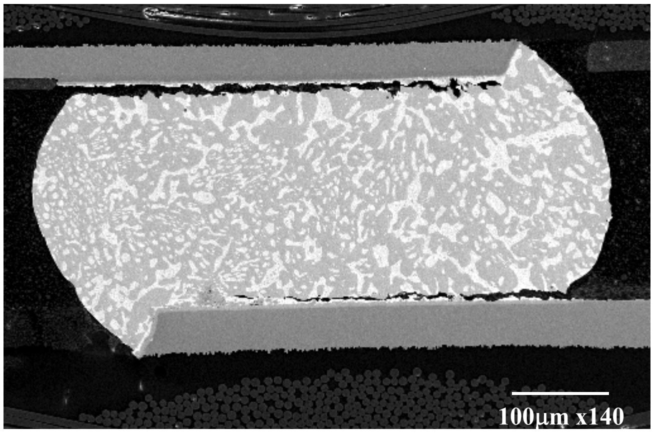


Figure 4.6: Simultaneous Crack Propagation Top and Bottom of the Solder Joint, 15 mm BGA, V1.

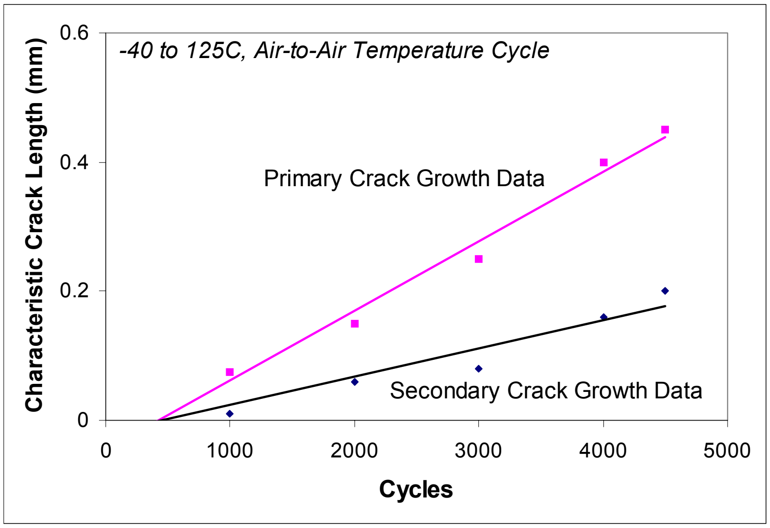


Figure 4.7: Primary and secondary crack growth rate during Thermal Cycling (-40 to 125°C).

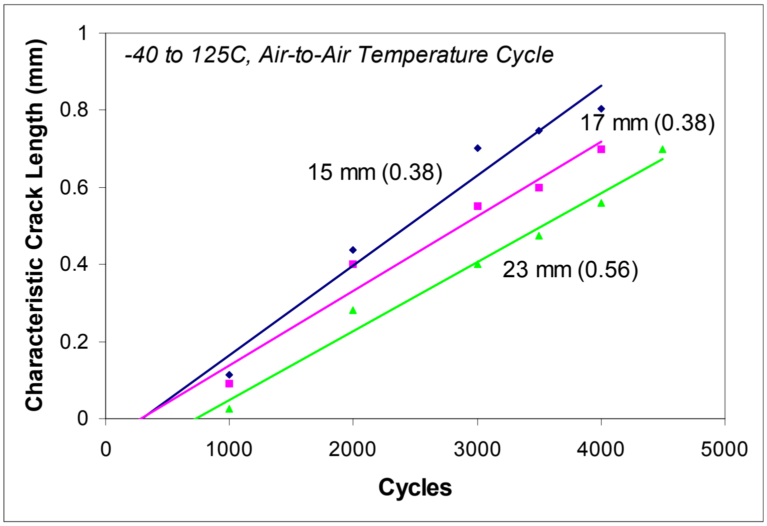


Figure 4.8: Crack propagation data for 15mm, 17mm, and 23 mm BGAs.

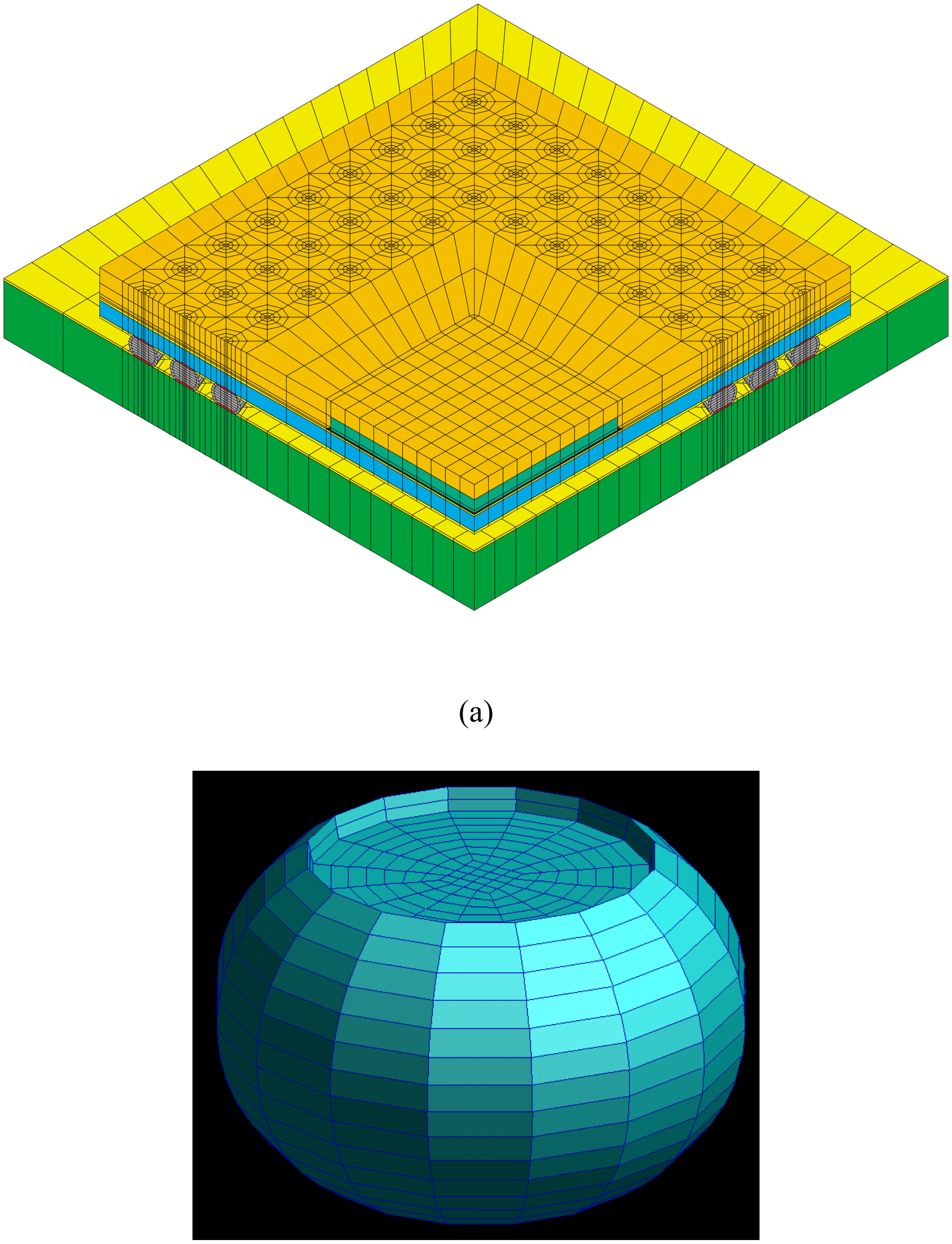
$$\Delta W_{ave} = \frac{\sum \Delta W.V}{\sum V} \qquad \text{(eq. 4.5)}$$

where ΔW_{ave} the average viscoplastic strain energy density is accumulated per cycle at the interface elements, ΔW is the viscoplastic strain energy density accumulated per cycle of each element, and V is the volume of each element.

The difference in viscoplastic strain energy density has been correlated with the measured crack growth data. Initially the viscoplastic strain energy density values were averaged over the entire worst solder ball to minimize the mesh density effect on the finite element simulation. Extensive analysis of this technique proved that fatigue life results are way off the experiment. The viscoplastic strain energy density values were averaged over the interface elements. The typical interface layer varies from 1.5 to 3 mils (1 mm = 40 mils). Figure 4.10 and Figure 4.11 show the correlation of the strain energy with the crack initiation and crack propagation cycles respectively. Two data sets have been plotted – (a) Darveaux's data set from [7], and (b) center for advanced electronics (CAVE) data.

Package Type	Crack Initiation (Cycle)	Crack Growth Rate (μmm/Cycle)
15 mm (.38)	127.26	231.56
15 mm (.56)	169.5	174.93
17 mm (.38)	130.68	182.08
23 mm (.56)	417.4	164.79

Table 4.6: Crack Initiation and Crack Propagation Rates.



(a)

(b)

Figure 4.9: 3D Quarter Symmetry Finite-Element Mesh for (a) Assembly and (b) Solder Joint.

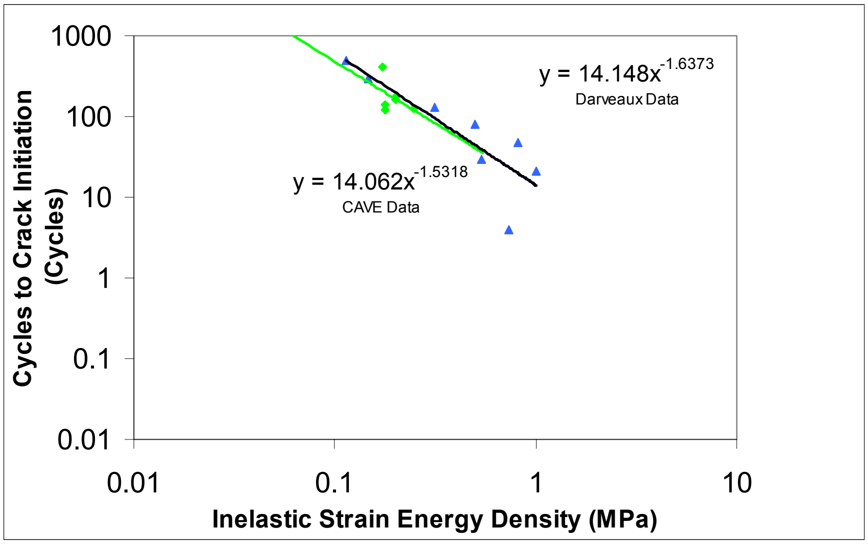


Figure 4.10: Crack Initiation Correlation, Quarter Symmetry, Non-Linear FEA, Anand's Constitutive Model.

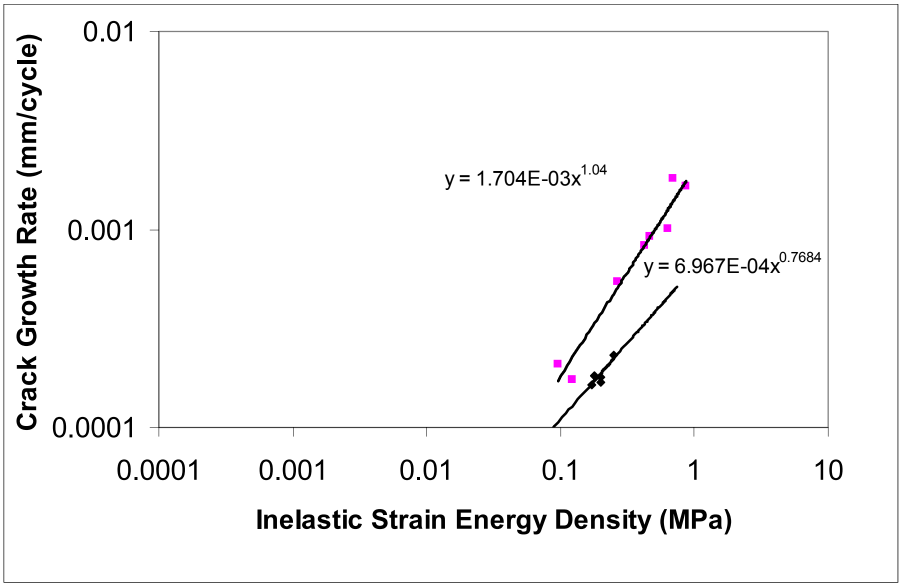


Figure 4.11: Crack Growth Rate Correlation, Quarter Symmetry, Non-Linear FEA, Anand's Constitutive Model.

The slope of the crack initiation curves match very closely for the two data-sets. Damage relationships developed in the present study correlate well with the damage relationships developed in [7] in order-of-magnitude of both intercept and slope. However, the values of the damage relationships differ significantly. The intercept for the CAVE data set is approximately 0.5x of Darveaux data set. The CAVE data has a slope of –1.53 compared to –1.64 from Darveaux data (Table 4.7). A major difference exists in the crack propagation constants for the two data sets (Table 4.8). CAVE data on high-T_g laminates predicts a lower sensitivity to increase in the inelastic strain energy density for both crack initiation and increase in crack propagation rate. In addition, CAVE data set indicates a lower crack propagation rate at any inelastic strain energy density. In general, the number of cycles to crack initiation and propagation in Sn63Pb37 joints can be expressed as

$$N_i = K_1 \left(\Delta W_{ave}\right)^{K_2} \qquad \text{(eq. 4.6)}$$

$$\frac{da}{dN} = K_3 \left(\Delta W_{ave}\right)^{K_4} \qquad \text{(eq. 4.7)}$$

	K_1	K_2
CAVE Data	14.062	-1.53
Darveaux's Data	14.148	-1.64

Table 4.7: Crack Initiation Constants.

	K_3	K_4
CAVE Data	6.967E-04	0.7684
Darveaux's Data-	1.704E-03	1.040

Table 4.8: Crack Propagation Constants.

4.8 Fatigue Life Prediction

When comparing the various component reliabilities in this study, we have used the value of N(1%) for correlation purposes. The cumulative distribution of failures (CDF), for the 3 parameter weibull distribution is given by –

$$\mathrm{CDF} = 1 - e^{-\left(\frac{N - N_0}{\alpha_W - N_0}\right)^{\beta_W}} \quad \text{(eq. 4.8)}$$

Where, N is the number of cycles, N_0 is the failure free life, α_W is the characteristic life at which 63.2% of the population has failed, and β_W is the slope or shape parameter which indicates the class of failure mode.

Since the crack growth rate is constant during the thermal cycling (Figure 4.8), the fatigue life of a joint can be calculated by adding the number of cycles to grow the cracks across the joint interface. The characteristic life can be expressed as

$$\alpha_W = N_i + \frac{a}{da/dN} \quad \text{(eq. 4.9)}$$

Where “a” is the joint diameter at the interface. Darveaux [6] found that the maximum crack length in the population was approximately one half of the characteristic length. The characteristic crack length can be defined as the total joint diameter of the solder ball with the cu pad. Typically in the NSMD pads, the pad diameter is equivalent to the chrematistic crack length. Hence we would expect the failure free life to be approximately one half of the characteristic life.

$$N_0 = \alpha_W / 2 \quad \text{(eq. 4.10)}$$

To calculate the 1% failure time from the first failure equation, it has been assumed that the sample size being predicted is 100 samples. Therefore, the 1% failure time and time-to-first failure are the same value. If the data is used for a sample size of less than 100, the prediction should only be interpreted as 1% failure. The cycles to first failure is given by

$$N = N_0 + (\alpha_W - N_0)[-\ln(1 - CDF)]^{1/\beta_W} \qquad \text{(eq. 4.11)}$$

Where the CDF is calculated in terms of median rank

$$CDF = \frac{(1 - 0.3)}{(S_S + 0.4)} \qquad \text{(eq. 4.12)}$$

Where S_S is the sample size. The characteristic life, time to first-failure and the time to 1% failure has been predicted for each of the datasets based on the two damage relationships – (a) CAVE Data (Table 4.9) and (b) Darveaux Data-Set (Table 4.10). The shape parameters used for predictions have been kept the same for both data-tables. The values of the shape parameter are based on experimentally observed values for the packaging technology and the thermal condition in accelerated test. The experimentally observed values for the 3-parameter weibull fit for time-to-1%-failure has been listed in Table 4.11. In most cases, the error with respect to experimentally observed 1% failure time has been reduced by 50% using the new damage constants.

4.9 Discussion

Significant variability in life predictions is typically observed in thermal fatigue failure of IC packages. No two data-sets even if identical in every measured parameter will produce the same response in accelerated tests. On the experimental side, there are lot-to-lot variations in the material properties, PCB pad finish, and solder joint quality. Excessive warpage in packages can cause joints to be already cracked after the SMT process. Sometimes interface failures are observed, for example due to electroless Ni/Au plating problems. Measuring the material properties of packaging materials is not an easy task. There is often quite a large scatter in both elastic modulus and thermal expansion coefficient

Package Size (Pad Size) (mm)	ΔW (MPa)	N_i (Cycles)	da/dN (mm/Cycle)	α_W (Cycle)	N_0 (Cycle)	N(1%) Failure (cycle)
15 (.38)	0.2499	118	2.40092E-04	1784	892	1293
15 (.56)	0.1999	166	2.02228E-04	2144	1072	1589
17 (.38)	0.1799	195	1.86518E-04	2339	1170	1712
23 (.56)	0.1725	207	1.80600E-04	3530	1765	2881

Table 4.9: Model Predictions based on CAVE Data.

Package Size (Pad Size) (mm)	ΔW (MPa)	N_i (Cycles)	da/dN (mm/Cycle)	α_W (Cycle)	N_0 (Cycle)	N(1%) Failure (cycle)
15 (.38)	0.2499	137	4.02963E-04	1130	565	819
15 (.56)	0.1999	197	3.19437E-04	1450	725	1075
17 (.38)	0.1799	235	2.86318E-04	1632	816	1194
23 (.56)	0.1725	251	2.74093E-04	2440	1220	1992

Table 4.10: Model Predictions based on Darveaux Data.

Package Size (Pad Size) (mm)	Three-Parameter Weibull Distribution Fit of Experimental Data N(1%) (Cycles)	Prediction Error based on CAVE Data (%)	Prediction Error based Darveaux Data Set (%)
15 (.38)	1368	-5.46	-40.27
15 (.56)	1886	-15.73	-43.17
17 (.38)	1468	16.62	-18.88
23 (.56)	3054	-5.63	-34.89

Table 4.11: Prediction Correlation.

data. There is the possibility of improper handling of the test boards causing cracks due to mechanical loading (PC board bending). Test chambers are often stopped during a test that last several weeks or months. An excessive number of stops in the test usually affect the accelerated testing. The more number of chamber stops causes the irregular pattern of component failures. Control of the chamber to the specified thermal cycle test profile can be a problem. The event detector that monitors joint failure can malfunction.

On the simulation side, there are several simplifying assumptions made. Individual material layers are often omitted, and detailed features of the metal traces are rarely incorporated. There are singularities at the edges of the joint, so volumetric averaging of values is used. The averaging surely does not capture the true stress / strain distribution effects. A crack free joint is typically modeled, even though it is known that most of the life of a joint is spent in propagating a crack. Hence, the relative stiffness of the assembly increases as the joint cracks. The effect of this change in stiffness would also depend on the initial assembly stiffness and the degree of cracking in neighboring joints.

The prediction of 1% life or time-to-first failure needs careful attention. The predicted values may be vastly different depending on the parameter chosen. In most cases, the time-to-first failure may not correspond to 1% failure. This is especially true if the datasets are less than a 100 devices or more than 100 devices. The former may be true in most accelerated tests, while the latter may be true for most shipping products. For datasets of 30-40 devices, typical of accelerated tests, the time to first failure in fact corresponds to more than 1% failure. By the same token, the first failure in large volume shipping products may correspond to significantly less than 1% failure. The prediction of first failure largely depends on the shape parameter of the weibull distribution. A large value of the shape parameter (i.e. $\beta = 10 - 14$) may provide a time to first failure much closer to the characteristic life than a shape parameter of 2.5 – 3. In general the accuracy of the predictions can be improved significantly by better estimates of shape parameter for a given technology and thermal condition.

All of these factors, both experimental and analytical, combine to produce error in the predicted life correlation. If one is diligent about all the details, reasonable accuracy can be obtained. However, if the analyst makes additional errors, quite poor results are possible. Given the experimental and modeling variability the intent of the present effort is to eliminate some of the known sources of error in life prediction of automotive underhood electronics. The state-of-art damage relationships have been based on data from CBGA, on predominantly SMD pads and 62Sn36Pb2Ag solder. The packaging and board technologies have evolved over the years. Plastic BGAs are more frequently used in higher volumes than CBGAs. NSMD pads are favored over SMD pads because of better thermal fatigue reliability. Therefore, the data acquired in the present study represents typical electronic structures in material and architecture. Crack propagation and initiation graphs in the present study correlate well in shape and form with Darveaux's Data on CBGAs. However, the intercept and slope of the damage relationships differ significantly. While, graphically, the shift in the curve appears small on a log-log plot – the change is sufficient to reduce the prediction error with respect to experimentally measured data by 50%. Inelastic strain energy density is dependent on the mesh in ANSYS. The damage relationships in the present analysis have been derived for a mesh size of 1.5 mils close to the interfaces. Analysts using the published damage constants should therefore use a mesh thickness of 1.5 mils for correlation. It is possible that the lower inelastic strain energy densities have lower crack propagation slopes. Most of Darveaux's data on CBGAs was acquired over a very large range of inelastic strain energy density. Thus, changes in the slope at the lower end of the spectrum may not have been detected. The present data set will be populated with more devices and crack propagation rates and even lower inelastic strain energy densities will be measured in undergoing studies.

4.10 Conclusions

It has been shown that a better correlation of model prediction with experimental data can be obtained with the revised relationships. Since modeling methodology and solder constitutive behavior has not been varied between the two studies – it is reasonable to assume that the variation in predicted life is due to the damage relationships. Probable sources of difference may include – crack propagation data acquired predominantly on ceramic BGAs and SMD pads in previous studies versus plastic BGAs and NSMD pads in the present study. An additional difference is the use of High T_g printed circuit boards in the present study with 63Sn37Pb solder versus a mix of high-T_g and FR-4 boards with 62Sn36Pb2Ag in the previous studies. The new damage relationships imply a lower sensitivity to increase in inelastic strain energy density for both crack initiation and crack propagation than previously believed indicated by a smaller slope. The main objective of this study was to build a better solder damage relationship for the underhood application that can minimize the predicted error. In most cases predicted error with respect to experimental data has been reduced by approximately 50%. More accurate results can be predicted by carefully measuring the crack growth data on a large sample size.

CHAPTER 5

DAMAGE MECHANICS OF ELECTRONICS ON METAL-BACKED SUBSTRATES IN HARSH ENVIRONMENTS

5.1 Introduction

In this section, the reliability of electronics directly mounted on the engine and transmission has been investigated. Increased shock, vibration, and higher temperatures necessitate the fundamental understanding of damage mechanisms which will be active in these environments. Electronics typical of office benign environments uses FR-4 printed circuit boards. Automotive application typically use high glass-transition temperature laminates such as FR4-06 glass/epoxy laminate material (T_g = 164.9°C). In application environments, metal-backing of printed circuits boards is being targeted for thermal dissipation, mechanical stability and interconnections reliability.

The test vehicle is a metal backed FR4-06 laminate. The printed circuit board has an aluminum metal backing, attached with pressure sensitive adhesive (PSA). Component architectures tested include – plastic ball grid array devices, C2BGA devices, QFN, and discrete resistors. Reliability of the component architectures has been evaluated for HASL.

Crack propagation and intermetallic thickness data has been acquired as a function of cycle count. Reliability data has been acquired on all these architectures. Material constitutive behavior of PSA has been measured using uni-axial test samples. The measured constitutive behavior has been incorporated into non-linear finite element simulations. Predictive models have been developed for the dominant failure mechanisms for all the component architectures tested.

Currently most harsh environment electronics are designed to withstand a temperature range of – 40°C to +125°C. These systems must also typically meet automotive vibration requirements while exceeding 10 years and 100,000 miles of operation. To limit the effects of the vehicle environment, electronics modules are often separated from the mechanical systems which they control. Locations like vehicle "firewalls" and fender wells offer the ability to sink module-generated heat while reducing exposure to temperatures created by the mechanical systems and allowing some access to airflow available under-the-hood. However, these modules are constantly under pressure to improve thermal efficiency while reducing cost. The effect of temperature cycling on the reliability of microelectronic packages is the topic of much research.

Increasing automotive engine controller functionality, plus smaller and hotter engine compartment are placing greater demands on the thermal design of engine control modules. The traditional method of adding the heat sinks with the component (e.g. Transistors) on the printed circuit board (PCB) is very costly and provides significant thermal resistance to the surroundings. The thermal requirements have been met with improved heat-sink design, and thermal attachment materials promoting thermal conductivity between the electronics and the module casing. Traditional module using double sided reflowed components and thermally conductive pads to thermally connect the substrate and the metal housing. This design increases the material cost of the module by adding the thermal enhancing material and creates an added manufacturing process for attaching the thermal pad to the housing. While this design meets the thermal and reliability requirements for the module, the system design is not optimal

Metal-backed substrates are attractive alternative from the thermal point of view. An alternative to the previous design involves, structurally attaching the metal directly to the substrate providing a direct thermal path. This design has the added advantage of allowing the metal to act as a module "cover" and employs a single-path manufacturing process. Utilizing this design significantly reduces the module system cost, and improves product quality by limiting the assembly to single-pass reflow exposure. However, attaching the metal directly to the substrate (FR-4) increases the assembly's effective coefficient of thermal expansion (CTE).

Metal backed printed circuit board's disadvantage of high coefficient of thermal expansion relative to bare FR4-06, leads to increased susceptibility to solder joint fatigue failure due to thermal cycling. The focus of this research is to evaluate the system-level issues related to metal-backed substrate interconnections reliability, damage mechanism, provide modeling techniques to further investigate design alternatives, reliability prediction, and to provide recommendations to automotive system designers.

In this work, the effect of metal-backed boards on the interconnect reliability will be evaluated. The crack propagation data as a function of thermal cycle has been collected. The cycles-to-crack initiation and the crack propagation rate have been benchmarked with the previous non-metal backed board studies. Solder crack propagation as a function of electrical resistance has also been investigated. The relationship between the normalized resistance changes with the crack propagation has been investigated. Other failure mechanisms investigated include –delamination of PCB from metal backing. Non-linear finite element analysis has been used to develop predictive models, which have been correlated with experimental data.

5.2 Test Vehicle

Test vehicle was designed to evaluate the performance of metal-backed technology, using components and materials available for high volume automotive programs. The test vehicle targeted both the thermal efficiency and the component reliability of a wide variety of substrate, attachment, and encapsulant options. The substrates used were standard HASL finished high glass-transition temperature, glass-epoxy laminate (FR4-06) attached to 2.54 mm aluminum with a variety of adhesives. Crack propagation data was acquired on printed circuit boards attached with pressure sensitive adhesive (PSA). The boards contain six trace layers to simulate the thermal mass of a true production board, though all functional traces were run on the topmost layer. All pads on the board were non solder mask defined (NSMD) and had a HASL finish. The resistor and BGA daisy chains were routed to plated-through holes at the edge of the board where soldered wire connections could be made for use in resistance monitoring during the thermal cycling tests. A photograph of an assembled test board is shown in Figure 5.1. The Component test matrix of this project is provided in Table 5.1. A typical Cross-Section of an uncycled 15 mm BGA on metal-backed boards with other

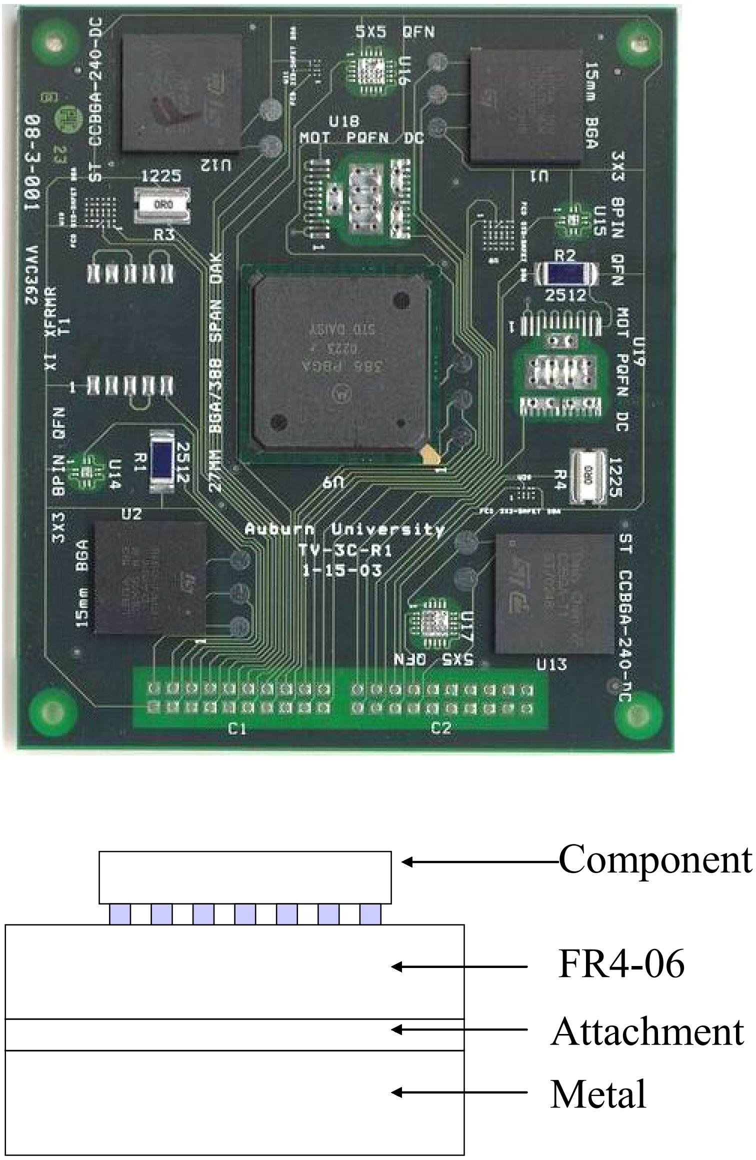


Figure 5.1: BGA and Chip Resistors Test Vehicle.

Body Size	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	BT Thickness (mm)	BT Pad Diameter (mm)	BT Pad Type	Ball Diameter (mm)
27 mm BGA	388	1	36 (6X6)	10X10X0.35	.56	.5	SMD	.60
16 mm C2BGA	240	.8	None	5.0X5.0X0.23	.56	.45	SMD	.53
15 mm BGA	193	.8	25 (5X5)	8.6 X 8.6 X 0.37	.56	.4	SMD	.60

Table 5.1: Component Test Matrix.

adjacent material layers are shown in the Figure 5.2. Components analyzed include I/O counts in the range of 193 to 388, I/O pitch in the range of 0.8mm to 1mm, and package sizes in the range of 15mm to 27mm. Resistors including 2512 and 1225 have also been included in the study. The test board contains two 15 mm BGA, one 27 mm BGA, two 16 mm C2BGA, two 2512 chip resistors, and two 1225 chip resistors.

5.3 Reliability Testing

Thermal cycling (-40 to 125°C) of the assembled test boards was performed in a Blue-M environmental chamber. The thermal cycle duration was 90 minutes, with 20 minutes at each extreme. Typical thermocouple results from under a component on the test board are illustrated in Figure 5.3.

A total of 39 boards were used for the crack propagation study. The boards were placed vertically in the chamber, and the wiring passed through access ports to the data acquisition system. Monitoring of the various daisy chain networks was performed throughout the cycling using a high accuracy digital multimeter coupled with a high performance switching system controlled by LabView software. Failure of a daisy-chain network was defined as the point when the resistance change became 10 Ω or higher.

Component failure in this section is assumed to mean failure of the solder joints that form the electrical connection between the component and the circuit board. The resulting failure data were statistically analyzed using two parameter Weibull models. The standard

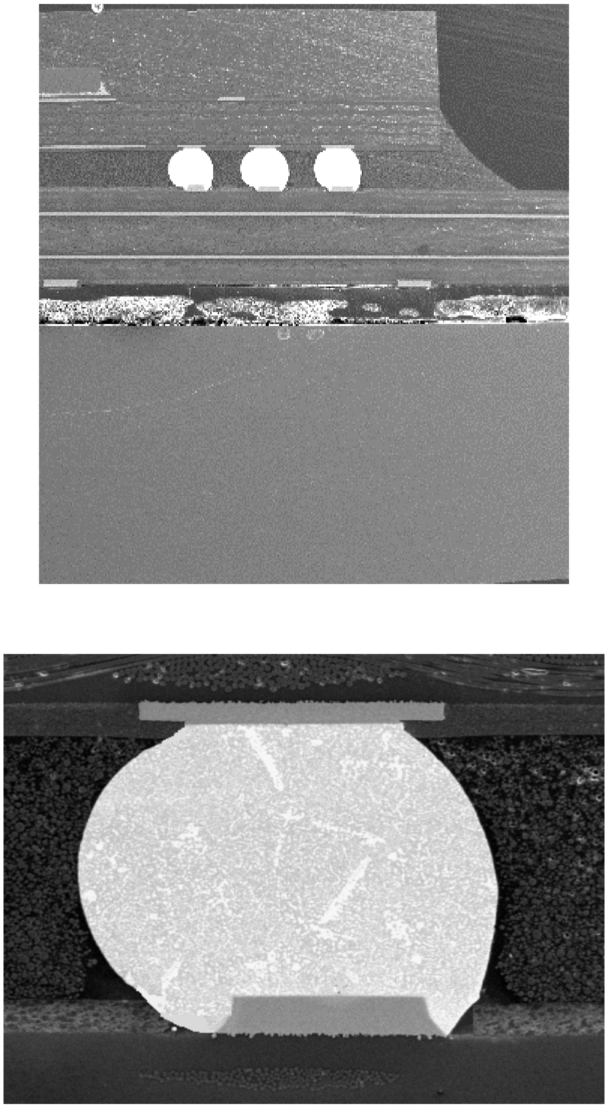


Figure 5.2: Images of Uncycled 15 mm BGA Cross-Section.

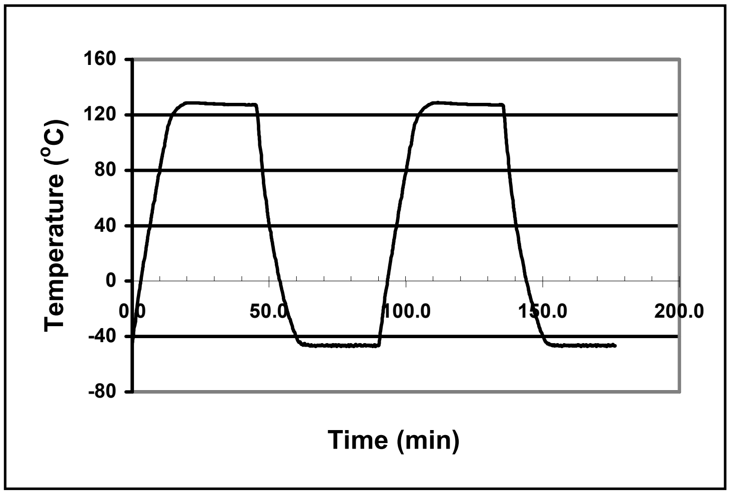


Figure 5.3: Test Board Thermal Cycle (-40 to 125 °C).

parameters in such an approach are the Weibull Slope β, and the Characteristic Life η, which is the number of cycles required to fail 63.2% of the samples from a particular component of the test matrix. From these values for a particular component configuration, the cumulative failures (percent) after any number of thermal cycles can be predicted. When comparing the various component reliabilities in this study, we have used the value of $N_{1\%}$, the number of cycles necessary to cause 1% of the parts in a sample set to fail.

The primary investigation of this research was to find a solution (or series of solutions) that will offer the needed thermal performance while meeting the reliability requirements. Ideally, the design would have the thermal performance of direct attachment to the metal while having the same reliability of components attached to laminate substrates without metal. This creates the need for the attachment material to have properties providing very good thermal conductivity while providing mechanical decoupling between the laminate and the metal. In this test vehicle PSA has been selected for both reliability and crack growth measurement studies

5.4 Reliability Data

Reliability data on 2512 resistors has shown that PSA provides higher thermal fatigue reliability than arlon, although lower reliability than bare FR4-06 (Figure 5.4). All the configurations have very similar β-slopes, in the neighborhood of 3-4, indicating similarity in failure mechanism, which is solder joint fatigue in this case. Data is consistent with expected behavior. Closed-form computations indicate that introducing metal back-planes will cause serious degradation in the life expectancy of the solder joints associated with the BGA and resistors components. The coefficient of thermal expansion of metal backplanes (e.g. aluminum has coefficient of thermal expansion 23.6 ppm/°C) is greater than that of FR4-06. A coupled assembly consisting of metal-backed laminate will have a higher effective coefficient of thermal expansion. This greater thermal expansion causes additional stress in the solder joints of the components and degrades component life (Figure 5.4).

Effect of various supplemental restraints including, selective encapsulation and conformal coats has also been examined. Only marginal improvements in reliability have been noticed. Addition of conformal coating improves the characteristic life cycles but reduces the shape factor for bare-FR406.

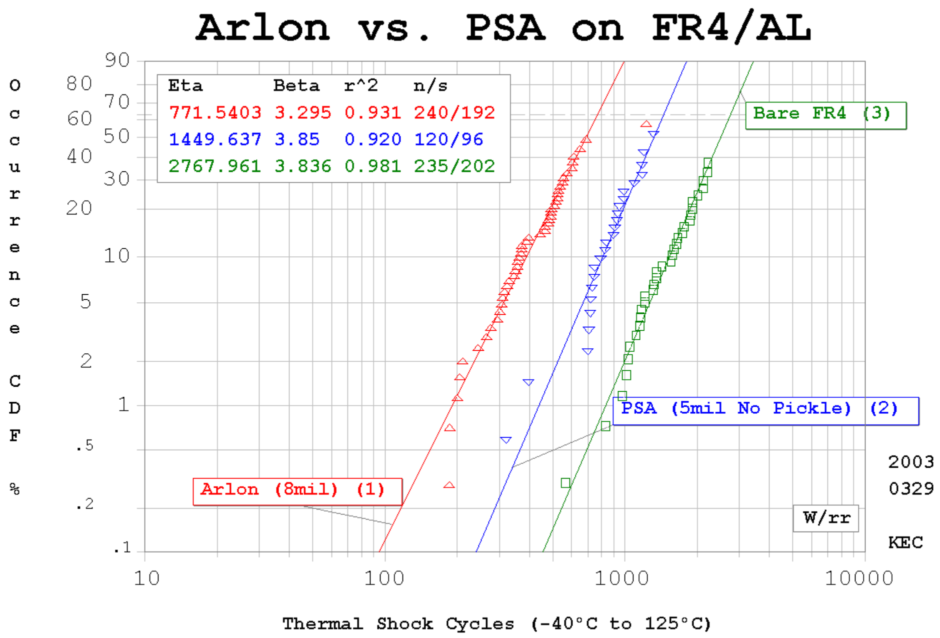


Figure 5.4: Effect of Aluminum Metal Backing on Reliability of 2512 Resistors with Arlon and PSA Adhesives.

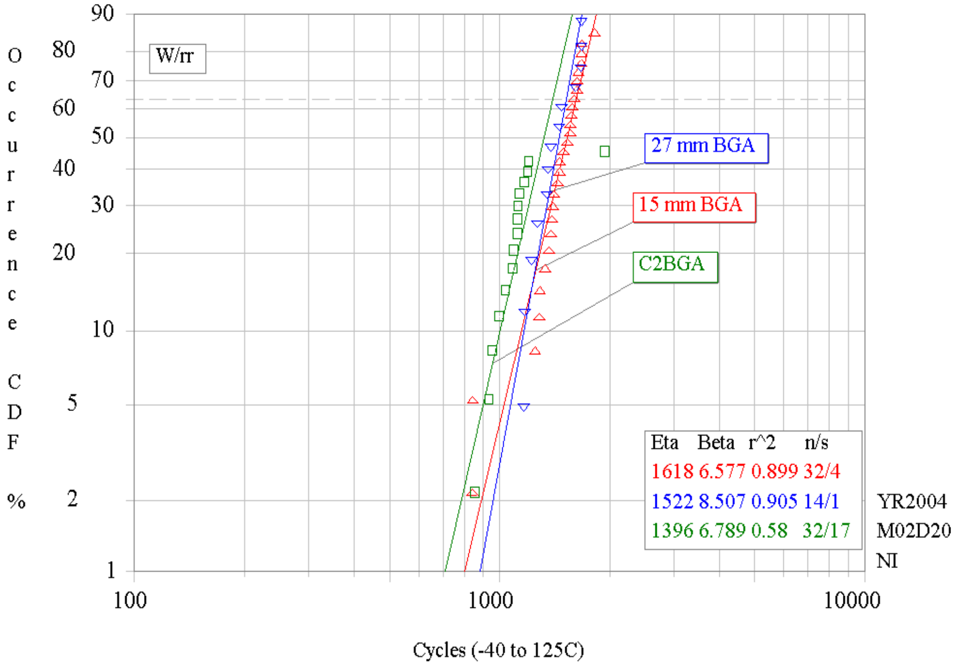


Figure 5.5: Weibull Plot of 1% Failure for BGA Component

The Weibull reliability data plot for the metal-backed BGA components is shown in Figure 5.5. Data indicates, that the relative reliability of the various components is strongly related to the die size. The 15 mm BGA and 27 mm BGA exhibited comparable reliabilities relative to each other, as shown in the plot, of time-to 1-percent failure. The 27 mm BGA exhibited a time-to 1-percent failure of 900 cycles. The C2BGA exhibited a time-to1 percent failure of 700 cycles. The 2512 resistors exhibited lower reliability than 1225 resistors (393 cycles). The 2512s are primarily composed of ceramic material; they have a CTE much lower than that of FR4-06. It is important to note that none of the packages exceed the desired 2000 cycle requirement on metal-backed substrates. All the packages have very similar β-slopes, indicating similarity in failure mechanism, which is solder joint fatigue in this case.

5.5 Crack Growth Measurement

5.5.1 Experimental Techniques

Samples were cross-sectioned at various level of thermal cycling. Several sections were made per sample to study the crack initiation and propagation in various rows. The cross-sections were characterized by scanning electron microscopy (SEM) using a JEOL JSM 840 instrument operated at an accelerating voltage of 20 kV. Thus, it was possible to obtain topographic contrast in secondary electron images (SEIs) of the polished samples without resort to etching. Backscattered electron images (BEIs) were also used to produce atomic number contrast (phases with a high average atomic number appear bright). All samples were imaged as polished.

5.5.2 Crack Propagation Measurement

Extensive failure analysis has been performed on the 15 mm, C2BGA, 27 mm BGA, 2512 and 1225 chip resistor solder joints, and only the highlights will be presented in this paper. Dedicated specimens for cross sectioning are also the parts of electrically monitored test matrix were removed from the cycling chamber after every 125 thermal cycles. Three test boards were periodically removed form the chamber after every 125 cycles. The samples were polished to match the measured crack length. Cross section measurements were validated by prying-off some of the samples. Fatigue cracks were typically found to initiate at package pad-to-solder interface and then propagate along a path parallel to the substrate pad (for BGA components) until complete separation (Figure 5.6 – 5.9). In most cases, solder joint cracking occurred simultaneously at both the top and bottom of the solder joint (Figure 5.7). In almost all cases, the primary crack initiated at the package interface and later a secondary crack initiated at the board interface. Once the primary crack initiated, it progressed to other edges of the joint, and caused complete failure.

The 2512s exhibited faster crack propagation compared to 1225s. Cracked initiated underneath the part for resistors and then typically follow along a path that parallels the resistor termination then it goes to bulk solder until complete separation has occurred. Once the crack initiate at 2512 parts, it propagated very faster rate compared to the other types of packages on the metal-backed boards. The typical 2512 crack initiation and propagation is shown in Figure 5.10 and Figure 5.11.

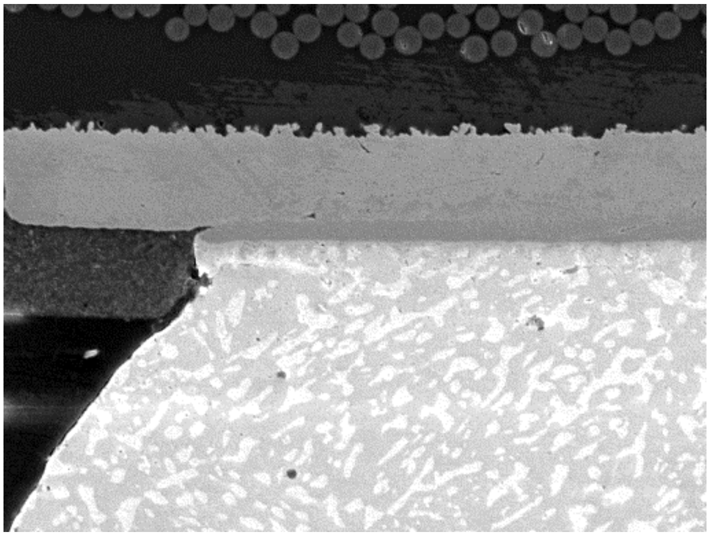


Figure 5.6: Image of Crack Initiation, Corner Ball, 15 mm BGA.

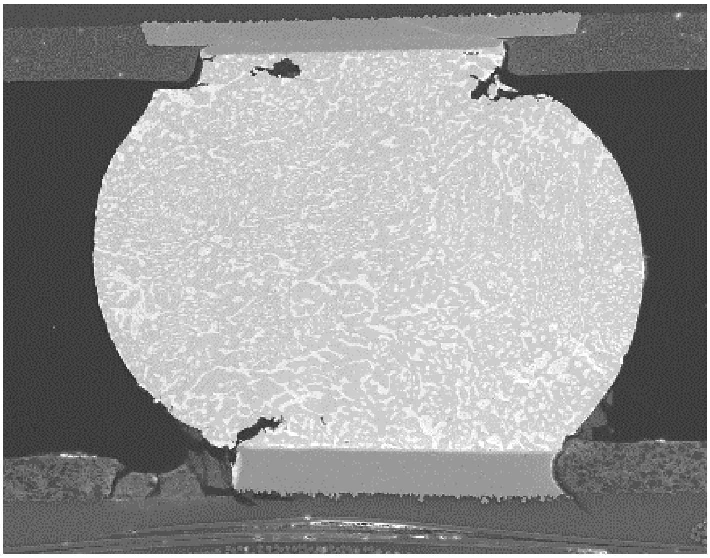


Figure 5.7: Simultaneous Crack Propagation Top and Bottom of the Solder Joint, 16 mm C2 BGA

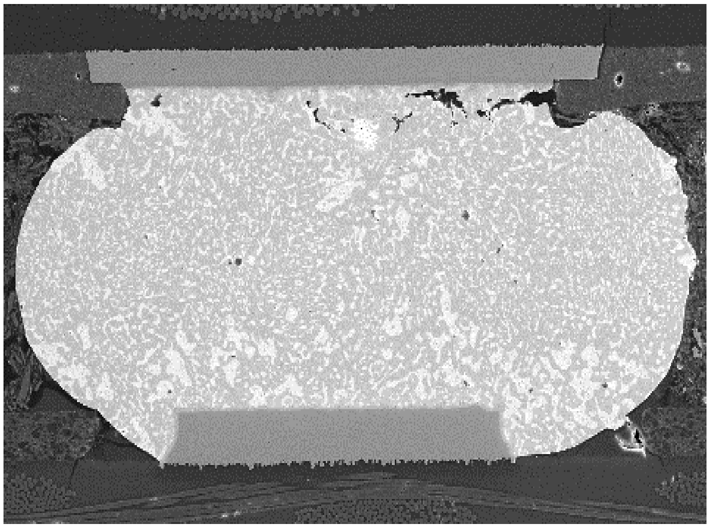


Fig 5.8: Simultaneous Crack Propagation Top Left and Right Corner of the Solder Joint, 27 mm BGA, Thermal Ball after 1000 Cycles

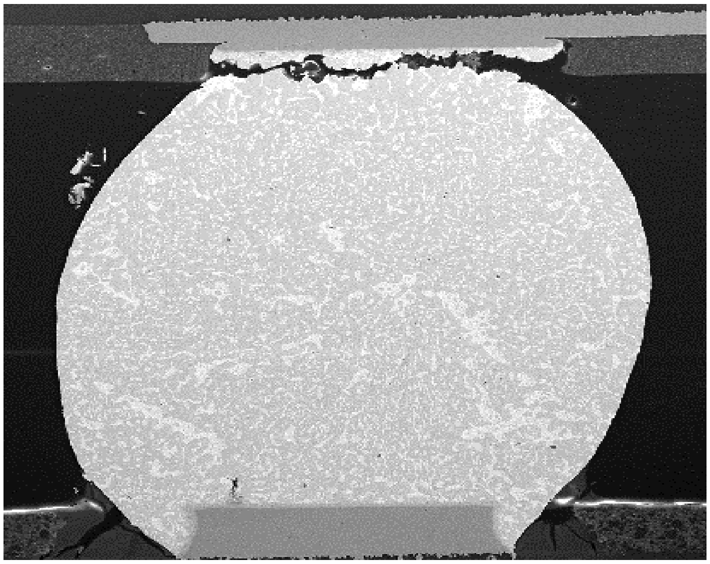


Fig 5.9: Typical X-Section of a Completely Cracked Solder Joint, C2 BGA after 750 Cycles

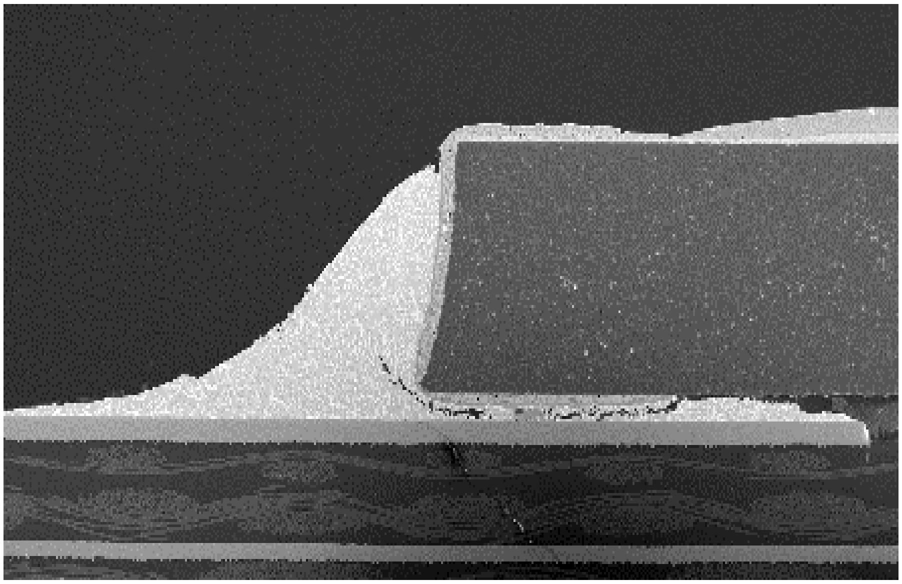


Figure 5.10: Typical Image of Crack Initiation and Propagation of 2512 Chip Resistor Solder Joint.

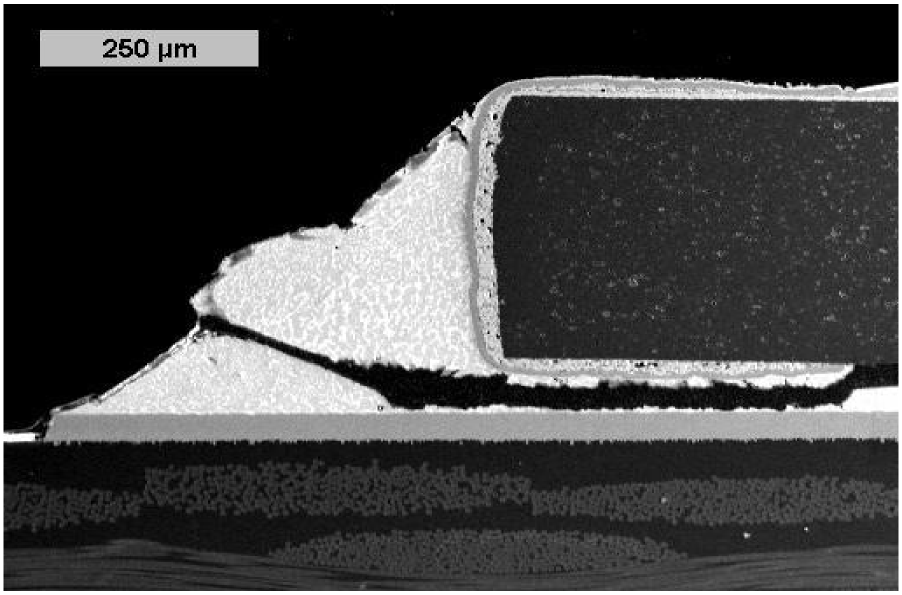


Figure 5.11: X-Section of a Completely Cracked 2512 Resistor

Solder joint cracks have been measured at each temperature cycling data-interval. An average value of crack length across samples has been calculated for each set and cycle-count. The typical crack length with the cycle count for BGA components is shown in Figure 5.12. In this figure, 27 mm BGAs perimeter fails faster than the 15 mm BGAs and same trends has been observed in the case of thermal balls shown in Figure 5.13. In the case of chip resistors, larger physical size parts fail faster than smaller sizes because of distance to neutral point which leads higher thermal strain in the solder joints. This mismatch becomes more accentuated for components with metal-backed boards. The typical crack length with the cycle count for discrete components has also been measured and plotted (shown in Figure 5.15). Crack growth rate in 2512 component is much higher than the 1225 parts (shown in Figure 5.15) because of the distance to neutral point which leads higher thermal strain in the solder joints. The characteristics solder joint length in Z direction for of 1225 parts is much higher than the 2512 resistors, which leads to lesser thermal strain and higher reliability compared to 2512. The crack growth data in this study indicates that characteristic crack growth rate stays fairly uniform during the thermal cycle tests. The primary and secondary crack lengths have been added and plotted together with the number of thermal cycles (Figure 13-15). Table 5.2 shows the crack initiation and crack propagation rates for each of the data sets. The number of crack initiation cycles has been found by solving the regression fit of the data for a crack length of zero. It is seen that the crack initiation only accounts for a range of 3 to 16.5 %

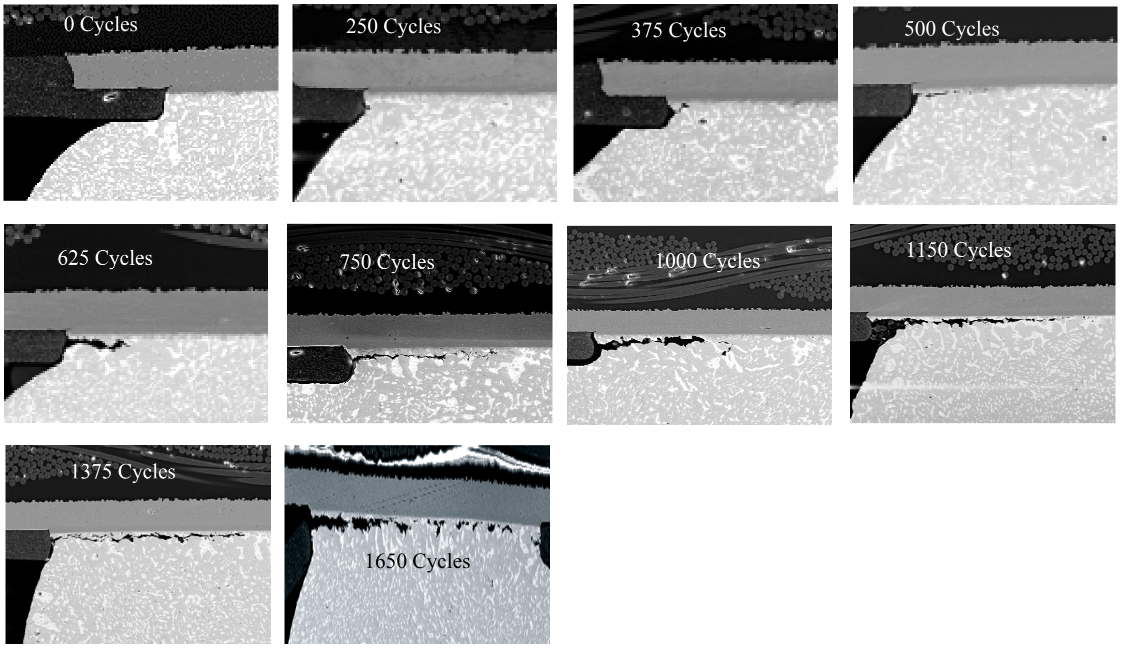


Figure 5.12: 27 mm BGA Solder Joints Crack Propagation or Growth on Metal-Backed Boards at Various Levels of Thermal Cycling (-40 to 125°C)

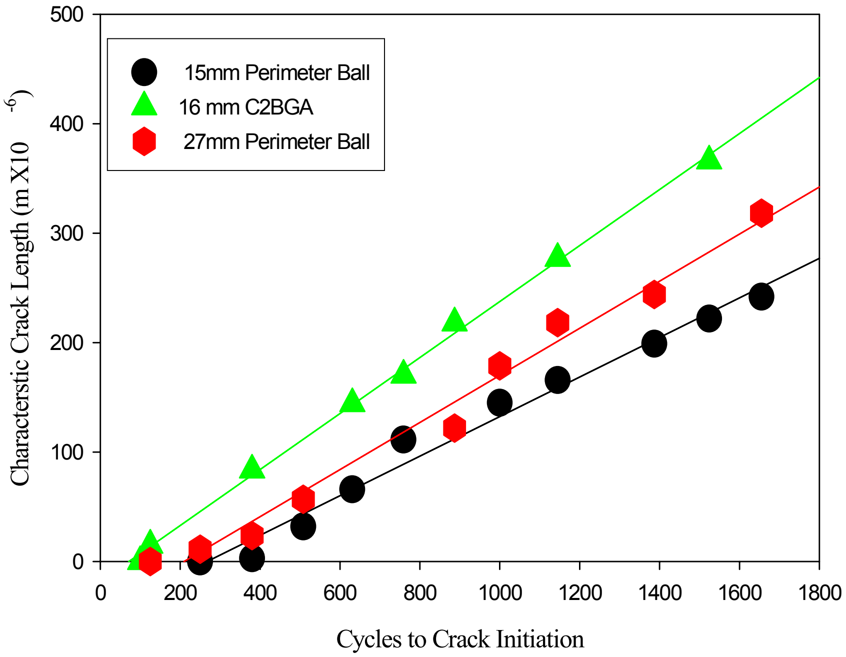


Figure 5.13: Crack Propagation Data for 15 mm BGA, 16mm C2BGA, and 27 mm BGA Perimeter Balls

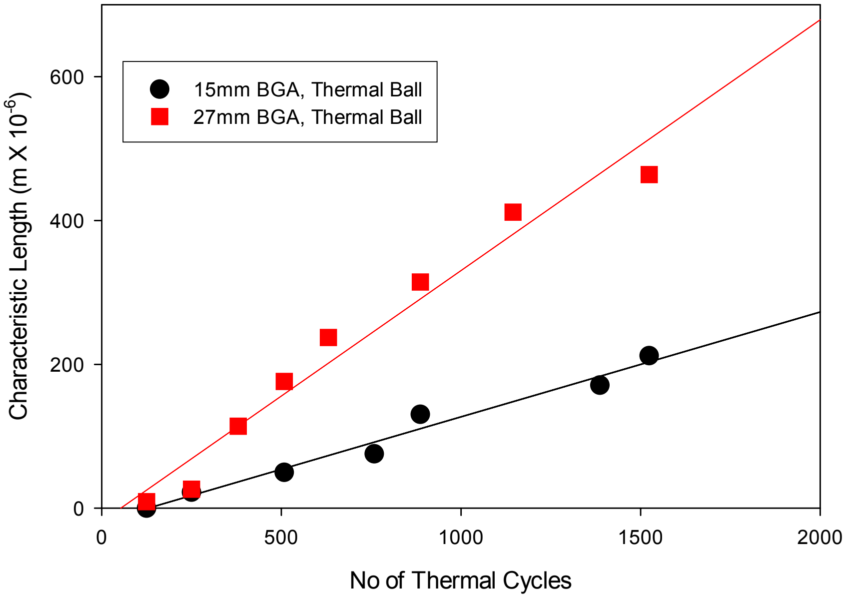


Figure 5.14: Crack Propagation Data for 15 mm and 27 mm BGA Thermal Balls

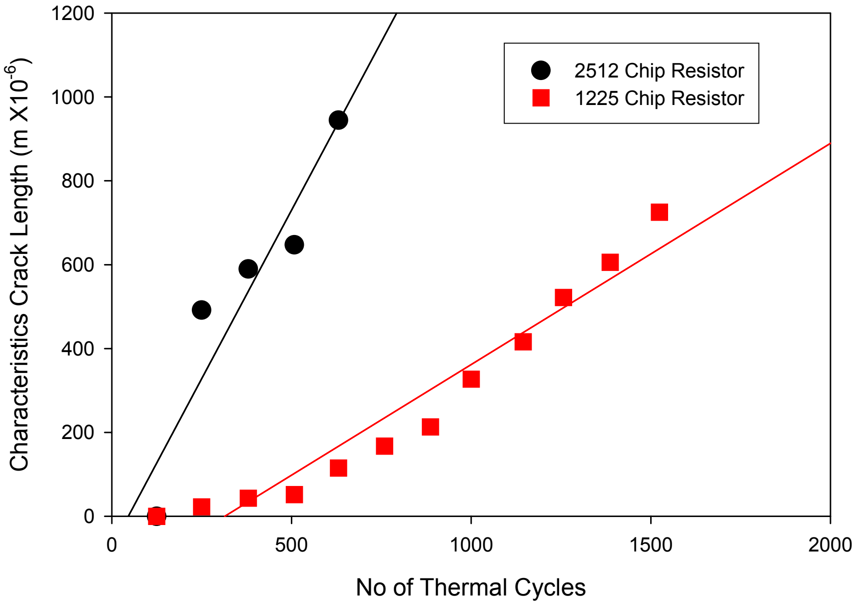


Figure 5.15: Crack Propagation Data for 2512 and 1225 Chip Resistors

Package Type	Crack Initiation Cycle	Crack Growth Rate (µ inch/Cycle)
15 mm (perimeter)	382	10.32
15 mm (thermal)	105	4.98
C2BGA	37	10.12
27 mm (perimeter)	156	5.63
27 mm (thermal)	160	22.27
1225 Chip Resistor	122	7.17
2512 Chip Resistor	59	61.28

Table 5.2: Crack Initiation and Crack Propagation Rates on Metal-Backed Boards.

of the fatigue life (Table 5.2). Components with the highest inelastic strain energy density showed the largest crack propagation rate and the lowest time to 1-percent failure. In this case, the 2512 resistor has been found the highest crack propagation rate (Table 5.2).

5.6 Intermetallic Growth Behavior

Intermetallic layers can be formed at elevated temperature or sometimes at storage temperature. Intermetallic compound can be identified as indication of good bonding, but in reality a brittle fracture has been found in the Intermetallic layers because of brittle nature of the Intermetallic compounds. Intermetallic growth was monitored as a function of cycle count. Intermetallic growth, which generally starts right after the solder reflow, is fairly thin prior to thermal fatigue damage. Studies on intermetallic growth of Cu-Sn compounds [35-37] show that two types of intermetallic compounds are generated namely Cu_3Sn on the copper pad side and Cu_6Sn_5 on the eutectic solder side. The metal backed samples in this study exhibited formation of thicker intermetallic layers. The loss of Sn resulting from its diffusion with Cu result in further localized coarsening of the eutectic solder microstructure where Pb-rich regions are observed adjacent to the Cu_6Sn_5 intermetallic layer (Figure 5.16). The growth of intermetallic compounds at the solder ball/pad interface in microelectronic joints may weaken the joint considerably. Intermetallic compounds on metal-backed boards have been found to be consistent with those on non-metal backed boards.

5.7 Materials Model

Linear and non-linear, elastic, plastic, creep, temperature and time dependent and time-independent material properties have been incorporated in the finite element models. It is well known that solder is above half its melting point at room temperature which is why time-dependent creep phenomena dominate solder joint fatigue.

The thermal fatigue failure of electronic packages is associated with combined plastic-deformation and creep of solder joints. One of the most popular and useful method to describe the solder material behavior during temperature cycling is the Anand material model [25]. This unified viscoplastic isotropic hardening model mainly describes the rate-dependent inelastic deformation characteristic of the material (creep behavior), but it disregards an explicit yield point and time independent plastic deformation. It uses nine material parameters to describe the strain rate as a function of the applied stress, the material deformation resistance and of the temperature. On the other side, the deformation resistance of the material depends on the strain rate value due to strain hardening or strain softening effects. This leads to a recursive formulation of the equation system, which is made up of the strain rate equation and of the evolution equation for the deformation resistance. How these equations are connected to each other can be seen in Figure 5.17. The parameter sets of Anand model for Sn63/Pb37 solder has been tabulated in Table 5.3. Four different adhesives have been used in this test board. Typical adhesive CTE's are measured to incorporate into the finite element models (Table 5.4).

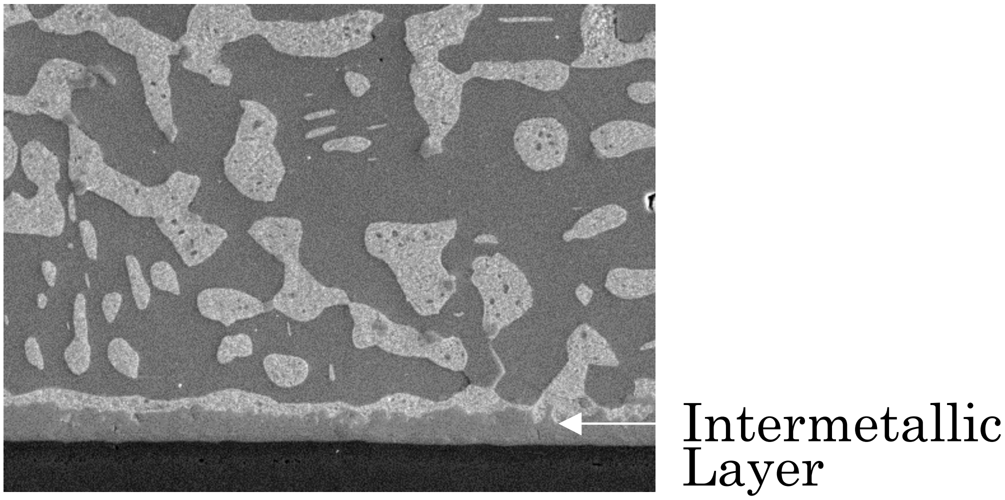


Figure 5.16: Typical Intermetallic Formation after 625 Cycles (40 to 125°C).

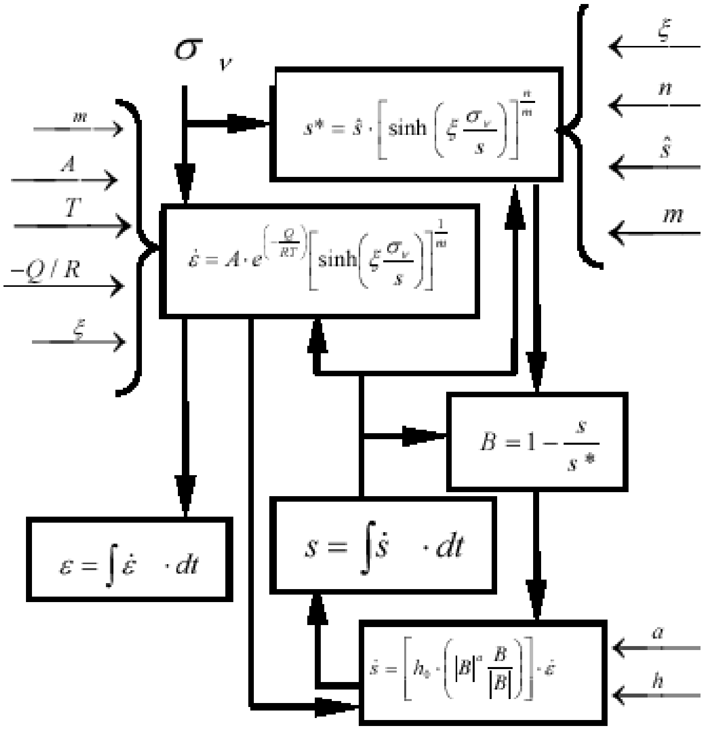


Figure 5.17: Anand Material Model [88]

Parameter	Value	Definition
S_0 (MPa)	12.41	Initial Value of Deformation Resistance
Q/k (1/K)	9400	Activation Energy/ Boltzmann's Constant
A (1/sec)	4.0E6	Pre-Exponential Factor
ξ (dimensionless)	1.5	Multiplier of Stress
m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
h_0 (Mpa)	1378.95	Hardening Constant
s^ (Mpa)	13.79	Coefficient of Deformation Resistance Saturation Value
n (dimensionless)	0.07	Strain Rate Sensitivity of Saturation (Deformation Resistance) Value
a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

Table 5.3: Values of Anand Constants used for Simulation.

Adhesive	Metal	CTE (PCB Side) [1/°C]	CTE (Metal Side) [1/°C]
Arlon	Aluminum	16.15×10^{-6}	24.37×10^{-6}
PSA (5 mil)	Aluminum	15.29×10^{-6}	23.67×10^{-6}
PSA (10 mil)	Aluminum	15.42×10^{-6}	13.05×10^{-6}
Prepreg (1-ply)	BeCu	15.18×10^{-6}	17.70×10^{-6}

Table 5.4: Room Temperature CTEs of Metal-Backed Adhesives.

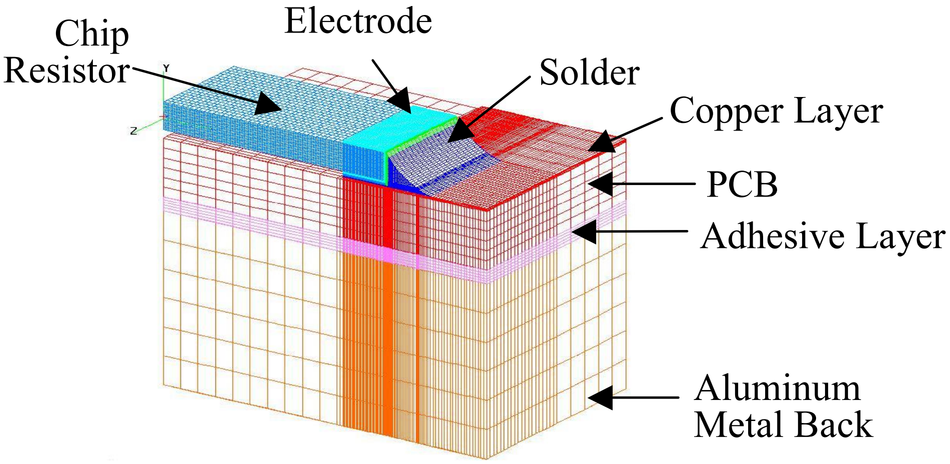
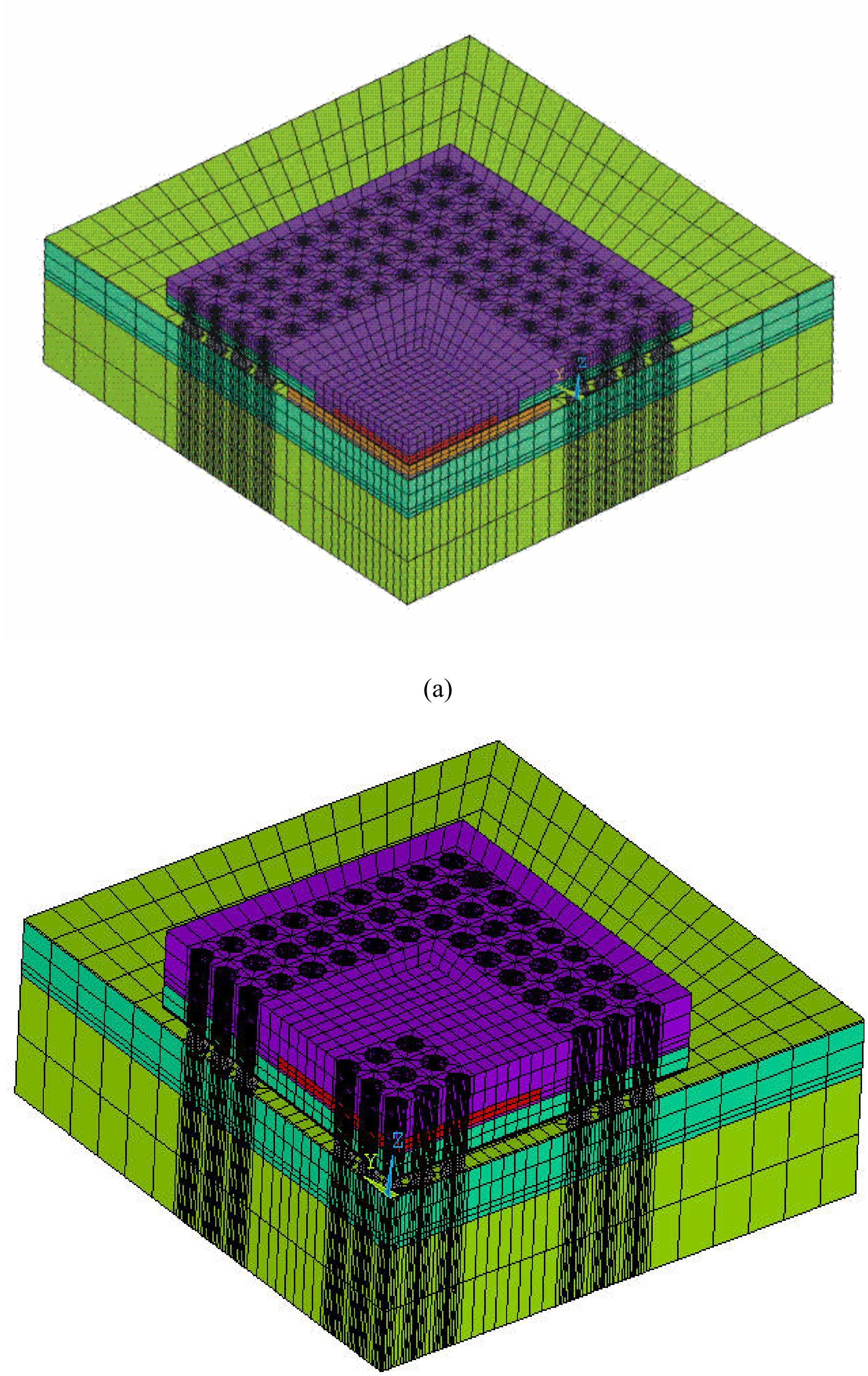


Figure 5.18: 2512 Quarter Symmetry 3D Mesh Plot on Metal-Backed Board.



(a)

(b)

Figure 5.19: 3D Quarter Symmetry Finite-Element Mesh for
(a) C2BGA Assembly (b) 15mm BGA

5.8 Finite Element Model

Solder ball elements were meshed in ANSYS™ with VISCO107 elements, whereas all other package materials were meshed with SOLID45 elements. Figure 5.18 and Figure 5.19 show the 3D quarter symmetry finite element models for 2512 chip resistor, C2BGA and 15mm BGAs mounted on metal backed FR4-06 laminate. ANSYS™ was used to simulate the thermal cycle fatigue. The quarter symmetry model was used with mapped finite element mesh that varied from approximately 40,000 nodes and 35,000 elements to 90,000 nodes and 81,000 elements depending on the complexity of the geometry and the number of solder balls. In most of the cases the corner solder ball is the critical joint and of highest deformation. Some initial fatigue life results on metal-backed components are shown in Table 5.4. The damage prediction is based on crack propagation relationships presented in Lall, et. al [8] with the modifications to crack initiation cycles and crack propagation rate presented in the current paper.

5.9 Crack Growth Correlations

The inelastic strain energy density has been correlated with the measured crack growth data. The viscoplastic strain energy density values were volume-averaged over the interface elements. The typical interface layers are two element layers of 1.0 mil thickness. Experimental data on crack propagation has been mapped with the inelastic strain energy density of components on metal-backed boards from nonlinear simulations. Figure 20 shows the comparison of some initial results of cycle-to-crack initiation vs. inelastic strain energy density. Cycles to crack initiation in BGA's on metal-backed boards have been benchmarked w.r.t crack propagation data in ceramic ball-grid arrays on non-metal backed boards reported in Darveaux [5-7] and crack propagation data in plastic ball-grid arrays on non-metal backed boards reported in Lall, et.al. [8]. Darveaux's damage relationships [5-7] were derived on CBGA assemblies, with predominantly SMD pads and 62Sn36Pb2Ag solder. In addition to significant differences in the crack propagation paths for the two pad constructions, SMD pads fail significantly faster than PBGA assemblies. Crack propagation in CBGA's is often observed predominantly on the

Package Size	Time-to-1-percent Failure ($N_{1\%}$)	
	FEM (Cycles)	Experiment (1%) (Cycles)
15 mm BGA	670	785
16 mm C2BGA	643	709
27 mm BGA	848	900
2512 Chip Resistor	399	393

Table 5.5: FEM Results on Metal-Backed Boards.

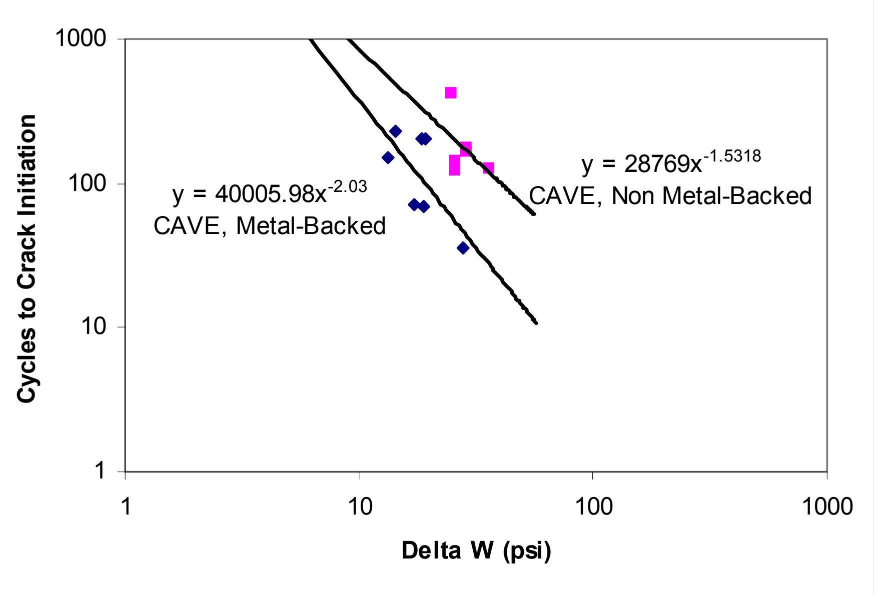


Figure 5.20: Comparative Crack Initiation/Unit Inelastic Strain Energy Between Metal/Non-Metal Boards

NSMD pads in thermal fatigue. The thermal mismatch on CBGA's is much larger than package side as opposed to both package and board side for PBGAs. Lall, et.al. [8] damage relationships were developed on plastic ball-grid array packages on high T_g laminates with NSMD pads. Data indicates that ball-grid arrays on metal backed boards exhibit lower cycles to crack initiation for all solder joint inelastic strain energy densities.

Figure 5.21 shows the propagation rate per unit inelastic energy on metal-backed and non-metal-backed boards. Crack propagation rate in metal backed boards has been measured to be 1.7x higher than ball-grid array packages with same inelastic strain energy densities on non metal-backed. Therefore, components on the metal-backed boards would have lower reliability than non metal-backed.

5.10 Effect of Isothermal Aging on Metal/Non Metal-Backed Boards

The choice of isothermal aging rather than thermal cycling aging in this investigation is owing to the fact that the isothermal aging process shows a higher coincidence with what happens in the practical application case (high temperature storage, such as burn-in) than the thermal cycling aging process [79]. In this study both metal and non metal backed boards with similar types of components are included in the test vehicles. The test vehicles are aged at 125^0C for 163, 300, 488, and 707 hours respectively. After isothermal aging, both samples are subjected to be molded in an epoxy resin, following the cross sectioning and polishing of the test vehicles for examination. In order to appropriately identify the thickness of the intermetallic compound layer, a wet grinding on successively finer grit abrasive papers is utilized, using from 600 grit through 2400 grit abrasives. Subsequently, the test vehicles are successively polished with .5 μm diamond abrasives on a rotating polishing wheel covered with a synthetic polishing cloth. The mean thickness of the interfacial intermetallic compound layer is measured using a powerful image processing system (IMAQ Vision Builder). Average intermetallic thickness has been measured on both the package side and PCB side. A significant difference in Intermetallic layer thickness has been observed between the metal-backed and non metal-backed boards. Figure 5.22 shows the Intermetallic thickness as a function of time for both metal and non metal-backed boards. The Intermetallic growth rate is almost the same in metal/non metal boards but the threshold value of thickness in metal-backed substrate is at least 50% higher than the non metal-backed substrates. Main reason for higher threshold Intermetallic layer in metal-backed substrate is the peak reflow temperature (232^0C in metal and 210^0C in non metal condition). Figure 5.23 and 5.24 show the comparison of intermetallic growth rate vs. $(\text{aging time})^{1/2}$ between the metal-backed and non metal-backed substrate condition for PCB and package side respectively. Similar to the intermetallic growth effect of solder microstructures on isothermal aging has been investigated for metal and non metal condition. A significant difference in grain growth rates has been observed between metal and non metal boards (shown in Figure 5.25). The grain growth rate in metal backed condition is found at least 25% higher than the non metal condition (shown in Figure 5.26). Moreover the higher Intermetallic and grain growth rate in metal-backed boards causes the potential impact of component reliability in extreme environment.

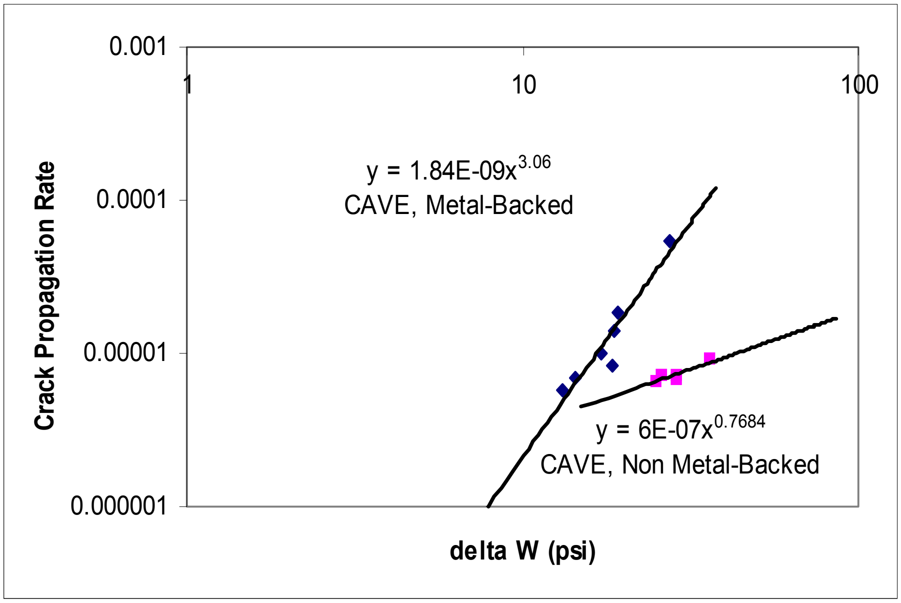
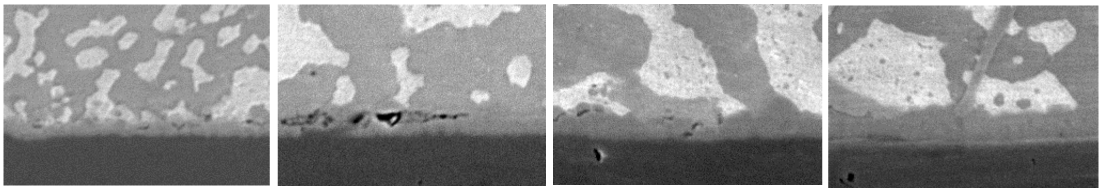
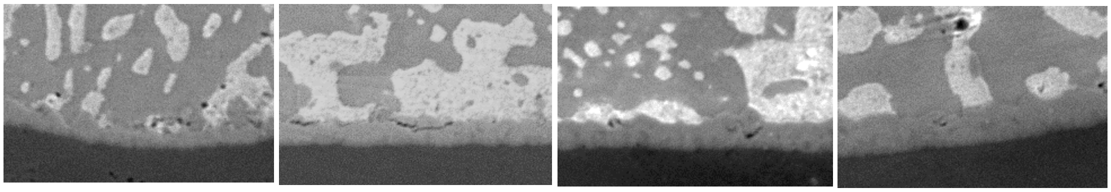


Figure 5.21: Comparative Crack Growth Rate/Unit Inelastic Strain Energy Between Metal/Non-Metal Boards.



163 hour 300 hour 488 hour 707 hour

Non Metal-Backed Board



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Metal-Backed Board

Figure 5.22: Intermetallic Thickness as a Function of Time for Both Metal and Non Metal Backed Boards.

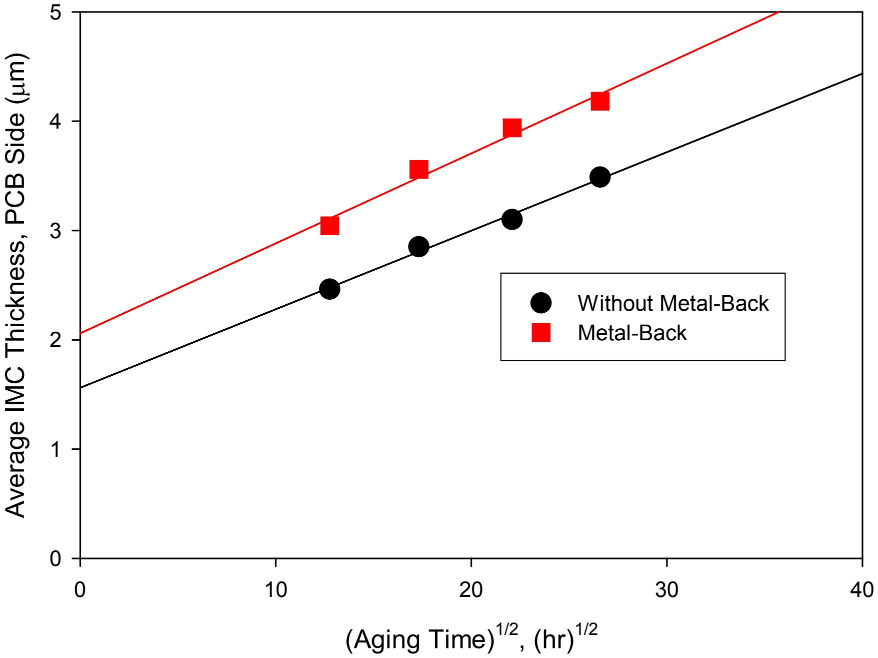


Figure 5.23: A Comparison of Intermetallic Compound Growth vs. (Aging time)$^{1/2}$ Between Metal and Non Metal at PCB Side

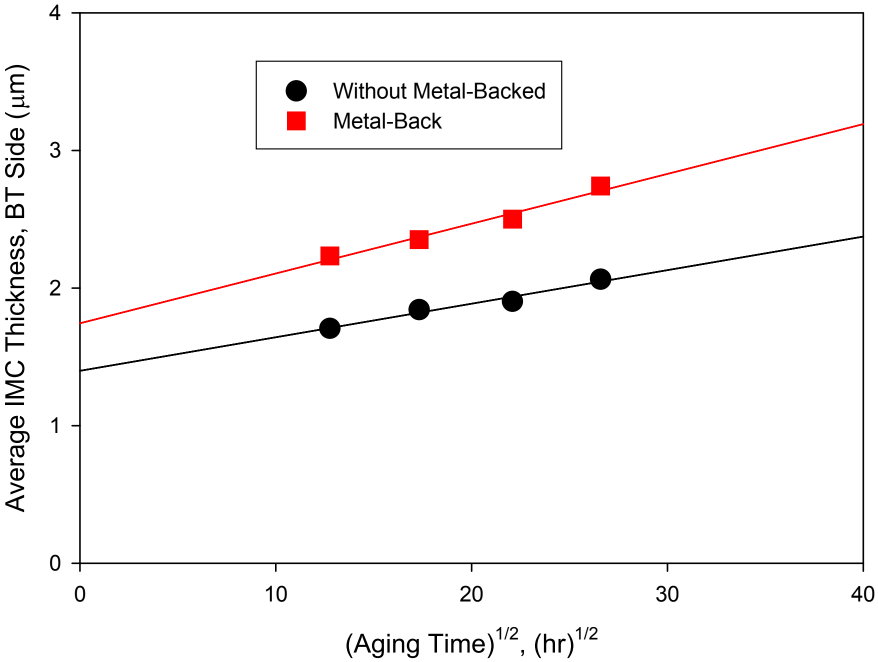
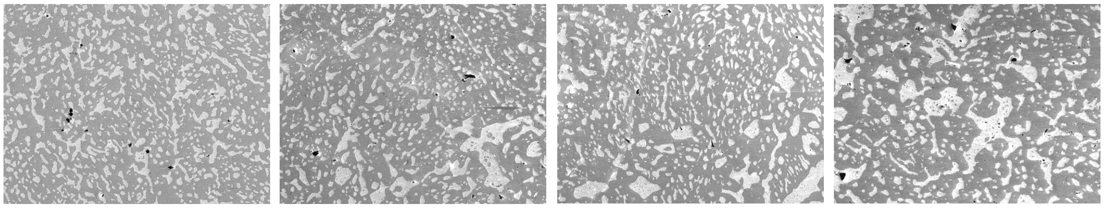
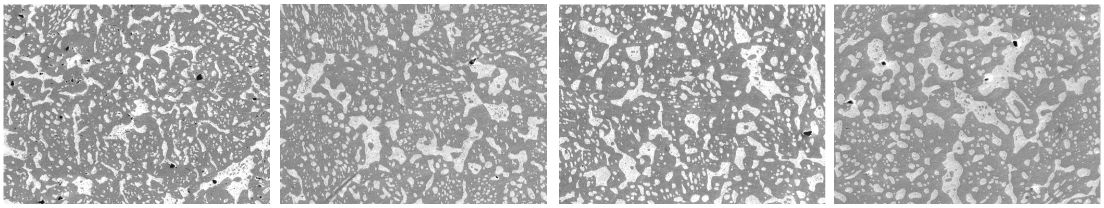


Figure 5.24: A Comparison of Intermetallic Compound Growth vs. (Aging time)$^{1/2}$ Between Metal and Non Metal at Package Side



163 hour 300 hour 488 hour 707 hour

Without Metal-Back Board



163 hour 300 hour 488 hour 707 hour

Metal-Back Board

Figure 5.25: Solder Grain Growth Rate as a Function of Time for Both Metal and Non Metal

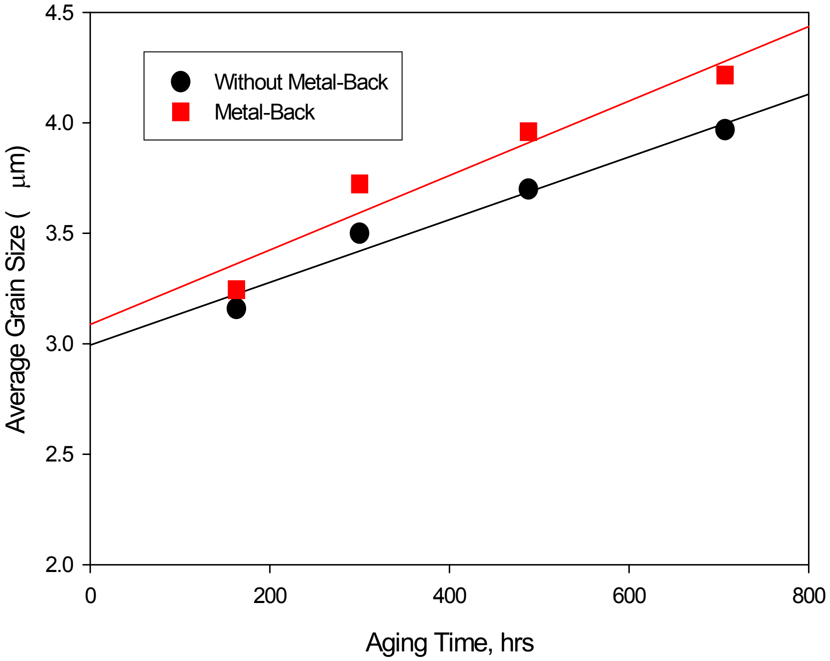


Figure 5.26: A Comparison of Solder Grain Growth vs. (Aging Time) Between Metal and Non Metal at Package Side

5.11 Conclusions

Results demonstrate that the metal backing of organic laminates (i.e., FR4-06) plays a critical role in meeting the reliability goals for harsh environments. The addition of metal backing increases the CTE of the substrate and creates potential reliability issues for many electronic packages. Thus, there exists a trade-off between an increased path for thermal conductivity and reduction in the overall reliability on metal backed boards. The crack measurements show that crack propagation rate on metal backed boards is much faster (≈ 1.7x) than non-metal backed boards. Further, ball-grid arrays on metal backed boards' exhibit lower number of cycles-to-crack initiation than packages on non-metal backed boards for any inelastic strain energy density.

CHAPTER 6

IMPACT OF MODELING METHODOLOGY ON ACCELERATED LIFE CORRELATION OF THERMAL FATIGUE COMPONENT FAILURES

6.1 Introduction

Finite element analysis (FEA) is a widely used for reliability prediction of solder joint reliability. A well known issue in this type of analysis is the presence of singular points in the FEA model, causing the predicted stress/strain in particular to be dependent on the level of mesh refinement. Finite element analysis results are generally used to predict the fatigue life of electronic packages. The typical result parameter strain or energy dissipation (ΔW) values are use to estimate the solder joint fatigue life using an empirical equation for some particular loading conditions. Generally the highest strain solder ball is used for solder fatigue life estimation. The location of highest strain/energy solder joint is typically depends on the DNP (distance to neutral point) parameters. Typically the highest strain/energy is found at the corner solder ball. The peak inelastic strain energy density (ΔW) values in finite element analysis usually depend on mesh density, due to singular points in the model. As the simulation is driven by mesh-dependent peak value, predicted life model is also likely to be meshing dependent. Generally the simplification of the 2D plane and 3D slice model gives inaccurate behavior [38, 89]. In some cases it is sufficient to study the trends of the packages with the simplified material properties.

To study the actual behavior of the packages, 3D model with fine mesh and accurate materials nonlinearity must include in the modeling. The damage volume is defined as the volume of the solder elements that has been selected for averaging the strain energy density (ΔW) in the highest strain region. The optimal damage volume of the solder is the choice of few elements selected from the highest strain solder ball. The selection of damage volume for averaging the strain energy density (ΔW) in the highest strain region is very significant in the solder joint life prediction model. The number of elements and the thickness of the interface elements are very important in calculating the damage volume. The average field quantity values decrease with increasing the damage volume. Darveaux recommends the damage elements from the interface between the eutectic solder and the copper pad. Number of interface layers typically varied from one to three. He developed the damage relation for three different interface layers thickness. His damage models behavior also depends on finite element model configurations (slice or quarter model). Vendevelde et al. [38] found that the selection only the top layer of elements overestimate the effect of solder joint shape, and underestimate the effect of distance to neutral point. He mentioned that optimal damage volume is a choice of a few elements selected out of two layers of elements near the location of highest strain. Instead of selecting only a few interface element layers, some of the researchers [45, 49] considered the entire solder ball as the damage volume. The main objective of this study is to optimize the damage volume of solder ball for thermal fatigue life reliability model. The damage volume is optimized by different types of BGA packages from different vendors.

Suhling et. al. [89] reported that extensive experimental results showed that maximum damage area typically found at the top of the solder ball. In some cases, solder joint cracking occurred simultaneously at both the top and bottom of the solder joint. Since the fatigue failure occurred top and bottom interface side, so both side crack growth data should be considered during damage volume study. Researchers [38, 7] have been studied the thermal fatigue failure only on the top interface layer of solder joint, but they never considered the bottom interface layer. Darveaux considered both primary and secondary crack growth data based on the top interface layers. In this work both top and bottom solder interface volume has been considered as damage region.

In this study, the optimal damage volume for fatigue life estimation of different PBGA solder (Sn63/Pb37) joint under different thermal cycle conditions have been investigated. BGA quarter symmetry packages have been analyzed with nonlinear Anand viscoplastic model [25]. In the simulation the actual scenario is as follows.

In the first cycle the inelastic strain energy induced in the solder joint cause's very minor damage. After many thermal cycles the accumulation damage results a minor crack at the intermettalic of the joint. Once the crack initiates the continuous accumulation of the damage propagates the crack along the intermettalic layer of the solder joints that leads to a complete joint failures. The initiation of cracks due to the damage accumulation depends on the local stress-strain distribution. In this case presence of crack influences the local stress-strain distribution, thus the prediction of crack propagation is dependent on the mesh refinement of the models.

In the actual thermal cycle, the microstructure of the eutectic (Sn63/Pb37) solders changes with the time and temperature that should be implemented in the simulation. Because of the complex simulation and enormous time involvement, this effect is ignored in this study. A simplified consideration is followed to achieve the most realistic outcomes. In this study, the amount of strain energy density (ΔW) induced per thermal cycle is calculated to measure the damage of the material. The ΔW in ANSYS can be calculated as

$$W_1 = \frac{\sum (PLWK)_e . V_e}{\sum V_e} \qquad \text{(eq.6.1)}$$

$$W_2 = \frac{\sum (PLWK)_e . V_e}{\sum V_e} \qquad \text{(eq. 6.2)}$$

$$\Delta W = W_2 - W_1 \qquad \text{(eq. 6.3)}$$

where, W_1 is the average plastic work of the damaged volume in the 1st thermal cycle, W_2 is the average plastic work of the same damaged volume in the 2nd thermal cycle, $(PLWK)_e$ is the plastic work of each damaged element, V_e is the volume of the element, and ΔW is the difference in plastic work between two consecutive thermal cycles over the damaged volume.

A correlation between the simulated strain energy density (ΔW) and experimental 1% solder joint reliability results in an empirical equation. Typically, 1% failure has been considered as crack initiation life cycles. A robust and efficient simulation technique has been used to achieve an optimal solder joint reliability. The final empirical model depends on chosen material properties of the solder, the selected damage parameter, and the finite element model consideration (slice or quarter model).

Several ways of damage volume calculation are systematically analyzed. Empirical relation for one layer of 1.5 mils, 1.0 mil, and 0.5 mils interface element thickness has been made. The effect of two and three layers of .5 mils thickness and full solder volume of highest strain ball has been investigated. The main objective of this study is to find an optimal damage volume for the solder fatigue empirical relation that can be used for fatigue crack initiation life ($N_{1\%}$) of any surface mount packages. In this study, an accurate correlation has been developed between the simulated inelastic strain energy density (ΔW) for optimum damage volume and the number of thermal cycles to 1% failure found by Weibull plots. The empirical model has been analyzed with all kind of damage volume as described.

6.2 Package Descriptions

A set of packages were selected from different vendors. For this test study, there are 10 different package configurations have been selected. The package sizes vary between 8 mm to 27 mm. The BGA components in this study are both SMD and NSMD type with two different BT thickness as well as PCB thickness. Figure 6.1 shows a typical FlexBGA with different packaging materials. The typical PCB use in this work is two metal layers, FR-406 glass/epoxy laminate material (T_g = 164.9°C), copper traces with different board finishes. In the actual experiment the packages are mounted on the printed circuit board. In the case of flexBGA polyimides flex substrate has been used. In this study eight PBGAs, three flexBGAs and one TABGA have been simulated.

The BGA package parameters included in the current study are tabulated in Table 6.1. In the actual test, the packages have been subjected to air-to-air temperature cycle.

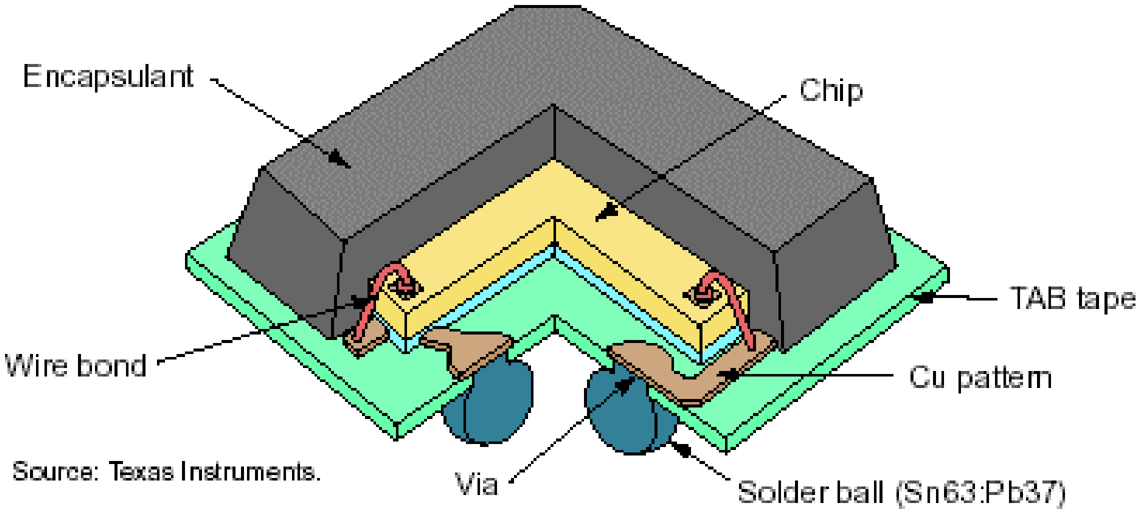
In this study the thermal cycle profile varies from vendor to vendor. Typical thermal cycle profile for different vendors is shown in the Table 6.2.

6.3 Failure Mechanism

In an earlier study [8], extensive failure analysis has been performed on the 15, 17, and 23 mm BGA solder joints. Thermal cycling fatigue crack initiation and failures were typically found at the top of the solder joint (package side). Usually the crack initiation occurred in the high strain regions near the corner of the NSMD/SMD pads. Crack growth typically proceeds across the entire joint, near intermetallic layer close to the package pad interface. In most cases, solder joint cracking occurred simultaneously at both the top and bottom of the solder joint (shown in the Figure 6.2). In almost all cases, the primary crack initiation starts at the package interface followed by a secondary crack initiation at the board interface. Once the primary crack initiation occurred it propagates to the other edges of the joint, and causes complete solder ball failure. The crack surface in the above figure indicates that thermal fatigue is the main failure mechanism.

6.4 Materials Model

Linear and nonlinear, elastic, plastic, creep, temperature and time dependent and time-independent material properties have been incorporated in the finite element models. It is well known that solder is above half its melting point at room temperature that’s why time-dependent creep phenomena dominate solder joint fatigue. The thermal fatigue failure of electronic packages is associated with combined plastic-deformation and creep



Source: Texas Instruments.

Figure 6.1 - Typical Flex BGA Cross-Section (Source: Texas Instruments)

Vendor	Package Type	Body Size (mm)	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	Substrate Thickness (mm)	Substrate Pad Diameter (mm)	Substrate Pad Type	PCB Pad /PCB Thickness	Ball Diameter (mm)
CAVE	PBGA	15	132	1	None	8.6 x 8.6 x .37	.38	.4	NSMD	NSMD/1.6	.60
	PBGA	15	132	1	None	8.6 x 8.6 x .37	.56	.4	NSMD	NSMD/1.6	.60
	PBGA	17	172	1	16 (4x4)	8.6 x 8.6 x .37	.38	.4	NSMD	NSMD/1.6	.54
	PBGA	23	168	1.27	None	8.6 x 8.6 x .37	.56	.6	NSMD	NSMD/1.6	.76
AMKOR	PBGA	15	160	1	None	6.5x6.5x.35	.56	.5	SMD	NSMD/1.6	.50
	PBGA	17	256	1	None	8.7x8.7x.35	.56	.5	SMD	NSMD/1.6	.50
	Flex BGA	12	132	.8	None	9.5x9.5x.3	.038	.35	SMD	NSMD/1.6	.50
	Flex BGA	12	144	.8	None	9.5x9.5x.3	.038	.35	SMD	NSMD/1.6	.45
	Flex BGA	12	144	.8	None	9.5x9.5x.3	.038	.35	SMD	NSMD/.85	.45
	TABGA	8	96	.5	None	6.5x6.5x.3	.038	.25	SMD	NSMD/1.6	.30

Table 6.1 - Package Parameters

Vendor	Low Temp °C	High Temp °C	Ramp Up Time (sec)	Dwell Time High (sec)	Ramp Down Time (sec)	Dwell Time Low (sec)
CAVE	-40	125	900	1800	900	1800
AMKOR (PBGA)	-40	140	720	180	720	180
AMKOR (FlexBGA)	-40	125	900	900	900	900

Table 6.2 - Profile for Temperature Cycle Chamber

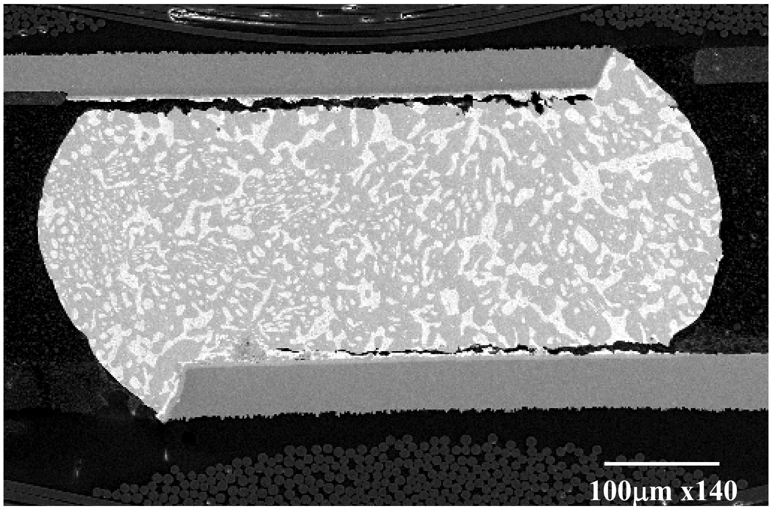


Figure 6.2 - Simultaneous Crack Propagation Top and Bottom of the Solder Joint, 15 mm BGA, CAVE

of solder joints. Anand viscoplastic model, a standard material in ANSYS, which has been used by several researchers to model the constitutive behavior of solder, has been used in this study. This constitutive law has been used by Darveaux [5-7] in development of damage relationships. The constitutive behavior model has therefore been kept the same to enable benchmark of damage relationships.

6.5 Numerical Errors and Convergence

Modeling error refers to the difference between a physical system and its mathematical errors. Generally the finite element modeling results depend on the mesh density of the physical structure. A question that frequently arises in a finite element analysis is, "How fine should the element mesh be in order to obtain reasonably good results?" Unfortunately, no one can give a definitive answer to this question. But there are some well known techniques to resolve this critical issue. Discretization technique is one of them; it refers to the error caused by representing the infinitely many d.o.f. of a continuous mathematical model by a finite number of d.o.f. in its discretized form.

In the discretization technique, the volume of the discretized structure should be the same as the mesh density increases. The discritization error can sometimes be determined by the order of error analysis. For a sufficiently refined mesh, the error in the finite element solution is bounded by the error in approximating the exact solution by shape function interpolation. According to this technique, the error of linear interpolation between exact nodal displacements of two nodes is the function of characteristic element length or number of elements. The acceptable percentage of relative error due to different mesh refinements is less than 10%. In multimesh extrapolation method, it is possible to minimize the higher error to zero. This process is completely depending on the regular mesh refinement. In each refinement, nodes and interelement boundaries of the coarser mesh are preserved, both in numbers and location, while adding new nodes, and new boundaries. If only a few refinement results are used, and the convergence rate is unknown, a reasonable assumption should be made for convergence rate, where the convergence rate is a function of characteristic element length. The discretization error can be referred as

$$e = O(h^{2q-2m}) \qquad \text{(eq. 6.4)}$$

Where, h is the "characteristic length" of the brick element, $q-1$ is the degree of highest complete polynomial in the element displacement field, in this example $q-1$=1, and $2m$ is the order of highest derivative in the governing equilibrium equation expressed in terms of displacement, in this case (e.g. beam problem) $2m$=2. So the final form of discritization error is $O(h^2)$.

In case of multimesh extrapolation, eq. 6.4 can be used to calculate the error from two or more different meshes to extrapolate to an improved results of any field variable, ϕ. If convergence is monotonic and the order of error, $e = O(h^2)$, then an improved result ϕ^0 is obtainable by Richardson extrapolation as

$$\phi^0 = \frac{\phi_1 h_2^2 - \phi_3 h_3^2}{h_3^2 - h_1^2} \qquad \text{(eq. 6.5)}$$

eq. 6.5 gives a value of ϕ^0 for infinitesimal element size. The percentage of error for the last refinement can be computed as

$$e = \left| \frac{\phi_3 - \phi^0}{\phi^0} \right| 100\% \qquad \text{(eq. 6.6)}$$

A typical convergence test of field quantity ΔW (ϕ) for the solder ball with VISCO107 elements has been analyzed with three different type of mesh density. In this study, a simple solder ball with PCB, copper, and silicon has been modeled to calculate the ΔW of the solder elements. The number of elements in the solder ball varies from 400 to 25000 elements.

The error estimation due the mesh refinement has been taken place over a fixed damage volume. The damage volume in this study has been considered both corner and interface elements. The typical finite element mesh for the interface elements of solder ball has been shown in the Figure 6.3, the red dotted points are new element boundaries introduced by regular mesh subdivision. Three different mesh refinements have been done for error estimation, and convergence test. Both corner element and interface elements are selected for the convergence test in this study. As the refinement process goes, ΔW increases and convergence rate is quadratic. The typical quadratic convergence rate has been observed in the Figure 6.4 for the corner elements. Similar trends have been observed for the interface elements shown in Figure 6.5. The detail result of this study has been tabulated in Table 6.3. Between the two plots, interface elements convergence rate is faster than the corner elements. The percentage of error calculated for the interface elements are much lower than the corner elements because in this case, averaging few elements from the interface supersedes the singularity problem

6.6 Finite Element Analysis and Results

Figure 6.6 shows a typical 3D finite element mesh plot of 12mm flexBGA mounted on FR-4 board. Since the model is symmetric along X and Y axis, so quarter symmetric model has been drawn in this study. ANSYS 7.0 was used to simulate the thermal cycle experiments. The quarter symmetry model was used with mapped finite element mesh that varied from approximately 40,000 nodes and 35,000 elements to90,000 nodes and 81,000 elements depending on the complexity of the geometry and the number of solder balls. In most of the cases the corner solder ball is the critical joint and of highest deformation. The critical solder ball elements are very fine meshed (shown in the Figure 6.7). The quarter model has a symmetry boundary condition along the symmetry line of the full package and vertical movement is free along the corner edge (centerline) of the package. Figure 6.8 shows the highest deformation solder ball found at the corner of the package. The plastic work distribution of the critical solder ball is shown in the Figure 6.9. The plastic work distribution clearly shows that the interface elements are the highest inelastic strain deformation in the solder ball.

The core objective of this study is to optimize the solder damage volume and develop a simple relationship among different damage volumes of solder balls. Therefore all possible types of solder ball damage volumes are analyzed to average the inelastic strain after two thermal cycle load. The ΔW calculated for each damage criteria is

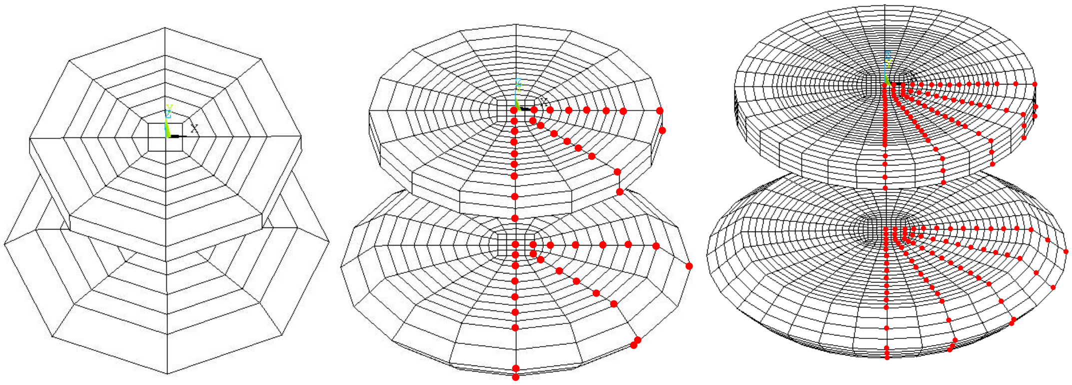


Figure 6.3: Finite Element Mesh of a Typical Solder Ball for Three Different Interface Element Refinements

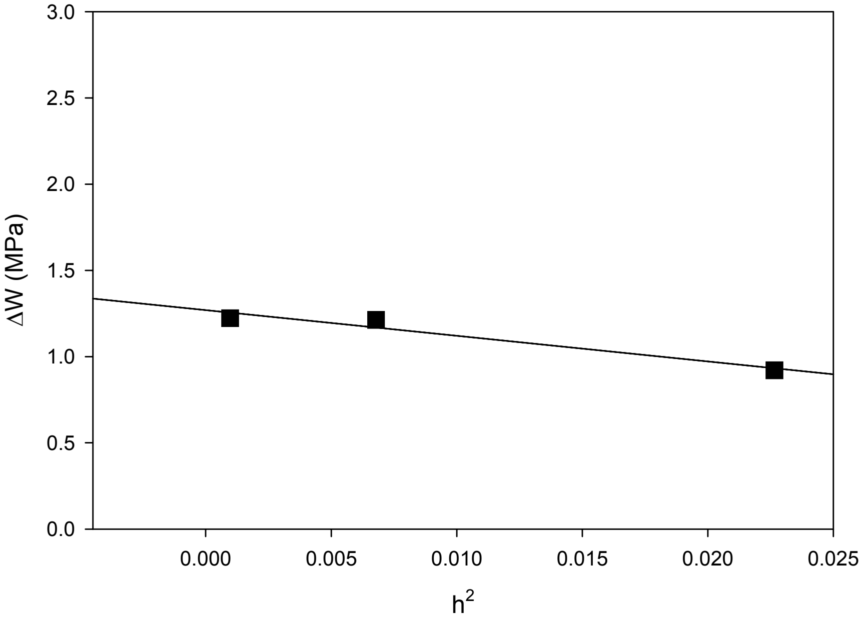


Figure 6.4: Quadratic Convergence of ΔW With Mesh Refinement of a Typical Solder Ball Corner Elements

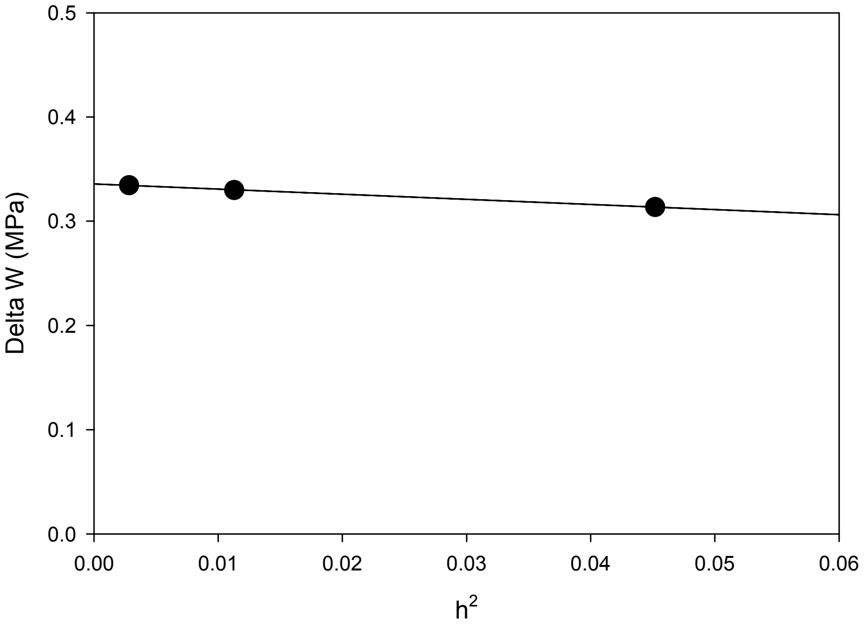


Figure 6.5: Quadratic Convergence of ΔW With Mesh Refinement of a Typical Solder Ball Interface Elements

Damage Region	Number of Elements	h	ΔW (MPa)	ϕ^0	% of Error
Corner Elements	1	.1505	.9209	1.2697	3.65
	8	.0824	.1213		
	64	.0312	1.2233		
Interface Elements	104	.2126	.3137	.3357	.357
	832	.1063	.330		
	6656	.05315	.3345		

Table 6.3: Computed ΔW for Figures 6.3-6.4, and Error Estimation

then plotted against 1% ($N_{1\%}$) failure cycle to develop a crack initiation relationship. The accuracy of each type of damage volume has been defined by the accuracy of the fitting (R-square) value. The relevant cases are shown in the Figure 10. Six different cases of damage volume have been analyzed in this study. Previous damage study [8] was based on one layer of 1.5 mils interface element thickness. Previous result is considered as the control of new analysis. Here the previous result is referred as the case 1, where the damage volume is the one element layer of 1.5 mils from both sides (package side and board side) of the highest strain solder ball. In this case total of 192 elements were selected form the interface layer for averaging the strain energy. The typical empirical relationships can be expressed as

$$\mathrm{Ln}\, N_{1\%} = .5369\, \mathrm{Ln}(\Delta W) + 8.5189 \qquad \text{(eq. 6.7)}$$

$$\text{or } N_{1\%} = 5008.7(\Delta W)^{-.5369} \qquad \text{(eq. 6.8)}$$

In this case, data are slightly scattered so the accuracy of fitting is lower. In the 2nd case, the damage volume is also the first element layer from both sides the highest strain solder ball. Here, .5 mils thickness interface element layers of 192 elements were selected for averaging the strain energy. In this case, data are slightly less scattered so the accuracy of fitting is little better than the 1st case. In the 3rd case, where each element layer is .5 mils, total of 384 elements were selected from the first two layers of the highest

strain solder ball, and hence a better accuracy of fitting than the case 2 has been obtained. In the 4th case, three layers of .5 mils thickness elements were chosen from the same solder ball and a lower fitting value is obtained. In the 3rd and 4th cases using two and three layers of .5 mils element thickness, predicts two different fatigue cycles.

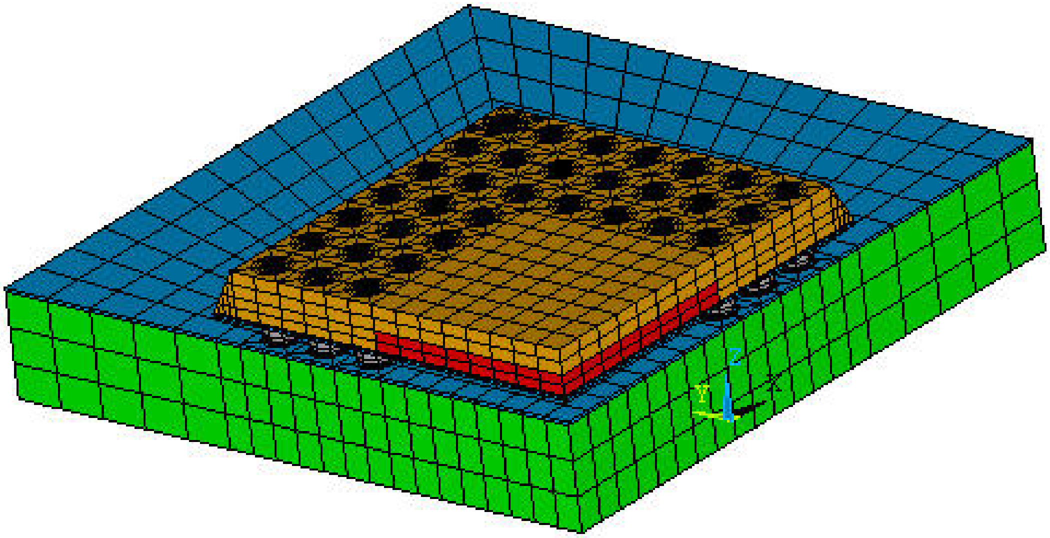


Figure 6.6: Typical Quarter Symmetry Finite Element Mesh Plot of FlexBGA

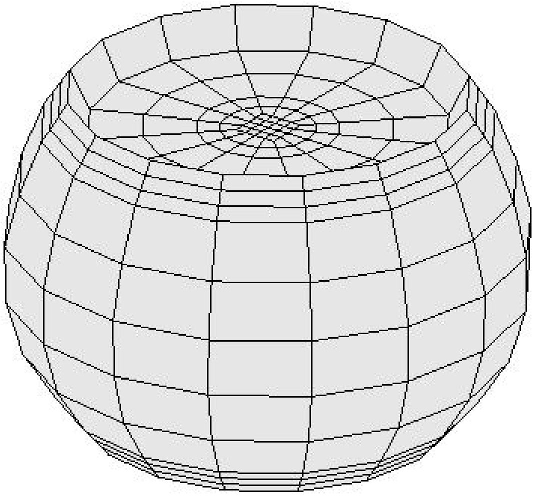


Figure 6.7: Highest Strain Solder Joint with Fine Mesh

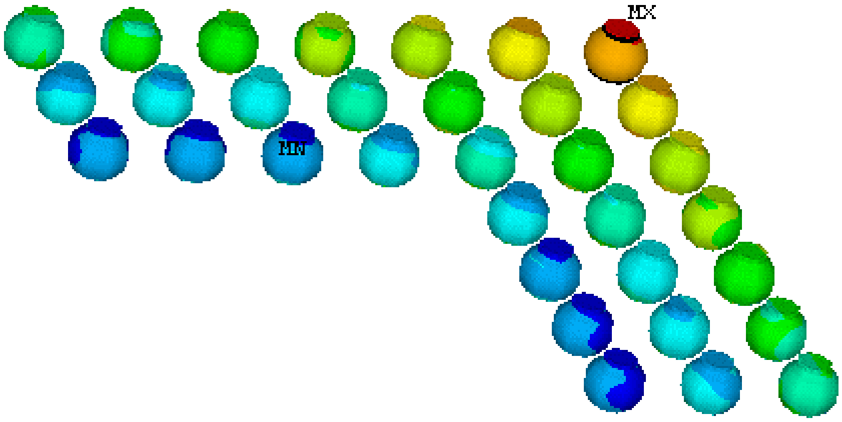
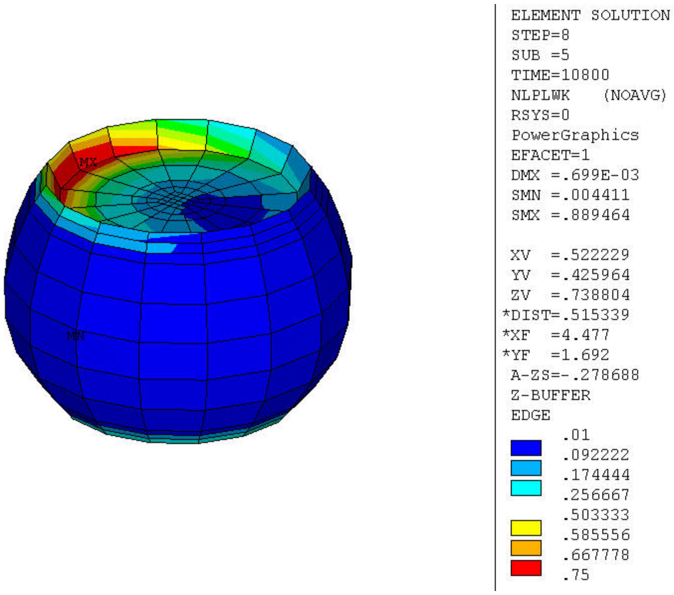


Figure 6.8: Location of the Highest Deformation Solder Ball after Two Thermal Cycles Load (-40 to 125 ^{o}C)



```
ELEMENT SOLUTION
STEP=8
SUB =5
TIME=10800
NLPLWK    (NOAVG)
RSYS=0
PowerGraphics
EFACET=1
DMX =.699E-03
SMN =.004411
SMX =.889464

XV  =.522229
YV  =.425964
ZV  =.738804
*DIST=.515339
*XF  =4.477
*YF  =1.692
A-ZS=-.278688
Z-BUFFER
EDGE
      .01
      .092222
      .174444
      .256667
      .503333
      .585556
      .667778
      .75
```

Figure 6.9: Plastic Work Contour Plot, Highest Strain Solder Ball after Two Thermal Cycles Load (-40 to 125 ^{o}C)

The accuracy of fitting in case 3 is much better than the case 4. Similar analysis has done for one layer of 1 mil interface element thickness, referred as case 5. The accuracy of fitting in these cases is almost equivalent to case 3. The reason is that in these cases, the averaging took place over a fixed damage volume even though the mesh density is different. The slightly better accuracy in case 3 has been found due to the more refinement of the interface elements. Similar cases have also been observed in case 1 and 5 even though the damage volume is fixed. These are the cases that overestimate the shape of the joint (strain concentration at the corner elements) and underestimate the effect of distance to neutral point. These two cases suggest that mesh refinement and size of damage volume are important factor in calculating the inelastic strain energy. Thus for a fixed damage volume, the average calculated inelastic strain energy is little better in refine mesh ball. The optimum damage (highest R-square) is found in the 6th case, where entire highest strain solder elements are considered as damage volume. The main reason for highest accuracy in this case is mesh sensitivity issue that has been reduced by averaging the strain energy over all elements of the highest strain solder ball. The total inelastic strain energy is smaller in this case and the damage takes place in the entire solder volumes. This contradicts with the actual failure analysis, where the solder joint failures occurred mainly in the interface between solder and copper. Even in the simulation, most of the plastic work has been observed in the top two interface layers shown in the Figure 6.9. Therefore case 3 is considered as optimum damage volume of solder ball for thermal fatigue reliability measurement. To calculate the crack initiation ($N_{1\%}$) fatigue life based on the damage volume of interface elements, it is recommended to use two layers of .5 mils element thickness. The empirical relationships of six different damage volume cases with their fitting accuracy shown in Figure 6.10. The empirical model constants for different damage volumes are normalized with the case 1 (previous study). The generalized form of empirical relationships can be written as

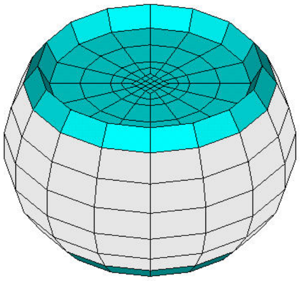
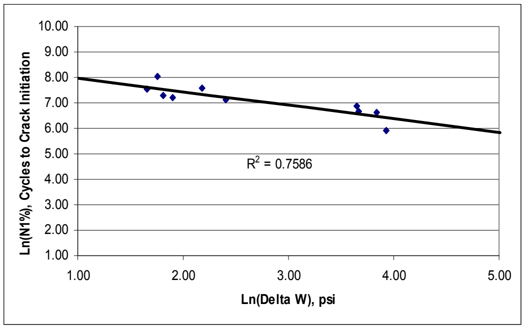
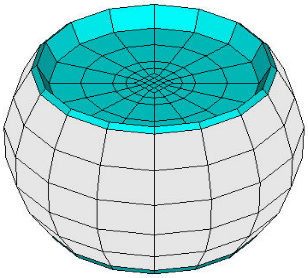
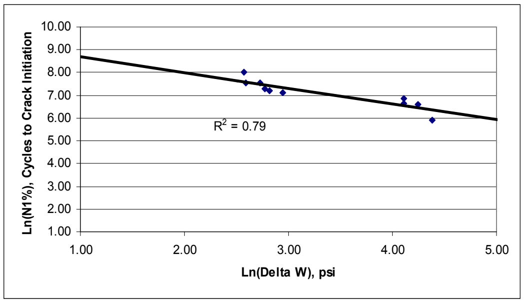
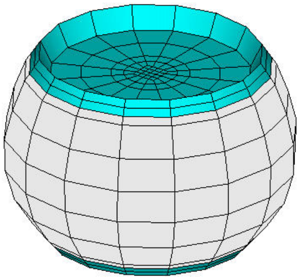
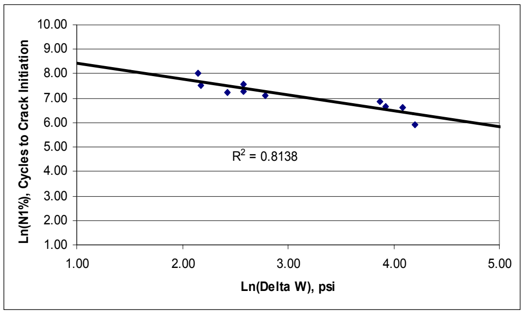
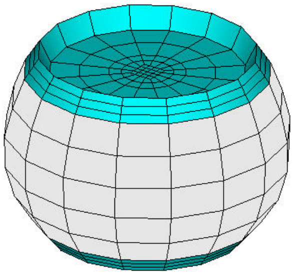
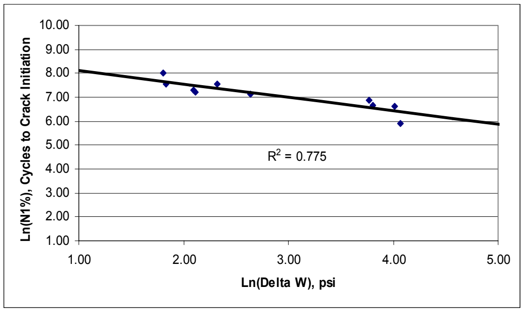
$$\mathrm{Ln}\,N_{1\%} = mC_m\mathrm{Ln}(\Delta W) + AC_A \qquad \text{(eq. 6.9)}$$

The constants C_m and C_A vary among the different damage volumes. The normalized variations of empirical constants are shown in the Figures 6.11 and 6.12.

6.7 Discussion

The simulated strain energy is not constant in the solder damage area. The energy varies with solder volume, stand-off height, and the effect of other packaging materials. In the PBGAs the optimum solder damage height is typically 10% of the total height of the solder ball. As the diameter of the solder ball changes the size of the damage volume also changes.

The effect of mesh refinement has been analyzed. Generally finer the mesh predicts the more accurate results. The stress/strain singularity problem can be solved by averaging the simulated results over the damage region. For a fixed size of damage volume, the averaged calculated result varies with the mesh density. For the same damage volume, one layer of 1 mil thickness predicts less conservative result than the two layers of .5 mils element thickness. Therefore, the choice of good empirical model somewhat depends on the mesh density. It is always better to have at least two layers of element in the solder interface region.

Type of Damage Volume	Location of Damage Volume	Empirical Models
Damage Volume, Case 1: one layer of 1.5 mils interface element thickness **Empirical Model:** Ln(N1%)=mLn(ΔW)+A Where, m=-.5369, A=8.5189 **or** N=5008.7(ΔW)$^{-.5369}$ **Fit (Accuracy):** R^2=.7586		
Damage Volume, Case 2: one layer of .5 mils interface element thickness **Empirical Model:** Ln(N1%)=mCmLn(ΔW)+A C_AWhere,Cm=1.2855, C_A=1.1005 **or** N=11798(ΔW)$^{-.6902}$ **Fit (Accuracy):** R^2=.79		
Damage Volume, Case 3: two layers of .5 mils interface element thickness **Empirical Model:** Ln(N1%)=mCmLn(ΔW)+A C_AWhere,Cm=1.1955, C_A=1.0630 **or** N=8569.2(ΔW)$^{-.6419}$ **Fit (Accuracy):** R^2=.8138		
Damage Volume, Case 4: three layers of .5 mils interface element thickness **Empirical Model:** Ln(N1%)=mCmLn(ΔW)+A C_AWhere,Cm=1.0376, C_A=1.0172 **or** N=5799.6(ΔW)$^{-.5571}$ **Fit (Accuracy):** R^2=.775		

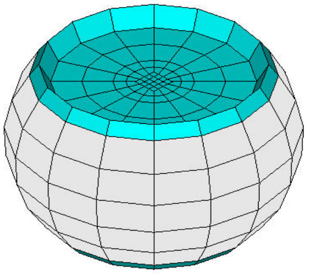
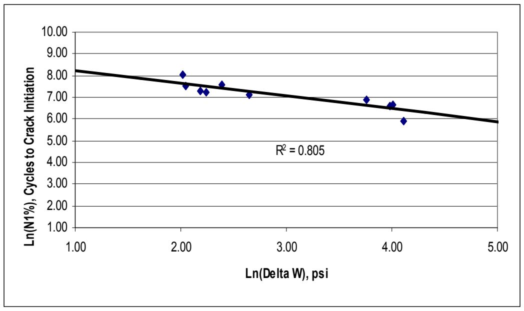
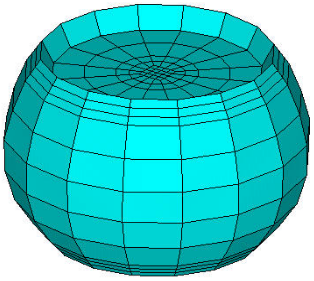
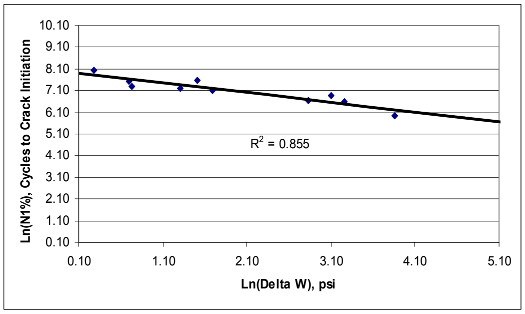
Damage Volume, Case 5: one layer of 1.0 mils interface element thickness **Empirical Model:** Ln(N1%)=mCmLn(ΔW)+A C_AWhere,Cm=1.0875, C_A=1.0326 **or** $N=6613.1(\Delta W)^{-.5839}$ **Fit (Accuracy):** R^2=.805		
Damage Volume, Case 6: All elements of highest strain solder ball **Empirical Model:** Ln(N1%)=mCmLn(ΔW)+A C_AWhere,Cm=0.8226, C_A=0.9310 **or** $N=2782.7(\Delta W)^{-.4417}$ **Fit (Accuracy):** R^2=.855		

Figure 6.10: Empirical Model Accuracy for Different Damage Volumes from the Highest Strain Solder Joint

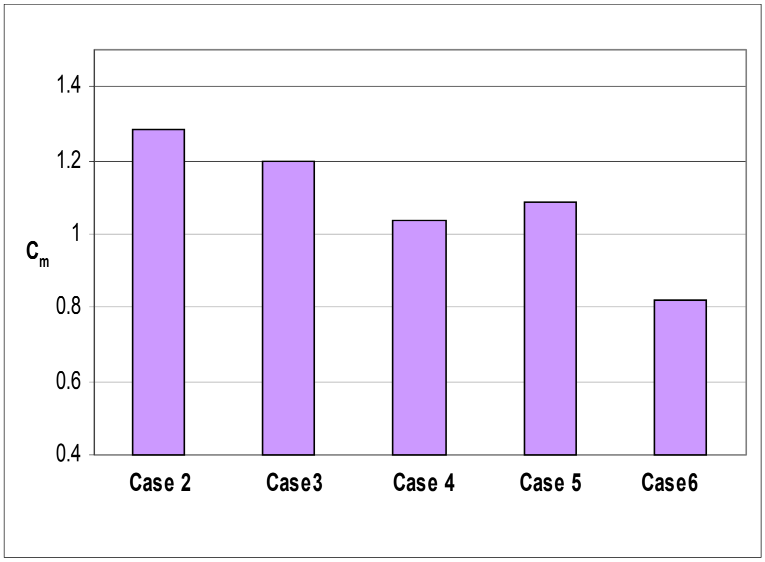


Figure 6.11: Variation of C_m with Different Damage Volumes

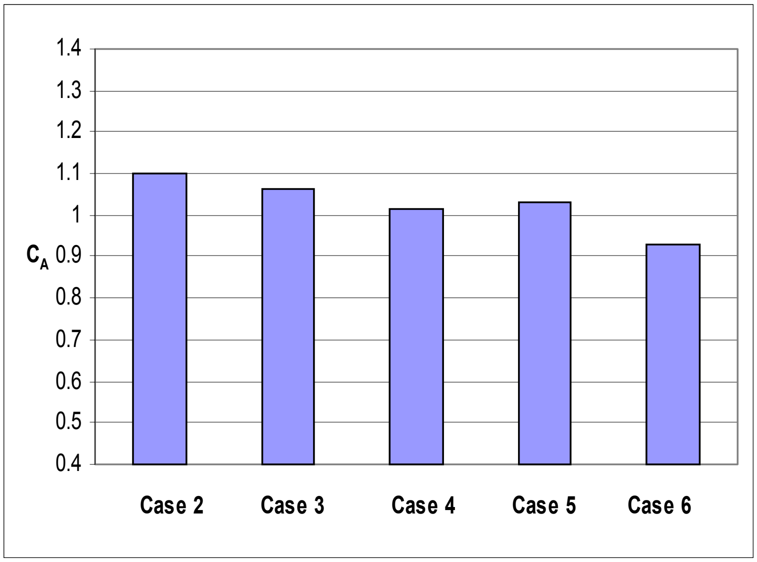


Figure 6.12: Variation of C_m with Different Damage Volumes

Thermal fatigue crack initiation life using the empirical model won't be the exactly the same as actual experimental life cycles. Significant variability in life predictions is typically observed in thermal fatigue failure of IC packages. No two data-sets even if identical in every measured parameter will produce the same response in accelerated tests. On the experimental side, there are lot-to-lot variations in the material properties, PCB pad finish, and solder joint quality. Excessive warpage in packages can cause joints to be already cracked after the SMT process. Sometimes interface failures are observed, for example due to electroless Ni/Au plating problems. Measuring the material properties of packaging materials is not an easy task. There is often quite a large scatter in both elastic modulus and thermal expansion coefficient data. There is the possibility of improper handling of the test boards causing cracks due to mechanical loading (PC board bending). Test chambers are often stopped during a test that last several weeks or months. An excessive number of stops in the test could affect the results. Control of the chamber to the specified thermal cycle test profile can be a problem. The event detector that monitors joint failure can malfunction.

On the simulation side, there are several simplifying assumptions made. Individual material layers are often omitted, and detailed features of the metal traces are rarely incorporated. There are singularities at the edges of the joint, so volumetric averaging of values is used. The averaging surely does not capture the true stress / strain distribution effects.

6.8 Conclusions

The damage volume of BGA solder joint has been optimized with different mesh density. It has been found that optimum damage volume in the interface elements consist of two layers of .5 mils element thickness. Since the largest deformation takes place at the interface of solder and copper pad so case 3 has been considered as optimum damage volume of solder ball and evaluated as best suited empirical model in this analysis. Lower accuracy of fitting has been obtained when considered only one element layer of interface elements. The main reason is that in this case solder joint shape is overestimated (strain concentration in the corner elements) and underestimate the effect of distance to neutral point. It has been found that for a fixed size of damage volume, the averaged calculated strain varies with the mesh density. This indicates that mesh refinement effect is also important for fatigue damage life prediction model. The empirical model in this study is independent of solder geometry. It deals only with the total amount of inelastic strain energy due to the thermal fatigue load. The empirical relation for optimum damage volume can be applied to other surface mount packages to predict the crack initiation life ($N_{1\%}$) of solder joint.

CHAPTER 7

LEADING INDICATORS-OF-FAILURE FOR PROGNOSIS OF ELECTRONIC AND MEMS PACKAGING

7.1 Introduction

Prognosis methodologies proposed in this work are distinct and different from the life-prediction relationships that exist today. The typical question answered by present day damage accumulation relationships including Paris's Power Law [11-12], Coffin-Manson Relationship [13] and the S-N Diagram, is – how long the material is going to last from a known good state starting at time t = 0. There are no existing correlations to assess damage from prior stress histories based on examination of material state. Further, given a material subjected to a an unknown or variable stress history, in absence of macro indicators of damage such as cracks, there are no means of evaluating percentage of useful life that has been consumed by usage or estimating the remaining useful life of the sub-system or system.

The ability to attain 6-sigma reliability and 5-nines availability in such advanced systems could be significantly impacted by tools for prognostication of systems. Comprehensive prognostic systems have significant potential to provide safer, reliable, and cost-effective electronic systems. Performance and life limits for structural materials in complex mechanical systems are often established based largely on a "fear of failure". In defense applications the potential impact of component failure, in terms of human, performance, and/or financial costs, is deemed so extreme that life-management procedures must go to almost any lengths to prevent failure. Conventional approaches for avoiding such failure often involve lengthy inspections, leading to highly conservative "go, no-go" operational decisions, or requiring maintenance processes may significantly impair system readiness [90]. US Air Force currently throws away 1000 components to remove an unknown one that is theoretically predicted to be in a failed state. [91] The cost impact of prognostic methodologies could be immense where the wasted life could be recovered without increasing risk.

There is need for methods and processes which will allow interrogation of complex systems and sub-systems to determine the remaining useful life prior to repair or replacement. This capability of determination of material or system state is called "prognosis". Prognosis based prediction of reliability in field profile, for example, may help us deduce that the present accelerated tests guarantee much more than the required design life and are thus an overkill. Results of like could help shorten the accelerated life test cycle and reduce our product development cycle time. On the other hand the methodology could help us fine-tune accelerated tests on an application specific basis or incorporate alternate accelerated tests to address new failure mechanisms in new technologies – instead of perfecting the universal hammer which is costly and often doesn't work [92].

7.2 Phase Growth as Leading Indicator of Failure

In this study, changes in solder microstructure have been investigated as a leading indicator of failure. The solder microstructure and the growth of intermetallic due to thermal fatigue has been reported previously by several researchers. Morris, Jr., et al. [35] reported that the thermal fatigue of Sn63/Pb37 solder was characterized by microstructural coarsening in the fatigue damaged region. Pang et al. [50] reported that the microstructural and intermetallic development due to thermal cycling aging had a major impact on the fatigue strength of solder joint. Solder joint fatigue life degrades with microstructure changes during thermal aging. Frear, et al. [51] analytically studied the microstructural evolution of solder and suggested that solder grain size could be used as an important parameter for thermal fatigue life prediction. Sayama, et al. [72] examined the changes in microstructure occurring in the Sn63/Pb37 chip resistor solder joints during thermal cycling. In previous studies, the use of phase growth as the evolution parameter for thermal fatigue life time of solder joint has been investigated. A power law relation has also been investigated between the number of cycles to crack initiation and the average increase in the α-Pb phase growth parameter. In this study, the use of rate-of-change of phase growth parameter has been investigated.

The previous studies have been conducted on regular FR4 boards. In the present study, high T_g FR4-06 laminates with metal backing have been used. The phase growth of Sn63/Pb37 solder has been derived on the basis of systematic microstructural observation of the solder joint under thermal cycling loading (-40 to 125°C). Several BGAs and chip resistors are investigated in the thermal cycling condition. For each configuration, thermal cycling phase growth data has been gathered and analyzed using commercial image processing software. Finally the phase growth parameter has been plotted with the experimental crack initiation and propagation life cycle. Relationships have been developed to facilitate interrogation of material state based on changes in the microstructure of the solder joint.

The test vehicle was designed to investigate both the thermal efficiency and the component reliability of a wide variety of substrate, attachment, and encapsulant options. Components analyzed include I/O counts in the range of 193 to 388, I/O pitch in the range of 0.8mm to 1mm, and package sizes in the range of 15mm to 27mm. Resistors including 2512 and 1225 have also been included in the study. The test board contains two 15 mm BGA, one 27 mm BGA, two 16 mm C2BGA, two 2512 chip resistors, and two 1225 chip resistors. The BGAs in this study have Sn63/Pb37 solder balls. The substrates used were standard HASL finished high temperature glass epoxy laminate (FR4-06) attached to 2.54 mm thickness aluminum plate with a variety of adhesives including Arlon and Pressure Sensitive Adhesive (PSA). The boards contain six trace layers to simulate the thermal mass of a true production board, though all functional traces were run on the topmost layer. All pads on the board were non solder mask defined (NSMD) and had a HASL finish. The resistor and BGA daisy chains were routed to plated through holes at the edge of the board where soldered wire connections could be made for use in resistance monitoring during the thermal cycling tests. The Component test matrix for the study is shown in Table 7.1.

Body Size	Ball Count	Ball Pitch (mm)	Thermal Balls	Die Size (mm)	BT Thickness (mm)	BT Pad Diameter (mm)	BT Pad Type	Ball Diameter (mm)
27 mm BGA	388	1	36 (6X6)	10X10X0.35	.56	.5	SMD	.60
16 mm C2BGA	240	.8	None	5.0X5.0X0.23	.56	.45	SMD	.53
15 mm BGA	193	.8	25 (5X5)	8.6 X 8.6 X 0.37	.56	.4	SMD	.60

Table 7.1: Component Test Matrix.

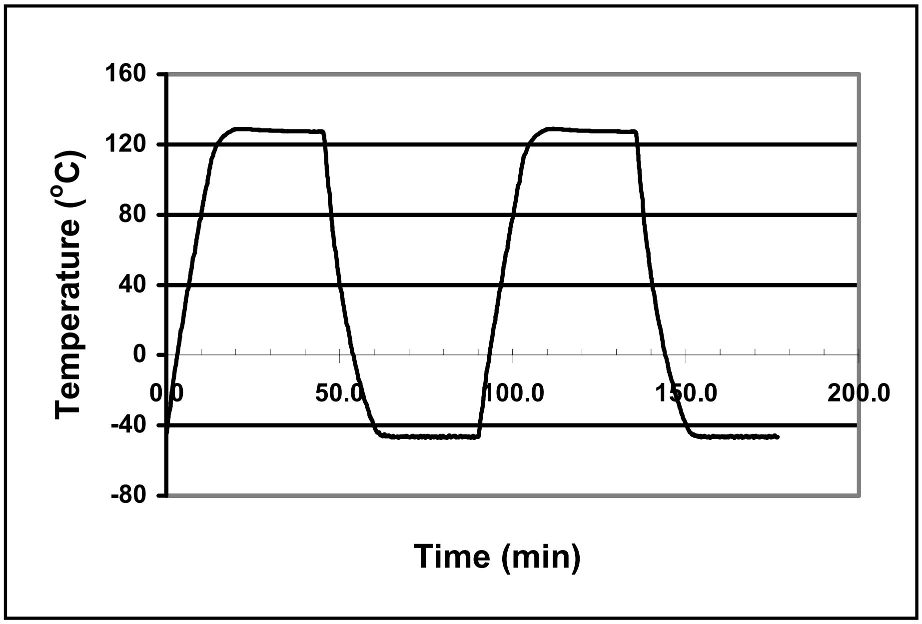


Figure 7.1: Test Board Thermal Cycle (-40 to 125 °C)

7.3 Thermal Cycle Test (-40 to 125 ^{o}C)

Thermal cycling (-40 to 125 ^{o}C) of the assembled test boards was performed a Blue-M environmental chamber. The thermal cycle duration was 90 minutes, with 20 minutes at each extreme. A total of 39 boards were used for the phase growth study. The boards were placed vertically in the chamber, and the wiring passed through access ports to the data acquisition system. Monitoring of the various daisy chain networks was performed throughout the cycling using a high accuracy digital multimeter coupled with a high performance switching system controlled by LabView software. Failure of a daisy-chain network was defined as the point when the resistance change became 10 Ω or higher. Typical thermocouple results from under a component on one of the test boards are illustrated in Figure 7.1. The resulting failure data were statistically analyzed using two parameter Weibull models. The Weibull reliability data plot for the metal-backed BGA components is shown in Figure 7.2.

7.4 Phase Growth Model

Samples were cross-sectioned at various level of thermal cycling. The cross-sections were studied by scanning electron microscopy (SEM) using a JEOL JSM 840 instrument operated at an accelerating voltage of 20 kV. All samples were imaged as polished. The quantitative measure of Pb phase size was established from a 200 μm x 150 μm rectangular region selected from a backscattered SEM image. The typical rectangular region for microstructural evaluation has shown in Figure 7.3.

The average phase size “g” in the selected region is measured using the IMAQ Vision Builder Software. The typical SEM pictures before and after the mapping of grain size using the IMAQ software is shown in Figure 7.4 and Figure 7.5. The phase growth parameter S can be expressed as

$$S = (g - g_0)^4 \qquad \text{(eq. 7.1)}$$

Where, g_0 is the average phase size of solder after reflow at zero thermal cycle. The average phase growth parameter S changes with the time in thermal cycle environment. The phase growth parameter S increases proportionately with the number of cycles. Figure 7.6 shown SEM backscattered images exhibiting an example of Pb-phase growth process in the 27 mm BGA solder ball during the thermal cycle test condition. The average phase growth parameter S measured at each level of cycle for BGA component has been plotted in the Figure 7.7. Similar measurement has been done on discrete components shown in the Figure 7.8. From these two figures (Figure 7.7-7.8), it is found that discrete component like 2512 has much higher phase growth parameter than the BGAs, and thermal cycling results of 2512 components support this argument. The phase growth data in this study indicates that phase growth rate stays fairly uniform during the thermal cycle tests. This is consistent with the stabilization of hysteresis loop that is observed in thermal fatigue simulations. Stabilization of the loop indicates that the damage is accumulated at more or less a constant rate.

Experimental data indicates that accumulation of damage in solder is accompanied with Pb-phase growth and grain coarsening. The damage manifests itself in ultimate appearance of cracks. Figure 7.9 shows the grain coarsening at a BGA interface with the appearance of crack. The solder joint effective crack length for different

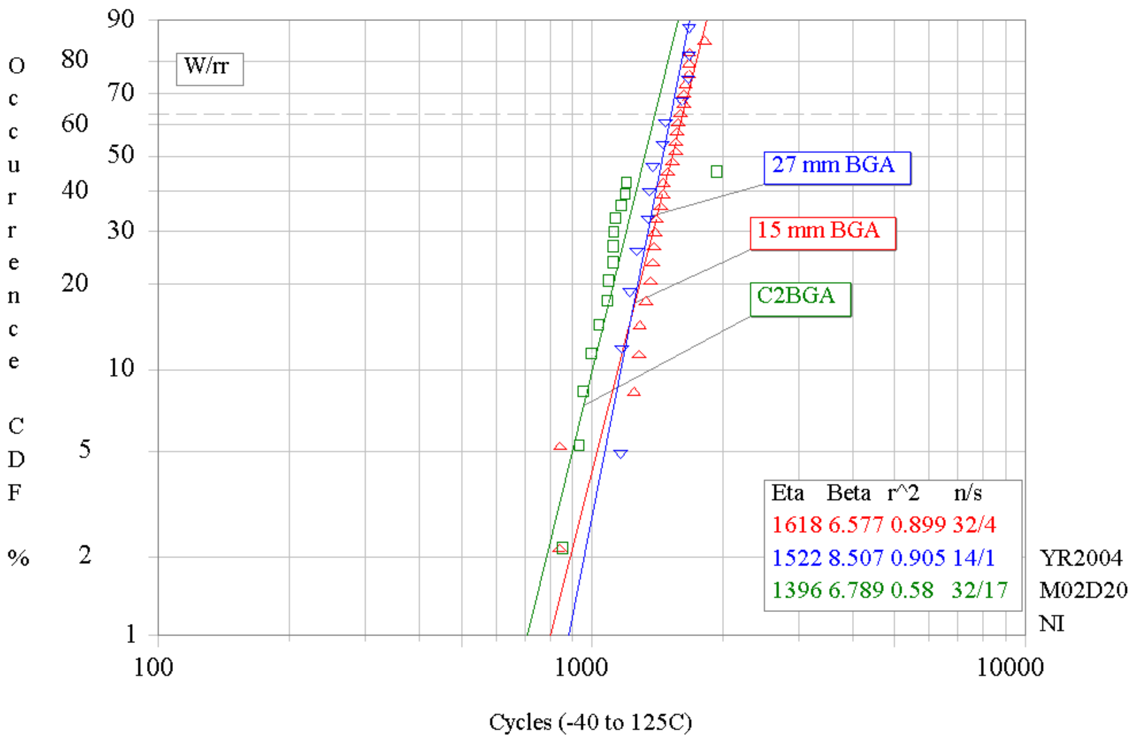


Figure 7.2: Weibull Plot of 1% Failure for 15mm BGA, 27mm BGA, and C2BGA

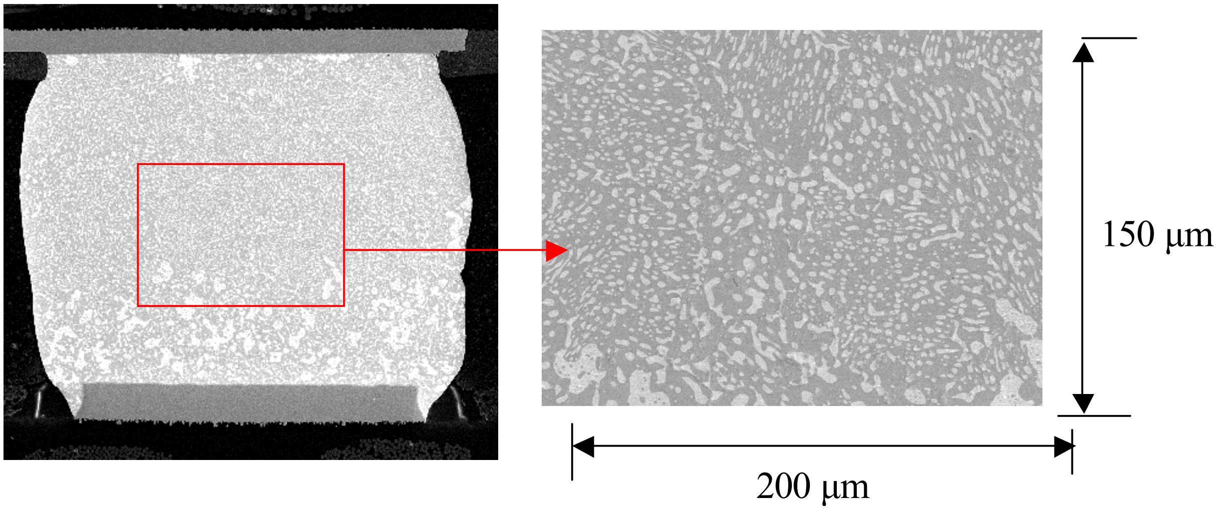


Figure 7.3: Typical Selected Region for Bulk Solder Phase Growth Measurement, 27 mm BGA (Sn63/Pb37 Solder).

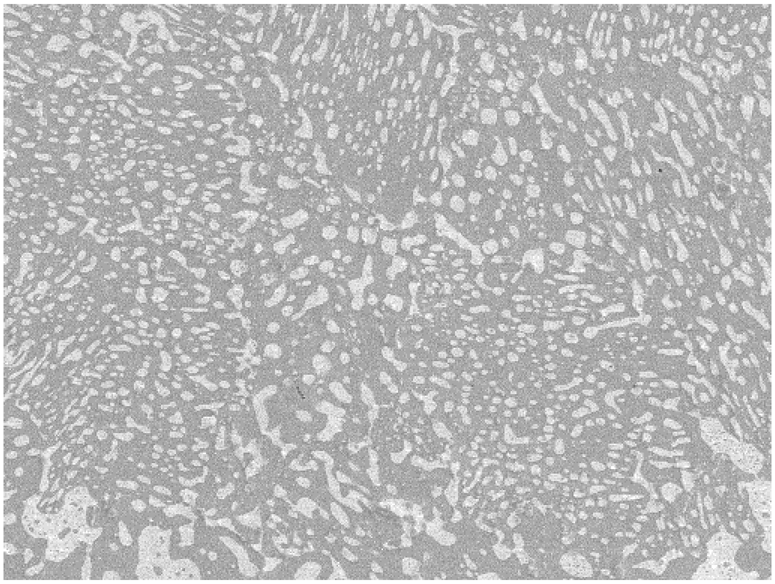


Figure 7.4: Original Micrograph.

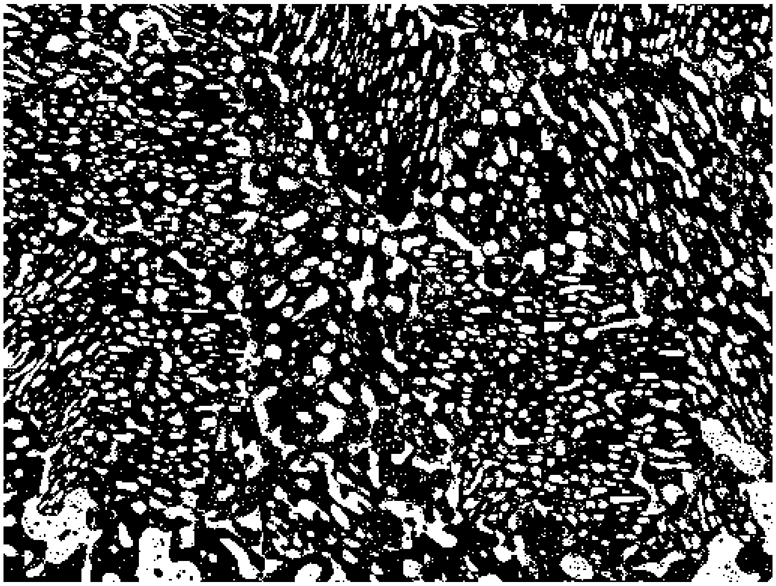
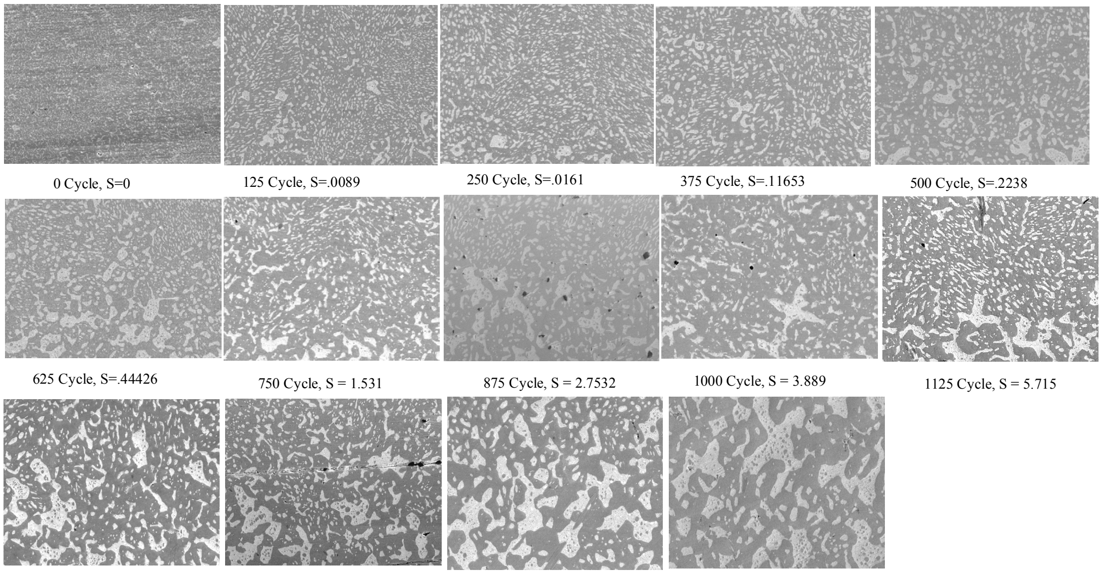


Figure 7.5: Mapped Micrograph.



0 Cycle, S=0

125 Cycle, S=.0089

250 Cycle, S=.0161

375 Cycle, S=.11653

500 Cycle, S=.2238

625 Cycle, S=.44426

750 Cycle, S = 1.531

875 Cycle, S = 2.7532

1000 Cycle, S = 3.889

1125 Cycle, S = 5.715

1250 Cycle, S = 8.665

1375 Cycle, S = 11.878

1500 Cycle, S = 34.533

1650 Cycle, S = 52.393

Figure 7.6: SEM Back-scattered Images of 27 mm BGA, Pb Phase Growth Measured After Various Level of Thermal Cycling (-40 to 125 °C, Sn63/Pb37 Solder).

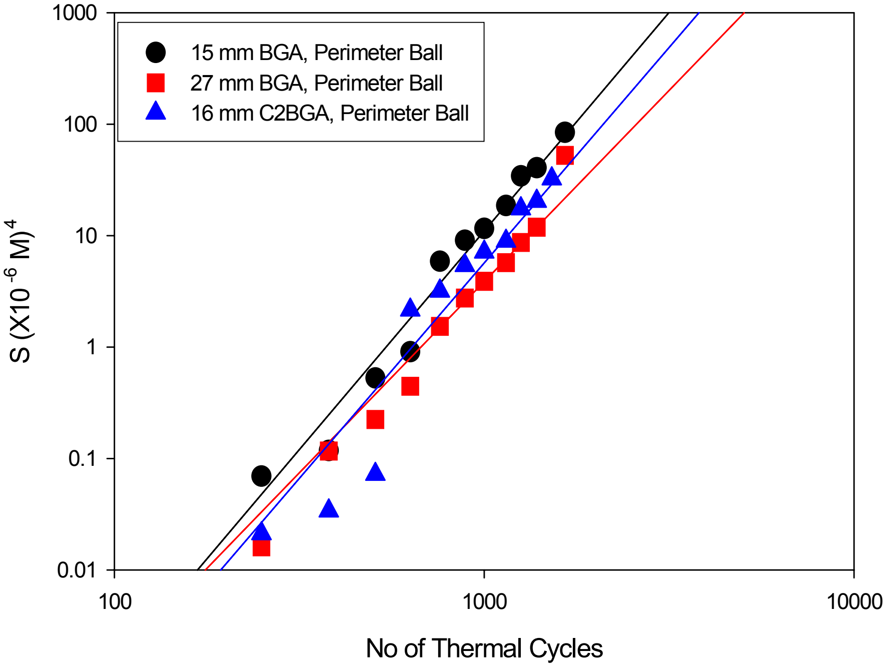


Figure 7.7: Phase Growth Parameter, at Various Levels of Cycles for 15 mm, 16 mm, and 27 mm BGAs.

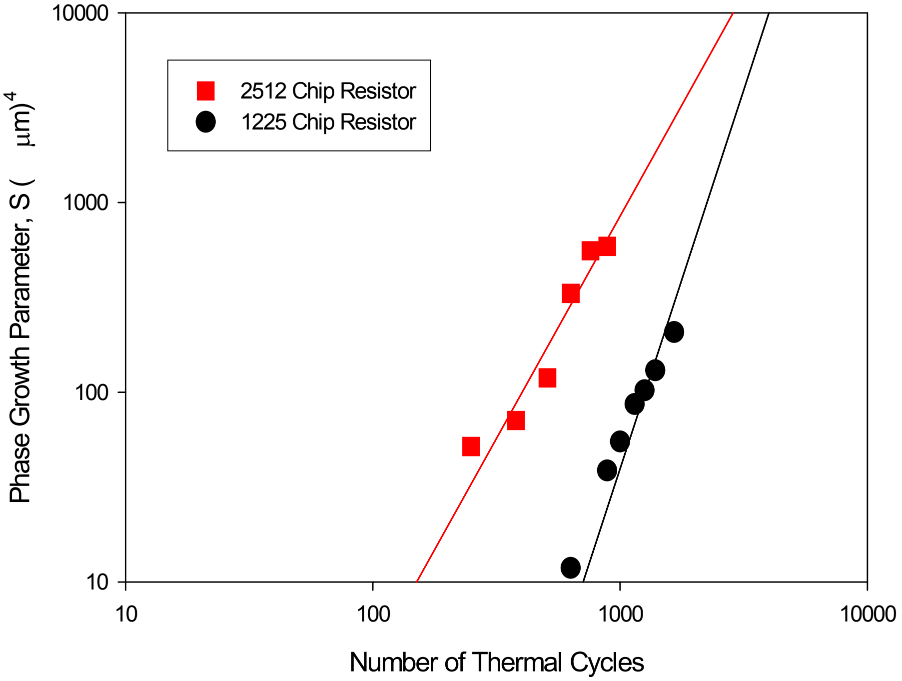


Figure 7.8: Phase Growth Parameter, at Various Levels of Cycles for 2512, and 1225 Chip Resistors.

components due to the thermal cycling (-40 to 125^{o}C) has been measured systematically. The solder joint effective crack length for different components due to the thermal cycling (–40 to 125ºC) has also been measured. Data indicates that phase growth parameter and its derivatives are potential candidate proxies for leading indicators of failure.

The time-to-1-percent failure ($N_{1\%}$) of solder joints has been correlated with the phase growth rate or average increase of phase growth parameter per cycle, $\frac{dS}{dN}$ of solder shown in Figure 7.10. It is hypothesized that the faster phase growth correlates with faster accumulation of inelastic work in the joint and a lower cycles to crack initiation (Figure 7.10). This trend is found to be true for the data-set tested. The following relationship has been developed between phase growth rate and time-to-1-percent failure.

$$N_{1\%} = C_2\left(\frac{dS}{dN}\right)^{-\gamma} \qquad \text{(eq. 7.2)}$$

Where C_2=141.71 μm^4/cycle, and γ =0.68

The relation enables the calculation of residual life. The phase growth rate in a deployed part can be monitored and the life time consumed to that point evaluated. The residual life can then be computed.

Further, the time-to-1-percent failure can be computed by subjecting the sample a very short accelerated test, e.g. 50 cycles. The computed phase growth rate from experimental observation can be used to compute the time-to-1-percent failure. The main advantage of this approach is one can calculate the crack initiation life cycle of the solder joint subjected to harsh environment by measuring the average phase growth parameter at any level of cycling. In this method, there is no need for an expensive thermal cycle life test. If the phase growth parameter at any two level of aging is known, then time-to 1% failure life can be computed from the Figure 7.10. Further, given the damage state of a deployed component, the prior-elapsed time in any thermal environment can be computed based on known phase growth rate, given the initial phase size after reflow. The residual life can then be computed based on the computed phase growth rate for the desired use environment. The phase growth rate per cycle has been correlated with the inelastic strain energy density per cycle from non-linear finite element simulations (Figure 7.11).

Prior studies have correlated the number of cycles to crack initiation and the crack propagation rate with the inelastic strain energy density [5-8, 79]. The correlation enables the evaluation of residual life in a deployed part. The rate of change of phase growth parameter of a deployed part can be measured under the intended use conditions of future part deployment. The corresponding damage accumulation rate can then be computed in terms of inelastic strain energy density, which can be used to evaluate residual life. The phase growth rate per cycle has been correlated to the crack propagation rate per cycle in the solder interconnects (Figure 7.12). Phase coarsening and phase growth has been demonstrated as a leading indicator of failure for solder interconnects. The correlation indicates that components which progress to failure faster will exhibit a faster damage proxy magnitude in the form of phase growth parameter. The correlations also provide validation for the prognostication methodology presented in the paper.

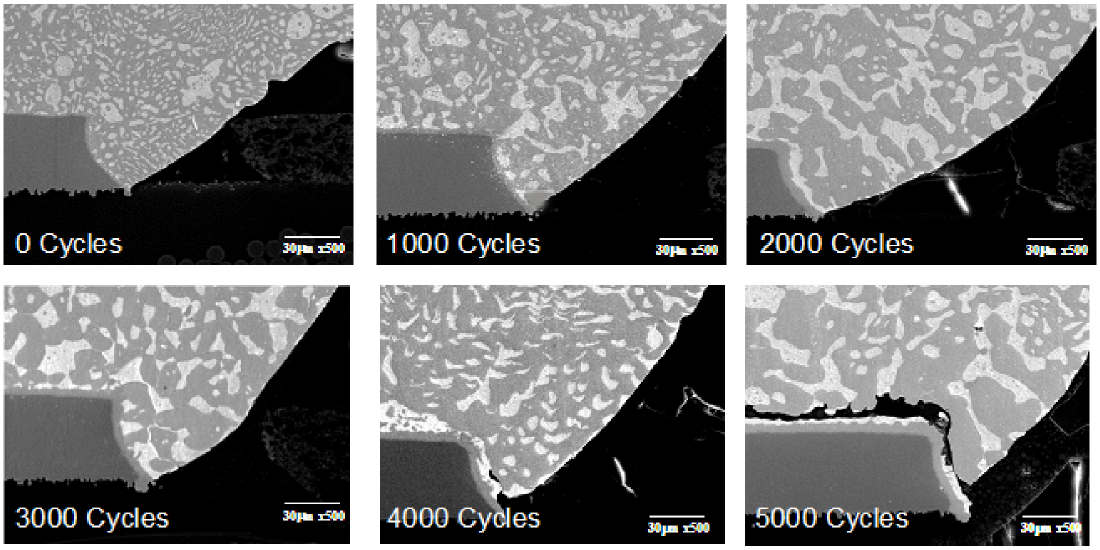


Figure 7.9: Correlation of Incipient Crack Growth with Phase Growth in Ball-Grid Array Packages (Sn63/Pb37).

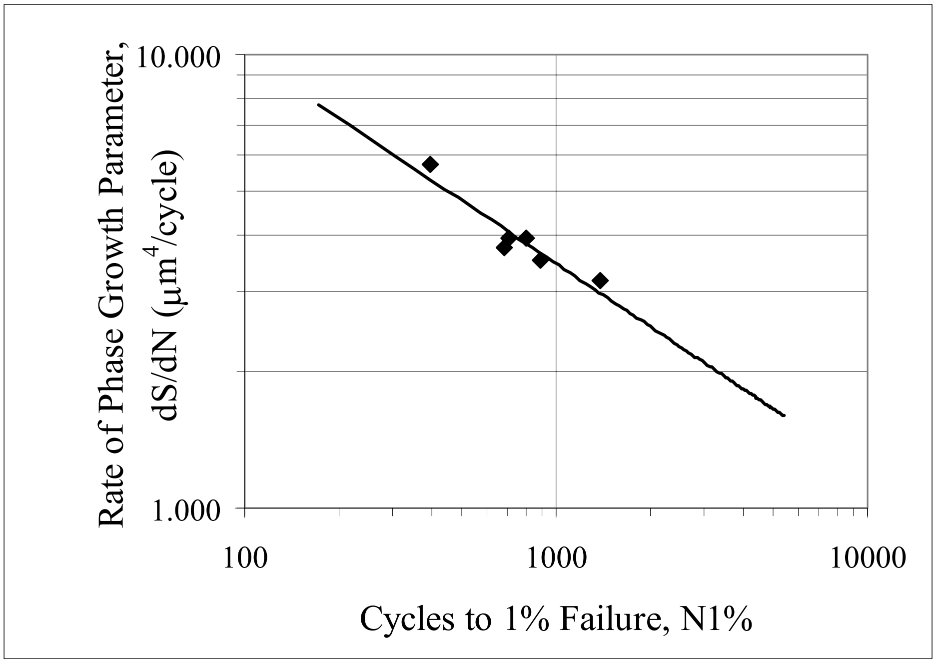


Figure 7.10: Relation between Number of Cycles to 1% Failure and Phase Growth Rate.

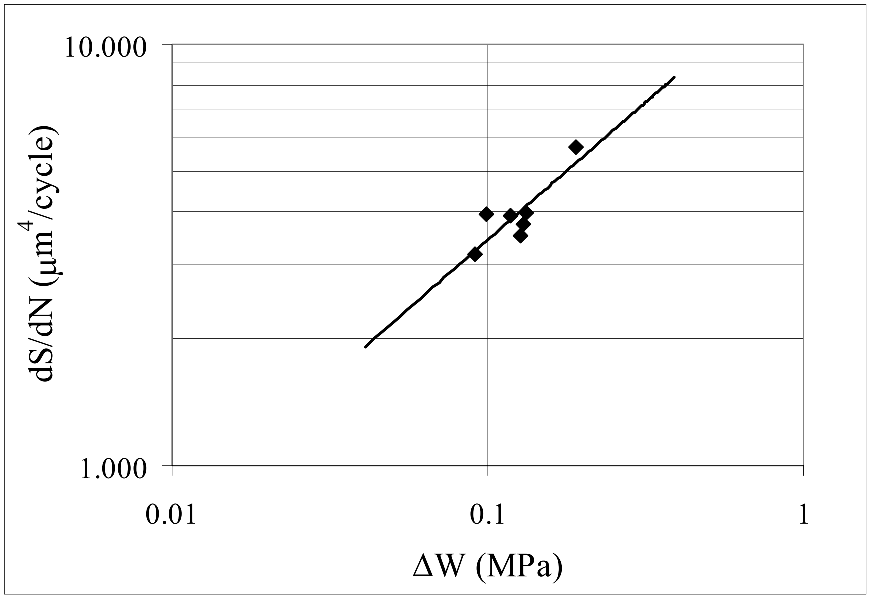


Figure 7.11: Relationship between Inelastic Strain Energy Density and Phase Growth Rate.

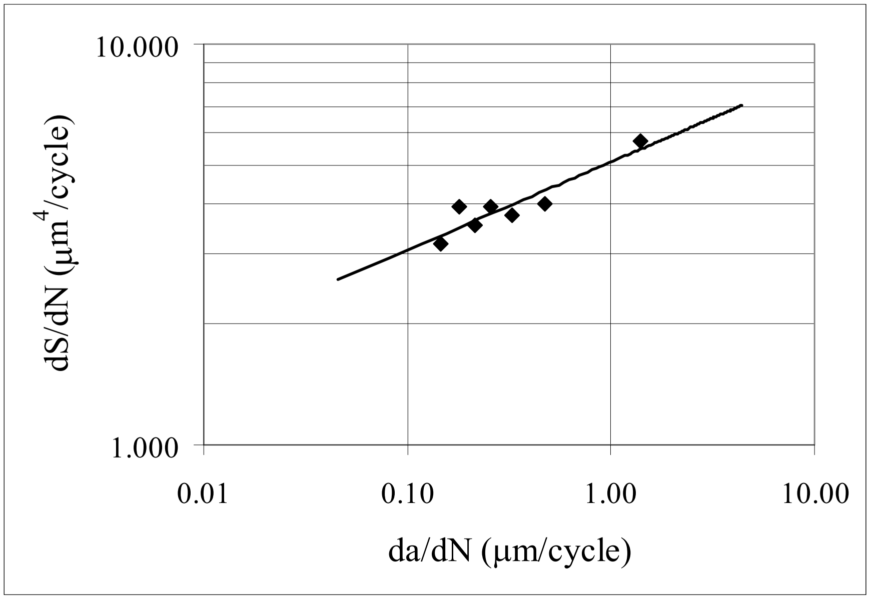


Figure 7.12: Relation between Crack Growth Rate per Cycle and Phase Growth Rate per Cycle.

7.5 Conclusions

A methodology for prognosis-of-electronics has been demonstrated with data on leading indicators of failure for accurate assessment of product damage significantly prior to appearance of any macro-indicators of damage. Phase growth rate has been identified as proxy of impending failure in electronic structures. A mathematical relationship has been developed between phase growth rate and time-to-1-percent failure. The relationship enables the assessment of life consumed based on phase growth rate and a forward-estimate of residual life. Phase growth parameter is the, leading indicators of failure.

CHAPTER 8

PROGNOSTICATION OF LEADED AND LEAD-FREE ELECTRONICS IN HARSH ENVIRONMENTS

8.1 Introduction

In this chapter prognostication methodologies for lead-free electronics have been investigated. Prognostics methodologies can be very valuable in development of field-life correlations and derivation of acceleration transforms. A scarce understanding of damage in field environments stems from limitations on quantification of prior stress histories for products. Most analytical tools, address damage estimation for known stress histories imposed on pristine materials. The field environment is often complicated and random based on usage profile and ambient environment. In absence of macro-indicators of damage, there are no means for evaluation of percentage useful life consumed or estimation of the residual life for electronics subjected to unknown prior stress histories.

Prognostication methodologies have potential of reducing accelerated test cycle time significantly. Prognostic indicators monitored incrementally over a much shorter test time in intended use environment can be used to evaluate residual life. Further, prognosis based prediction of reliability in field profile, for example, may help us deduce that the present accelerated tests guarantee much more than the required design life and are thus overkill. Results of like could help shorten the accelerated life test cycle and reduce our product development cycle time. On the other hand the methodology could help us fine-tune accelerated tests on an application specific basis or incorporate alternate accelerated tests to address new failure mechanisms in new technologies – instead of perfecting the universal hammer which is costly and often doesn't work [92].

8.2 Phase Growth as Leading Indicator of Failure

SnAgCu compositions, which have been targeted as the defacto standard for a wide variety of applications may out-perform or under-perform the SnPb solders depending on temperature range. Accelerated test data on 2512 chip resistors, [Yang, et. al., 2004; 98] indicates that reliabilities of 63Sn37Pb and 95.5Sn3.8Ag0.7Cu solder joints may be similar for the – 40 to 125ºC thermal cycling range. However, 63Sn37Pb dramatically outperforms the lead free Sn-Ag-Cu alloy for the more extreme – 40 to 150ºC testing (Figure 8.1).

Phase growth has been identified as one of the proxies for understanding progression of damage in this paper. Evolution of solder microstructure and the growth of intermetallic due to thermal fatigue have been reported previously by several researchers. Frear, et. al. [53] reported that microstructure of solder changes under thermo-mechanical fatigue. Morris, et al. [35] reported that the thermal fatigue of Sn63/Pb37 solder was characterized by microstructural coarsening in the fatigue damaged region. Pang et al. [50] reported that microstructural evolution and intermetallic growth due to thermal cycling aging had a major impact on the fatigue strength of solder joint. Solder joint fatigue life degrades with microstructure changes during thermal aging. Frear, et al. [51] analytically studied the microstructural evolution of solder and suggested that solder grain size could be used as an important parameter for thermal fatigue life prediction. Bangs and Beal [54], Wolverton [55], and Tribula, et al. [56] have

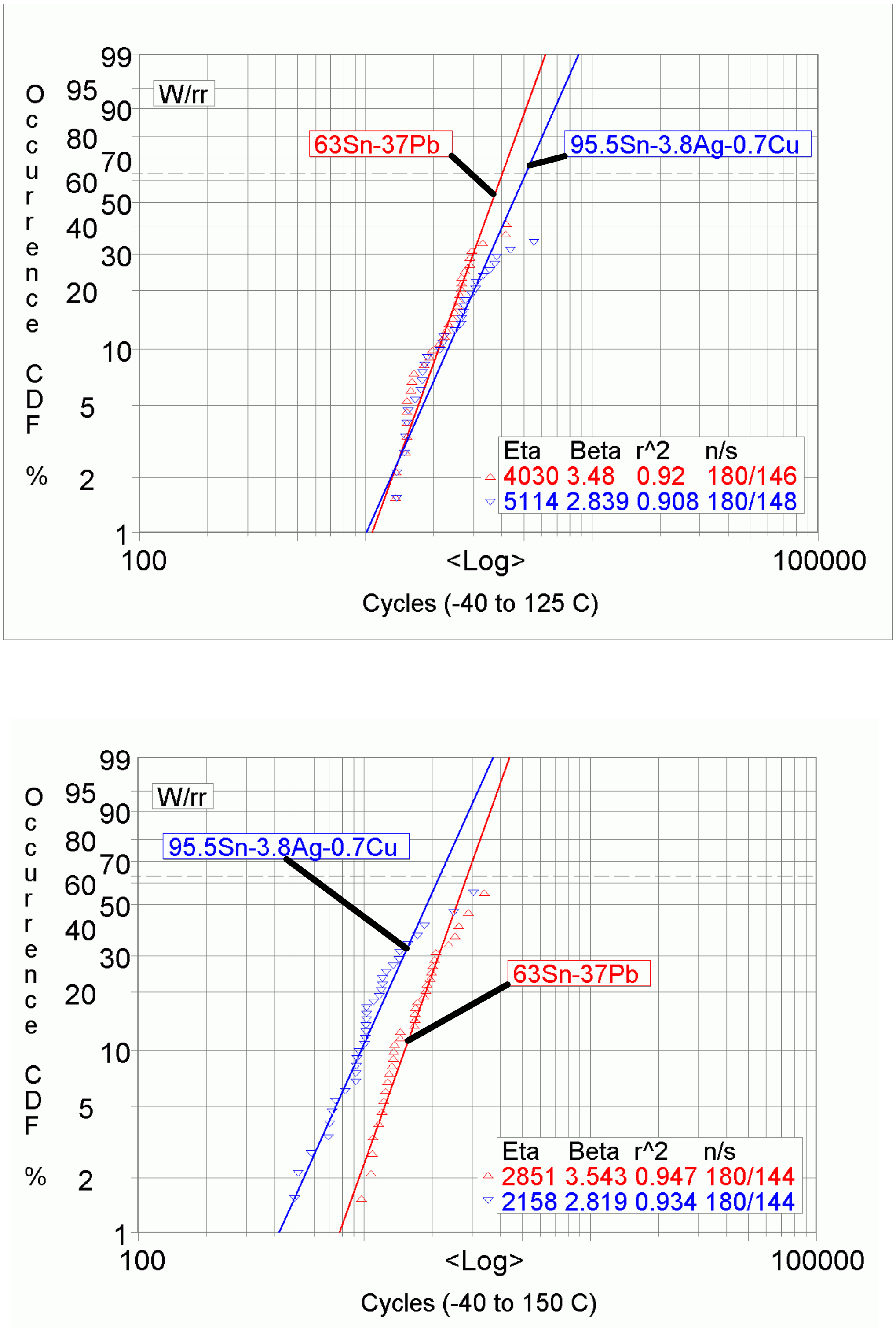


Figure 8.1: SnAgCu Solders Under Perform the SnPb Solders for Higher Strain Ranges.

shown that during thermal fatigue of eutectic and high lead solders grain coarsening happened and the fatigue failure initiates in the coarsened region. Sayama, et al. [52, 72] examined the changes in microstructure occurring in the Sn63/Pb37 and lead free chip resistor solder joints during thermal cycling. Lall, et. al. [96] investigated the grain-size evolution and derivatives of phase growth rate as prognostics parameters on a wide range of leaded devices in underhood applications.

In this study, changes in solder microstructure and its derivatives have been investigated for use as the leading indicators of failure. Quantitative metrics of changes in microstructure have been identified and relationships developed to represent damage progression. Data presented covers a wide range of 63Sn37Pb leaded and 95.5Sn4Ag0.5Cu leadfree electronics for both discrete devices and high I/O packaging in extreme environments. The phase growth parameter has been defined as the relative change from phase-state after reflow, instead of the absolute value of phase state. The fundamental reason for selection of phase growth and its derivatives is that, superplastic alloys usually made of fine grain structure. Therefore a considerable growth of the matrix grains and the second phase particles frequently occurs during high temperature deformation. The grain growth rate (per unit time) is found to increase with increasing strain rate. Callister [57] found that after recrystallization is complete, the strain-free phases will continue to grow if the metal specimen is stored at an elevated temperature.

Phase growth in underhood environments and extreme temperature applications is driven by thermal strain driven by mismatch in the coefficient of thermal expansion. Increase in phase size is accompanied with decrease in total boundary area, yielding a reduction in the total energy, which is the driving force for phase growth. Phase growth occurs by migration of phase boundaries. Large phases grow at the expenses of the small phases. Boundary motion is diffusion of atoms from one side of the boundary to the other side. The diffusion takes place by a vacancy mechanism and the increase of diffusion coefficients is due to the appearance of the excess concentration of vacancies during deformation. Callister [57] states that for many polycrystalline materials phase size varies with time according to the following relations.

$$g^n - g_0^n = Kt \qquad \text{(eq. 8.1)}$$

Where g is the phase size at time t, and g_0 is the initial phase size, and K and n are time independent constants. The value n is generally varies between 2 to 5.

The process of the particle growth induced by volume diffusion was theoretically analyzed by Lifshitz, et al. [58]. It was reveled that the variation of the average particle radius with time is

$$r^3 - r_0^3 = B_1 \frac{\gamma \Omega C_0 D_b}{RT} t \qquad \text{(eq. 8.2)}$$

Where r is the average particle radius, r_0 is the initial radius of an average particle, B_1 is the parameter related to the volume fraction of the particles, γ is the free energy per unit area of the phase boundary, Ω is the molar volume of the particle phase, C_0 is equilibrium solute concentration near the phase boundary, D_b is the coefficient of solute diffusion in the phase boundary, R is the gas constant, T is the absolute temperature, and t is time. Ardel [59] and Speight [60] studied independently and proposed a phase diffusion theory, which states that when the phase boundary diffusion is dominant the average phase size to the fourth power (g^4) increases proportional to time. Senkov and Myshlev [61] extended the theory the phase growth process of a superplastic alloy and validated the theory in that of Zn/Al eutectic alloy. They expressed the evolution of the average phase size g with the time as bellows,

$$g^4 - g_0^4 = \frac{B\delta\Omega C_0 D_b}{RT} t \qquad \text{(eq. 8.3)}$$

Where g_0 is the initial average phase size, B is the phase geometry parameter, δ is the phase boundary width.

In the present study, Sn4.0Ag0.5Cu solder ball-grid arrays and discretes on high T_g FR4-06 laminates with immersion Ag finish have been studied under thermo-mechanical loads in the range of -40 to 125°C (Figure 8.2). Phase growth data has been gathered and analyzed using image processing. Prognostication parameters have been correlated with macro-indicators and reliability. Relationships have been developed to facilitate interrogation of material state based on changes in the microstructure of the solder joint. Components analyzed include I/O counts in the range of 208 to 416, I/O and pitch size is 1mm, and package sizes are 17mm, 27mm, and 2512 resistors. The boards contain six trace layers to simulate the thermal mass of a true production board, though all functional traces were run on the topmost layer. All pads on the board were non-solder mask defined (NSMD) and had an immersion silver finish. The resistor and BGA daisy chains were routed to plated through holes at the edge of the board for in-situ resistance measurements.

8.3 Phase Analysis

Samples were cross-sectioned at various level of thermal cycling. The cross sections were studied by scanning electron microscopy (SEM) using a JEOL JSM 840 instrument operated at an accelerating voltage of 20 kV. All samples were imaged as polished. The quantitative measure of Ag_3Sn particle size was established from a 100 μm

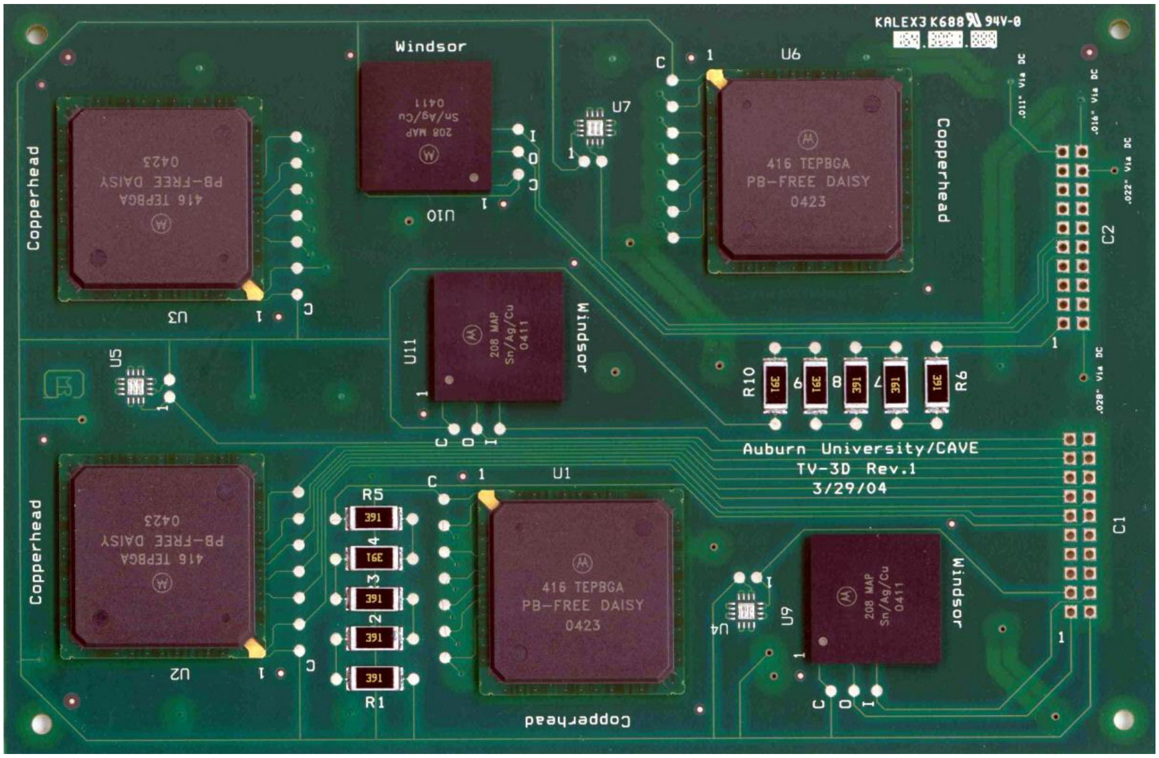


Figure 8.2: Test Vehicle

x 75 µm rectangular region selected from a backscattered SEM image of a highest strain corner solder ball. The typical SEM pictures before and after the mapping of phase size using image analysis is shown in Figure 8.3 and Figure 8.4.

The average phase size "g" in the selected region is measured using Image Analysis Software. The phase growth parameter S can be expressed as

$$S = (g - g_0)^4 \qquad \text{(eq. 8.4)}$$

Where, g_0 is the average phase size of solder after reflow at zero thermal cycles. The average phase growth parameter S changes with the time in thermal cycle environment. Figure 8.5 shows SEM backscattered images exhibiting an example of Ag_3Sn -phase growth process in the 27 mm BGA solder ball at different level of thermal cycle. Most of the SnAgCu solder is comprised of Sn-phases, so that the growth rate of tin and Ag_3Sn intermetallic crystals are significant. Since Ag atoms have a higher diffusion rate in the molten solder, they can diffuse out of the way and thus allow the Sn dendrites to grow. Particles of Ag_3Sn grow either to spheres or to needles shape. Since tin cannot anticipate the shape of the Ag3Sn intermetallic particles, they have to grow ahead of the tin phase [97].

8.4 Determination of Prognostication Parameters.

The average phase growth parameter, S measured at each level of cycle for each individual component has been shown in Figure 8.6. The phase growth data in this study

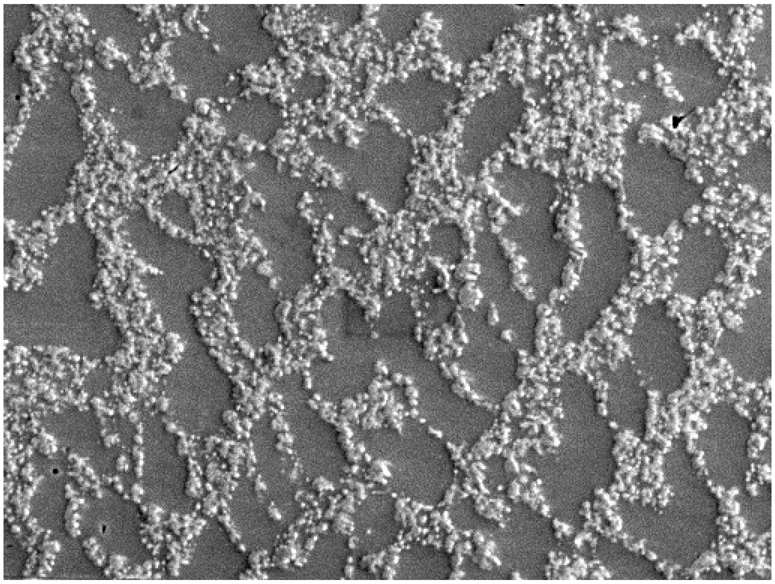


Figure 8.3: Micrograph from 27 mm BGA Showing Sn and Ag_3Sn Phases

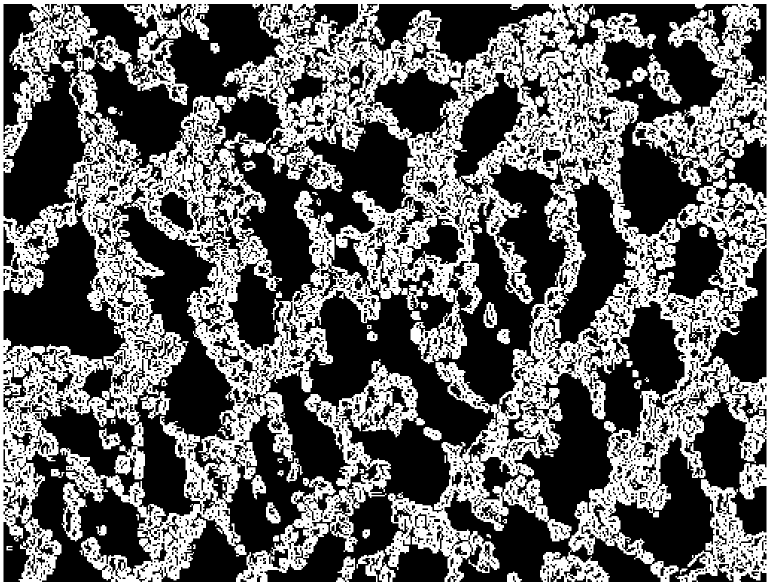
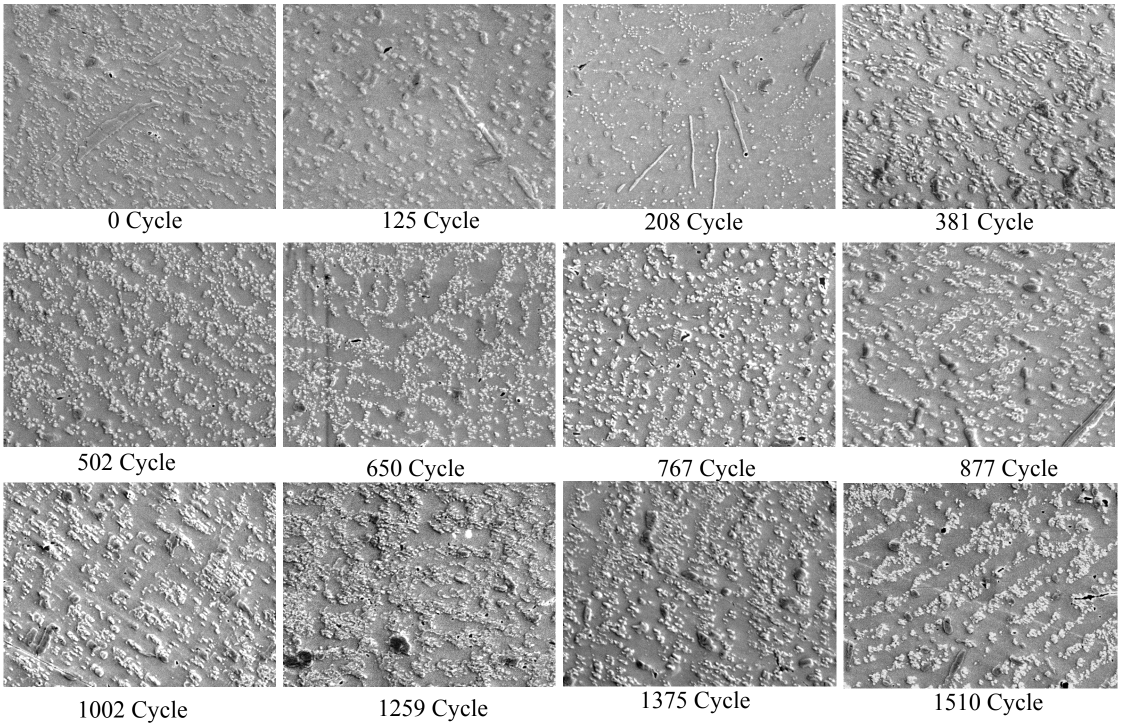


Figure 8.4: Microstructure Mapping Using Image Analysis.



0 Cycle

125 Cycle

208 Cycle

381 Cycle

502 Cycle

650 Cycle

767 Cycle

877 Cycle

1002 Cycle

1259 Cycle

1375 Cycle

1510 Cycle

Figure 8.5: SEM Back-Scattered Images of Phase Growth Versus Thermal Cycling (-40 to 125°C, 95.5Sn4Ag0.5Cu Solder, 27 mm BGA, Magnification: 1000)

indicates that phase growth rate stays fairly uniform during the thermal cycle tests. The phase growth rate for both 63Sn37Pb and 95.5Sn4Ag0.5Cu (SAC405) solder has been plotted in Figure 8.6. Microstructural evolution tracked in 63Sn37Pb solder is based on the growth of Pb-rich phases. Since, and electronic system may have variety of material sets, the linearity of microstructural evolution depicts the validity of phase growth as a proxy for damage progression. This is consistent with the stabilization of hysteresis loop that is observed in thermal fatigue simulations. Stabilization of the loop indicates that the damage is accumulated at more or less a constant rate. Previous studies have used products between derivatives of field quantities such an inelastic strain energy density (ΔW) to quantify damage and shown that it is accumulated at a constant rate [5, 79, 8, 98].

Experimental data indicates that accumulation of damage in solder is accompanied with Ag_3Sn -Phase growth and grain coarsening (Figure 8.5). The damage manifests itself in ultimate appearance of cracks. The grain growth rate for leaded solder is higher than lead free solders under thermal cycling conditions. A comparative study has been done for Sn/Pb and 95.5Sn4Ag0.5Cu solder. In the SnPb solder structure consists of a fine two phase mixture of Sn and Pb, but in the case of SnAgCu alloy Ag-Sn intermetallic randomly distributed in the bulk Sn. The needles/spherical intermetallic precipitates are Ag_3Sn and their mean phase diameter is much less than the phase diameter of Pb particle in Sn/Pb solder. Figure 8.7 shows a comparative study between 63Sn37Pb and 95.5Sn4Ag0.5Cu alloys grain growth rate for 17 mm BGA part. In our earlier study, [96] phase growth parameter of SnPb solder has been calculated on metal-backed board. In this study we have found that grain growth rate of SnPb solder is at least 1.6 times higher than the 95.5Sn4Ag0.5Cu solder.

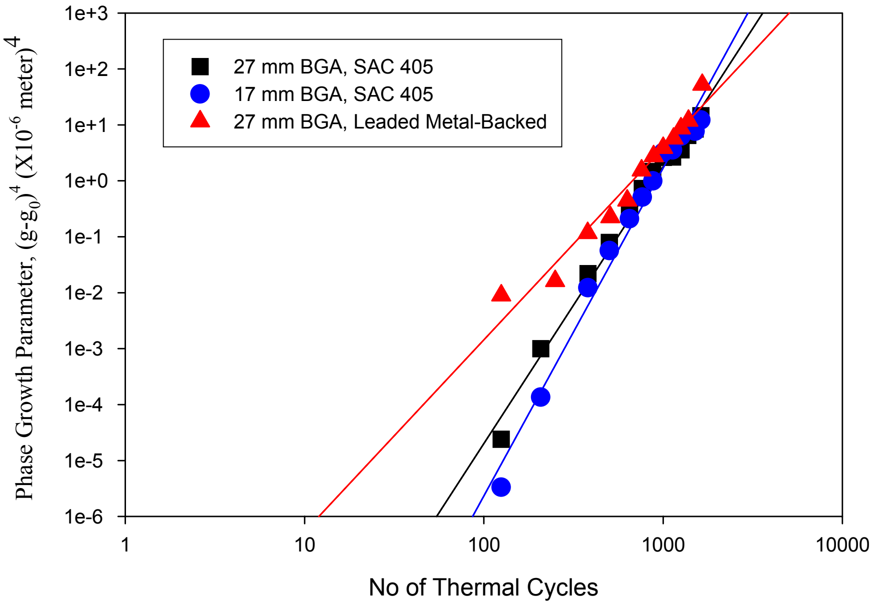


Figure 8.6: Phase Growth Parameter, at Various Levels of Cycles for 27 mm and 17 mm BGA.

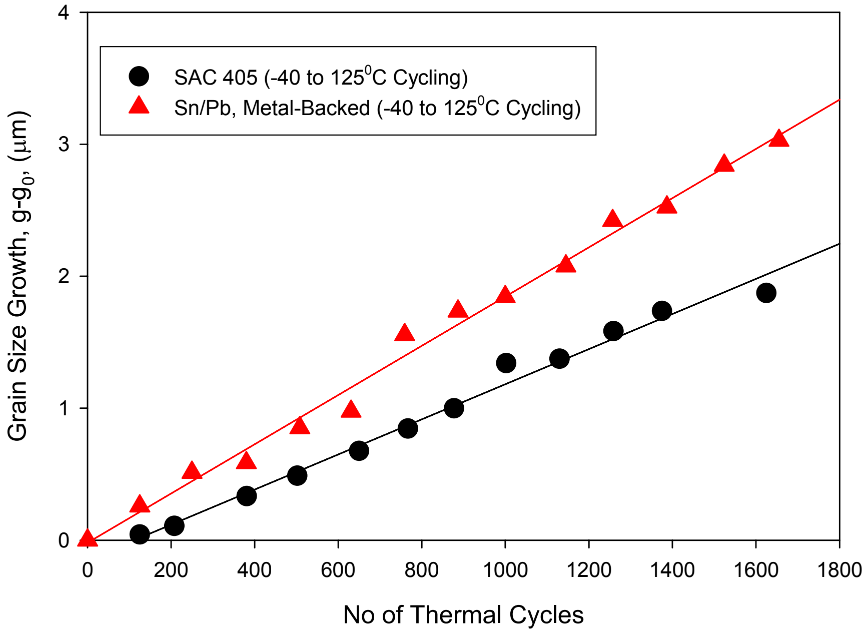


Figure 8.7: Grain Growth Rate versus Thermal Cycling.

8.5 Lead Free Solder Grain Coarsening Analytical Model

Accelerated microstructural coarsening during thermomechanical deformation is attributed to the generation of excess vacancies caused by the combined effect of local hydrostatic state of stress (σ_h), and the instantaneous inelastic strain rate ($\dot{\varepsilon}$). The total vacancy concentration at any location within the solder joint at any instant of t may be written as the sum of the equilibrium vacancy concentration, which is due to the applied instantaneous strain rate described in Dutta's work [162-163].

$$n_{total} = n_{eqlm} + n_{strn} \qquad \text{(eq. 8.5)}$$

$$\text{where, } n_{eqlm} = \exp\left(\frac{-Q_{f,v}}{kT}\right)\exp\left(\frac{\sigma_h \Omega}{kT}\right), \text{and} \qquad \text{(eq. 8.6)}$$

$$n_{strn} = \exp\left(\frac{-Q_{f,v}}{kT}\right)\exp\left(\frac{\sigma_h \Omega}{kT}\right)N\dot{\varepsilon}\left[1-\exp\left(\frac{-t}{\tau_c}\right)\right] \qquad \text{(eq. 8.7)}$$

Here, $Q_{f,v}$ is the enthalpy of formation of a vacancy, Ω is the molar volume, τ_c is a time constant associated with the decay of a vacancy following formation, and N is a constant that scales the vacancy concentration to $\dot{\varepsilon}$. Based on Lifshitz-Wagner theory, the coarsening rate of a second phase particles may be written as

$$\frac{dr}{dt} = \frac{B_1 \gamma_s V_m C_0}{3r^2 RT} K_2 n_{total} \qquad \text{(eq. 8.8)}$$

where, B_1 is a constant, γ_s is the specific energy of the particle-matrix interface, V_m is the molar volume of the second phase, C_0 is the equilibrium-solute concentration in the matrix, and K_2 is given by

$$K_2 = \frac{D_{sol}}{n_{eqlm}} = D^0_{sol}\exp[-(Q_{sol} - Q_{f,v})/kT] \qquad \text{(eq. 8.9)}$$

where, D_{sol} is the effective solute diffusivity in the matrix, and D_{sol}^{0} and Q_{sol} are the associated frequency factor and activation energy. Combining equations 8.5-8.9

$$3r^2\frac{dr}{dt}=\frac{B_1\gamma_s V_m C_0}{RT}D_{sol}\exp\left(\frac{\sigma_h\Omega}{kT}\right)\left[1+N\dot{\varepsilon}\left(1-e^{\frac{-t}{\tau_c}}\right)\right] \qquad \text{(eq. 8.10)}$$

In solution schemes where a stepwise updating of the particle radius equation by repeated recalculation of the history dependent term as

$$r(t+\Delta t)=r_0+r_{cum}+\Delta r \qquad \text{(eq. 8.11)}$$

where, r_{cum} is the cumulative increases in particle size from $t=0$ to $t=t$, such that $r(t)\approx r_0+r_{cum}$, and r_{cum} can be expressed as

$$r_{cum}=\left[\left(\frac{B_1\gamma_s V_m C_0}{RT}\right)\overline{D}_{sol}(t+2N\hat{\gamma}t_{hc}\nu_c\phi)+r_0^3\right]^{1/3}-r_0 \qquad \text{(eq. 8.12)}$$

The amount of inelastic strain accumulated during time t, may be approximated as $2\hat{\gamma}t_{hc}\nu_c\phi$, which gives the cumulative shear strain during ν_c thermal cycles, each with a half period of t_{hc}. Here $\hat{\gamma}$ is the average shear-strain rate during a half cycle, and can be approximated as $\hat{\gamma}\approx\frac{\Delta\alpha(T_{max}-T_{min})}{ht_{hc}}$, where $(T_{max}-T_{min})$ is the temperature range of the cycle. The term $\overline{D}_{sol}$ represents the solute diffusivity averaged over the temperature range of the thermal cycles corresponding to a time period of t_{hc}, and is given by

$$\overline{D}_{sol}=\frac{\int_0^{t_{hc}}D_0^{sol}\exp\left[\left(\frac{\sigma_h\Omega}{k}-\frac{Q_{sol}}{R}\right)\frac{1}{T}\right]dt}{\int_0^{t_{hc}}dt} \qquad \text{(eq. 8.13)}$$

For a linear time dependence of temperature $\left(T = T_{min} + \beta t\right)$ during thermal cycle, this yields the final expression of particle size, at any time $r(t)$ as

$$r(t) \approx \left\{ \left[\left(\frac{B_1 \gamma_s V_m C_0}{RT} \right) \overline{D}_{sol} (t + 2N\hat{\gamma} t_{hc} \nu_c \phi) + r_0^3 \right]^{1/3} \right\} \qquad \text{(eq. 8.14)}$$

In the above equation, when $\hat{\gamma} = 0,$ r represents the coarsened size caused by isothermal aging only, whereas when $\hat{\gamma} \neq 0,$ r includes contributions caused by both static aging and strain-enhanced (thermal cycling) coarsening. The parameters have been used to calculate the grain coarsening has been shown in Table 8.1. Figure 8.8 shows a plot of equation 8.14 for a 27 mm BGA solder joint for Sn95.5Ag4.0Cu0.5 solder alloy which subjected to thermal cycles at -40 to 125C. The experimental particle coarsening has also been plotted in the same plot. It is readily apparent that, in agreement with experimental observations the Ag_3Sn particle size coarsens rapidly in thermal cycling environment. The initial second phase particle is assumed to be the same as experimental particle size for analytical calculation. Equation 8.14 constitutes the second phase particle coarsening incorporating the creep formulation for the lead free solder. The main advantage of this analytical model are as follows: (a) the closed form of this formulation can be used in finite-element codes for joint reliability analysis; (b) It has built in coarsening effects, it directly accounts for local variations in microstructural scale within a joint, which is influenced by local strain history and state stress; (c) it explicitly accounts for effects of prior strain history, local hydrostatic stress, and the loading rate on the coarsening kinetics, and hence on the creep. The values of various parameters listed in the Table 8.1 are obtained from various literatures.

Properties and Constants Used in Calculation	
Thermal Cycling Parameters	$T_{min} = 233K$, $T_{max} = 398K$, $t_{hc} = 15 \min$ $\Delta\alpha = 12X10^{-6}/K$, $h = 0.65$ mm, $\phi = 0.9$
Particle Coarsening Parameters	$r_0 = 0.5\ \mu m$, $V_f(Ag_3Sn) = 0.007$, $B_1 = 5X10^{-3} m^3/moles^2$ $\gamma_s = 0.5 J/m^2$, $V_m(Ag_3Sn) \approx 1X10^{-5} m^3$, $N = 1000 s$ $C_0(Ag_3Sn) \approx 20\ moles/m^3$, $D_0^{sol} = 7X10^{-7}\ m^2/s$, $\Omega \approx 8.53X10^{-27}\ mole/m^3$, $Q_{sol} = 51.5\ KJ/mole$, $\sigma_h = 10\ MPa$ (assumed constant)

Table 8.1: Parameters Used for Particle Coarsening Calculation

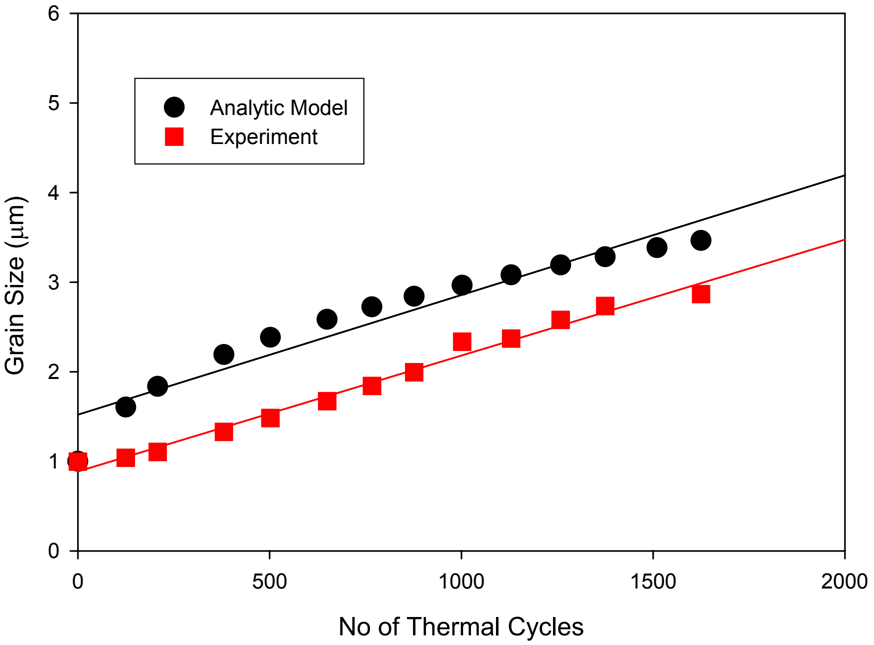


Figure 8.8: Comparison between Analytical and Experimental Increase in the Ag_3Sn Particle Size for 27mm Lead Free Solder Joint Subjected to -40 to 125C.

8.6 Crack Growth Measurements

Samples were cross-sectioned at various level of thermal cycling. Several sections were made per sample to study the crack initiation and propagation in various rows. The cross-sections were characterized by scanning electron microscopy (SEM). Primary and secondary crack lengths have been added. Multiple test boards were periodically removed form the chamber after every 125 cycles. Solder joint cracks have been measured at each temperature cycling data-interval. An average value of crack length across samples has been calculated for each set and cycle-count. The typical crack length with the cycle count for BGA components is shown in Figure 8.9. Figure 8.10 and Figure 8.11 show the crack initiation and propagation under thermo-mechanical stresses. The crack-growth rate for 63Sn37Pb solder has been compared with 95.5Sn4Ag0.5Cu solder interconnects for both the 27mm ball-grid arrays and 2512 resistors. The crack growth rate is constant w.r.t. number of cycles and comparable in both material systems. There is a significant difference in the crack-growth rates between chip resistors and ball-grid arrays. The 2512 chip resistors have much higher crack growth rate compared to ball-grid arrays for both material systems. Comparison of the crack growth rates for 17mm and the 27mm ball-grid arrays has been presented in Figure 8.10.

Fatigue cracks were typically found to initiate at package pad-to-solder interface and then propagate along a path parallel to the substrate pad (for BGA components) until complete separation (Figure 8.12). In almost all cases, the primary crack initiated at the package interface and later a secondary crack initiated at the board interface. Once the primary crack initiated, it progressed to other edges of the joint, and caused complete failure.

The 2512s exhibited faster crack propagation compared to 1225s. Cracked initiated underneath the part for resistors and then typically follow along a path that parallels the resistor termination then it goes to bulk solder until complete separation has occurred. Once the crack initiate at 2512 parts, it propagated very faster rate compared to the other types of packages on the metal-backed boards. The typical 2512 crack initiation and propagation is shown in Figure 8.13.

8.7 Prognostication Framework

8.7.1 Inelastic Strain Energy Density

The phase growth rate per cycle is closely related with the inelastic strain energy density per cycle. Prior studies have correlated the number of cycles to crack initiation and the crack propagation rate with the inelastic strain energy density [5, 79, 8, 98].

In this study, linear and non-linear, elastic, plastic, creep, temperature and time dependent and time-independent material properties have been incorporated in the finite element models. The thermal fatigue failure of electronic packages is associated with combined plastic-deformation and creep of solder joints. The Anand Viscoplasticity model for SnAgCu alloy [68-69], which has been previously used by several researchers to model the constitutive behavior, is used in this study. Figure 8.14 shows the 3D quarter symmetry finite element model for 17mm BGA, mounted on FR4 laminate. ANSYS™ was used to simulate the inelastic strain energy density.

The phase growth rate per cycle has been correlated with the inelastic strain energy density per cycle from non-linear finite element simulations (Figure 8.15). Data indicates that phase growth parameter and its derivatives are potential candidate proxies for leading indicators of failure. The correlation enables the evaluation of residual life in

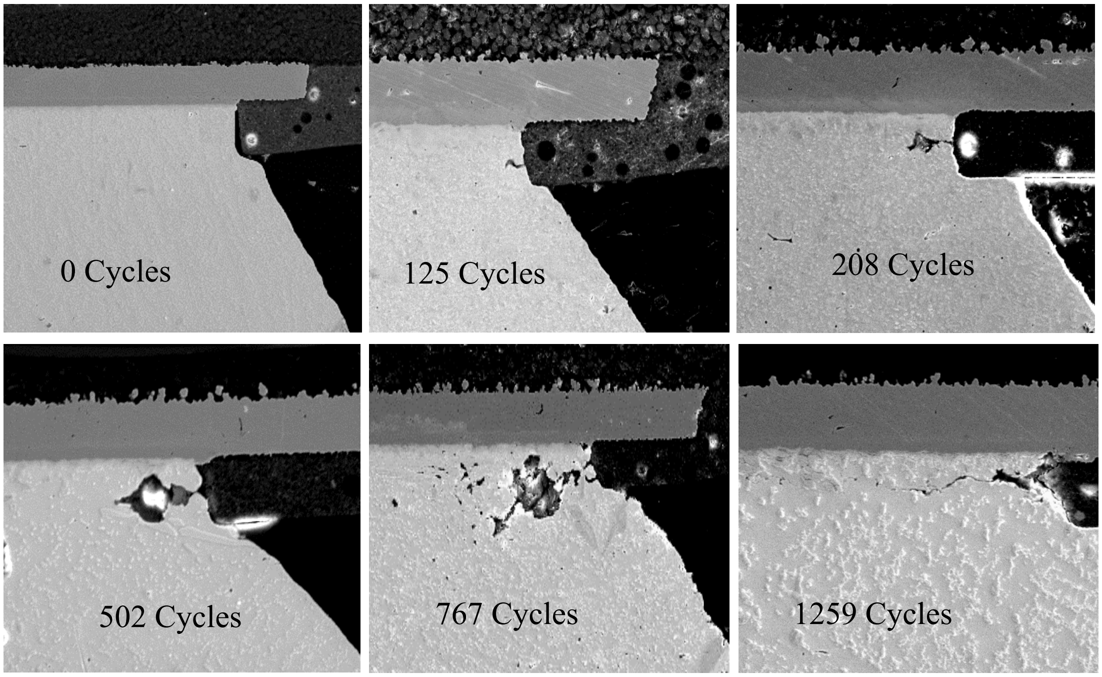


Figure 8.9: 27 mm BGA Solder Joints (95.5Sn4Ag0.5Cu Solder) Crack Propagation or Growth at Various Levels of Thermal Cycling (-40 to 125°C, Mag: 250).

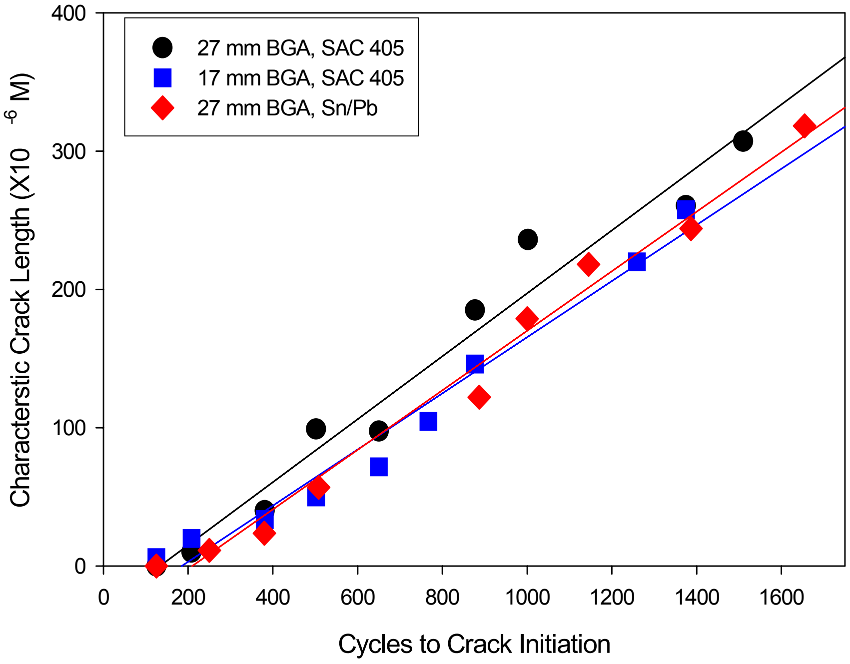


Figure 8.10: Crack Propagation Under Thermo-Mechanical Loads in 27 mm, and 17 mm BGAs with 63Sn37Pb and 95.5Sn4Ag0.5Cu Solder Interconnects

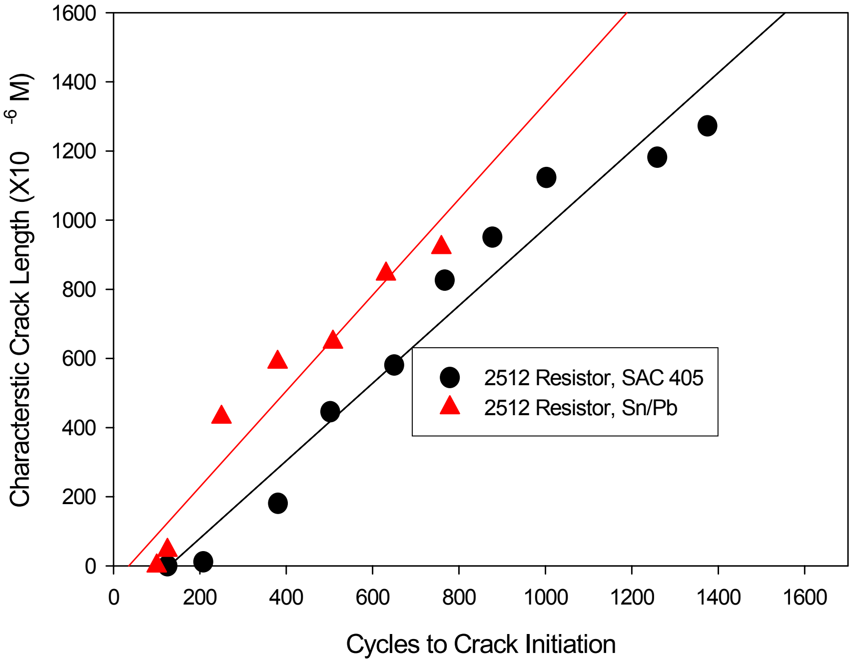


Figure 8.11: Crack Propagation Under Thermo-Mechanical Loads in 2512 Chip Resistor with 63Sn37Pb and 95.5Sn4Ag0.5Cu Solder Interconnects

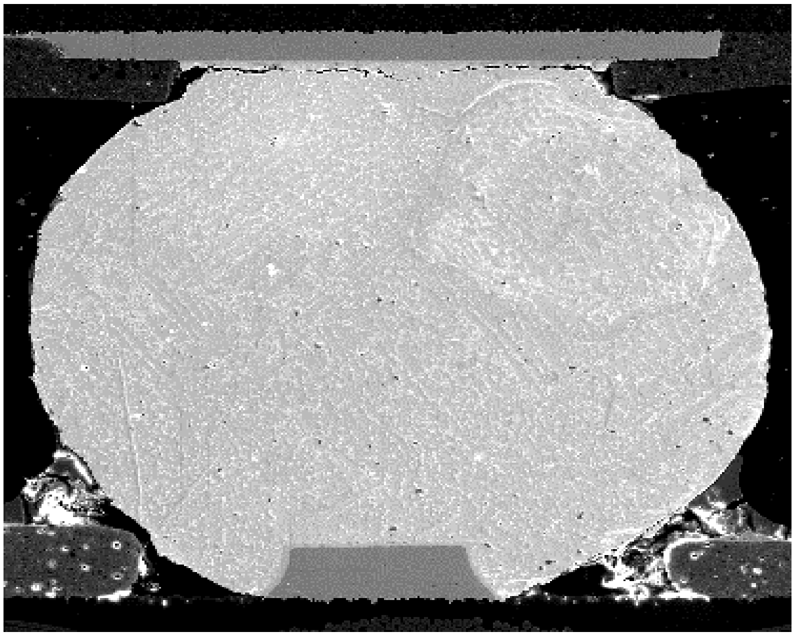


Fig 8.12: Typical X-Section of a Completely Cracked SnAgCu Solder Joint, 27 mm BGA after 1500 Cycles

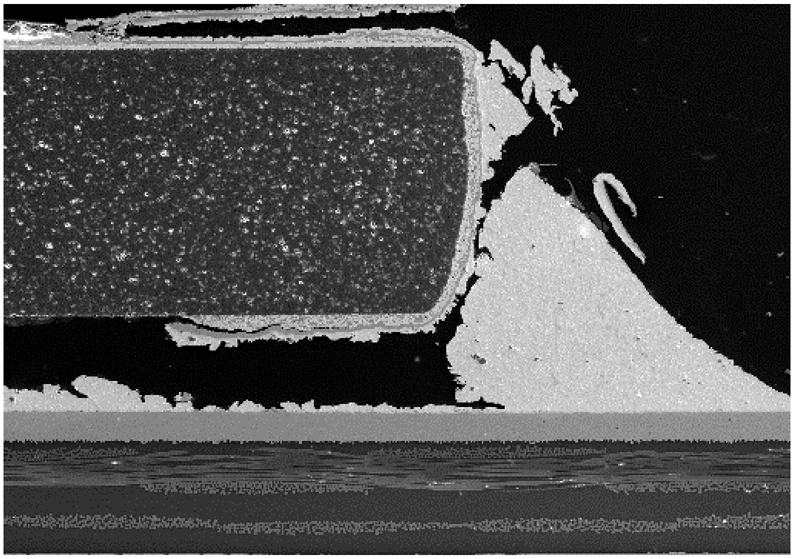


Fig 8.13: Typical X-Section of a Completely Cracked SnAgCu Solder Joint, 2512 Chip Resistor after 1250 Cycles

a deployed part. The rate of change of phase growth parameter of a deployed part can be measured under the intended use conditions of future part deployment. The corresponding damage accumulation rate can then be computed in terms of inelastic strain energy density, which can be used to evaluate residual life.

8.7.2 Time-to-First Failure

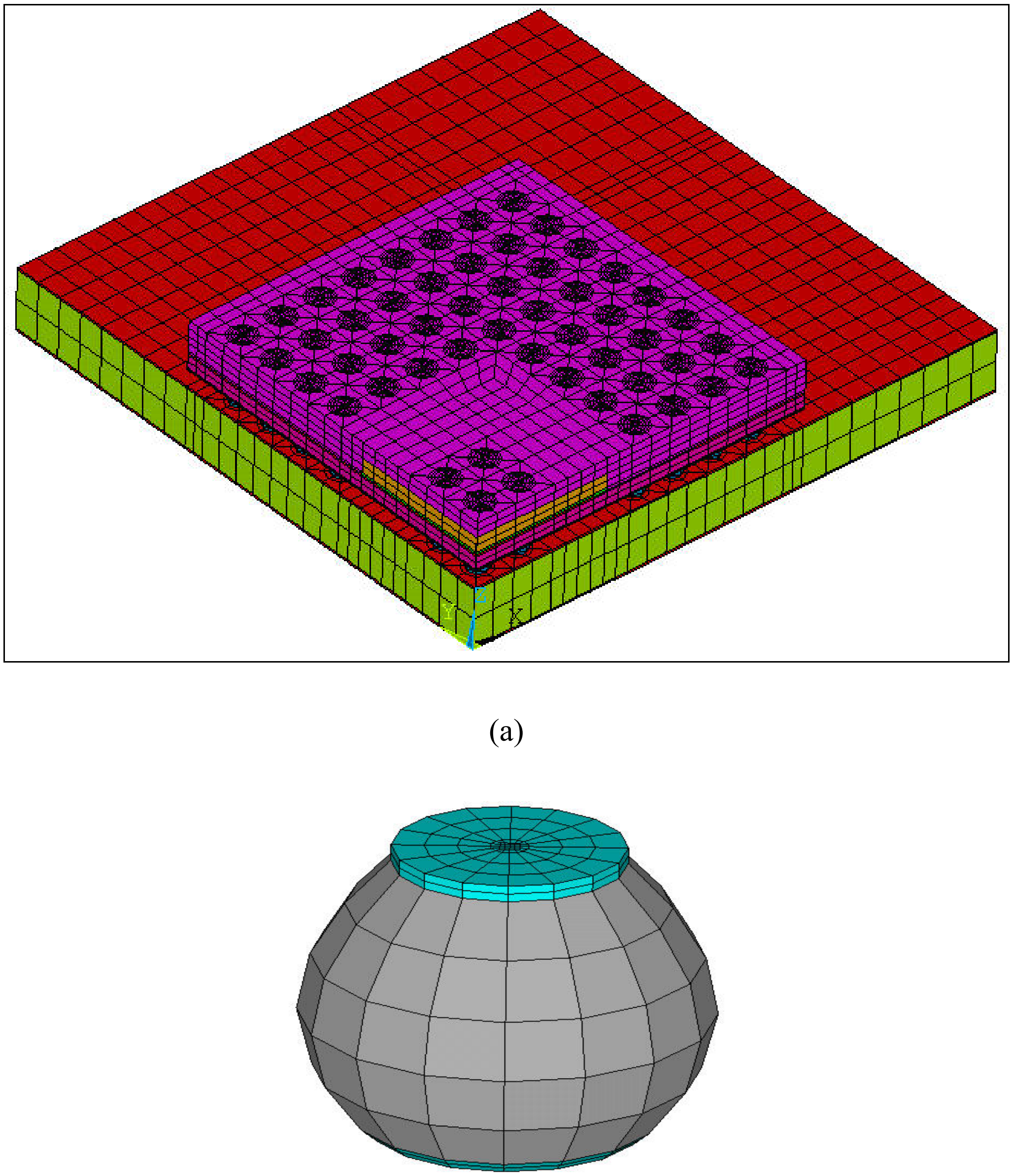
The time-to-1-percent failure ($N_{1\%}$) of solder joints can be correlated with the rate of change of phase growth parameter per cycle, $\frac{dS}{dN}$. Since the rate of change of phase growth parameter has been correlated to the inelastic strain energy density, ΔW, therefore, it is hypothesized that the faster phase growth correlates with faster accumulation of inelastic work in the joint and a lower cycles to crack initiation. The following power law type relationship has been developed for the solder interconnects,

$$N_{1\%} = C_2 \left(\frac{dS}{dN} \right)^{-\gamma} \tag{eq. 8.15}$$

Where C_2, and γ are constants. The relation enables the calculation of residual life. The phase growth rate in a deployed part can be monitored in the intended use-environment and the residual life evaluated (Figure 8.16).

8.7.3 Crack Growth Rate

The phase growth rate per cycle has been correlated to the crack propagation rate per cycle in the solder interconnects. Phase coarsening and phase growth has been demonstrated as a leading indicator of failure for lead free solder interconnects. The correlation indicates that components which progress to failure faster will exhibit a faster damage proxy magnitude in the form of Ag_3Sn phase growth parameter. The correlations



(a)

(b)

Figure 8.14: 3D Quarter Symmetry Finite-Element Mesh for 17 mm BGA, (a) Assembly, and (b) Fine Mesh Solder Ball with 1 mil Interface Layers.

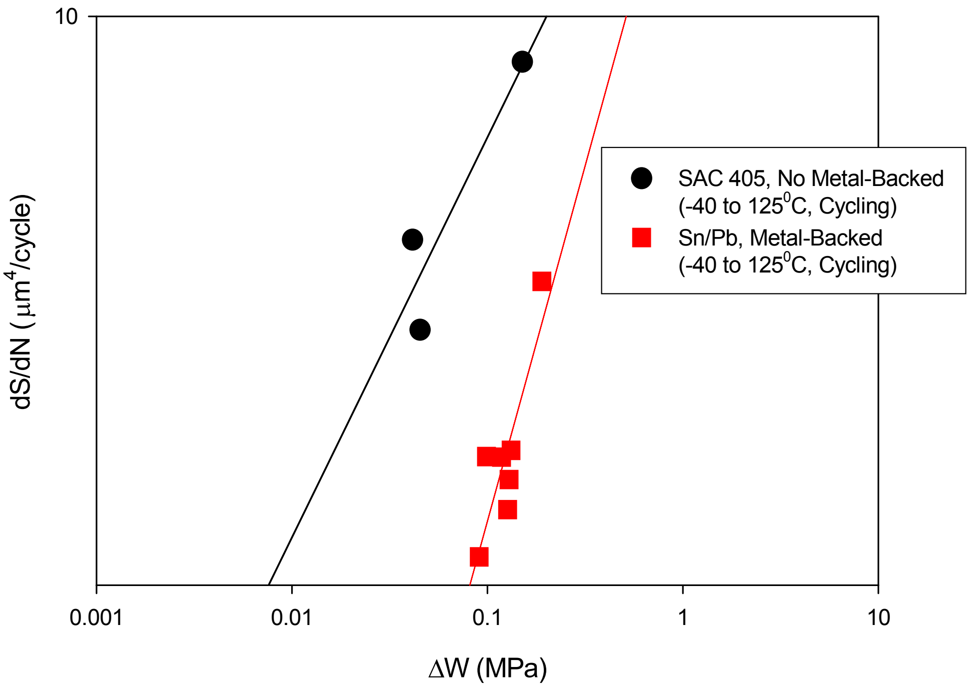


Figure 8.15: Relationship between Inelastic Strain Energy Density and Phase Growth Rate.

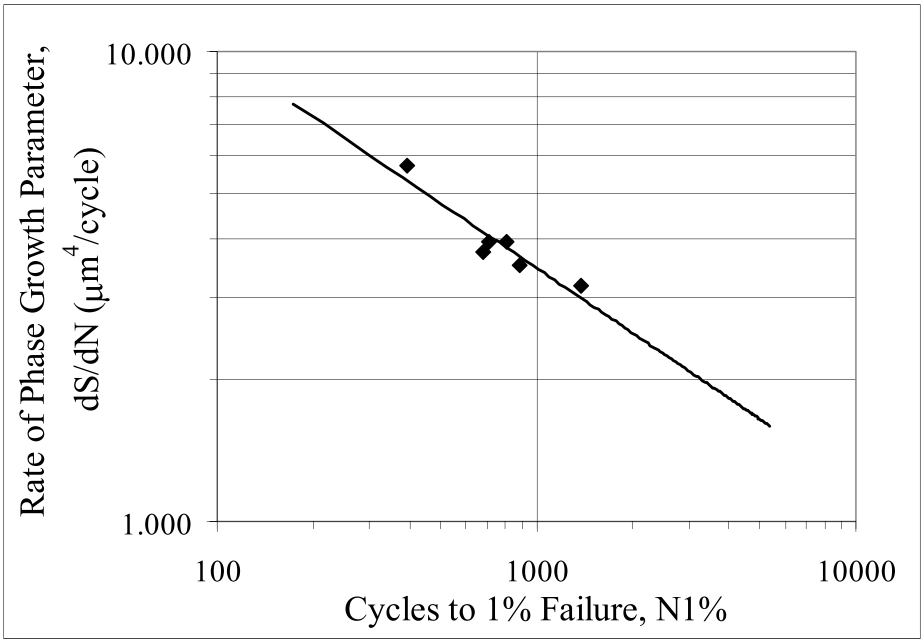


Figure 8.16: Relation between Number of Cycles to 1% Failure and Phase Growth Rate for 63Sn37Pb Solder.

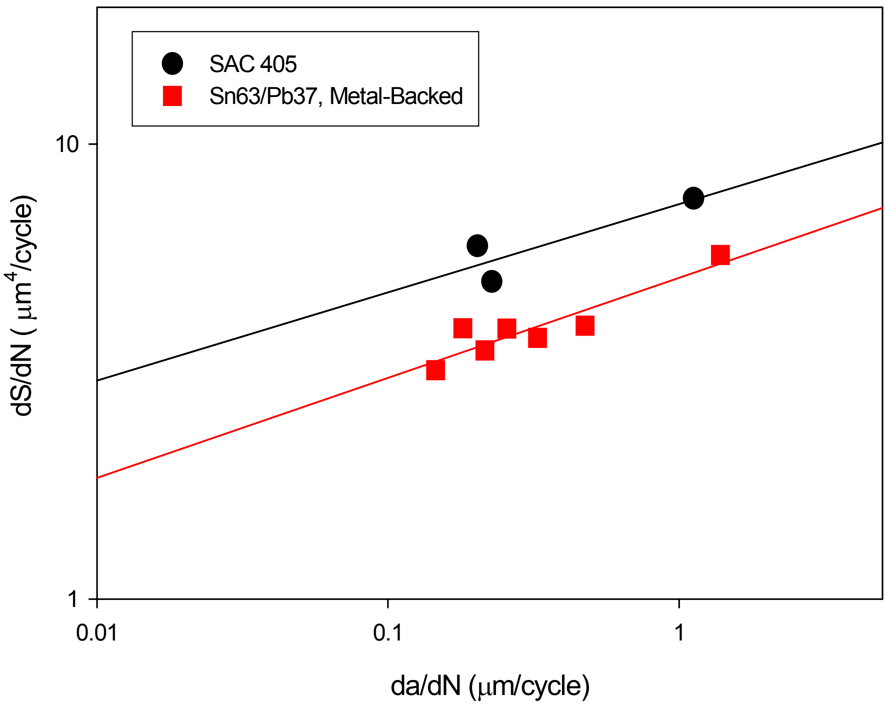


Figure 8.17: Relation between the Phase Growth Rate and the Crack Growth Rate for 63Sn37Pb and 95.5Sn4Ag0.5Cu Solders.

also provide validation for the prognostication methodology presented in the paper (Figure 8.17).

8.8 Intermetallic Thickness as Leading Indicator

In this portion of the study, the growth of the intermetallic thickness during thermal aging as leading indicator of failure has been explored. The present test vehicle has been used to investigate the correlation of interfacial intermetallic thickness growth versus thermal aging. In order to see the effect of intermetallic layer, the aged components are sliced periodically to measure the thickness. The mean thickness of IMC layers are measured using commercial image processing software on SEM images. An energy dispersive X-ray (EDX) has been used to examine the morphology and the composition of the intermetallic compound layer at the copper/solder interface. Colloidal silica solution has been applied for the detailed intermetallic compound composition observation and detection. Figure 8.18 shows the EDX analysis of the intermetallic compound layer of the 95.5Sn4Ag0.5Cu solder systems on immersion silver board.

The interfacial intermetallic layers are formed between solder and copper, and some precipitates appeared near the interface of the IMCs/solder. The intermetallic layers were identified in SEM micrograph and the morphologies are identified by EDX as Cu_3Sn and Cu_6Sn_5 phases. The compositions of the IMC layer are identified as Cu_6Sn_5 for the layer near the Solder Interconnect, and Cu_3Sn, for the layer near the Copper Pad. With the increasing aging time, the IMC layers thicken, and the local irregularities appear to gradually smooth out. Figure 8.19 shows SEM backscattered images exhibiting an example of intermetallic growth process in the 17 mm BGA solder ball during the thermal aging test condition.

Trend analysis of intermetallic thickness growth on SEM using image processing software, indicates a square root dependence of IMC thickness versus aging time,

$$y(t) = y_0 + kt^{1/2} \qquad \text{(eq. 8.16)}$$

Where $y(t)$ is IMC growth thickness during aging, y_0 is the initial thickness of intermetallic compounds, k is the coefficient standing for the square root of the diffusivity at aging temperature, and t is test time. The exponent value, 1/2, in the above equation reveals a diffusion-controlled mechanism during aging. The average IMC growth measured at each level of test time for each component set cross-sectioned has been shown in Figure 8.20. The IMC growth data in this study indicates that growth rate

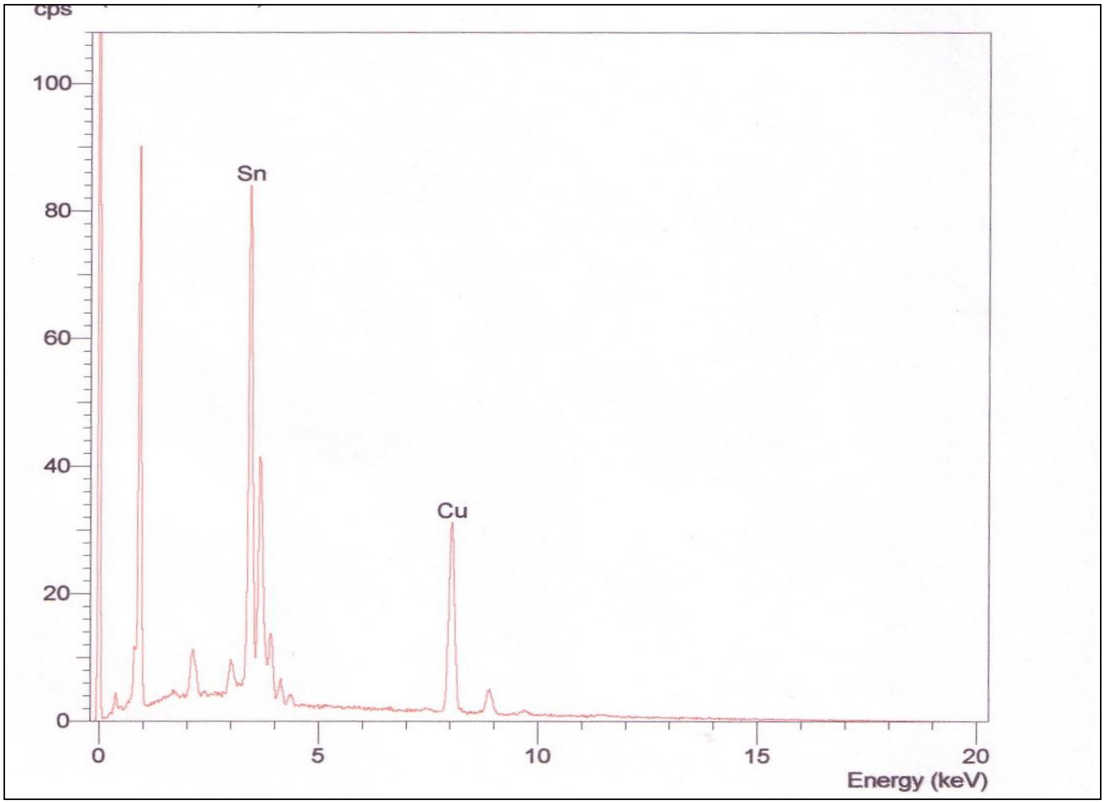


Figure 8.18: EDX Analysis for Morphology and the Composition of Intermetallic Compound.

stays fairly uniform during the thermal aging. It is observed that for both Sn-Ag and Sn-Pb solder systems, the intermetallic compound thickens roughly as $t^{1/2}$ in a linear manner, where t is the aging time as expected for diffusion-controlled growth. From this study we have found that IMC growth rate of SnPb solder is at least 1.5 times higher than the 95.5Sn4Ag0.5Cu solder. Similar to the grain growth rate for leaded and lead free solders, IMC growth rate for SnPb and lead free solder is not the same for thermal aging. A comparative study has been done for SnPb and 95.5Sn4Ag0.5Cu solder. Figure 8.20 shows a comparative study between Sn/Pb and 95.5Sn4Ag0.5Cu alloys IMC growth rate. The IMC thickness in the lead free solder is much thicker than the SnPb solder at unaged stage but the growth rate is higher in SnPb solder than 95.5Sn4Ag0.5Cu. A correlation between IMC growth rate and time can be used as a proxy parameter and evaluation of time at temperature for a deployed part.

8.9 Implementation of Prognostic Parameters

Prognosis is a “forecast of future performance or condition. The ability to detect failures before they happen, or before they would occur, i.e. high confidence of no failures during a defined mission length, early enough to do something about it. Implementation details are practical design aspects, which may be addressed differently by different programs. The prognostics approach presented in the paper may be implemented using sacrificial devices, which can be cross-sectioned to determine the failure progression of the assembly. It is envisioned that the sacrificial devices will be small, low cost, such that several of these can be conveniently located along edge of card assemblies to enable cross-sectioning or on a separate card within an electronic module or card cage. For example, in the case of solder interconnects, chip resistors may be included on the board assembly and serve as sacrificial devices, which can be periodically cross-sectioned.

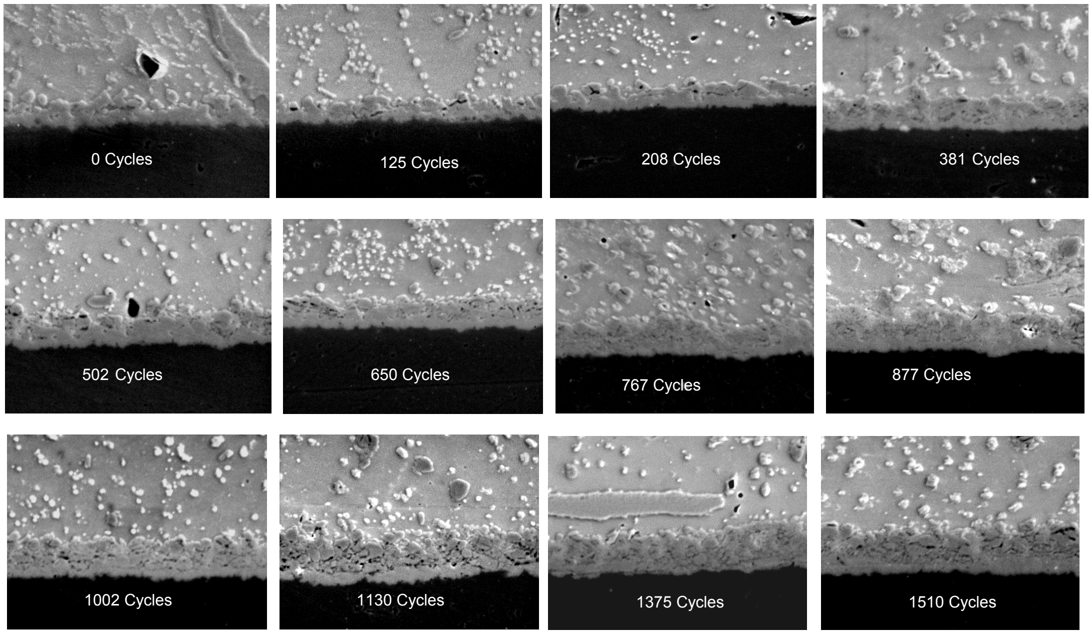


Figure 8.19: SEM Back-scattered Images of IMC Growth versus Thermal Aging (-40 to 125°C, 95.5Sn4Ag0.5Cu solder, 17 mm BGA, Mag: 2000)

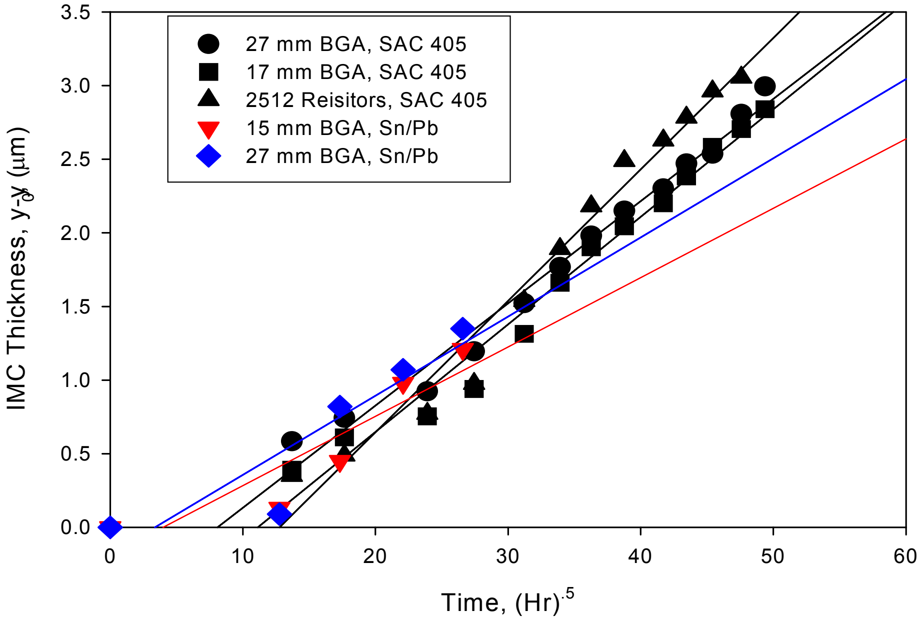


Figure 8.20: IMC Growth, at Various Levels of time for15 mm, 17 mm, 27 mm BGA, and 2512 Chip Resistor with 95.5Sn4Ag0.5Cu, and Sn/Pb Solder.

It is not required to assume that all the components mounted on the same board have the same exposure to environmental or operational stresses. However, it is required that the stress variation for the different devices be known and characterized. The sacrificial components are cross-sectioned when the card assemblies, e.g. avionic card assemblies aboard aircraft, need to be redeployed. The baseline phase-size is then measured. The part assemblies to be deployed in the intended use environment will then be subjected to finite-cycles of controlled environmental temperature exposure characteristic of the intended use environment. Another sample of the sacrificial device is then cross-sectioned to enable calculation of the phase growth rate. The residual life can then be calculated based on knowledge of the accumulated initial damage and the phase growth rate in intended use environment.

The correlation of prognostic damage proxies with inelastic strain energy density enables the evaluation of residual life in a deployed part. The rate of change of phase growth parameter of a deployed part can be measured under the intended use conditions of future part deployment. The corresponding damage accumulation rate can then be computed in terms of inelastic strain energy density, which can be used to evaluate residual life.

The sacrificial components include the same mechanisms that lead to failure in standard components: failures occur within the sacrificial device in same package elements (e.g. solder joints) they occur in other components. The advantage of the proposed approach is that any extrapolation using acceleration factors not necessary. Passive indication of damage/environmental exposure: no data storage is required. Further, the time-to-1-percent failure can be computed by subjecting the sample a very short accelerated test, e.g. 50 cycles. The computed phase growth rate from experimental observation can be used to compute the time-to-1-percent failure. The main advantage of this approach is one can calculate the crack initiation life cycle of the solder joint subjected to harsh environment by measuring the average phase growth parameter at any level of cycling. In this method, there is no need for an expensive thermal cycle life-test. If the phase growth parameter at any two level of aging is known, then time-to 1% failure life can be computed from the Figure 8.16. Further, given the damage state of a deployed component, the prior-elapsed time in any thermal environment can be computed based on known phase growth rate, given the initial phase size after reflow. The residual life can then be computed based on the computed phase growth rate for the desired use environment.

8.10 Summary and Conclusions

A methodology for prognostication-of-electronics has been developed and demonstrated with data on leading indicators of failure for accurate assessment of product damage significantly prior to appearance of any macro-indicators of damage. Phase growth rate and interfacial intermetallic layers growth rate have been identified as proxies for determination of residual life in electronic structures. The theoretical basis for the selection of prognostic parameters has been discussed. Mathematical relationships have been developed between phase growth, derivatives of phase growth, intermetallic growth for interrogation of residual life and damage state. Prognostic parameters have been validated versus macro-indicators including cracks initiation, crack propagation rates and inelastic strain energy density for both SnPb and SnAgCu solders. A framework for implementation of the prognostication approach has been discussed including, sacrificial devices, which can be examined to determine the damage state of the assembly.

CHAPTER 9

SUMMARY AND CONCLUSION

Under-the-hood reliability of fine pitch packages have been evaluated for automotive thermal cycling environment. Various methods of enhancing reliability have been explored including increased BT substrate thickness, the utilization of NSMD pads on the BGA component, alternative PCB plating finishes, and the use of four different underfill encapsulants. In most of the cases, larger package size yields better reliability. Components with thicker BT substrate have higher reliability both with and without underfill condition. Overall reliability enhancements with underfill ranged from 1.5X to greater than 4.4X, relative to the non-underfilled BGAs. Smaller packages (15, 17 mm) can be used for under-the-hood application by incorporation appropriate Underfill encapsulants.

Solder joint thermal fatigue damage model has been developed for fine pitch packages in automotive under-the-hood application. The damage relationships imply a lower sensitivity to increase in inelastic strain energy density for both crack initiation and crack propagation than previously believed indicated by a smaller slope. The damage relationships in the present analysis have been derived for a mesh size of 1.5 mils close to the interfaces. The main objective of this study was to build a better solder damage relationship for the underhood application that can minimize the predicted error. In most cases predicted error with respect to experimental data has been reduced by approximately 50%. More accurate results can be predicted by carefully measuring the crack growth data on a large sample size.

Component reliability for metal-backed condition has been analyzed. Results demonstrate that the metal backing of organic laminates (i.e., FR4-06) plays a critical role in meeting the reliability goals for harsh environments. The addition of metal backing significantly increases the board level thermal performance as well as structural stability during the application in real environment but on the other hand CTE of the metal substrate threatens a potential reliability issues for many electronic packages. Thus, there exists a trade-off between an increased path for thermal conductivity and reduction in the overall reliability on metal backed boards. Impact of several different types of metal substrates and different types of adhesives for thermal cycling environment has been analyzed. The crack measurements show that crack propagation rate on metal backed boards is much faster (≈ 1.7x) than non-metal backed boards. Further, ball-grid arrays on metal backed boards' exhibit lower number of cycles-to-crack initiation than packages on non-metal backed boards for any inelastic strain energy density. A new set of damage relationships for the metal-backed substrate has been developed for N1% life prediction models.

Optimum damage volume for fine pitch packages in automotive underhood application has been analyzed. It has been found that optimum damage volume in the interface elements consist of two layers of .5 mils element thickness. Since the largest deformation takes place at the interface of solder and copper pad so two layers of .5 mils element thickness has been considered as optimum damage volume of solder ball and evaluated as best suited empirical model in this analysis. Lower accuracy of fitting has been obtained when considered only one element layer of interface elements. Mesh refinement error in the modeling methodology has been analyzed, and it is found that acceptable percentage of relative error due to different mesh refinements is less than 10%. Three different mesh refinements have been done for error estimation, and convergence test. Both corner element and interface elements are selected for the convergence test in this study. The percentage of error calculated for the interface elements are much lower than the corner elements because in this case, averaging few elements from the interface supersedes the singularity problem.

A methodology for prognosis-of-leaded electronics has been demonstrated with data on leading indicators of failure for accurate assessment of product damage significantly prior to appearance of any macro-indicators of damage. A power law relation has also been investigated between the number of cycles to crack initiation and the average increase in the α-Pb phase growth parameter. In this study, the use of rate-of-change of phase growth parameter has been investigated. A mathematical relationship has been developed between phase growth rate and time-to-1-percent failure. The relationship enables the assessment of life consumed based on phase growth rate and a forward-estimate of residual life. The phase growth rate per cycle has been correlated with the inelastic strain energy density per cycle from non-linear finite element simulations. The corresponding damage accumulation rate can then be computed in terms of inelastic strain energy density, which can be used to evaluate residual life.

Thermal cycling reliability of lead free electronics has been evaluated for automobile underhood application. There have been many reports that solder joint reliability can actually be increased for a given application by using a lead-free replacement alloy such as of Sn-Ag-Cu instead of conventional Sn-Pb. Mixed results have been found in our experiment.

Similar to leaded electronics prognostication of lead free electronics for health monitoring has been investigated. Lead free solder (SnAg4.0Cu0.5) phase growth rate and interfacial intermetallic layers growth rate have been identified as proxies for determination of residual life in electronic structures. The theoretical basis for the selection of prognostic parameters has been discussed. Mathematical relationships have been developed between phase growth, derivatives of phase growth, intermetallic growth for interrogation of residual life and damage state. A framework for implementation of the prognostication approach has been discussed including, sacrificial devices, which can be examined to determine the damage state of the assembly.

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