THERMAL PERFORMANCE OF BALL GRID ARRAYS

AND THIN INTERFACE MATERIALS

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THERMAL PERFORMANCE OF BALL GRID ARRAYS

AND THIN INTERFACE MATERIALS

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VITA

Yasser Ahmed Elkady was born on December 25, 1968, in Cairo, Egypt. He joined the faculty of engineering at Ain Shams University, Cairo, Egypt in 1986. He graduated in 1991 with a B.Sc. in Mechanical Engineering. Following graduation, he filled the position of Senior Integrated Manufacturing Engineer for a major international CAD/CAM/CAE solution provider in Cairo, Egypt. In 2000, he joined the Department of Mechanical Engineering at Auburn University, to pursue the degree of Doctor of Philosophy in Mechanical Engineering.

DISSERTATION ABSTRACT

THERMAL PERFORMANCE OF BALL GRID ARRAYS

AND THIN INTERFACE MATERIALS

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Current electronic packages exhibit very high and ever increasing power densities. That trend mandates the need for enhanced thermal performance. This study introduces a state of the art apparatus to measure thermal resistance of electronic packages. The apparatus was designed to minimize human interaction and to maximize measurement accuracy through the use of a computer automated data acquisition and control system.

The developed apparatus was used to measure thermal performance of Ball Grid Array packages. The impacts of different package configurations and board and assembly parameters on thermal performance were investigated. The parameters under investigation were die size, use of thermal balls, number of perimeter balls, use of underfill, and PCB heat spreader and thermal via design. By comparing the thermal

performances of different packages, it was observed that utilization of larger die, use of thermal balls, use of underfill and rich copper PCB thermal vias can reduce thermal resistance by up to 60%. The number of perimeter balls did not have a notable impact on thermal performance due to their remote location from the die surface. Numerical thermal simulations of all test parameters combination were developed and were found to be in good agreement with the experimental measurements.

The impact of thermal cycling on thermal performance was also investigated experimentally. Packages expected to be least reliable (with large die and no underfill), showed initial increase of thermal resistance after 750 thermal cycles. Further increases in thermal resistance were observed with continuous thermal cycling until solder joint failure occurred at 1250 cycles, preventing additional measurements. The correlation between thermal cycling and thermal resistance was then analyzed using a numerical structural simulation model that predicted crack initiation in the solder joints.

A second apparatus based on the ASTM 5470D standard was developed to measure thermal resistance of thin components and interface materials used in electronic packaging. Thermal contact resistance versus applied force at the aluminum metering block surfaces was evaluated by testing 2 copper samples of different thicknesses. The established correlation can be used to correct future thermal resistance measurements. A new RTD Assembly was proposed to overcome current bare RTD fragility problems. The new proposed temperature probe dimensions and material were selected based on a numerical optimization study using a design variable sweep technique.

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CHAPTER 1

INTRODUCTION

1.1 History of Electronic Packaging

In 1947, Bardeen, Brattain and Shockley invented the first bipolar transistor at Bell Labs. In 1958 Jack Kilby of Texas Instruments invented the first integrated circuit (IC) [1]. Subsequently, larger scales of integration were developed, producing miniature circuits capable of performing complex tasks. The newly developed ICs needed some sort of packaging. The electronic packages had to perform specific tasks, such as protecting the fragile electronic circuit, providing connections for input/output connections, providing power connections, supporting the package and removing the heat generated by the package.

There are numerous designs of electronic packages depending on application, number of I/Os and power dissipation. The first electronic packages were of "Through-hole" type where the package leads were inserted into through holes in the PCB. That was followed by surface mounting technology where components were mounted directly on the substrate surface [2]. The next breakthrough was the introduction of area array packages like flip chip and Ball Grid Array configurations. The pin counts these packages offered were at least ten fold of what was possible with the DIP and SOP packages. The first area array package was the Ceramic Pin Grid Array [3].

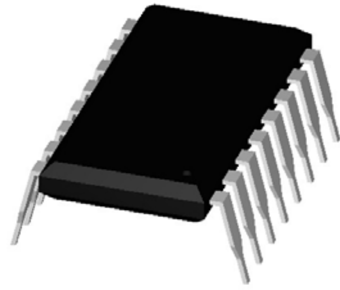
The BGA did not gain popularity until 1989 when Motorola introduced the first BGA with a lower cost Bismaleimide Teriazine (BT) substrate, which was called OMPAC (Over Molded Plastic Pad Array Carrier). Illustrations of some of older and recent electronic packages are shown in Figure 1.1.

1.2 Ball Grid Array Construction

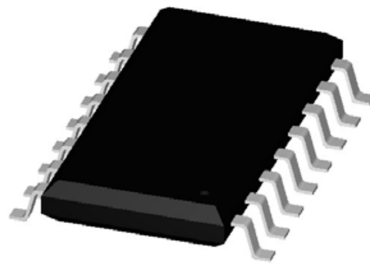
The high pin count of BGA (typically in the range of > 250 connections) is one of the most popular packages of choice in the electronic packaging industry [1]. BGAs also offer additional advantages such as small foot print, self alignment, elimination of the need for lead inspection/straightening, and convenience of using standard processes and equipment for surface mounting.

In spite of these advantages, BGAs have their share of manufacturing problems such as difficulty of solder joint inspection and reworking, which the industry is tackling by using good process control such as paste inspection and reflow profiling to ensure good solder joints [2]. BGAs come in different varieties depending on the construction materials and leads geometry. However, almost all construction variations share the common feature of a BGA substrate that connects the die bumps to the package connections [3].

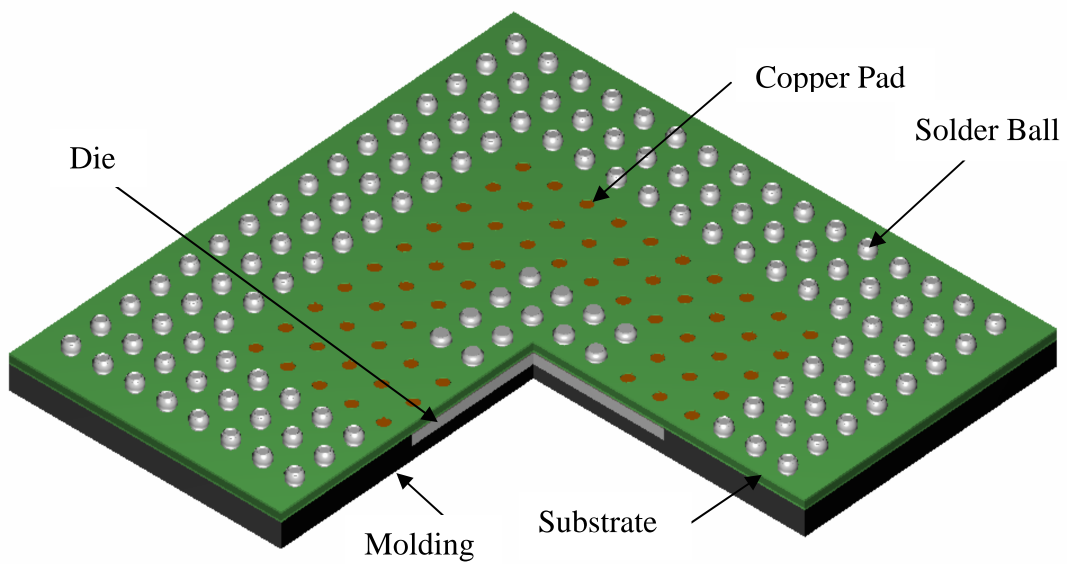
The first distinct variation of BGA packages is the material used for the BGA substrate (sometimes referred to as the interposer board). BGAs with ceramic substrates are called CBGAs, while those with plastic substrates are called PBGAs. CBGAs are typically hermetically sealed to eliminate the negative influence of moisture on the package reliability.



(a)



(b)



(c)

Figure 1.1 - Types of electronic packages
(a) Dual In Line Package (DIP)
(b) TSOP (Thin Small Outline Package)
(c) PBGA (Plastic Ball Grid Array)

CBGAs also exhibit higher thermal expansion coefficient mismatch with the PCB, which is major factor effecting package reliability. On the other hand, PBGAs offer simpler manufacturing techniques, less thermal expansion coefficient mismatch with the PCB and lower cost [2]. Another variation of the BGA construction is TBGA (Tape Automated Bonding Ball Grid Array), where the substrate is made of thin flexible material with two copper planes for ground and signal [3].

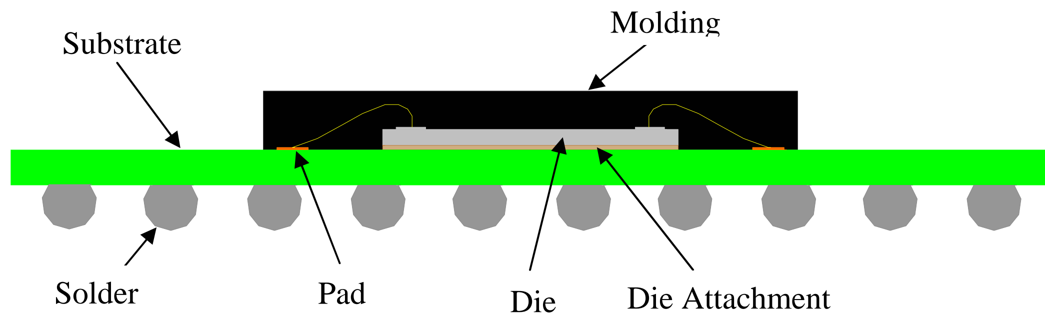
The second distinct variation is the method of routing the connections from the die to the substrate. Die may be bonded to the substrate using die attachment adhesive, then gold or aluminum wires connect bond pads on the die to bond pads on the substrate. Alternately, the chips may be flipped upside down and connected through a set of solder balls to pads on the substrate; such configuration is typically called FCBGA (Flip Chip Ball Grid Array) [3].

The third distinct variation is the shape of the connection between the BGA and the PCB. The connection may be in the form of solder balls or solder columns [4]. The selection of a specific BGA construction detail and material is dictated by cost limitations, reliability concerns and type of application. Illustrations of different types of BGA packages are shown in Figure 1.2.

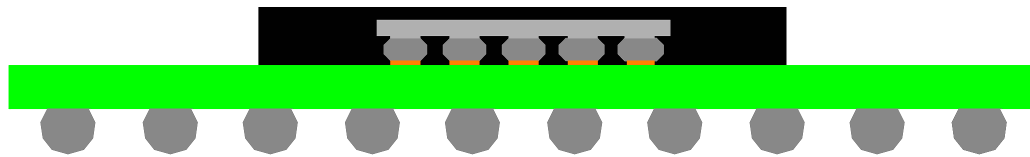
1.3 Impact of Temperature on Electronic Packages

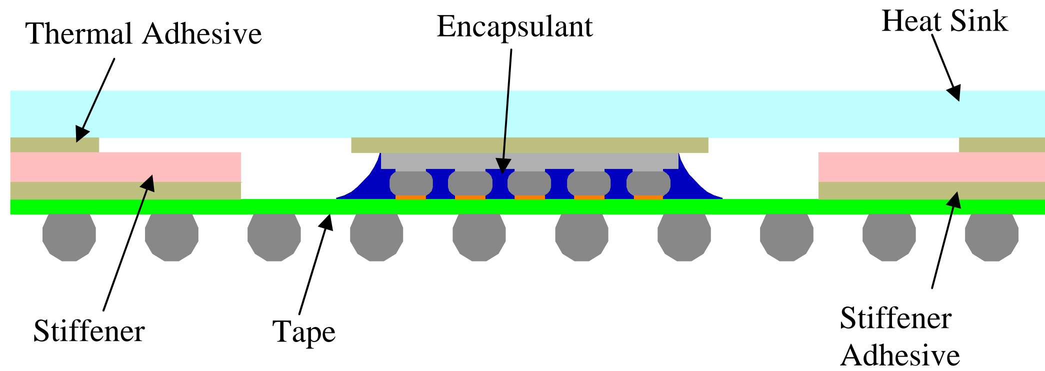
The life of all materials including semiconductors is normally observed to vary logarithmically with the reciprocal of the absolute temperature as expressed by the Arrhenius equation:

$$L = A(e^{b/T} - 1) \quad \text{(Eq. 1.1)}$$



(a) Plastic ball grid array


(b) Flip chip ball grid array



(c) Tape automated bonding ball grid array

Figure 1.2 - Types of ball grid array packages

where:

L = expected life

A = constant for the material

b = a constant related to Boltzman constant

T = absolute temperature [K]

The solution of Arrhenius equation predicts that the life of any device is halved for every 20° C rise in temperature [4]. The problem of high operating temperature of electronic packages is continuously growing due to continuous decrease of feature size of circuit chips as well as the massive increase in number of circuits per chip. In fact, since the invention of the IC in 1958, there has been a huge increase in the number of circuits per chip [2]. This trend has outlined the importance of thermal management for today electronic packages in order to minimize the maximum operating temperature by maximizing the efficiency of heat transfer from the package to the ambient [1].

The impact of temperature goes beyond material degradation and affects reliability of electronic packages as well. Temperature rise generates thermal stresses in structures that consist of different materials with different thermal expansion coefficients. The impact of the mismatch of thermal expansion coefficient may be augmented by non-uniform temperature distribution within the structure, as in the case of electronic packages. The level of thermal stresses within electronic packages is a key factor directly effecting package reliability.

1.4 Heat Removal Modes

Heat removal from electronic packages is usually done trough a combination of two distinct modes. The first mode is convection, which is defined as the heat transfer between a solid and a moving fluid and governed by:

$$Q = hA(T_s - T_f) \qquad \text{(Eq. 1.2)}$$

where:

h = heat transfer coefficient

A = cross sectional area for heat flow

T_s = surface temperature

T_f = Fluid temperature

The convection heat flow equation indicates that heat removal can be enhanced by either increasing the flow surface area, as in the case of using finned heat sinks, or by increasing the heat transfer coefficient. [5]. The later approach is more complex as it depends on many parameters such as type of cooling fluid, fluid velocity, surface orientation, surface shape and surface dimension. However, since the cooling fluid in most electronic packaging applications is air, the improvement of heat transfer coefficient by increasing the cooling fluid flow velocity may have considerable restrictions imposed by limitation of space, power and type of application.

The second mode is conduction heat flow which is defined as the heat transfer through a solid and governed by:

$$\rho C \frac{\partial T}{\partial t} = \ddot{q} + \frac{\partial}{\partial x}\left(k_x \frac{\partial T}{\partial x}\right) + \frac{\partial}{\partial y}\left(k_y \frac{\partial T}{\partial y}\right) + \frac{\partial}{\partial z}\left(k_z \frac{\partial T}{\partial z}\right) \qquad \text{(Eq. 1.3)}$$

where:

T = Temperature

t = time

ρ = Density

C = Specific heat

$\ddot{q}$ = Heat generation rate per unit volume

k_x, k_y, k_z = Thermal conductivity in x,y and z directions respectively

The continuous trend of minimizing electronic packages footprint limits the choice of increasing heat flow by increasing the heat flow cross section [5]. The alternative is to increase the overall thermal conductivity of the package by us which is governed by constituent materials thermal properties as well as package geometry.

1.5 Definition of Thermal Resistance

Thermal resistance is defined as a measure of the ability to resist heat flow. The concept of thermal resistance may be simplified by taking advantage of the analogy between thermal and electrical systems. Using this analogy, current is analogous to heat flow; voltage difference is analogous to temperature difference and thermal resistance is analogous to electrical resistance.

The three dimensional resistance to heat flow may be approximated by modeling a network of one dimensional resistors representing the various layers inside an electronic package. An approximate thermal resistor network for a PBGA package is shown in Figure 1.3. Thermal resistance definition differs depending on mode of heat transfer. For

conductive resistors, the thermal resistance is defined as $\frac{L}{Ak}$ while for convective resistors the resistance is defined as $\frac{1}{Ah}$, where L is the length of the heat flow path, A is the cross section area of the heat flow path, k is the material thermal conductivity and h is the convection heat transfer coefficient.

The overall thermal resistance of the package is dependent on the thermal resistance of its constitutive layers. The challenge of designing thermally efficient electronic packages arises from the fact that there is a difference of more than three orders of magnitude of thermal conductivity among the materials that affect the thermal performance of the package [3]. Table 1.1 lists thermal conductivity of common materials used in electronic packaging

1.6 Experimental Measurement of Thermal Resistance

Experimental thermal resistance measurements offer an insight for how to make design decisions and geometrical details and material choices for electronic packages in order to affect their thermal performance. Thermal resistance of electronic packages can be measured by powering the package with a known input power and measuring the temperature difference between the die surface and a constant reference temperature.

JEDEC Standards JESD51 [6], JESD51-1 [7] and, JESD51-8 [8] offer tentative details for thermal resistance measurements describing geometry of board, package and test fixture as well as environmental test requirements. For packages equipped with external heat sinks, the temperature difference is measured between the die surface and

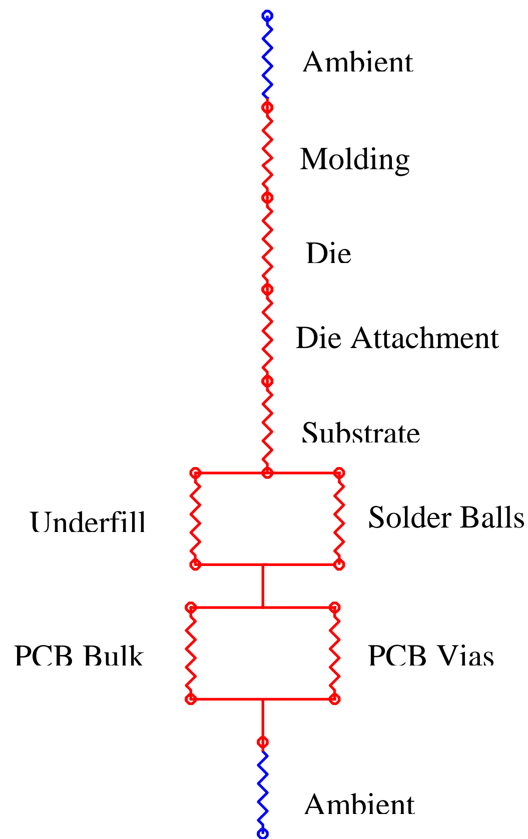


Figure 1.3 - Approximate thermal resistor network of a PBGA package

Table 1.1 - Typical thermal conductivity of common materials used in electronic packaging

Material	Thermal Conductivity [W/(m K)]
Solder mask	0.25
Solder	50
Molding compound	0.8
Die attachment	2
Silicon Die	140
PCB	0.36
Copper	390

the PCB. The cold plate is usually constructed from a high conductive material such as copper with embedded cooling water channels. Die surface temperature may be measured using integrated devices such as on-chip diodes or resistors while the board temperature is measured using T, J or K type thermocouples.

Although the standards offer great detail of test setup and procedures, they do not offer solutions to some practical problems such as how to overcome the unevenly distributed contact resistance between the board and the cold plate, which can be attributed to flatness deviation of the cold plate surface and/or board warp. Another cooling method is to directly expose the back surface of the PCB to a flow of cooling water. That later approach, however, is limited to board designs that do not allow coolant to leak to the front surface of the board.

1.7 Correlation between Thermal Performance and Package Reliability

Historically, thermal performance and package reliability have been researched as two distinct areas despite the fact that the state of stress in an electronic package depends on temperature distribution within the package, which is directly related to package thermal performance. On the other hand, cracks induced by thermal stresses can impede heat flow which might cause drastic changes in the package thermal resistance. Thus, it would be beneficial to study the impact of structural failure (such as crack initiation and propagation) on thermal performance of electronics. Typically, experimental package reliability studies are time consuming as they involve thermal cycling of electronic packages for extended periods of time as well as cross sectioning and polishing of multiple electronic packages at different levels of thermal cycling to check for crack

initiation and speed of propagation. However, recent research efforts offered numerical simulation models that are capable of predicting crack initiation and speed of propagation with a high degree of accuracy.

1.8 Experimental Thermal Resistance Measurements of Constitutive Components

Since thermal resistance of individual components and materials used in the construction of an electronic package have direct impact on the thermal performance of that package, it would be helpful to be able to accurately measure thermal resistance of those materials and components. The problem of measuring thermal resistance of electronic packaging materials such as underfill and BT substrate is that they are typically very thin. Intrusive temperature measurement methods where temperature sensors are inserted/attached to a measured sample are not possible. ASTM standard D5470-95 [9] offers construction outlines of an apparatus that is capable of measuring thermal resistance of such thin components. The apparatus generates a measured one dimensional heat flow that passes through the sample. Temperature at the upper and lower sample surfaces are calculated by extrapolating measured temperature variations in the two metal columns of known thermal conductivity. ASTM standard D5470-95 also specifies that the measurements should be conducted in a vacuum environment to minimize heat loss to the environment. The standard defined a few recommendations for test procedure and construction details:

1- Contacting surfaces should be within 0.4 μm of a true plane.

2- Apply a 3 MPa ± 0.1 MPa pressure on the sample surface to minimize contact resistance between the sample and the metering blocks.

3- Average sample temperature of 50 ºC during testing.

1.9 Scope of Study

In this work, the impact of key design and assembly parameters on thermal performance of plastic BGA packages will be identified by measuring and comparing thermal resistance of different BGA designs and assembly options. The study parameters were chosen to be die size, use of thermal balls, use of underfill, number of perimeter balls, and thermal via design (In this study the term thermal via is used to refer to both copper plated through holes and their associated copper spreader). Comparison of thermal resistance measurements will help to identify the optimum parameters set to minimize package temperature. Experimental measurements were conducted using a fully automated computerized test setup specifically designed to facilitate testing procedures, data collection and report generation.

As a second part of this investigation thermal FEA models were developed of the experimentally tested packages to identify major heat flow paths inside plastic BGA packages. In addition structural FEA models were formulated to predict crack initiation in the solder joints under thermal cycling loads. By comparing experimentally measured changes in thermal resistance due to thermal cycling with crack initiation data form FEA models, correlation between number of thermal cycles and degradation in thermal resistance can be established as well as quantifying the importance of solder balls as an effective heat flow path inside plastic BGA packages. In the final part of this study a new test setup based on ASTM 5470-95 [9] was developed that is capable of measuring the through the thickness thermal conductivity of thin components used in electronic

packaging. This data can be used to help guide design and assembly decisions that influence the overall thermal performance of electronic packages.

CHAPTER 2

LITERATURE REVIEW

2.1 Thermal Performance of BGA Packages

An examination of a BGA cross section reveals that many layers inside a BGA assembly share low values of thermal conductivity such as the molding compound, BT substrate, PCB and air layer between substrate and PCB. The challenge of designing high thermal performance BGA packages may be approached by establishing relatively highly conductive flow paths that allow heat to escape through the low thermal conductivity layers. Research in BGA thermal performance have indicated that high conductive paths can be in the form of thermal vias in the BT substrate, perimeter and thermal solder balls, or underfill and thermal vias in the PCB.

The benefit of using underfill material was reported by Edwards and Handt [10] who conducted a set of numerical simulations to investigate different design and assembly parameters on BGA thermal performance. Their study reported that up to a 50% decrease in junction to air thermal resistance was observed when underfill was used with a BGA with 176 perimeter balls. This investigation also cited that perimeter balls were effective in reducing thermal resistance only when the die size was large enough to overlap perimeter balls locations. The study noted superior thermal performance of BGA packages when compared to QFP packages.

An analysis of the different design parameters affecting thermal performance of BGA packages was performed by Zhan [11] who conducted a sensitivity analysis that used 86 finite element models. This study reported that die size and number of perimeter balls had a linear impact on junction to air thermal resistance, while there was a non-linear impact due to changing the number of PCB copper planes and heat sink thickness.

The importance of thermal balls was cited in a parametric study by Lall [12], who reported that using a matrix of 36 thermal balls decreased junction to air thermal resistance of a PBGA having 256 perimeter solder balls by 25% when compared to similar packages without thermal balls. However, this work also showed that in thermal cycling, the added coupling between the package and the board associated with the higher number of thermal balls caused a 33% drop in mean fatigue life when compared to packages without thermal balls as calculated using the modified Coffin-Manson law. The effective number of thermal balls that may have significant impact on thermal performance of PBGA packages was reported to be in the range of 24 to 48 thermal balls based on a 3 dimensional FEA parametric study conducted by Mertol [13].

Numerical simulation of PBGA packages can be expensive in terms of computational time, especially if small details like BT thermal via geometry are included. On the other hand, thermal via details must not be overlooked due to their significant impact on thermal resistance. In an effort to reduce computational time, Pinjala, et al. [14] introduced the possibility of using a simple geometry with anisotropic properties instead of the multilayer isotropic detailed geometry typically used in numerical simulations. The simple geometry model was reported to be 98% accurate when compared to the detailed geometry model. This study also reported that enhancement of

thermal conductivity of via fill material would have negligible impact on junction to air thermal resistance.

Further research on thermal vias was conducted by Ramakrishna and Lee [15], who studied the impact of thermal vias in BT substrates on thermal performance of flip chip BGA packages. This study reported that placing a sufficient number of thermal vias in the substrate within the area defined by the die foot print may help reduce package thermal resistance by 35 to 40%. This investigation also showed that the impact of the number of thermal vias on package performance diminished when the thermal conductivity under the die was greater than 2 W/(m·K).

The impact of PCB construction on PCB thermal conductivity was studied by Azar and Graebner [16], who conducted experimental measurements using infrared imaging to evaluate PCB orthotropic thermal conductivity as well as possible contact resistance at the interfaces between different layers inside the PCB. Their experimental results proved that no significant contact resistance was observed at the different interface surfaces inside the PCB. This study also introduced approximate mathematical models to calculate the effective in-plane and normal thermal conductivity of the PCB as a function of copper and glass-fiber layers thicknesses.

Research in thermal resistance of electronic packages has not been limited to experimental and numerical simulation techniques. Guenin, et al. [17] introduced a nonlinear lumped analytical parametric model for a cavity down thermally enhanced BGA to predict junction to air thermal resistance. This model accounted for natural, mixed, and forced convection, as well as radiation heat transfer. Their study reported that in a natural convection environment, radiation plays an important role in cooling a cavity

down thermally enhanced BGA, and was responsible for 42% of the total heat transfer from the package to environment.

Loh, et al. [18] introduced two analytical models that can be used to predict thermal resistance of a depopulated PBGA. The first proposed model used an equivalent area approach, while the second used an equivalent thermal conductivity approach to simplify package geometry to the extent that an analytical model could be derived. Their study used numerical simulation as a bench mark for analytical model accuracy. Analytical prediction of thermal resistance was reported to be within 10% of the values predicted by numerical simulation.

The literature also includes research work that investigates package deterioration due to exposure to thermal loads. Edwards, et al. [19] employed FEA models for PBGAs to investigate the impact of delamination on junction to air thermal resistance in a still air environment. This study reported that the highest increase of thermal resistance was due to delamination at the chip/die attachment interface. This study also reported that thermal resistance was least sensitive to delamination at the upper die surface, between the die and the molding compound.

Joiner and de Oca [20] conducted experimental measurements to identify the impact of aging on thermal performance of thermal grease used with heat sinks. Five different thermal grease materials were tested for 1900 hours at 150 ºC. Their study reported that non-cleanable silicon based and alcohol-cleanable non silicon based thermal greases were the materials that did not exhibit filler separation at the end of aging test.

2.2 Numerical Simulation of BGA Reliability

Reliability of BGA packages is a major concern for the electronic packaging industry, which has driven research efforts to develop effective methods that are capable of predicting failure initiation and propagation under cycling loads. Typically, the reliability problem has been approached using a combination of experimental measurements and numerical simulation.

Experimental measurements are conducted by thermally cycling BGA packages and visually inspecting sliced packages for crack initiation and speed of propagation in solder joints at successive intervals of thermal cycling. Numerical simulation models are also normally created for the packages used in the experimental measurements, and loaded with thermal loads similar to those applied experimentally. Finally, failure prediction models are developed by correlating experimental measurements with numerical simulation.

The bulk of recent BGA reliability studies have used the Anand model [21] to simulate creep behavior of solder joints. With this approach, the amount of plastic strain energy density in critical solder joints is calculated using a volume averaging technique to reduce dependency of solution accuracy on mesh density as suggested by Darveaux [22]. The strain energy density calculated values are then plugged in the correlation equations to calculate fatigue life.

Two different sets of correlation coefficients have been reported: the first by Darveaux [23] for CBGA packages and solder mask defined pads, and the second set by Lall, et al. [24] for PBGA packages and non solder mask defined pads.

Syed [25] preformed similar studies based on the proposed constitutive models for creep developed by Wong, et al. [26]. He also introduced another set of damage correlation coefficients based on the Monkmann-Grant equation for creep rupture. Numerical simulation prediction of fatigue life based on the mentioned correlation was reported to be within 25% of experimental measurements.

Other studies have followed the same approach including the work done by Zhang et al. [27], Zhan [28], and Yan, et al. [29]. These investigations involved both slice models, and one quarter or one eighth symmetry coarse global models with finer submodels in an effort to reduce model processing time.

In a study by Gustafsson [30], a survey of five modeling approaches was conducted and numerical results were compared to experimental measurements. The five modeling approaches were nonlinear slice model, nonlinear global model with linear super elements, linear global model with nonlinear submodel, nonlinear global model with nonlinear submodel, and nonlinear global model. This study reported that the nonlinear slice model was the most conservative approach. The nonlinear global model with linear super elements was not recommended to be used due to large errors reported. The most accurate approach reported was the global nonlinear model with non linear sub model.

2.3 Thermal Resistance Measurements of Thin Components

ASTM D-5470 [9] guidelines have been implemented in many studies to evaluate thermal resistance of thin interface materials. However, the ASTM Standards give only schematic representation of apparatus construction and theory of operations. Thus, there

have been significant differences in the results obtained in different studies due to the differences in construction details such as type of temperature sensors, size of temperature sensors, heater powers and the temperature sensor pitch.

The ASTM Standard also does not specify a recommended value for the metering block surface roughness, despite of its impact on contact resistance between the sample and metering blocks which in turn influences measurements accuracy. The impact of contact surface conditions on contact conductance was reported by Yovanovich, et al. [31]. Other factors that affect measurement accuracy were reported in the study introduced by Gwinn, et al. [32] such as temperature sensors location uncertainty, distortion of temperature gradient by temperature sensors, uniformity of heat flux at temperature sensors, and heat losses. The device developed by Gwinn, et al. [32] was used to measure 3 different interface materials in free air environment. This study reported significant change in bare contact resistance (60% drop) between the metering blocks after conducting tests for thermal interface materials. The change of contact resistance was reported to be an indication of residue interface material on the metering block surfaces even though the metering blocks were frequently cleaned with acetone and dish detergent.

Solbrekken, et al. [33] also developed a similar apparatus following the ASTM D-5470 guidelines and used K-type thermocouples as temperature sensors and 50 Watt Kapton film heaters. This study recommended using a more accurate temperature sensor and more powerful heaters. Another apparatus following ASTM D-5470 standards was developed by Cullham, et al. [34], who used Platinum RTDs as temperature sensors and

cartridge heaters. Their apparatus also addressed the problem of in-situ measurement of sample thickness using laser detectors.

CHAPTER 3

EXPERIMENTAL MEASUREMENT OF PARAMETERS IMPACTING THERMAL PERFORMANCE IN BALL GRID ARRAY PACKAGES

3.1 Study Parameters

Underfill materials are gaining wide acceptance in harsh environment electronic packaging applications due to their ability to enhance solder joint reliability. Underfill materials should have a positive impact on thermal performance as well since they offer a less resistive conductive path between the package and the PCB when compared to air.

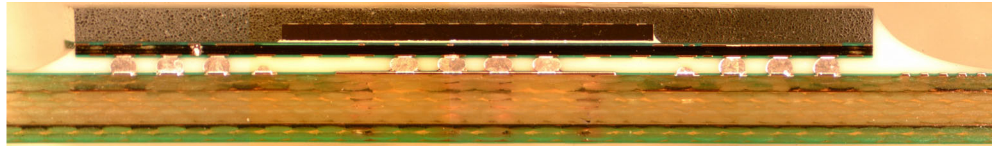
In this work, one of the study parameters chosen was the impact of using underfill material on thermal performance of plastic ball grid array packages. In order to allow a clear comparison between using and not using underfill, some test samples were underfilled while identical package/board combinations were assembled without underfill. Since underfill materials provided by different vendors have varying chemical compositions that could impact thermal performance, three different commercially available underfill materials were examined.

The importance of thermal balls as efficient heat paths between the package and the PCB was also investigated in this work. Thermal balls were removed from some of the test samples to quantify the impact of the thermal balls on thermal performance.

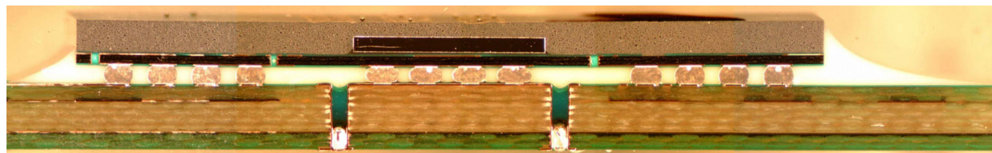
Cross sections of packages with and without thermal balls are shown in Figure 3.1 and Figure 3.2, respectively. Current trends in electronic packaging include increasing power levels and decreasing die size, both of which have direct impact on thermal performance. To quantify the impact of these trends, two different BGA packages with similar major dimensions and different die sizes were tested.

For BGA packages with no thermal balls and no underfill, the only paths available for heat flow from the package to the PCB are the air gap between the BT and the PCB, and the perimeter solder balls. The efficiency of perimeter balls to conduct heat from the package to the PCB should be dependent on the proximity of the perimeter balls to the die, the number of perimeter balls, and the cross sectional area of each ball. To quantify the effect of number of perimeter balls on thermal performance, thermal performance measurements were conducted for two different packages with different number of perimeter balls. To quantify the impact of PCB thermal via geometry, two different thermal via designs were included in the test boards.

Internal connections in electronic packages are expected to deteriorate and/or fracture under thermal cycling with the effect of severing efficient heat flow paths inside the package. However, thermal resistance is usually and incorrectly treated as a static parameter. To quantify the impact of thermal cycling on thermal performance, samples in this work were thermally cycled between -40º C and 125º C in a 90 minute cycle. After initial measurements were preformed on initial samples, thermal resistance measurements were then repeated for all packages after every 250 cycles of exposure.

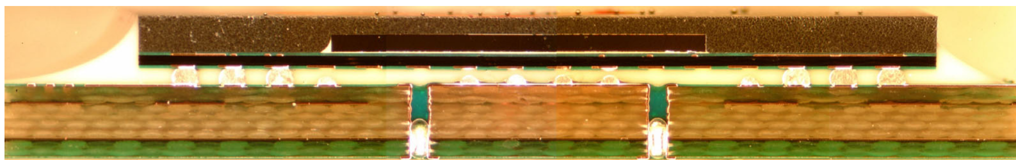


BGA #1

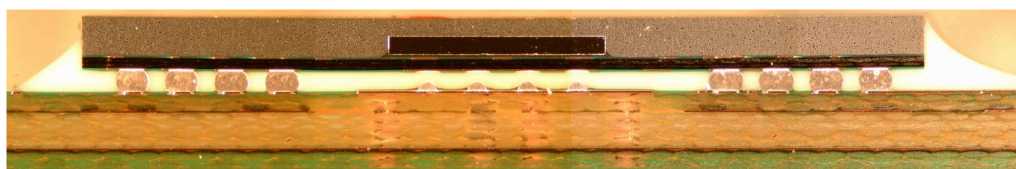


BGA #2

Figure 3.1 - Cross sections of BGA packages with thermal balls



BGA #1



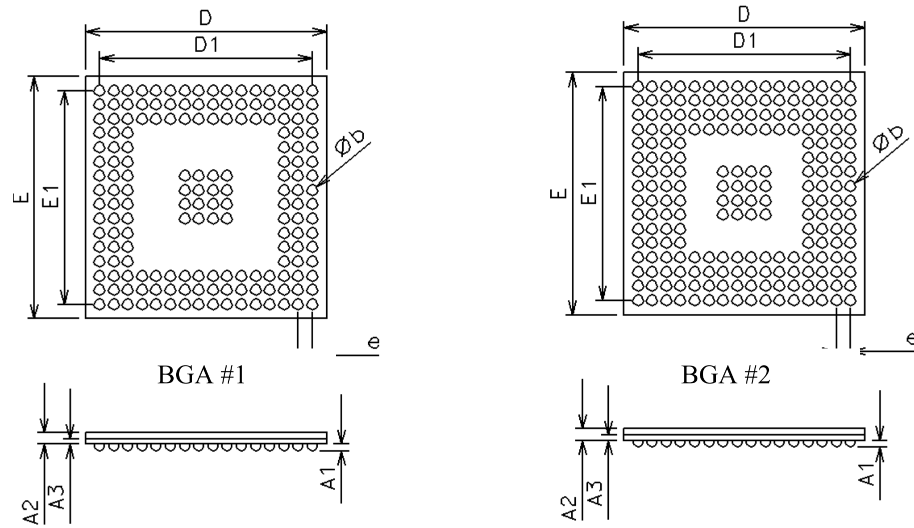
BGA #2

Figure 3.2 - Cross sections of BGA packages without thermal balls

3.2 Test Packages and Test Board

Two different 17 mm plastic BGA packages were tested. The first PBGA featured an 8.2 x 8.2 mm square die, and the second PBGA had a 7 x 4.4 mm rectangular die. Schematic representations of both packages layout and major dimensions are shown in Figure 3.3. The thermal test chip in the first BGA was equipped with 4 quadrant heaters and 4 P-N diodes to be used as temperature sensing devices. However, only 3 diodes were operational due to wire bond limitations. The thermal test chip in the second package contained one heater and one P-N diode. Both packages had 16 thermal balls. BGA #1 had 144 perimeter balls arranged in 3 rows, while BGA #2 had 192 perimeter balls arranged in 4 rows. Both packages had a ball pitch of 1 mm. Schematic representations of the die layouts for both packages are shown in Figure 3.4.

Up to four different packages could be mounted on one test board (2 packages of type 1 and 2 packages of type 2). The four mounting locations on the test board were arranged in a 2 by 2 square matrix. The upper two package mounting locations were equipped with thermal via type one, which consisted of a heat spreader with a set of intersecting copper traces extending to 12 plated through holes. For the lower two package mounting locations, a second via design (thermal via type 2) was used, which consisted of a solid square copper heat spreader extending to a similar set of 12 plated through holes. Both via designs were connected to a copper ground plane buried inside the PCB through analogous sets of plated through holes, and differed from each other by their top level heat spreader layouts. A fully populated test board and thermal via details are shown in Figure 3.5. A schematic of the thermal via connections to the copper ground plane inside the PCB is shown in Figure 3.6



	BGA #1	BGA #2
D [mm]	17	17
D1 [mm]	15	15
E [mm]	17	17
E1 [mm]	15	15
b [mm]	0.5	0.6
e [mm]	1	1
A1 [mm]	0.45	0.5
A2 [mm]	0.8	1.15
A3 [mm]	0.36	0.36
Number of perimeter balls	156	192
Number of thermal balls	16	16
Number of Heaters	4	1
Heater resistance [Ohm]	5.5	10.7
No of diodes	3	1
Die Size [mm]	8.2 x 8.2	7 x 4.4

Figure 3.3 - Schematic representation of BGA dimensional parameters

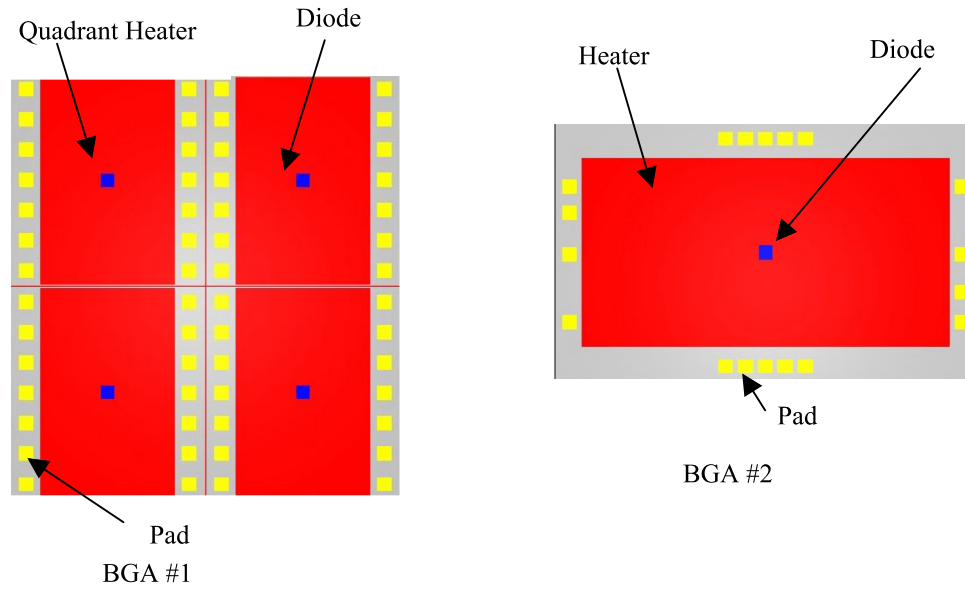


Figure 3.4 - Schematic representation of thermal test chips

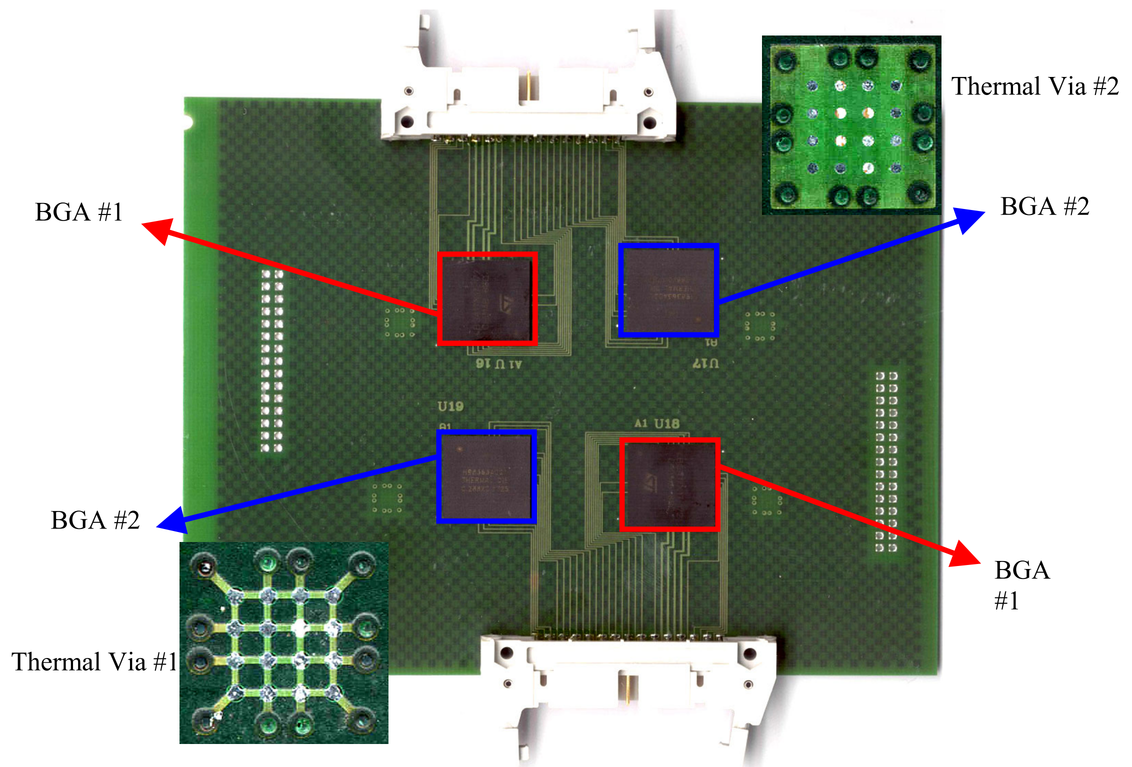


Figure 3.5 - Test board

3.3 Test Matrix

The test matrix consisted of 48 PBGA packages of type one and 48 PBGA packages of type two, mounted on 32 test boards. The BGAs were mounted on the test boards and underfilled with 3 different underfill materials so that any given leg of the test matrix was represented by four samples. The complete test matrix is listed in Table 3.1.

3.4 Testing Thermal Aspects

The heaters on the thermal test chips were activated by means of a DC power supply. This method was appropriate for direct calculation of the input power by measuring the supply output current and the applied voltage. A 1.5” (3.81 cm) thick glass fiber insulation layer covered the top BGA surface, while a stream of water at known constant temperature was impinged on back of the PCB board. The flowing water temperature was monitored using four immersed K-type thermocouples touching the back of the board at the centers of the packages, while the on chip diodes were used to sense the die surface temperatures. A cross-sectional schematic of the test apparatus is shown in Figure 3.7.

Using this approach, the heat flowed only from the die surface to the back of the board in a path that can be approximated as one-dimensional. The package thermal resistance can be calculated knowing the heating power, the die surface temperature, and the flowing water temperature according to:

$$\theta_{jc} = \frac{T_j - T_c}{P} \qquad \text{(Eq. 3.1)}$$

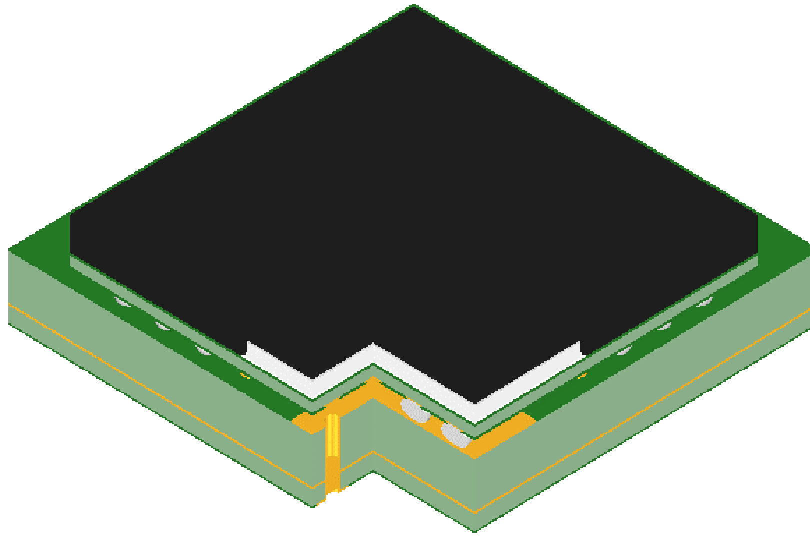


Figure 3.6 - Thermal via connection with ground plane

Table 3.1 - Test matrix

	Packages with Thermal Balls			
	No Underfill	Underfill #1	Underfill #2	Underfill #3
BGA#1/Via#1	4	4	4	4
BGA#2/Via#1	4	4	4	4
BGA#1/Via#2	4	4	4	4
BGA#2/Via#2	4	4	4	4

	Packages without Thermal Balls			
	No Underfill	Underfill #1	Underfill #2	Underfill #3
BGA#1/Via#1	0	0	0	0
BGA#2/Via#1	0	0	0	0
BGA#1/Via#2	4	4	4	4
BGA#2/Via#2	4	4	4	4

where:

θ_{jc} = Junction to case thermal resistance [K/W]

T_j = Junction temperature [K]

T_C = Case temperature [K]

P = Input Power [W]

3.5 Testing Electronic Aspects

Using diodes for characterization of the die surface temperature offered the advantage of good linear behavior as well as being non-intrusive. However, due to inherent semiconductor device manufacturing variability, each diode needed to be in individually calibrated in order to ensure the measurement accuracy. The diode current-voltage relation is given by:

$$I_d = I_s\left[e^{\frac{qV_d}{nkT}} - 1\right] \qquad \text{(Eq. 3.2)}$$

where:

I_d = Diode current [A]

I_s = Saturation current [A]

q = Electron charge (1.6 x 10^{-19} C)

V_d = Diode forward voltage [V]

n = Non-ideality factor $\approx$ 1

k = Boltzman constant (1.36 x 10^{-23} J/K)

T = Temperature [K]

This expression can be reformatted as:

$$T = \frac{q}{nk\ln\left(\frac{I_d}{I_s}\right)} V_d \qquad \text{(Eq. 3.3)}$$

The term $\frac{q}{nk\ln\left(\frac{I_d}{I_s}\right)}$ is known as the diode temperature coefficient and ranges from -1.8 to -2.0 mV/K, and is a unique value for every diode.

An important experimental detail was the selection of the diode excitation current. This current can be chosen from a few μA to $1\ mA$ depending on the device size. Low excitation currents can lead to erroneous temperature readings due to relatively high leakage currents. On the other hand, high excitation currents may cause localized heating of the device, again causing erroneous temperature readings. The correct selection of the excitation current was achieved by measuring the diode current versus voltage, plotting it on a semi log scale, and selecting the current region which exhibits the best linear relation.

3.6 Testing Fixture and Cooling Circuit

The test fixture was first designed as CAD solid model including the test board, water fittings, and gasket; and then it was manufactured from commercial grade aluminum alloy. Cooling water at the back of board was maintained at a constant temperature using a water chiller. The water inlet hoses were equipped with ball valves. The ball valves were used to shock the system a few times at the beginning of each test to purge any trapped air pockets from the system to avoid localized hot spots under the

BGA packages. A solid model and a photographic image of the test fixture are shown in Figure 3.8.

3.7 Data Acquisition and Control

The huge number of temperature measurements required (about 1600 temperature measurements per board) and the need for repetitive measurements after every 250 thermal cycles necessitated the development of a fully automated data acquisition and control system. An image of the test setup is shown in Figure 3.9.

The data acquisition and control system consisted of:

1. Personal computer.
2. Current source for diode excitation.
3. DC power supply to power the heaters.
4. Switch with 12 channels to select tested package as well as to route the diode excitation current to diodes and power to the heaters.
5. GPIB card to interconnect all previous components.
6. Data acquisition card for collecting thermocouple readouts and diode voltage.

A special program was written in Visual Basic and Labview to set test parameters, read calibration data for each board, control the test sequence, acquire data and archive the results. The user interface of the data acquisition and control software is shown in Figure 3.10. A schematic of the data acquisition and control system is shown in Figure 3.11.

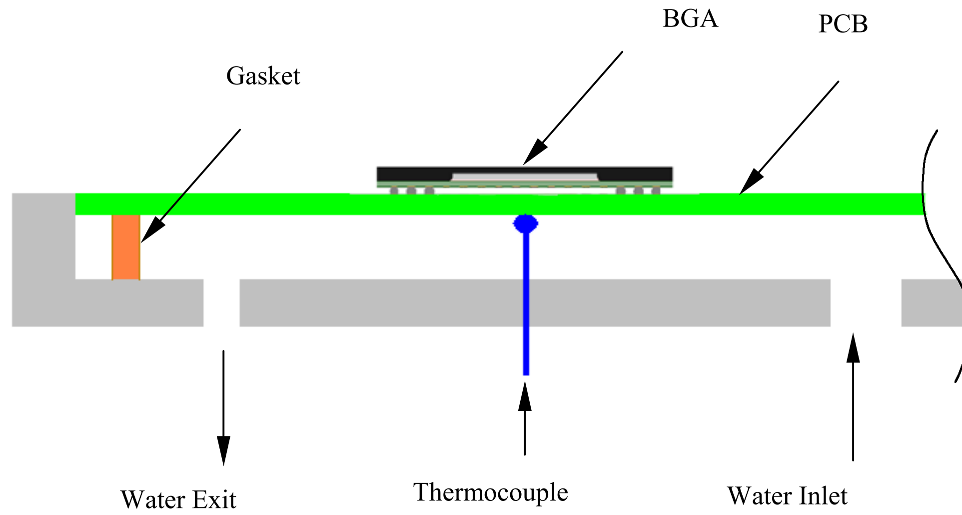


Figure 3.7 - Cross–sectional schematic of the test fixture

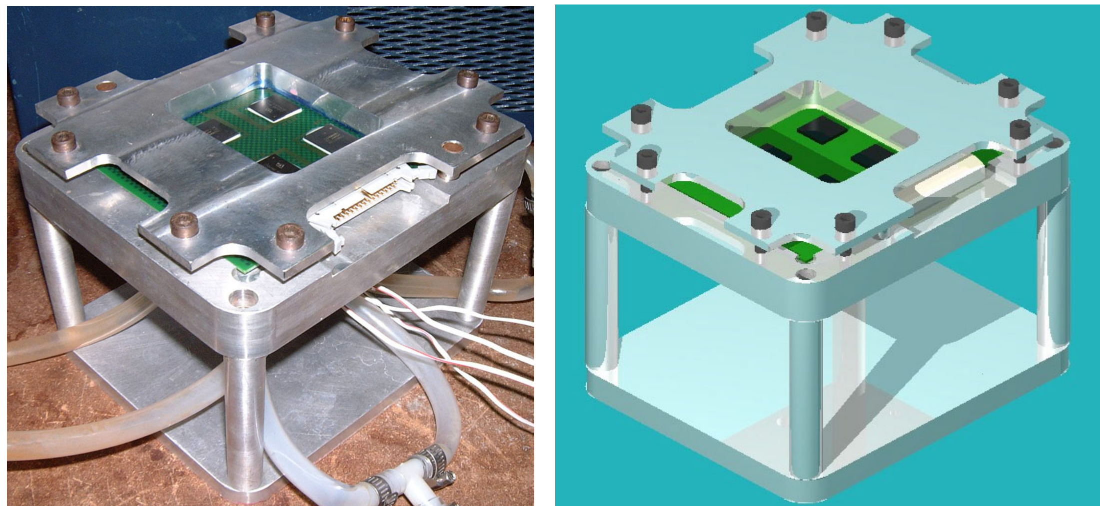


Figure 3.8 - Test fixture

3.8 Diode Characterization and Calibration

During initial testing, the diode current versus voltage was plotted on a semi log scale ranging from 0 to 1 mA of excitation current. The best linear behavior was observed in the region of 450-550 μA, with a mean squared error of 0.7 μA. Hence, the diode excitation current was selected to be 500 μA for the remainder of the experiments. The diode calibration process was performed by placing the test boards in an oven and recording each diode voltage at different temperatures while they were being excited with 500 μA. The average diode temperature coefficient was found to be about –1.75 mV/K. A sample of the calibration output from one of the test boards is shown in Figure 3.12. A sample diode calibration report is given in Appendix A.

Observation of diode characteristics after thermal cycling indicated a slight variation in diode temperature coefficients, which can be attributed to permanent deformations in the BGA packages. To ensure the accuracy of the diode temperature measurements, the calibration procedure was repeated for each diode after every 250 thermal cycles. The data acquisition and control program was designed to automatically calculate the temperature coefficient of each diode and generate a report that was read by the testing program at the beginning of each test.

3.9 Testing Procedure

For each package, the input power during thermal performance testing was gradually increased from 0.1 W to 1 W, with a step of 0.1 W. At each power step, the average die surface and cooling water temperatures were monitored. Steady state heat

Figure 3.9 - Test setup

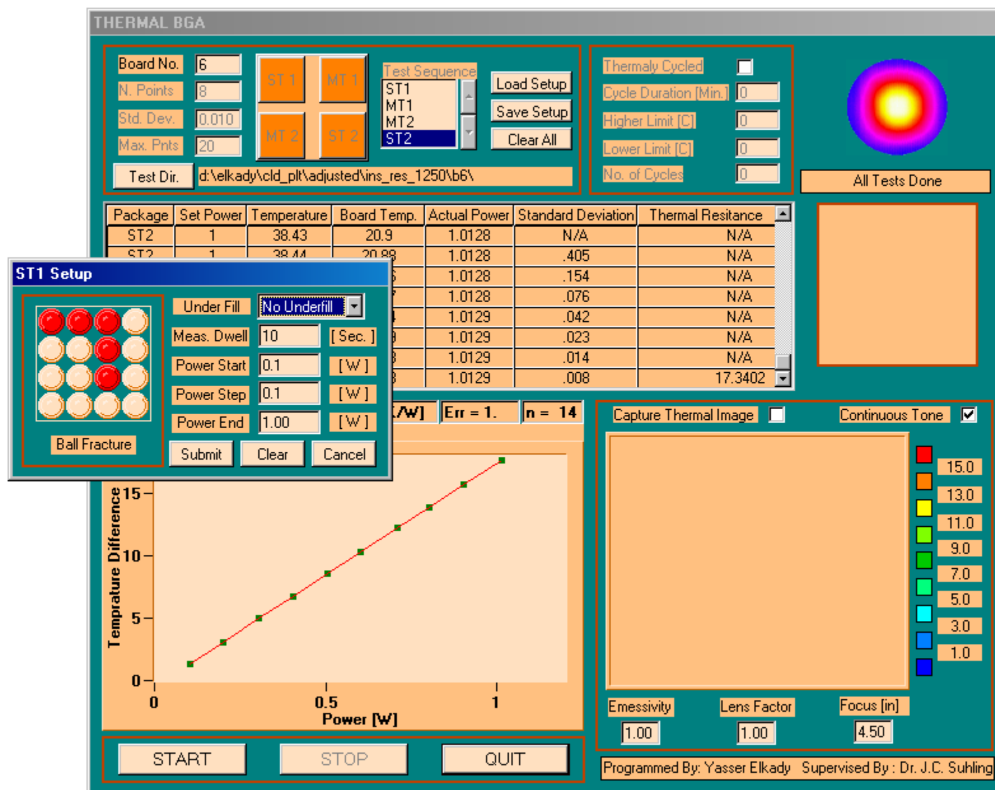
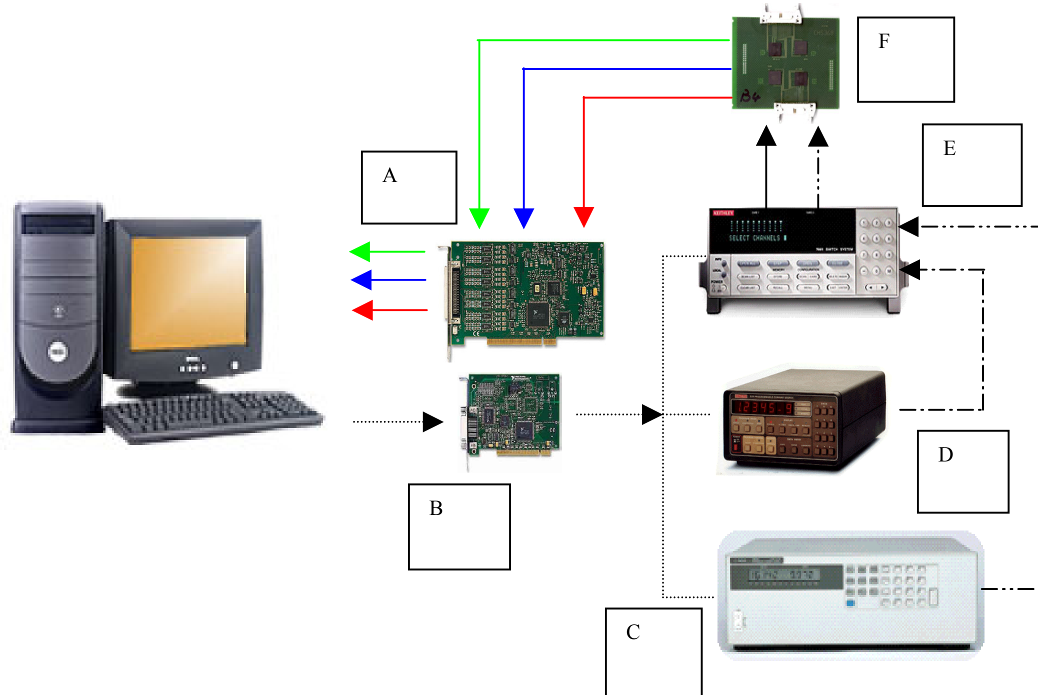


Figure 3.10 - Data acquisition and control software



A	Data Acquisition Board
B	GPIB Card
C	Power Supply
D	Current Source
E	Switch Box
F	Test Board
·······▶	GPIB Instructions
—··▶	Power to Heaters
—·▶	Diode Excitation
—▶	Thermocouple Readout
—▶	Diode Voltage Readout
—▶	Heater Resistance Readout

Figure 3.11 - Data acquisition and control system

transfer was assumed to be present when the standard deviations of 8 successive temperature measurements fell below 0.05 °C. This criterion was determined based on preliminary observations of the system behavior. The temperature difference between the die surface and the cooling water was plotted against the heater power at steady state. A sample of a measured temperature difference versus input power data plot is shown in Figure 3.13. Thermal resistance, which is the slope of the observed linear variation, was then evaluated using a linear regression fit. A sample thermal resistance report generated by the data acquisition software is given in Appendix B.

The system also incorporated an infrared thermal camera set to capture thermal images of the tested package at equal intervals. The sequence of still images was then compiled into a digital video format showing an animation of the steady state increments from test start to end. Sample infrared thermal images from one of the test boards are shown in Figure 3.14.

3.10 Experimental Results

To evaluate the impact of the various study parameters on thermal performance, the average test data from similar packages were calculated and then compared. All of the thermal resistance measurements for packages with thermal balls and without thermal balls are shown in Figures 3.15 and 3.16, respectively. A complete list of all recorded thermal resistance test data is given in Appendix C.

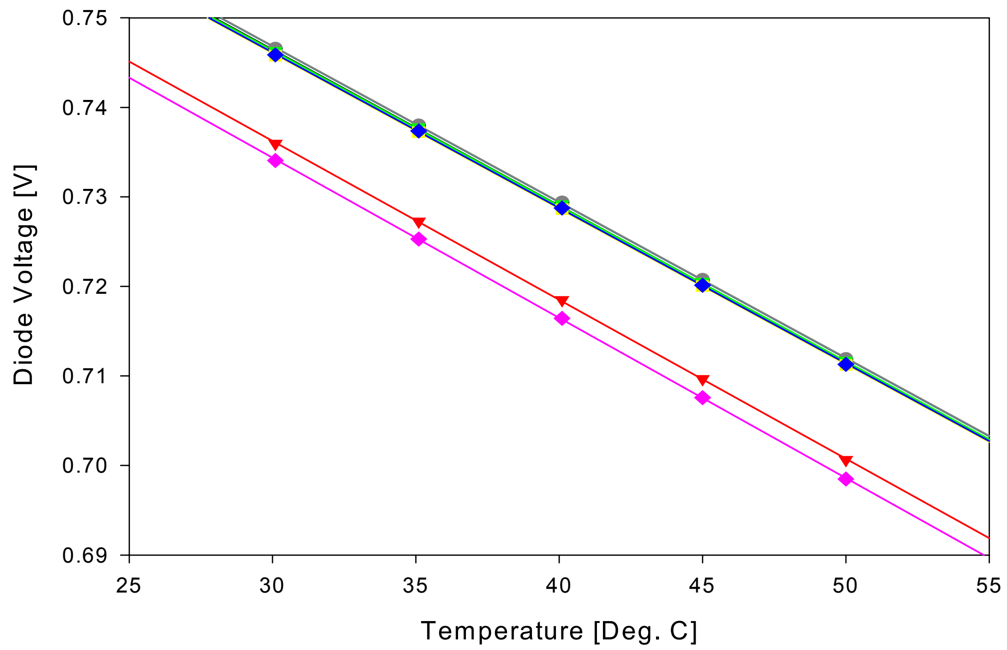


Figure 3.12 - Diode calibration data

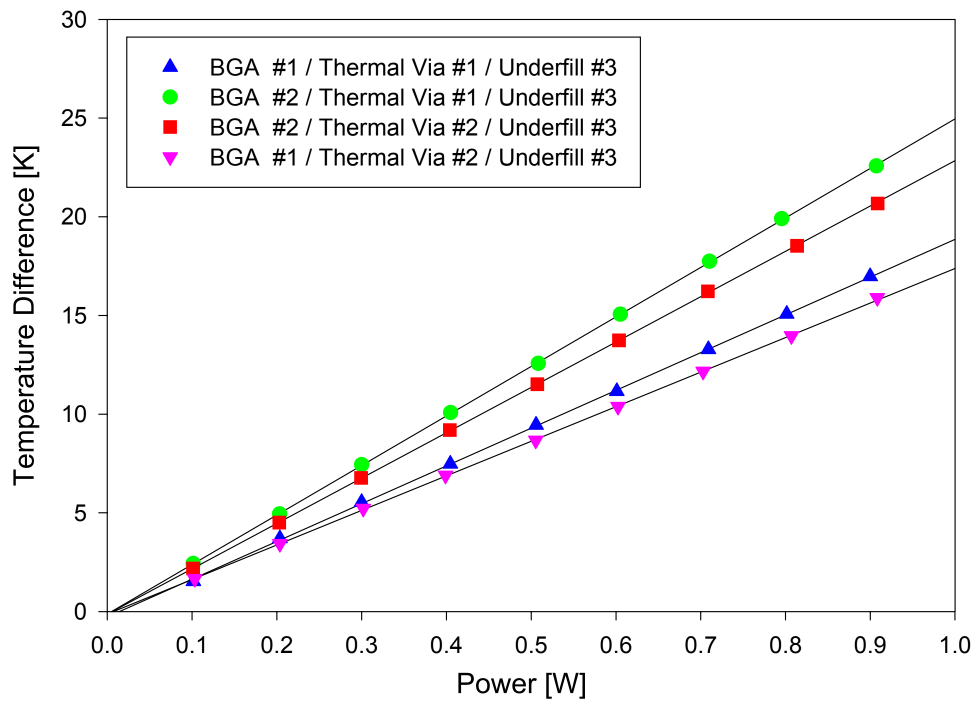
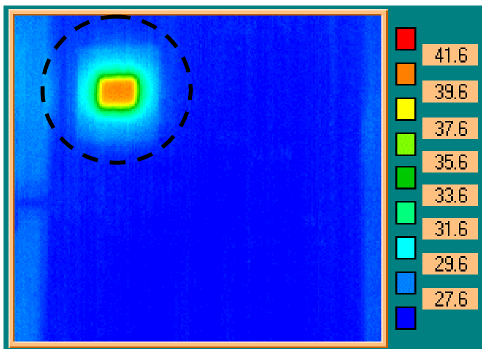
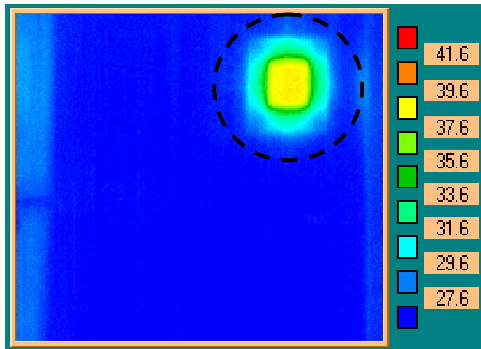


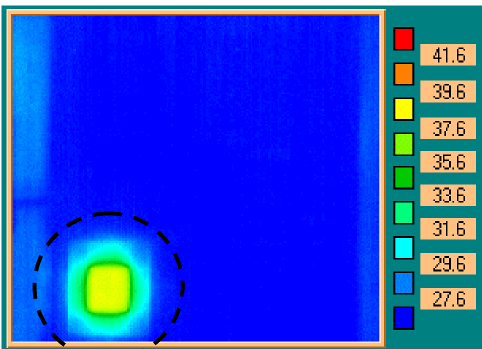
Figure 3.13 - Sample of temperature measurements

BGA #2 / Via #2

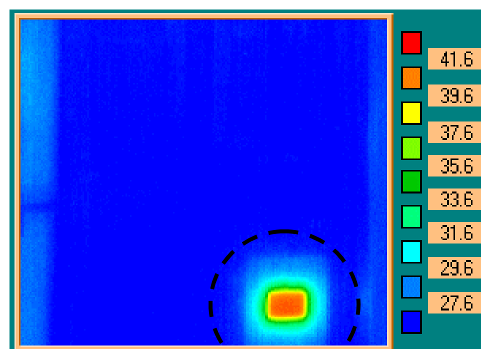


BGA #1 / Via #1





BGA #1 / Via #2



BGA #2 / Via #1

Figure 3.14 0 - Sample IR thermal images of test packages at steady state

3.10.1 Use of Underfill

Underfilled packages consistently showed less thermal resistance than those with no underfill. All three underfill materials performed equally. For example, the thermal resistances of underfilled BGA #1 packages with thermal balls which were mounted on thermal via #1 were found to be 18.64 K/W, 18.74 K/W, and 18.7 K/W, when underfilled with underfill #1, underfill #2, and underfill #3, respectively.

3.10.1.1 Packages with Thermal Balls

The thermal resistance of BGA #1 mounted on thermal via #1 was reduced from 23.9 K/W to 18.7 K/W (22% reduction) by using underfill. Similarly, BGA #1 packages mounted on via #2 exhibited a reduction in thermal resistance from 22.7 K/W to 17.9 K/W (21% reduction) by using underfill. For BGA #2 mounted on via #1, use of underfill reduced the thermal resistance from 27.9 K/W to 25.5 K/W (9% reduction), while for BGA #2 packages mounted on via #2, the thermal resistance was reduced from 25.7 K/W to 23.7 K/W (8% reduction).

3.10.1.2 Packages without Thermal Balls

The thermal resistance of BGA #1 mounted on thermal via #2 was reduced from 36.3 K/W to 20.1 K/W (45% reduction) by using underfill. For BGA #2 mounted on via #2, use of underfill reduced the thermal resistance from 47.6 K/W to 30 K/W (37%

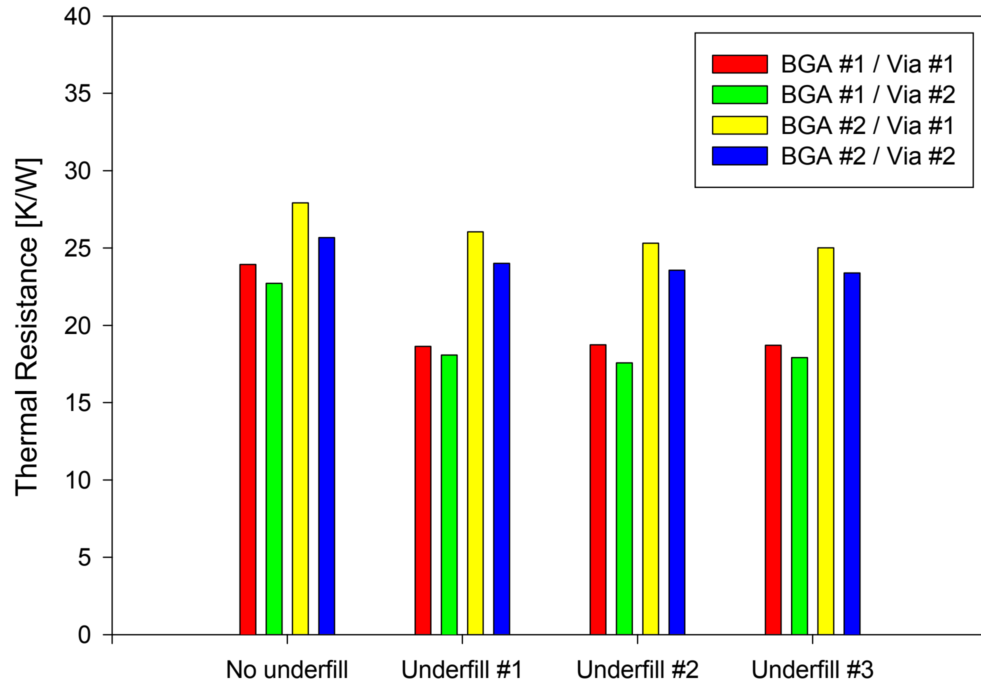


Figure 3.15 - Thermal resistance measurements
(packages with thermal balls)

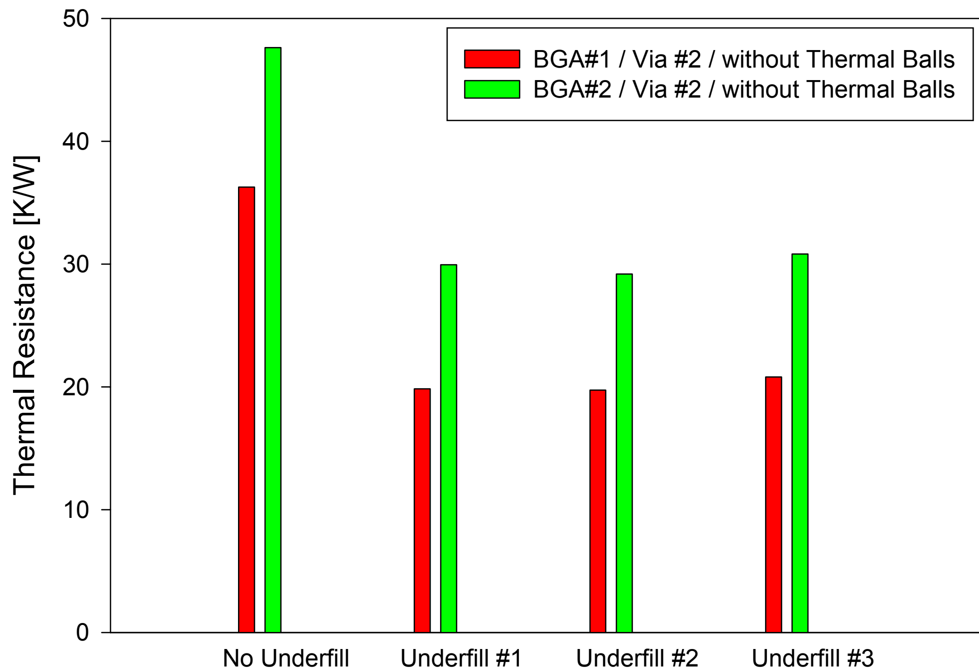


Figure 3.16 - Thermal resistance measurements
(packages without thermal balls)

reduction). These observations indicated that underfill material can be considered an heat conduit (even with its low thermal conductivity of about 0.35 W/(m·K)), because of its large cross sectional area. For example, the underfill cross sectional area was 289 mm^2, while the sum of all of the perimeter and thermal solder ball cross section areas was only 17.8 mm^2.

3.10.2 Use of Thermal Balls

Investigation of the impact of thermal ball removal was conducted only for the more effective thermal via #2. For BGA #1, removal of the thermal balls increased the thermal resistance from 22.7 K/W to 36.3 K/W (60% increase) for packages without underfill, and from 17.9 K/W to 20.1 K/W (12% increase) for packages with underfill. For BGA #2, removal of the thermal balls increased the thermal resistance from 25.7 K/W to 47.6 K/W (85% increase) for packages without underfill, and from 23.7 K/W to 30.0 K/W (27% increase) for packages with underfill.

3.10.3 Die Size

The thermal resistances for BGA #1 were found to be consistently lower than the analogous configurations for BGA #2 for all test parameter combinations. These differences in thermal performance can be attributed to the large die surface area of BGA (67.24 mm^2), which was more than double the die surface area of BGA #2 (30.8 mm^2).

3.10.3.1 Packages with Thermal Balls

The thermal resistance of BGA #1 without underfill when mounted on thermal via #1 was 23.9 K/W. For similar BGA #2 packages, the value was 27.9 K/W (17% increase). For packages mounted on thermal via #2 and without underfill, the thermal resistances were 22.7 K/W for BGA #1 and 25.7 K/W for BGA #2 (13% increase).

The thermal resistance of BGA #1 with underfill when mounted on thermal via #1 was 18.7 K/W. For similar BGA #2 packages, the value was 25.5 K/W (37% increase). For packages mounted on thermal via #2 and with underfill, the thermal resistances were 17.9 K/W for BGA #1 and 23.7 K/W for BGA #2 (32% increase).

3.10.3.2 Packages without Thermal Balls

The thermal resistance of BGA #1 without underfill when mounted on thermal via #2 was 36.3 K/W. For similar BGA #2 packages, the value was 47.6 K/W (31% increase). For packages mounted on thermal via #2 and with underfill, the thermal resistances were 20.1 K/W for BGA #1 and 30.0 K/W for BGA #2 (50% increase).

3.10.4 Number of perimeter balls

BGA #2 had 48 more perimeter balls than BGA #1. The extra balls increased the area of heat transfer among perimeter balls by 33%. However, BGA #2 consistently showed a higher thermal resistance than BGA #1 in all measured configurations. This was an indication that little heat flows through perimeter balls, a fact mainly due to their relatively large distance from the die surface where heat was generated.

3.10.5 Thermal Via Geometry

For packages with thermal balls, BGA #2 packages with no underfill mounted on thermal via #1 showed a 9% higher thermal resistance than similar packages mounted on thermal via #2 (27.9 K/W and 25.7 K/W, respectively). Similarly BGA #2 packages with underfill when mounted on via #1 showed a 8% higher thermal resistance than similar packages mounted on thermal via #2 (25.5 K/W and 23.7 K/W, respectively).

For packages with thermal balls, BGA #1 packages with no underfill mounted on thermal via #1 showed a 5% higher thermal resistance than similar packages mounted on thermal via #2 (23.9 K/W and 22.7 K/W, respectively). Similarly BGA #1 packages with underfill when mounted on via #1 showed a 4% higher thermal resistance than similar packages mounted on thermal via #2 (18.7 K/W and 17.9 K/W, respectively).

The data clearly indicated that all packages mounted on thermal via #2 performed better than their counterparts that were mounted on thermal via #1. Since both via configurations featured exactly the same plated through hole connections to the ground planes inside the PCB, the difference in thermal performance can be directly attributed to the geometries of the copper heat spreaders used under the thermal balls. For thermal via #1 (cross-hatched copper heat spreader), the copper area was only 1.6 mm^2. For thermal via #2 (solid copper heat spreader), the copper area was 17.6 mm^2 (over 10 times higher)

3.10.6 Thermal Cycling

After initial measurements, the test boards were subjected to thermal cycling from -40 to 125 ºC. By repeating the thermal resistance measurements every 250 cycles, the increases in thermal resistance associated with material degradation and/or fracture could be evaluated. The temperature profile of the 90 minute thermal cycle is shown in Figure 3.17.

Details of the number of thermal cycles completed for all packages are shown in Table 3.2. The measured variations in thermal resistance are plotted versus the number of thermal cycles in Figures 3.18 and 3.19 for BGA #1 and BGA #2, respectively. The first 500 thermal cycles revealed no noticeable change in thermal performance for all BGA Packages. Major changes initiated at 750 cycles for BGA #1 for the case of no underfill and thermal balls. An accelerated increase in the thermal resistance then occurred until 1250 thermal cycles. The thermal resistance increased from 23.9 K/W at 0 cycles to 30.5 K/W at 1250 cycles (28% increase) for BGA #1/Via #1. Similarly, for BGA #1/Via #2, the thermal resistance increased from 22.7 K/W at 0 cycles to 26.4 K/W at 1250 cycles (16% increase). After 1250 cycles, the connection to most diodes and heaters were lost due to perimeter ball solder joint failures. These early failures were not unexpected due to the lack of underfill as well as the large die size in BGA #1. After 750 cycles, BGA #1 with no underfill and no thermal balls showed a continuous increase of thermal resistance from 36.3 K/W at 0 cycles to 43.1 K/W at 1500 cycles (19% increase).

BGA #2 with no underfill illustrated small increase in thermal resistance after 2000 cycles. This trend is expected to continue until failure at a higher number of thermal

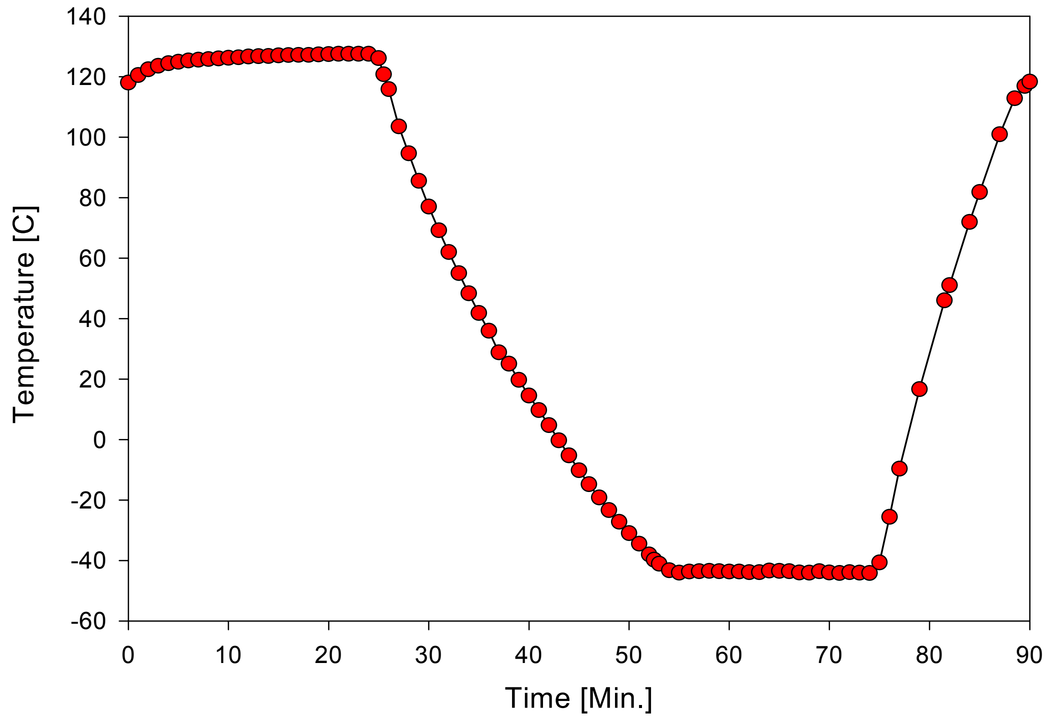
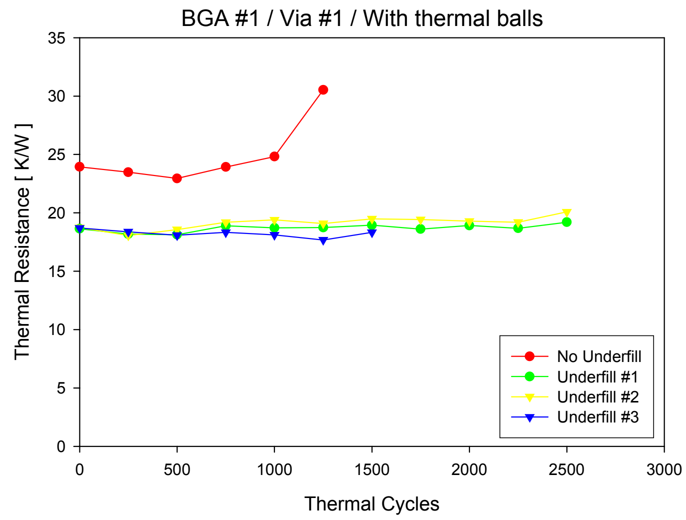


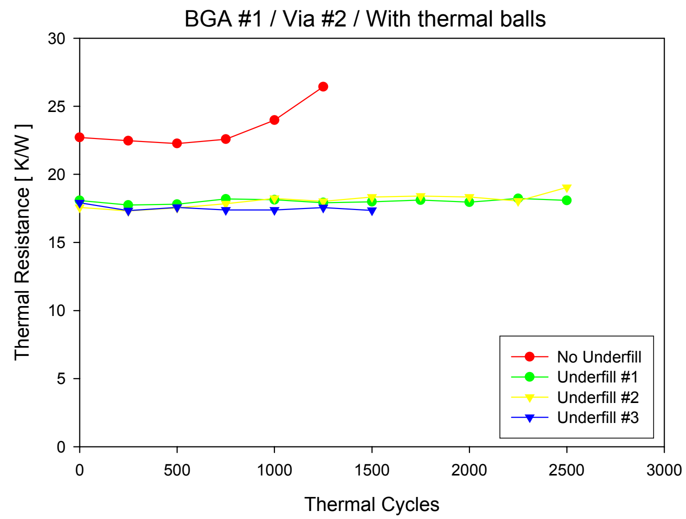
Figure 3.17 - Thermal cycling profile

Table 3.2 - Number of completed thermal cycles

	Packages with Thermal Balls			
	No Underfill	Underfill #1	Underfill #2	Underfill #3
BGA#1/Via#1	2500	2500	2500	1500
BGA#2/Via#1	2500	2500	2500	1500
BGA#1/Via#2	2500	2500	2500	1500
BGA#2/Via#2	2500	2500	2500	1500

	Packages without Thermal Balls			
	No Underfill	Underfill #1	Underfill #2	Underfill #3
BGA#1/Via#2	1500	1500	1500	1500
BGA#2/Via#2	1500	1500	1500	1500





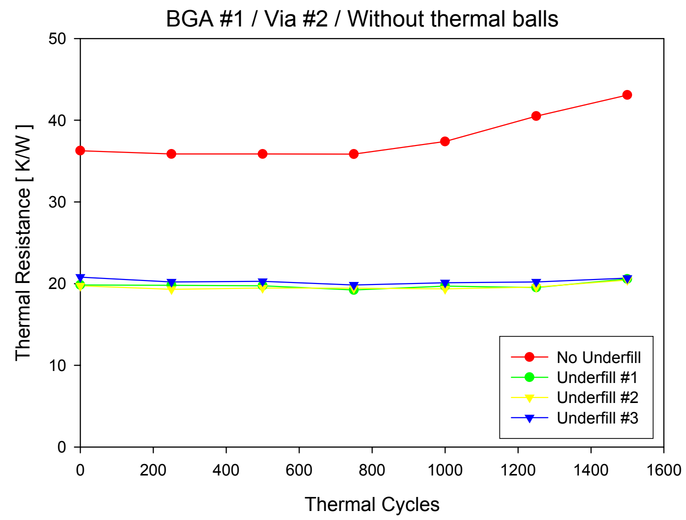
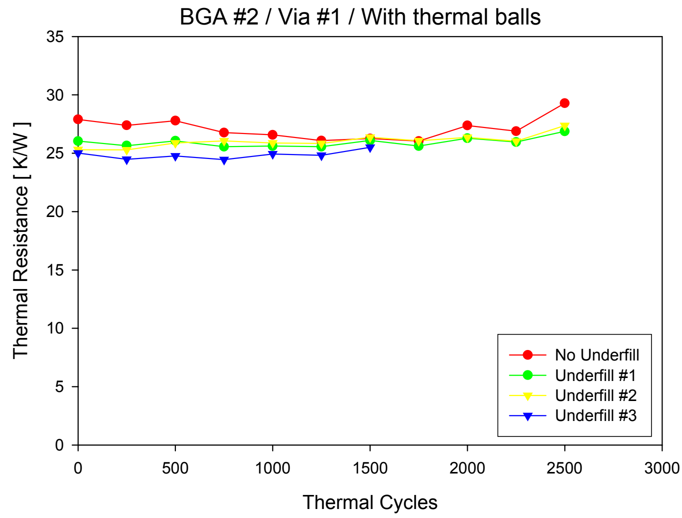
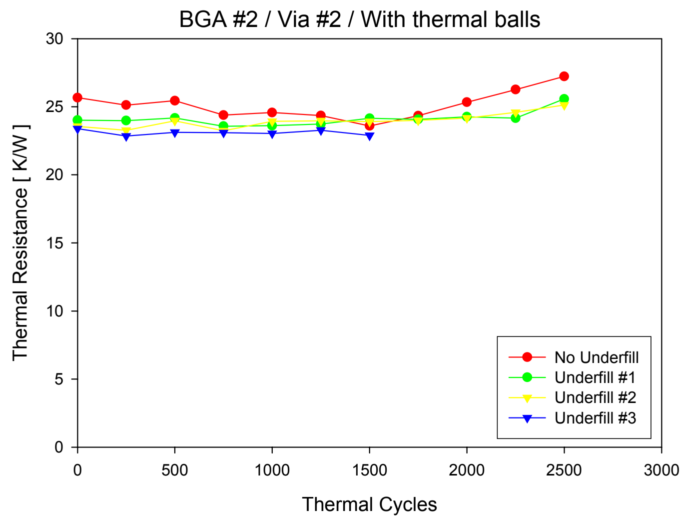


Figure 3.18 - Impact of thermal cycling (BGA #1)





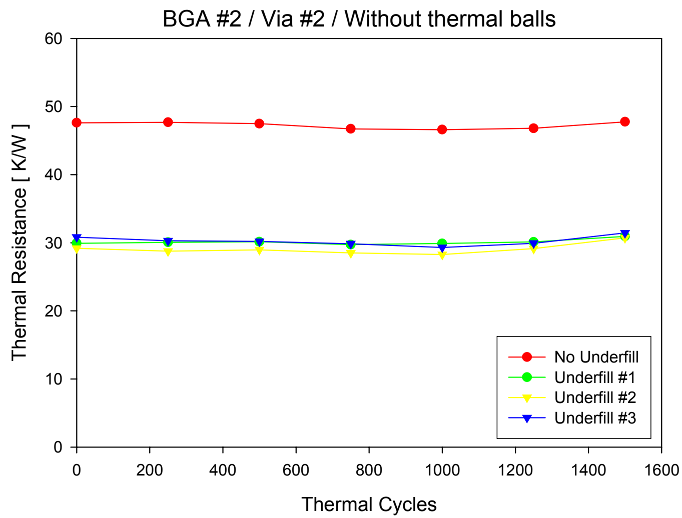


Figure 3.19 - Impact of thermal cycling (BGA #2)

cycles. In the underfilled BGA #2 packages, no signs of deterioration in the thermal resistance were observed up to 2500 cycles. This underscores the ability of underfill to increase reliability of BGA packages.

3.11 Comparison of Study Parameters

By comparing the experimental results of the study, it was possible to identify the best configurations that minimize thermal resistance. Plots of the influences of various study parameters on the thermal resistance of BGA #1 and BGA #2 are shown in Figures 3.20 and 3.21, respectively. The best thermal performance was achieved using BGA #1 (larger die), using underfill, having thermal balls, and mounting the package on thermal via #2. This configuration reduced thermal resistance by 64% relative to the worst parameter combination, which was BGA #2 (small die), no underfill, no thermal balls, and mounting the package on thermal via #1.

Another important observation was the comparison of the impact of using underfill versus the impact of using thermal balls. From the BGA #1 results, it can be concluded that underfill was more important than the addition of thermal balls. Adding underfill reduced thermal resistance by 16.42 K/W, while adding thermal balls reduced thermal resistance by 13.56 K/W. However, the opposite was true for BGA #2, where adding underfill reduced thermal resistance by 17.69 K/W, while adding thermal balls reduced thermal resistance by 21.95 K/W. This apparent contradiction can be attributed to the different die sizes in the packages.

The ratio of the effective die area of BGA #1 to that of BGA #2 was about 2.1 to 1. This significant difference in size allowed BGA #1 to spread heat flow over a larger projected area that could take better advantage of the underlying underfill encapsulant layer. On the other hand, the smaller die in BGA #2 concentrated heat flow on a smaller area that could not take as much advantage of the underfill layer, and was thus more influenced by the thermal balls.

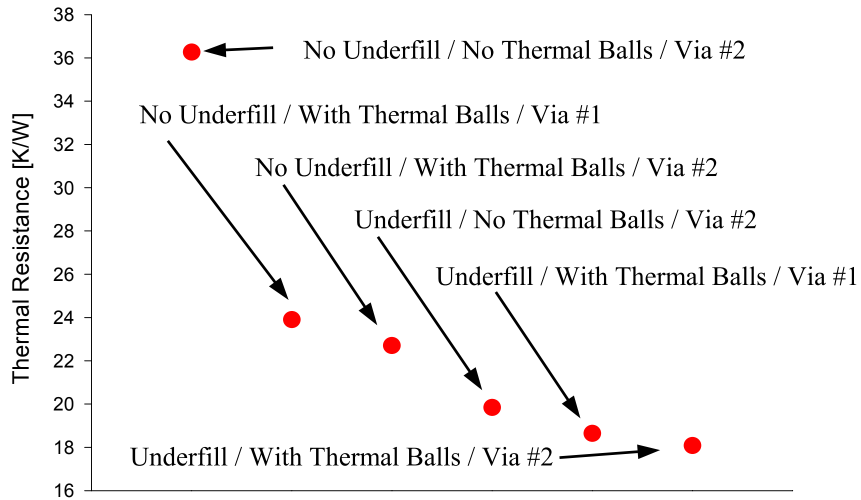


Figure 3.20 Impact of study parameters on thermal performance of BGA #1

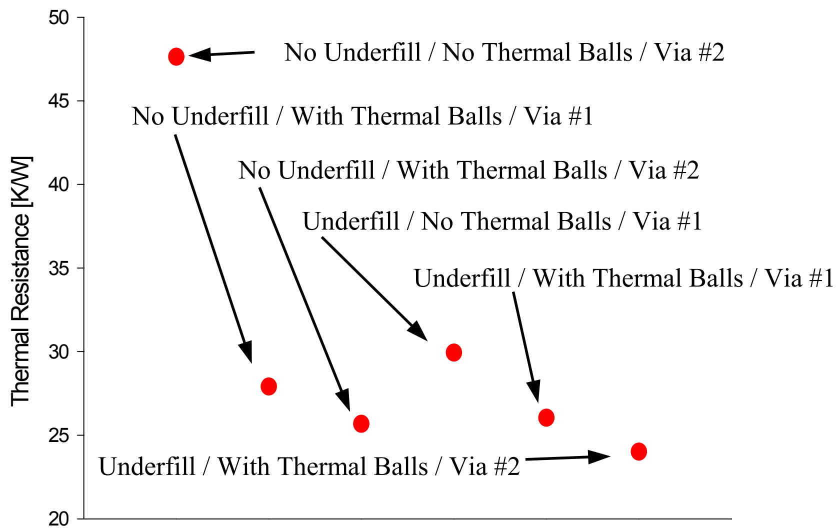


Figure 3.21 - Impact of study parameters on thermal performance of BGA #2

CHAPTER 4

THERMAL SIMULATIONS OF THE BGA PACKAGES

4.1 Model Construction

To further investigate the effects of the various packaging configurations on the heat conduction inside the BGA packages, 16 finite element models were developed that covered every combination in the experimental study discussed in the previous chapter. A heads up digitizing technique was used to capture package dimensions and details from cross-sectional photographs of the BGA assemblies. Using this method, a 2-D wire frame sketch was drawn against a backdrop of every package cross-section. Figure 4.1 shows the details of an example wire frame sketch superimposed on a package cross-sectional photograph.

The 2-D sketches were then used to create detailed solid models of the BGA assemblies. For example, Figure 4.2 shows a sectioned solid model of one of the packages. Such assembly files were produced for all of the tested BGA configurations. This approach allowed for accurate capturing of geometrical details like thermal via geometry and connectivity with copper ground planes buried inside the PCB.

Symmetry was utilized to reduce the sizes of the FEA models. Only 1/8th of each BGA #1 configuration was modeled, taking advantage of the square dimensions of

the die and BGA component. For BGA #2, the die had a rectangular shape and 1/4 models were developed.

The assembly files were imported into a commercial FEA package (Cosmos), where they were automatically meshed with 4 node tetrahedral heat conduction elements. Since all parts were modeled as solids, the FEA package was capable of automatically detecting contact surfaces and adjusting mesh nodes and mesh continuity accordingly. One of the meshed models is shown in Figure 4.3. Different mesh densities were applied to different parts within the assembly files to accommodate for the large variations of the major dimensions in different regions. The number of nodes and elements in the various finite element models are listed in Table 4.1.

Heat generation boundary conditions were applied to simulate heat generation of 1 Watt at the top surface of the die. The effect of the cooling water at the back surface of the PCB was modeled by applying a constant temperature of 20 ºC at that surface. The top surface of the BGA and PCB were modeled as perfectly insulated. Material properties were obtained from vendor data sheets and the literature, and are listed in Table 4.2. For models with no underfill, the underfill layer mesh was not removed. Instead, the value of the thermal conductivity was changed from that of underfill material to that of air. Thus, the effects of heat conduction in the air layer between the BT substrate and the PCB were included in the BGA configurations without underfill.

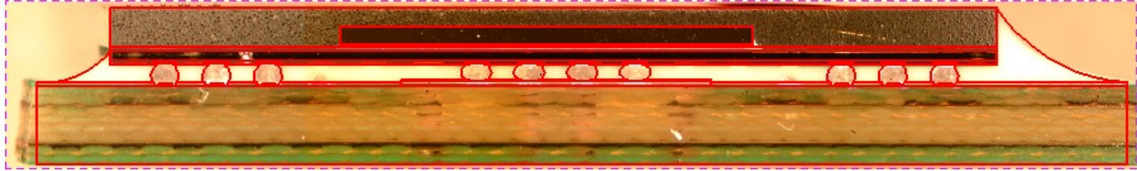


Figure 4.1 - Wire frame sketch overlaid on package photo

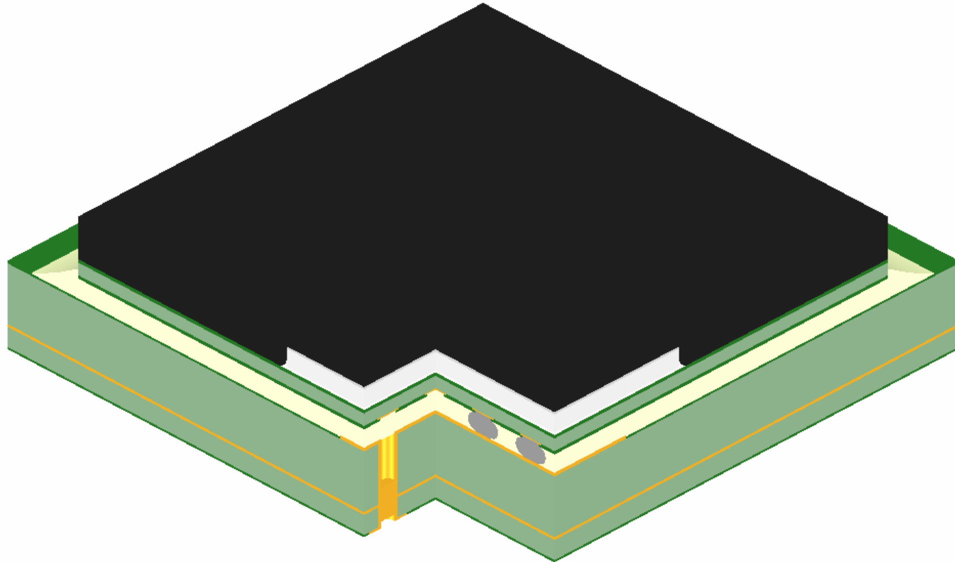


Figure 4.2 - Section solid model of BGA #1, with thermal balls

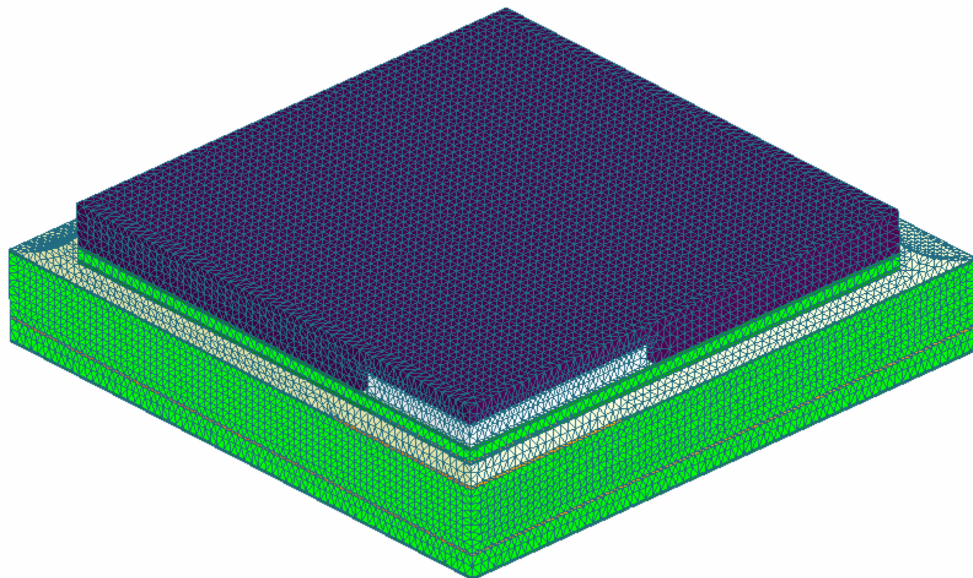


Figure 4.3 - Automatic mesh generated from a solid model (BGA #2)

Table 4.1 - Mesh sizes including underfill/air layer

	Number of Nodes	Number of Elements
BGA #1 / Via #1	102958	588790
BGA #1 / Via #2	79717	448677
BGA #2 / Via #1	137343	785677
BGA #2 / Via #2	154575	887189

Table 4.2 - Material properties for thermal FEA models

Material	Thermal Conductivity [W/(m·K)]	Specific Heat [J/(kg·K)]	Density [kg/m^3]
Soldermask	0.25	920.9	1910
Solder (Sn-Pb)	50	167	9630
Mold Compound	0.8	920.9	1910
Die Attachment Adhesive	2	920.9	1910
Silicon Die	140	703	2330
BT Substrate	1	920.9	1900
Underfill #1	0.38	920.9	1520
PCB	0.36	1369	1666
Copper	390	390	8900

4.2 Calculation of Thermal Resistance

The difference between the average temperature of the upper die device surface and the temperature of the back surface of the PCB (held constant at 20 ºC) was calculated for each model. Since the input power (heat generation) was chosen to be 1 Watt, the calculated temperature difference was equal to the package thermal resistance. The calculated thermal resistance values were then compared to those measured experimentally. Comparisons between numerical and experimental results from packages with thermal balls and without thermal balls are shown in Tables 4.3 and 4.4, respectively. The percent differences were reasonable, ranging from 0 to 12%. Plots of the numerical temperature predictions for each BGA geometry are presented in Appendix D.

The steady state simulations were used to calculate the amount of heat flowing through the various parts of the BGA assemblies. The three primary heat flow paths from the package to the board include the thermal balls, perimeter balls, and underfill/air layer. The average resultant heat fluxes were calculated for each of these paths at the plane defining the bottom of the BT substrate. Figure 4.4 shows an example vector plot of the resultant heat flux in one of the thermal balls. It can be seen that the heat flow tends to parallel the spherical surface of the solder. The heat flux vector at the top and bottom of the solder balls was found to be essentially normal to the BT substrate (z-direction), although there was a small in-plane component that will be neglected in further discussions.

Table 4.3 - Comparison between experimental measurements and numerical simulations for packages with thermal balls

Packaging Configuration	Thermal Resistance (K/W)		% Difference
	Experimental	Simulation	
BGA#1/Via#1 No Underfill	23.94	26.14	-9.2
BGA#2/Via#1 No Underfill	27.90	26.89	3.6
BGA#1/Via#2 No Underfill	22.71	24.52	-8
BGA#2/Via#2 No Underfill	25.67	23.73	7.6
BGA#1/Via#1 Underfill #1	18.64	20.18	-8.3
BGA#2/Via#1 Underfill #1	26.04	24.05	7.6
BGA#1/Via#2 Underfill #1	18.08	18.51	-2.4
BGA#2/Via#2 Underfill #1	24.01	21.27	11.4

Table 4.4 - Comparison between experimental measurements and numerical simulations for packages without thermal balls

Packaging Configuration	Thermal Resistance (K/W)		% Difference
	Experimental	Simulation	
BGA#1/Via#2 No Underfill	36.26	36.27	0
BGA#2/Via#2 No Underfill	47.62	48.18	1.1
BGA#1/Via#2 Underfill #1	19.84	21.92	-10.5
BGA#2/Via#2 Underfill #1	29.93	33.6	-12.2

4.2.1 Impact of Using Thermal Balls.

The numerical simulation results illustrated the importance of using thermal balls. For BGA #1 mounted on thermal via #2, it was seen that 0.14 Watts flowed normal to the thermal balls with the use of underfill, and 0.21 Watts flowed normal to the thermal balls without using underfill. This means that at least 20% of the heat flowed through the thermal balls, in spite of their small net cross sectional area, which was less than 0.5% of the total projected area of the bottom face of the package. In fact, the highest value of heat flux (12×10^5 W/m^2) was located in the thermal balls.

Another important observation was that the effective cross-sectional areas of the thermal balls were highly governed by the cross-sectional areas of the matching copper pads. A typical plot of z-direction flux in one of the BGA configurations is shown in Figure 4.5. The highest values of flux in the solder balls were found to occur in a set of virtual cylinders axially concentric with the connecting copper pads on the PCB.

4.2.2 Impact of Number of Perimeter Balls.

Although the number of perimeter balls was ten times larger than the number of thermal balls in BGA #1, and 12 times larger in BGA #2, the perimeter balls were found to make relatively little contribution to the heat flow. This was mainly due to their remote location from the die when compared to the thermal balls. For BGA #2, mounted on thermal via #2, the contribution of the perimeter balls was only 0.02 Watts for the case with no thermal balls and no underfill. In addition, the heat flux distribution was observed to be non-uniform over the perimeter balls. The highest value of heat flux (42×10^3

W/m^2) was observed at the perimeter ball closest to the die edge. The lowest value of heat flux (42 x 10^2 W/m^2) was observed at the perimeter ball furthest from die edge. An example plot of the z-direction heat flux distribution in the perimeter balls is shown in Figure 4.6.

4.2.3 Impact of Using Underfill Material.

The surface temperature dropped from 44.5 °C to 18.5 °C when using underfill with BGA #1 mounted on thermal via #2, which was in close agreement with the analogous experimental measurements. Significant variation in the z-direction heat flux magnitude was found at the BT/underfill interface. Fluctuation patterns changed according to the use of underfill and/or thermal balls. However, all package configurations shared one important feature, which was a strong reduction in the heat flux outside the die shadow. For example, in the case of BGA #1 with underfill and without thermal balls, the z-direction heat flux in the area underneath the die varied between 7,000 W/m^2 and 12,000 W/m^2, while in the area outside of the die shadow, the values declined to around 500 W/m^2. Plots of the z-direction heat flux at the package center line on the bottom surface of the BT laminate for different BGA #1 configurations are shown in Figure 4.7.

4.2.4 Impact of Die Size

The numerical simulation results also verified that die size was a major factor effecting the thermal performance and heat flux distribution within the BGA packages.

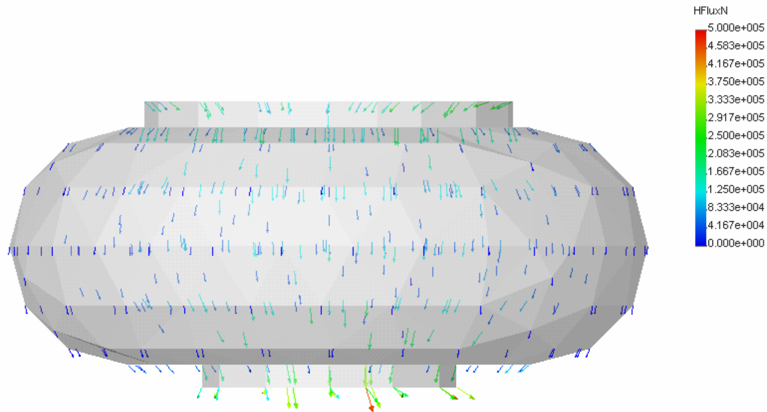


Figure 4.4 - Vector plot of resultant heat flux in a thermal ball
(BGA #2 / Via #2 / No underfill)

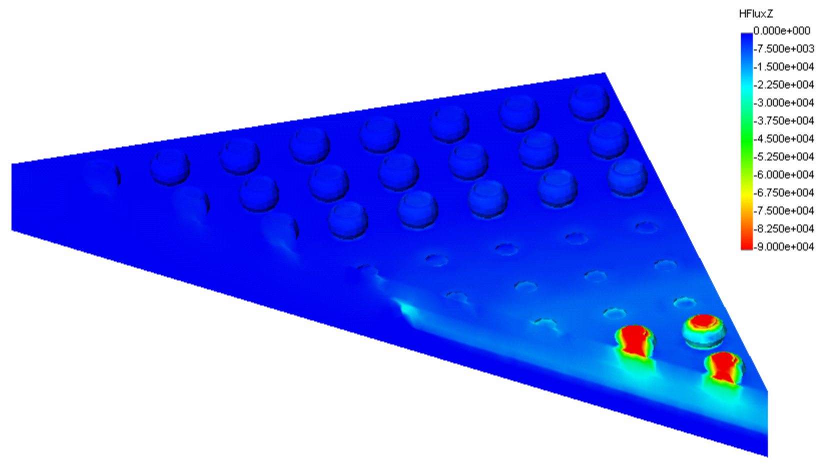


Figure 4.5 - Example plot of the z-direction heat flux in BGA #2 package
(Via #2 / No underfill)

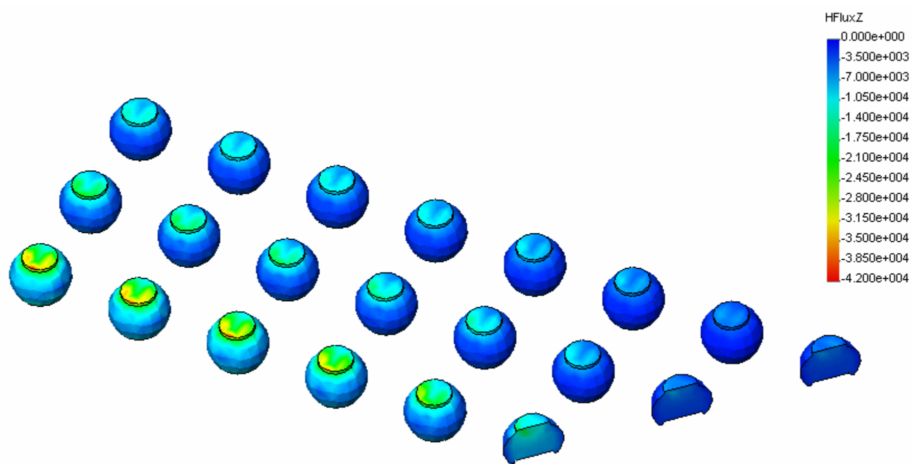


Figure 4.6 - Example plot of the z-direction heat flux in the perimeter balls
(BGA #2 / Via #2 / No underfill)

Similar to the experimental measurements, the BGA #2 packages with smaller die were found to exhibit poorer thermal performance when compared to the analogous BGA #1 packages. The BGA #2 packages were equipped with a copper thermal via on the BT side that should have enhanced performance. However, the die area effect was found to be a much more decisive factor in the ranking of relative thermal performances.

The smaller die area in BGA #2 had a strong impact on the maximum z-direction heat flux values at the bottom of the BT laminate. For example, the maximum value was 12,000 W/m^2 for BGA #1 with via #2, and 80,000W/m^2 for BGA #2 with via #2. An example contour plot of the heat flux on the bottom surface of the BGA #2 BT substrate is shown in Figure 4.8. This plot indicates that the highest z-axis heat flux values exiting the bottom surface of the BT laminate were contained within the areas defined by the die perimeter and PCB thermal via.

4.2.5 Impact of Thermal Via Geometry

Comparing the resultant heat flux patterns for analogous BGA #1 configurations with thermal via #1 and thermal via #2 revealed that the maximum heat flux in thermal via #1 (7×10^5 W/m^2) was almost 3 times as much as the maximum heat flux in thermal via #2 (2.5×10^5 W/m^2). This was due to the increased copper area in the heat spreader in thermal via #2. Example vector plots of the heat flux in thermal via #1 and thermal via #2 are shown in Figures 4.9 and 4.10, respectively for the case of BGA #1 with thermal balls and without underfill. These results all support the experimental observations that packages mounted on thermal via #2 had better thermal performance relative to similar packages mounted on thermal via #1.

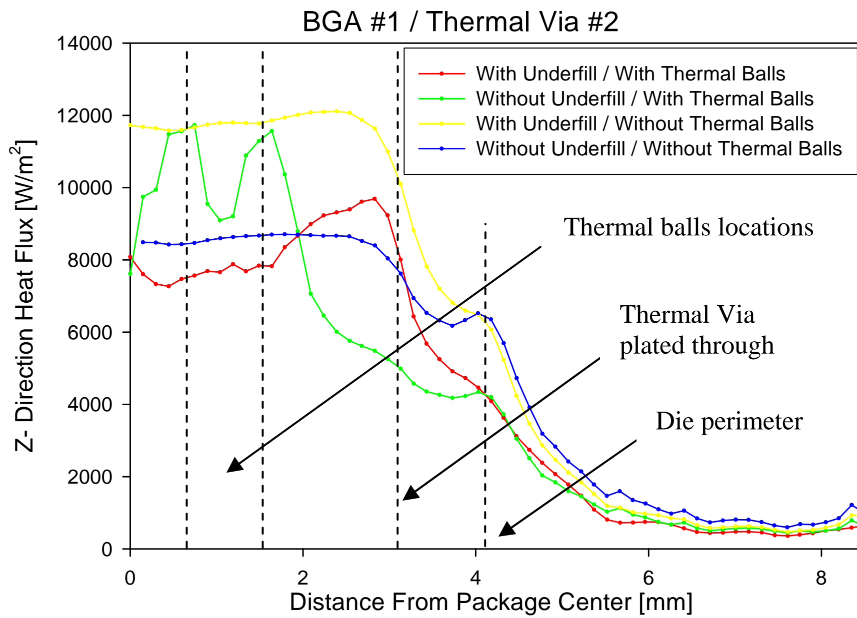


Figure 4.7 - Plots of z-direction heat flux at the bottom of BT substrate for BGA#1

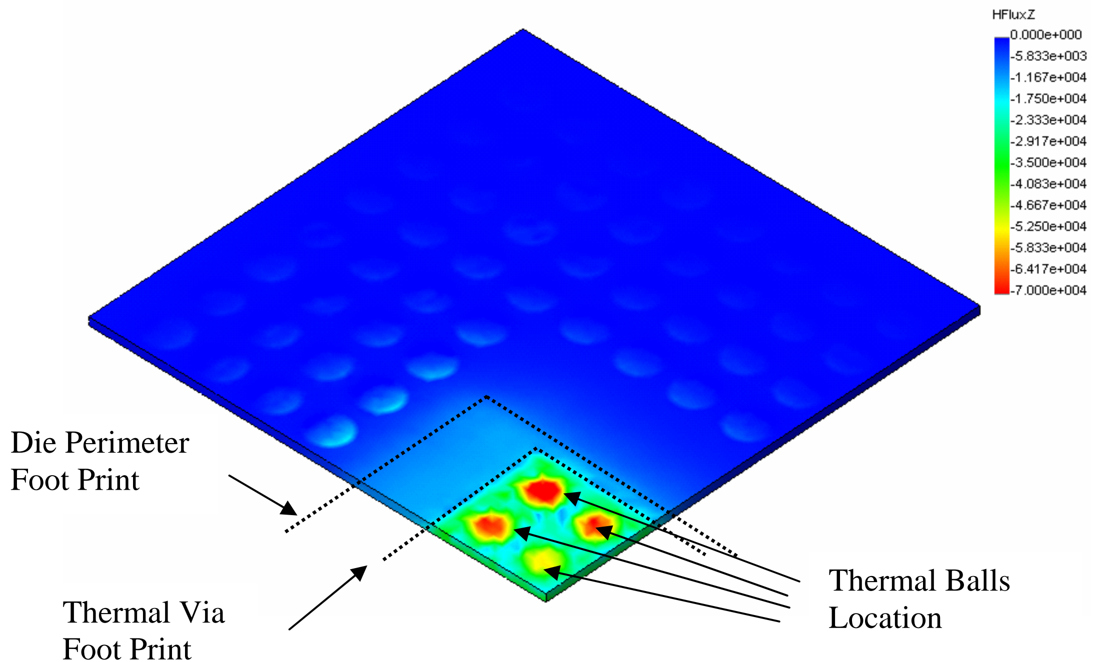


Figure 4.8 - Example contour plot of the z-direction heat flux at the bottom of BT substrate (BGA #2)

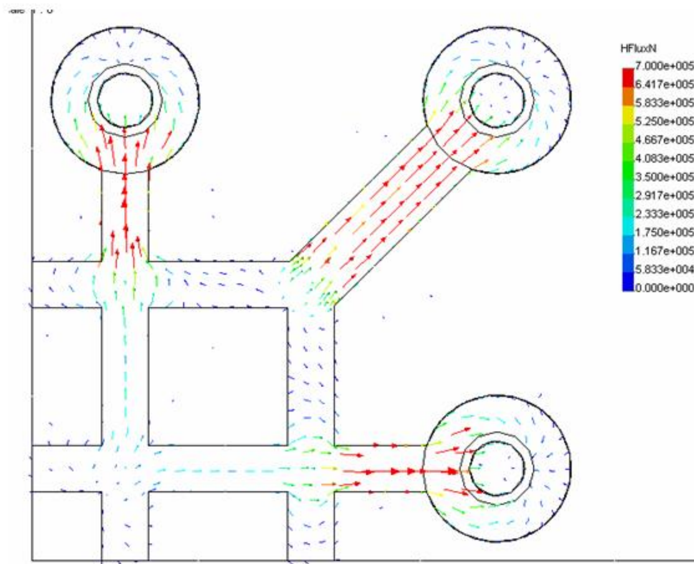


Figure 4.9 - Vector plot of heat flux in thermal via #1
(BGA#1, with thermal balls, no underfill)

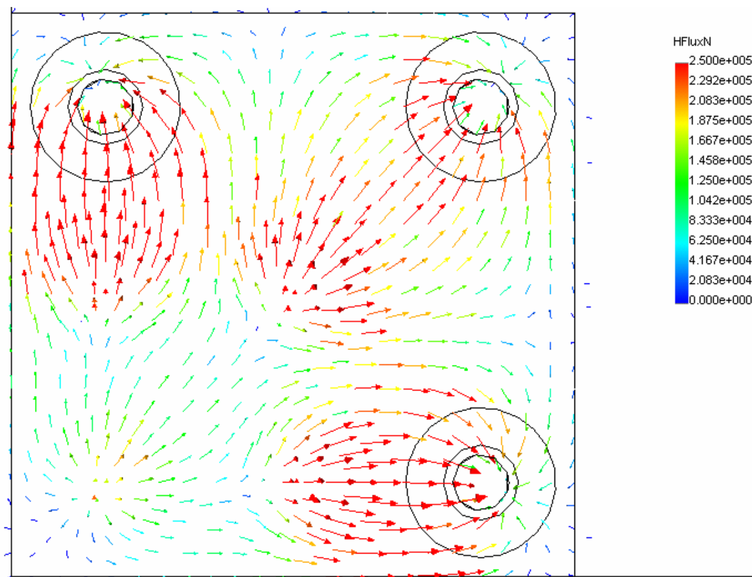


Figure 4.10 - Vector plot of heat flux in thermal via #2
(BGA#1, with thermal balls, no underfill)

4.3 Transient Thermal FEA Simulation

Transient numerical simulation models were developed to investigate the times needed for the various package configurations to reach steady state. For the time dependent models, the same materials and boundary conditions as the steady state models were used. The temperature distributions were output at equal intervals of one second. At every solution sub-step, the average temperature of die surface was calculated. Using this data, temperature versus time plots were created as shown in Figures 4.11 and 4.12 for BGA #1 and Via #1, and BGA #1 and Via #2, respectively. BGA packages with the smallest thermal resistances reached steady state conditions faster than those with higher thermal resistances. For example, BGA #1 mounted on via #2 was predicted to reach steady state after 60 seconds for the case without underfill and without thermal balls. For the case with thermal balls and with underfill, the time to steady state was reduced to 40 seconds.

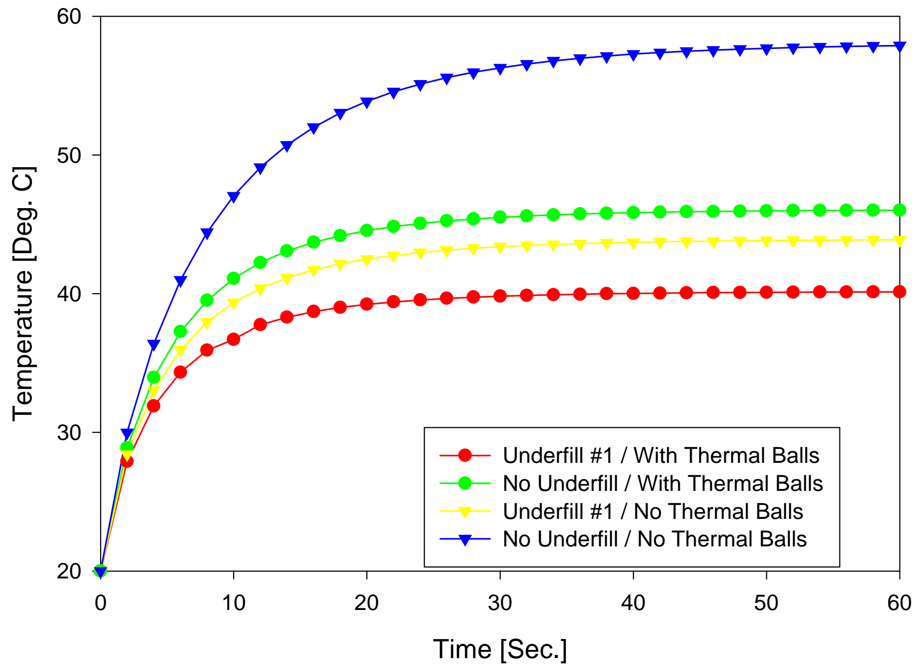


Figure 4.11 - Temperature vs. time plots for BGA #1 and Via #1

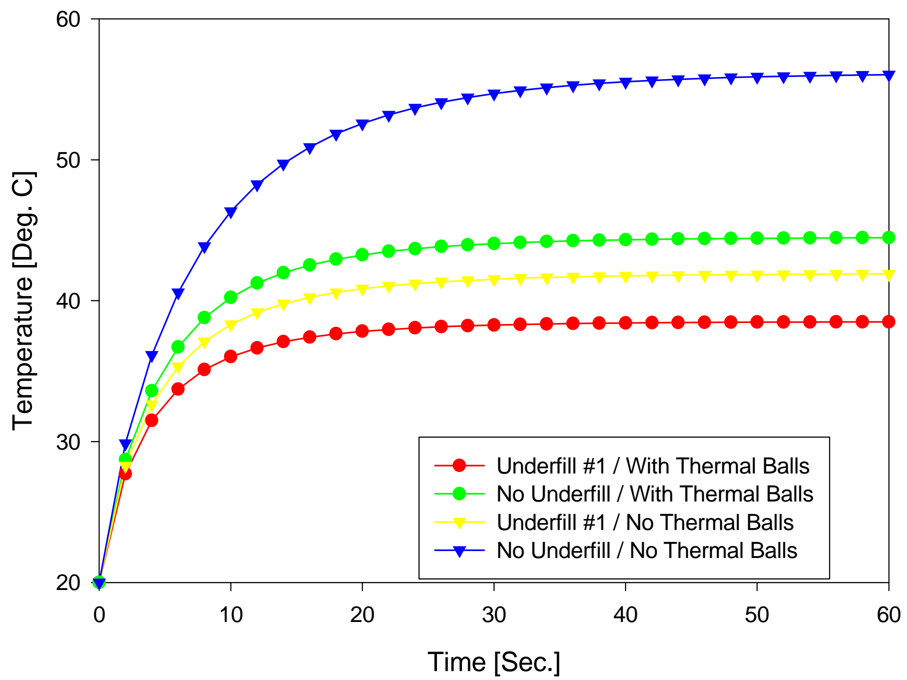


Figure 4.12 - Temperature vs. time plots for BGA #1 and Via #2

CHAPTER 5

STRUCTURAL SIMULATIONS OF THE BGA PACKAGES

5.1 Model Objectives

Temperature variations within electronic packages coupled with mismatches of the thermal expansion coefficients of the constituent materials induce thermal stresses that can cause cracks and or fractures. The most common failure mode during thermal cycling of BGA packages is fatigue cracking of the solder joints. Typically, the cracks initiate at the top and/or bottom interfaces of the solder joints. Further exposure to thermal cycling causes growth of the initial crack until there is a total fracture across the solder joint.

Reliability and thermal analyses are usually conducted as two distinct research studies. However, since the previously presented experimental and numerical thermal studies have indicated the importance of the solder joints as effective heat paths within BGA packages, it is important to understand the impact of crack growth in solder joints on thermal performance. The experimental measurements in this study have demonstrated that the thermal resistance of a BGA package will increase with the continued exposure to thermal cycling. The objective of the structural simulation part of this research is to predict the number of thermal cycles needed to cause cracking of the

solder joints. Using these results, it will be possible to establish a correlation between observed deterioration of thermal performance and the occurrence of solder joint crack initiation and propagation.

5.2 Model Construction

Although meshed models were already available from the thermal simulations presented in the previous chapter, there are concerns regarding the accuracy of tetrahedral elements in structural finite element simulations. Manual generation of brick element meshes for BGA packages can be a tedious task, and is especially burdensome if mesh or dimensional modifications are needed. Such modifications would typically necessitate a restart of the model generation from the beginning. However, by investing a little more time, it was possible in this work to develop a parametric modeling program capable of generating a one quarter symmetry FEA model of any plastic BGA package (with certain limitations) given its internal dimensions and the required mesh density.

Using the developed parametric modeling approach, mesh generation time was lowered to less than one hour instead of days or weeks. The program also offered the advantage of allowing experimentation with different mesh densities with minimal time and effort. For example, two parametrically generated models with the same dimensions and different mesh densities are shown in Figures 5.1 and 5.2. The program for parametric generation was written using the ANSYS parametric development language (APDL). The internal dimensions of the BGAs were extracted from a set of 2-D sketches

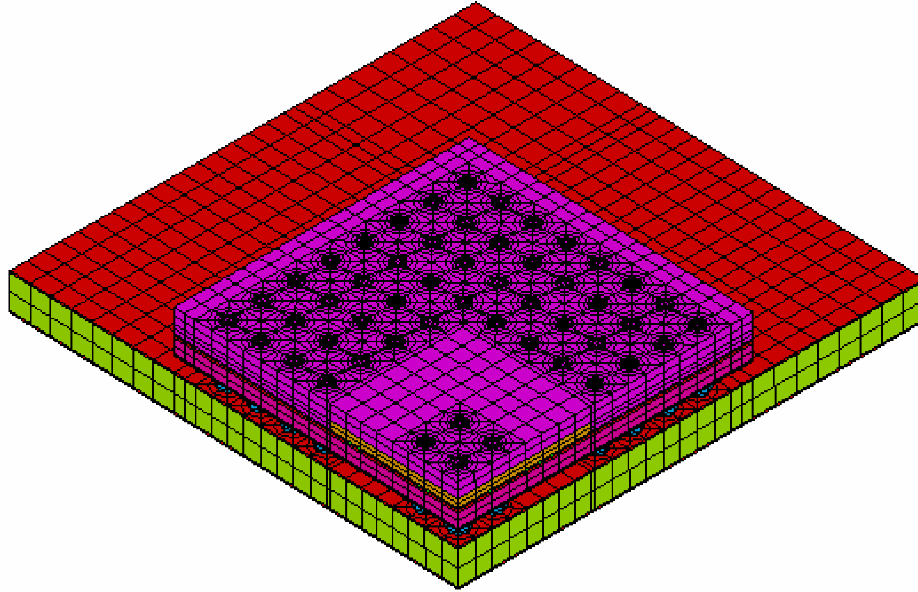


Figure 5.1 - Parametrically generated FEA model with the solder ball perimeter divided into 8 elements

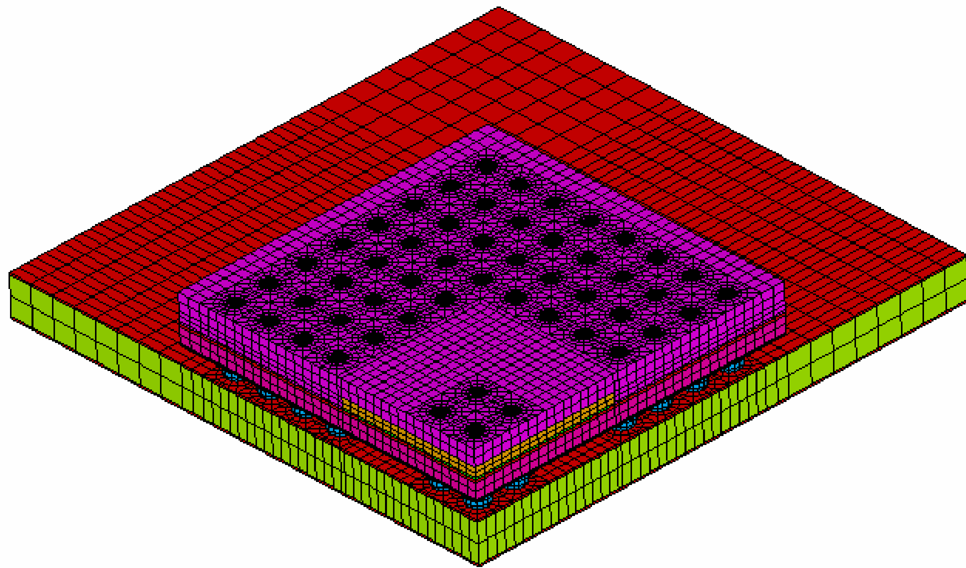


Figure 5.2 - Parametrically generated FEA model with the solder ball perimeter divided into 16 elements

using the method described in the previous chapter. Using these dimensions and a set of prescribed mesh densities, the APDL algorithm successfully generated a set of meshes for structural analysis of BGA #1.

The developed parametric modeling program had several limitations. These limitations were:

1. No underfill layer can be present.
2. The die perimeter can not extend beyond the inner row of perimeter solders balls.
3. The die must be square.
4. The die width must be a multiple of the solder ball pitch
5. The two symmetry planes of the package must not pass through the solder balls

The algorithm implemented in the parametric model generation involved dividing the BGA assembly into 6 subparts. Every subpart is generated and saved to a separate mesh file using the model dimensions and mesh densities defined in a single mesh description input file. The six model subparts are:

1. Array of thermal balls.
2. Extent of thermal vias.
3. Extent of die perimeter.
4. Connection from die perimeter to array of perimeter balls.
5. Array of perimeter balls.
6. Extent of package and PCB perimeter.

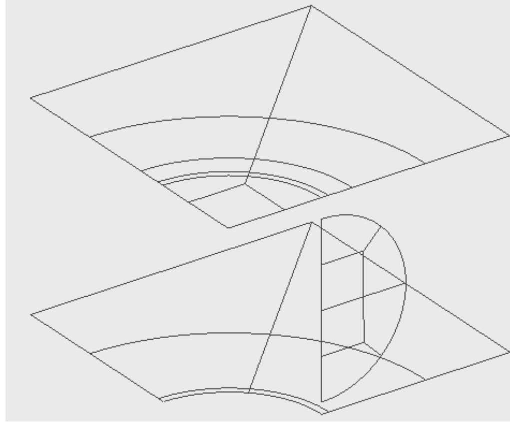
Since every subpart model is created using parameters from the same master file, mesh continuity between the different subparts was automatically preserved. After the generation of the subpart models, a new empty file is created into which all of the subpart

models were read in and merged. Finally, the material models, symmetry boundary conditions, and thermal loads are then applied to complete the finite element input file.

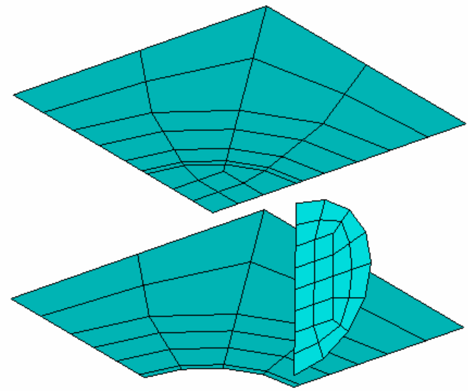
5.3 Mesh Generation

The mesh generation techniques for the different subpart models were identical. The first step was to create a 3-D wire frame sketch using a set of points, lines and arcs that define the major dimensions of the subpart. The wire frame sketch lines and arcs were then assigned the mesh densities values defined in the master mesh description input file. The sketch elements were merged to form a set of 2-D areas that were auto meshed with 2-D elements. These meshed areas were then used to generate a set of meshed volumes through as series of extrusions and revolutions. Finally, mirror and symmetry commands were applied and the subpart file was saved. As an example, details of the 4 steps needed to create one of the subpart files are shown in Figure 5.3. The 6 steps needed to assemble the various subpart meshes into a mesh for the complete assembly are shown in Figure 5.4.

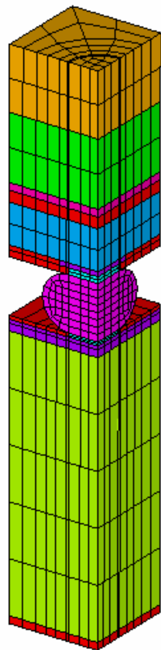
Since the thermal balls had a shorter standoff than the perimeter balls due to the thickness of the copper heat spreader, the thermal ball shape was considerably different than the perimeter ball shape. This necessitated a different meshing approach to avoid highly distorted elements. To model the no bonding behavior present between the solder balls and the PCB and BT laminate soldermask layers, small gaps of 0.0125 mm were introduced to separate the solder balls from the soldermask layers. Figure 5.5 shows details of the gaps between the solder ball and the soldermask layers.



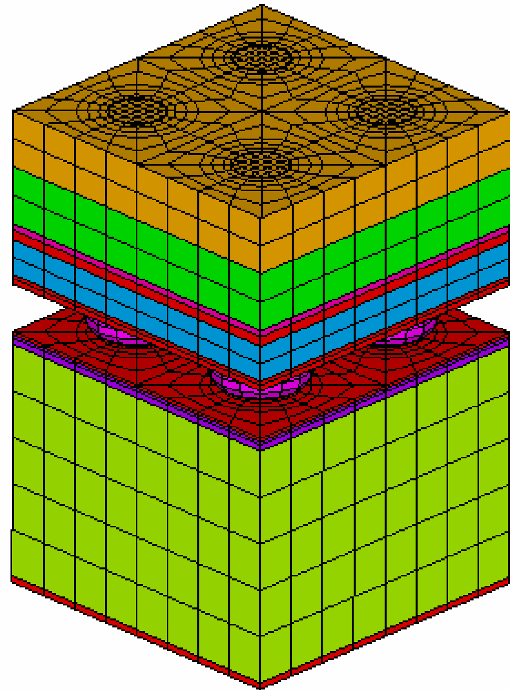
Step 1: Read dimensions from master file and create a 3-D wire frame sketch



Step 2: Read mesh densities from master file, and create meshed areas



Step 3: Execute a set of extrusion and rotation commands to create meshed volumes



Step 4: Apply mirror and array commands to complete subpart mesh

Figure 5.3 - The four steps needed to generate a subpart mesh (Array of thermal balls)

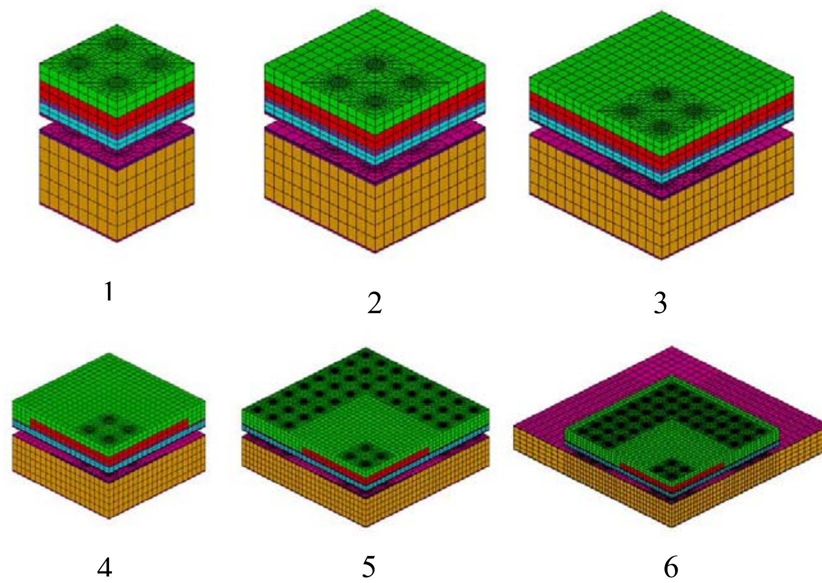


Figure 5.4 - Six progressive steps for generation of the mesh for the complete BGA assembly

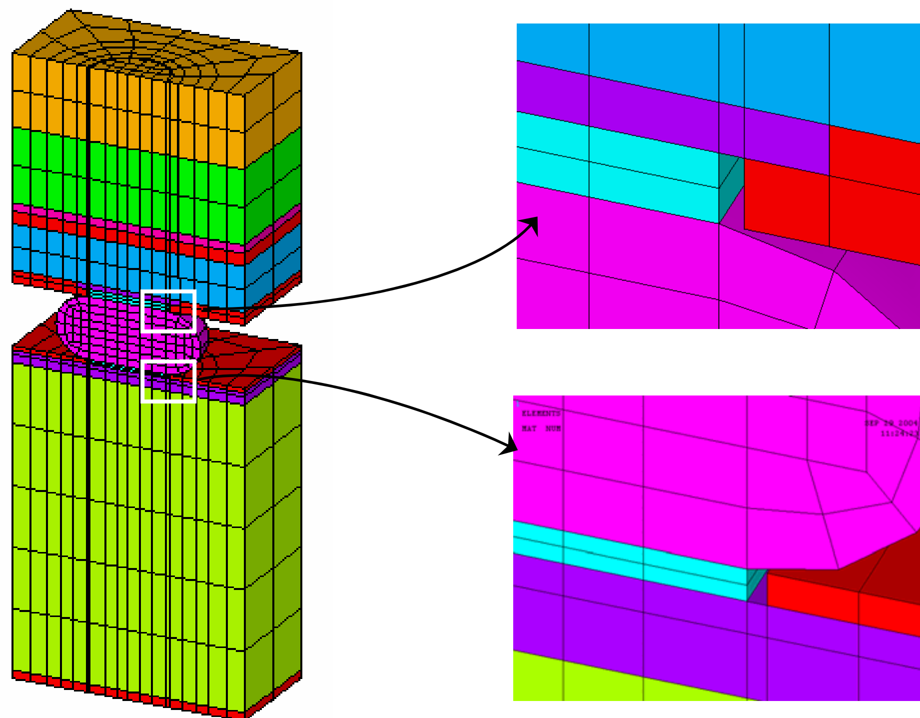


Figure 5.5 - Mesh at the gaps between the solder ball and the soldermask

Two parametric models were generated for BGA #1 and no underfill for the cases of with and without thermal balls. The model with thermal balls consisted of 177,369 nodes and 159,572 elements. The model without thermal balls consisted of 174,029 nodes and 156,500 elements. A second more simple version of the parametric generation program was also developed, which was capable of generating more general BGA constructions (i.e. with no thermal vias and identical thermal and perimeter balls).

5.4 Material Models and Thermal Loads

A thermal cycling temperature load was applied to the developed finite element models for the BGA assemblies. As shown in Figure 5.6, two thermal cycles from -40 to 125 ºC were simulated. As in the experimental testing, the cycles were 90 minutes in duration with 15 minutes ramps and 30 minutes dwells at the lower and upper extremes. Material property data were collected from several publications [21-23] and the CINDAS database [35]. The BT substrate and PCB were modeled as linear elastic orthotropic materials. The copper layers, silicon die, die attachment adhesive, soldermask, and molding compound were all modeled as linear elastic isotropic materials. Temperature dependent properties were utilized for the PCB, BT substrate and solder. The material properties used in the analysis are listed in Table 5.1.

The solder joints were modeled using the temperature dependent Anand viscoplasticity model to capture the creep-plasticity behavior of the 63/37 tin/lead solder alloy [22-23]. The input temperature dependent stress-strain curves for solder are shown in Figure 5.7. The Anand viscoplasticity model consists of one flow equation and 3 evolution equations. The flow equation is defined by:

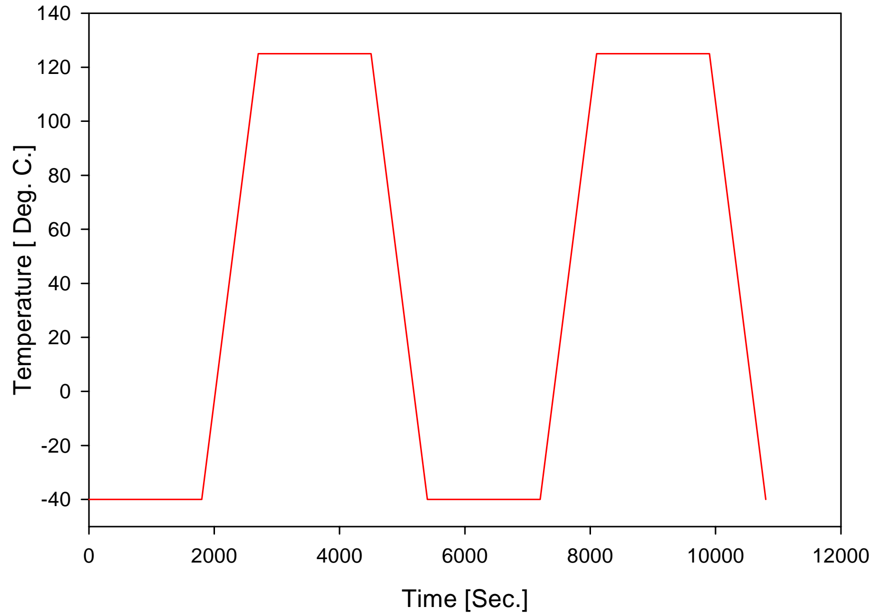


Figure 5.6 - Thermal cycling load profile

Table 5.1 - Material properties used in the finite element structural analyses

Material	Elastic Modulus [MPa]	Shear Modulus [MPa]	Poisson Ratio	CTE [1/K]
BT Substrate	(XY) 1.789×10^4 (Z) 7.846×10^3	(XY) 8061 (XZ & YZ) 2822	(XY) 0.11 (XZ & YZ) 0.39	(XY) 12.42×10^{-6} (Z) 57×10^{-6}
Copper	1.29×10^5		0.34	16.3×10^{-6}
Silicon Die	$163 \times 10_3$		0.278	2.5×10^{-6}
Die Attachment Adhesive	6769		0.35	83.6×10^{-6}
Soldermask	3100		0.3	30×10^{-6}
Molding Compound	23520		0.25	10×10^{-6}
PCB	(XY) 19303 @ -40º 13198 @ 125º (Z) 8476 @ -40º 5836 @ 125º	(XY) 8709 @ -40º 5953 @ 125º (XZ & YZ) 3799 @ -40º 2595 @ 125	(XY) 0.11 (XZ & YZ) 0.39	(XY) 14.5×10^{-6} (Z) 67.2×10^{-6}
Solder	40426 @ -40º 34471 @ 125º		0.35	24.5×10^{-6}

$$\frac{d\varepsilon_p}{dt} = A(\sinh(\xi\sigma / s_0))^{\frac{1}{m}} \exp\left(\frac{-Q}{kT}\right) \qquad \text{(Eq. 5.1)}$$

The 3 evolution equations are defined by:

$$\frac{ds_0}{dt} = \left\{h_0(|B|)^a \frac{B}{|B|}\right\}\frac{d\varepsilon_p}{dt} \qquad \text{(Eq. 5.2)}$$

$$s^* = s\hat{}\left[\left(\frac{d\varepsilon_p}{dt}\Big/A\right)\exp\left(\frac{Q}{kT}\right)\right]^n \qquad \text{(Eq. 5.3)}$$

$$B = 1 - \frac{s_0}{s^*} \qquad \text{(Eq. 5.4)}$$

Definitions and values of the parameters in the Anand model are shown in Table 5.2. The advantage of using the Anand model over other available creep models in ANSYS was the ability to capitalize on damage relationships that were calibrated using that model in several recent publications [23-24].

5.5 Evaluation of Number of Cycles to Crack Initiation

After solving the finite element models, the critical solder balls (balls with maximum value of the accumulated viscoplastic strain energy density per cycle) were located. A plot of the viscoplastic strain energy density in the perimeter and thermal solder balls of BGA #1 is shown in Figure 5.8. A similar plot for the BGA #1

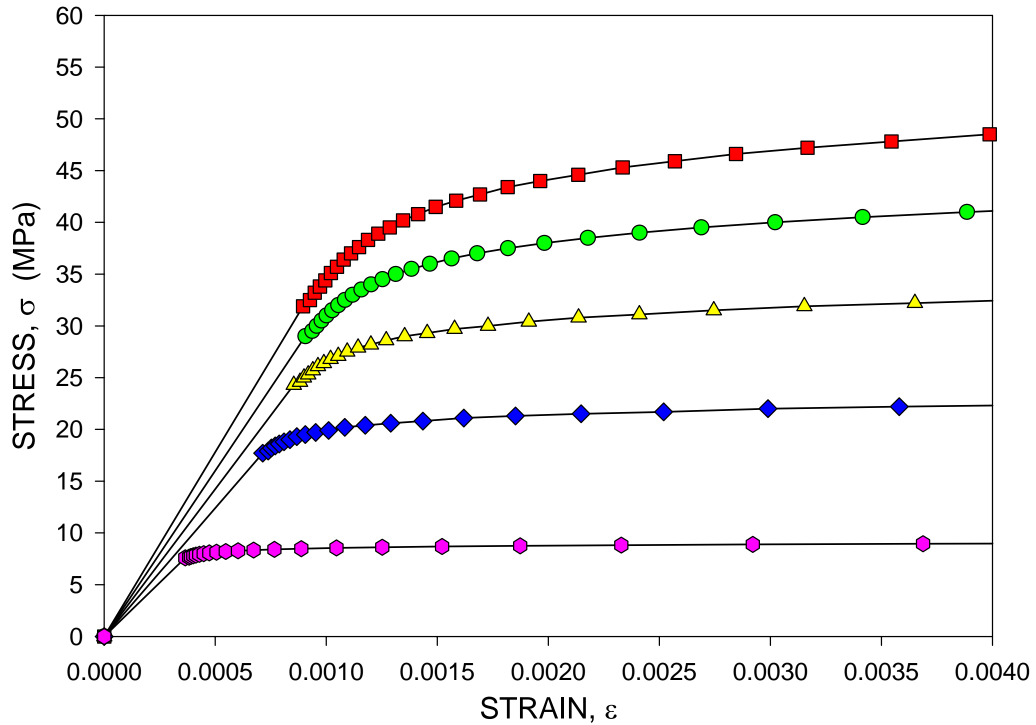


Figure 5.7 - Temperature dependent stress strain curves for 63Sn-37Pb solder

Table 5.2 - Definitions and values of the Anand model parameters

Parameter	Value	Definition
S_0 (MPa)	12.41	Initial Value of Deformation Resistance
Q/k (1/K)	9400	Activation Energy/ Boltzmann's Constant
A (1/sec)	4.0E-6	Pre-Exponential Factor
ξ (dimensionless)	1.5	Multiplier of Stress
m (dimensionless)	0.303	Strain Rate Sensitivity of Stress
h_0 (MPa)	1378.95	Hardening Constant
S* (MPa)	13.79	Coefficient of Deformation Resistance Saturation Value
n (dimensionless)	0.07	Strain Rate Sensitivity of Saturation (Deformation Resistance) Value
a (dimensionless)	1.3	Strain Rate Sensitivity of Hardening

configuration without thermal balls is shown in Figure 5.9. In both cases, the critical perimeter solder ball was located on the package diagonal, farthest from the package center. Similarly, the critical thermal ball in Figure 5.8 was located on the package diagonal, furthest from package center.

Volumetric averaging of the viscoplastic strain energy density was preformed to minimize the effects of mesh density on the calculation accuracy. The accumulated energy density was calculated at the first and the second thermal cycles. The thermal balls were soldermask defined (SMD) at both the top and bottom interfaces. In this case, the portions of the solder used for calculating the volumetric average of the viscoplastic strain energy density were the parts protruding inside the solder mask (see Figure 5.10). The perimeter balls were soldermask defined at their top interface and non-soldermask defined (NSMD) at their bottom interface. In this case, the volumetric averaging was preformed on the protruding portion at the top interface and in a 5 mil thick layer at the bottom interface (see Figure 5.10).

The accumulated plastic work per thermal cycle was calculated according to:

$$\Delta W_{ave} = \left[\left. \frac{\Sigma W_e . V_e}{V_e} \right|_{Time=180\,minutes} \right] - \left[\left. \frac{\Sigma W_e . V_e}{V_e} \right|_{Time=90\,minutes} \right] \qquad \text{(Eq. 5.5)}$$

where:

W_e = Element viscoplastic strain energy density

V_e = Element volume

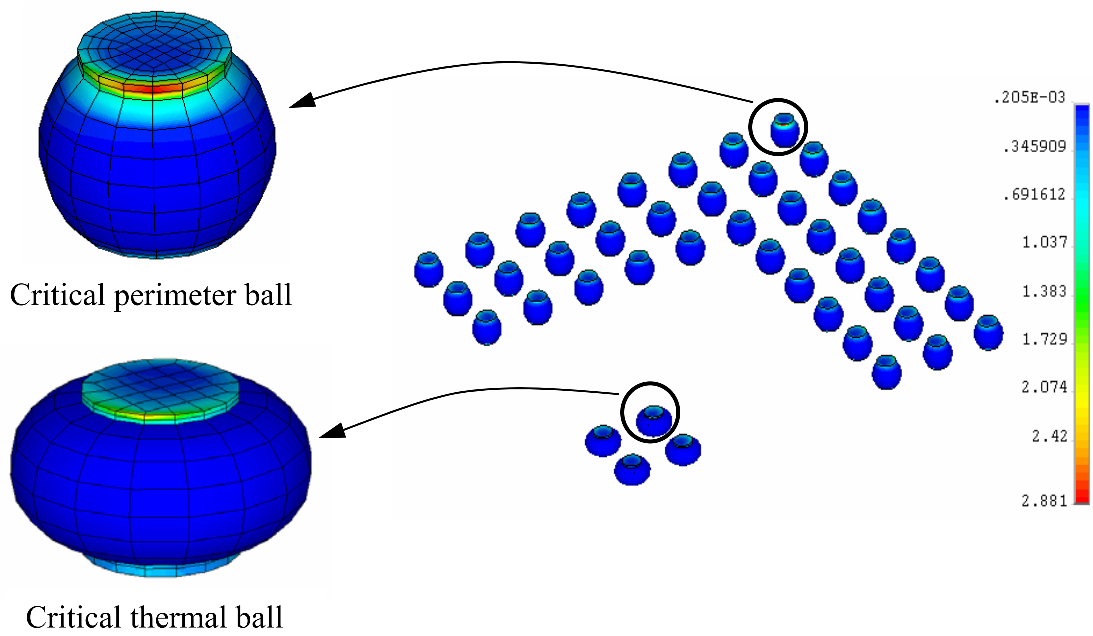


Figure 5.8 - Critical solder balls for BGA #1 with thermal balls

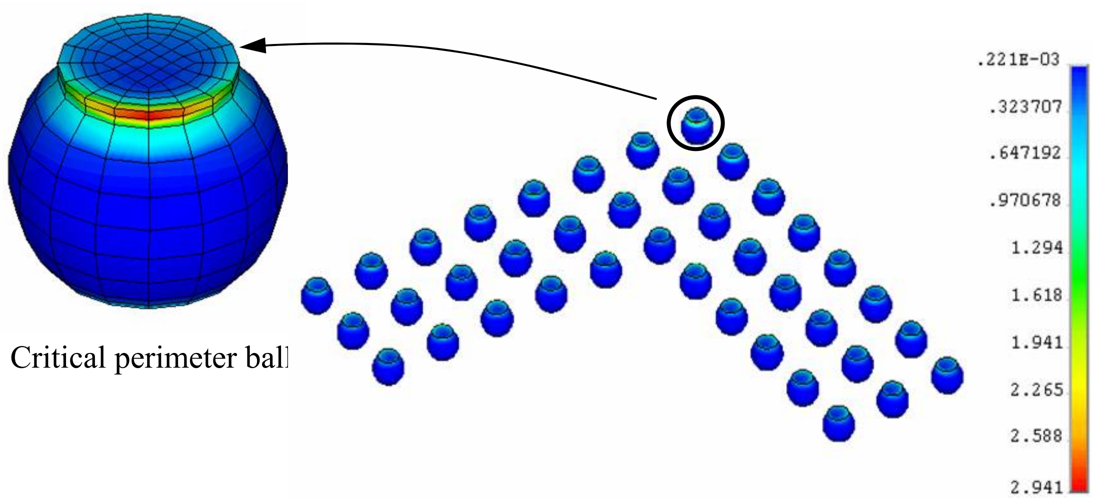
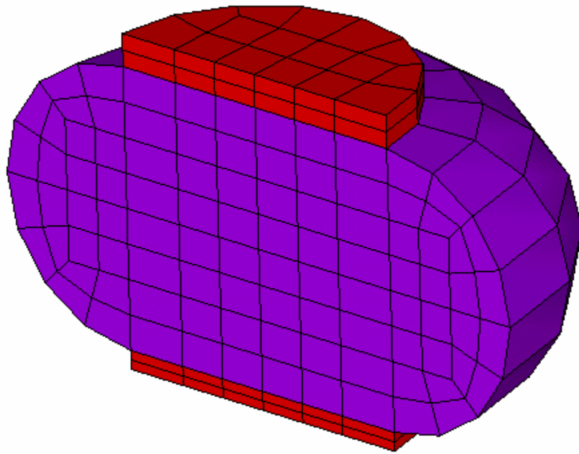
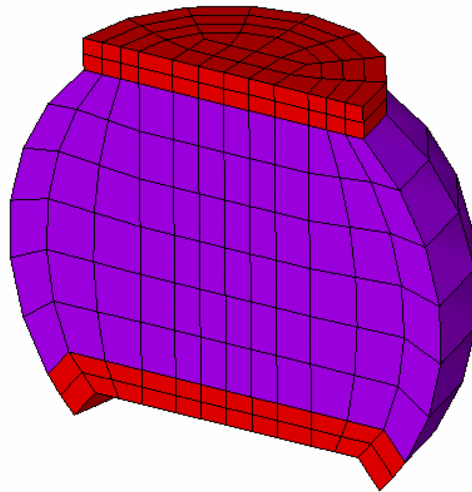


Figure 5.9 - Critical solder ball for BGA #1 without thermal balls



Thermal ball



Perimeter ball

Solder ball bulk

Portion used for volumetric averaging of the viscoplastic strain energy density

Figure 5.10 - Solder balls and regions used for volumetric averaging

Calculated values of the average viscoplastic work accumulated per cycle for the critical solder balls are listed in Table 5.3. Using material correlation data between number of cycles to crack initiation and plastic work developed by Darveaux, et al. [23] and Lall, et al. [24], the number of cycles to crack initiation of the two BGA packages was estimated according to:

$$N_0 = K_1 \left(\Delta W_{ave} \right)^{K_2} \qquad \text{(Eq. 5.6)}$$

where:

N_0 = Number of cycles to crack initiation

ΔW_{ave} = Volumetric average of viscoplastic work accumulated per thermal cycle

K_1, K_2 = Material correlation constants given in Table 5.4.

The calculated number of thermal cycles to crack initiation for the critical solder balls are listed in Table 5.5.

5.6 Impact of Critical Solder Joints Crack Initiation on Thermal Resistance

Plots of the crack initiation predictions overlaid on the thermal resistance measurements during thermal cycling are shown in Figures 5.11 and 5.12 for BGA #1 without underfill and configurations with and without thermal balls, respectively. In the BGA with thermal balls, it was clear that the first observation of thermal resistance increase occurred in close proximity to the number of cycles where the finite element model predicted initiation of cracking in the thermal solder balls. This further confirms

Table 5.3 - Calculated values of the average viscoplastic work accumulated per cycle (BGA #1, no underfill)

	Critical Perimeter Ball (without thermal balls)	Critical Perimeter Ball (with thermal balls)	Critical Thermal Ball
$\frac{\sum W_e.V_e}{\sum V_e}$ [psi] @ Time= 5400 Sec. (1 Cycle)	41.04	40.25	29.88
$\frac{\sum W_e.V_e}{\sum V_e}$ [psi] @ Time= 10800 Sec. (2 Cycles)	55.73	54.5	47.07
ΔW_{ave} [psi]	14.69	14.25	17.19

Table 5.4 - Darveaux and Lall material correlation constants [23,24]

	K_1	K_2
Darveaux	48300	-1.64
Lall	28769	-1.53

Table 5.5 - Calculated number of thermal cycles to crack initiation (BGA #1, no underfill)

	Critical Perimeter Ball (without thermal balls)	Critical Perimeter Ball (with thermal balls)	Critical Thermal Ball
Darveaux	589	619	455
Lall	471	494	371

the importance of thermal balls to thermal performance. For the case without thermal balls, the observed increases in thermal resistance were also observed to initiate in close proximity to the number of cycles where the finite element model predicted initiation of cracking in the perimeter solder balls.

An important observation was that the FEA models predicted that cracks would initiate in the critical thermal ball (which is close to package center) before crack initiation occurred in the critical perimeter ball (which is furthest from package center) using both sets of material constants in the failure model. This contradicted the conventional wisdom that the critical perimeter balls usually crack earlier than the critical thermal balls. This contradiction can be attributed to the fact that thermal balls were mounted on a relatively thick copper heat spreader (via). That meant that the thermal expansion coefficient mismatch between the die and the PCB near the thermal balls was 13.8×10^{-6} [1/K], while the analogous mismatch near the perimeter balls was only 12×10^{-6} [1/K]. Also, due to the copper heat spreader thickness, the standoff between the package and the PCB was only 0.3 mm for the thermal balls, while it was 0.35 mm for the perimeter balls.

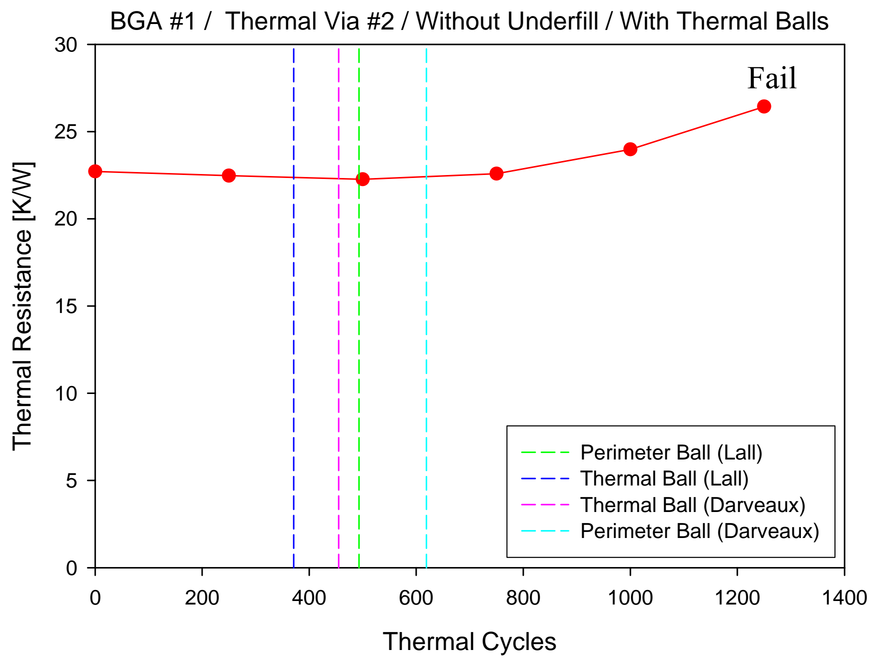


Figure 5.11 - Crack initiation prediction values superimposed on thermal resistance measurements for BGA packages with thermal balls

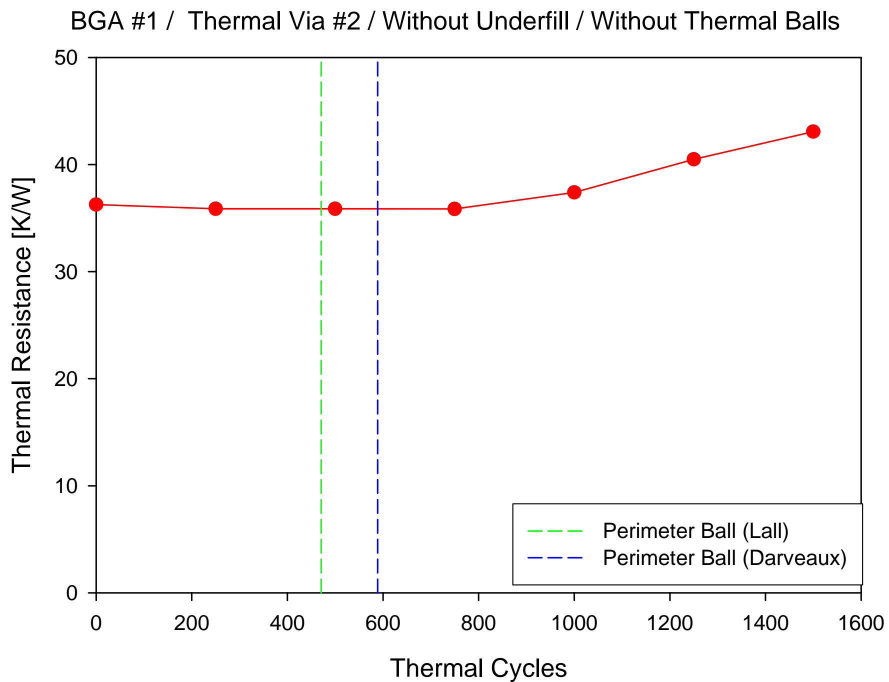


Figure 5.12 - Crack initiation prediction values superimposed on thermal resistance measurements for BGA packages without thermal balls

CHAPTER 6

EXPERIMENTAL THERMAL RESISTANCE MEASUREMENTS OF THIN ELECTRONIC PACKAGING MATERIALS

6.1 Motivation and Objective

Since the thermal properties of individual materials and sub assemblies used in manufacturing of ball grid array packages have a direct impact on the package overall performance, it is important to be able to accurately measure thermal resistance of such materials and sub assemblies. Conventional methods such as guarded hot plate method are not suitable to measure the thin electronic packaging materials [9, 32-34]. ASTM standard D5470-95 offers an alternative non-intrusive approach to measure thermal resistance of thin components used in electronic packaging. The suggested apparatus consists of two long metering blocks featuring equi-spaced holes for temperature sensors insertion. The first metering block (hot metering block) is heated by means of several electric heaters attached to one of its ends. The opposing end of the other metering block (cold metering block) is attached to a serpentine tube in which cooling fluid flows. The sample to be examined, which has a cross sectional area identical to that of the metering blocks, is placed in between the free ends of the two metering blocks and an axial

pressure of up to 3 MPa is applied on the assembly to minimize the effect of contact resistance between the sample and the metering blocks. The whole assembly is placed in vacuum to minimize heat loss to the environment.

6.2 Apparatus Theory of Operation

Heaters attached to the base of the hot metering block generate heat that flows through the hot metering block, the sample, the cold metering block and ultimately the cooling serpentine. The heat flow generates a temperature drop across the metering blocks and the sample. The temperature drop across the metering blocks is sensed using the temperature sensors embedded inside the metering blocks. By knowing the thermal conductivity of the metering block material and the temperature drop across any of the metering blocks, the heat flowing through the system may be calculated according to:

$$Q = k_m A_m \frac{\Delta T_m}{L_m} \qquad \text{(Eq. 6.1)}$$

where:

Q = Heat flowing through the system [W]

k_m = Thermal conductivity of metering blocks material [W/(m·K)]

A_m = Cross sectional area of metering blocks [m^2]

ΔT_m = Temperature drop across one of the metering blocks [K]

L_m = Length of metering block portion corresponding to the temperature drop [m]

The temperature drop across the thin sample is calculated by extrapolating temperature measurements in the cold and hot metering blocks to the sample lower and upper surfaces.

The thermal conductivity of the sample can then be calculated according to:

$$k_s = \frac{Q}{A_s}\frac{L_s}{\Delta T_s} \qquad \text{(Eq. 6.2)}$$

where:

k_s = Thermal conductivity of sample material [W/(m·K)]

Q = Heat flowing through the system [W]

A_s = Cross sectional area of sample [m^2]

ΔT_s = Temperature drop across sample [K]

L_s = Sample Thickness [m]

A schematic of the theory of operation for the apparatus is shown in Figure 6.1.

6.3 Apparatus Construction

The apparatus was constructed from aluminum alloy 2024-T3 material. It included a pneumatic actuator, capable of applying up to 2358 N of axial force, attached to the bottom of a base plate. The metering blocks and cooling serpentine were allowed to slide freely on four cylindrical guides mounted on the upper surface of a base plate. The sliding movement was restricted to a maximum of 25 mm which defined the maximum sample thickness. Compressive force from the actuator was transmitted to metering blocks through a rubber diaphragm that also acted as vacuum seal. The value of the axial force was measured using a load cell sandwiched between the serpentine and a stationary stopper. Water and electrical feedthrough connectors were attached to base plate to allow routing of cooling water, power and measurements signals to the vacuum environment.

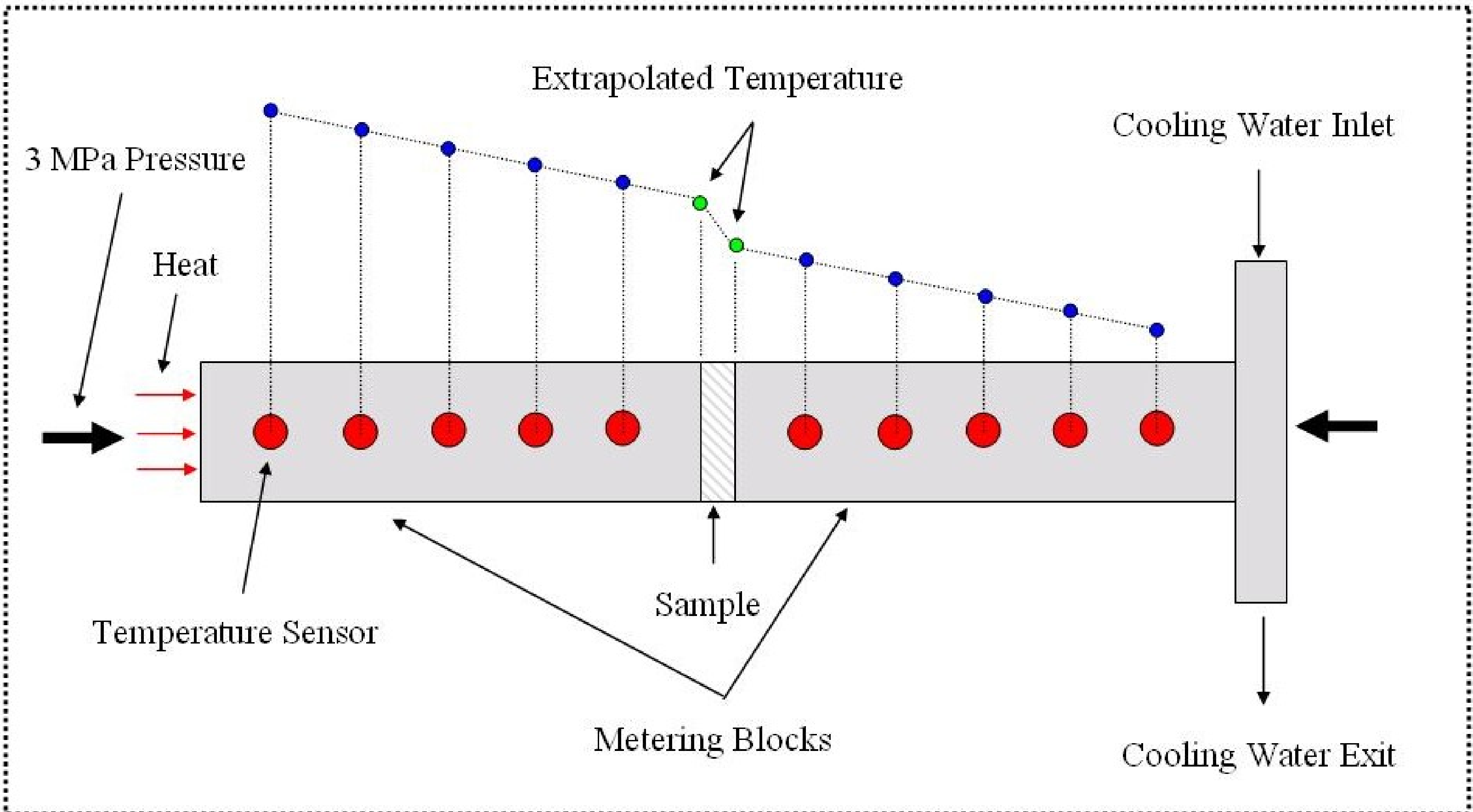


Figure 6.1 - Theory of operation of apparatus used to measure thermal resistance of thin components

The power feedthrough was equipped with 8 high voltage contact points while the instrumentation feed though was equipped with 55 contact points. The water feedthrough connected cooling water lines between a water chiller and the cooling serpentine to maintain the temperature at the upper surface of the cold metering block constant. The base plate was also equipped with a vacuum port connected to a vacuum pump; the vacuum line was outfitted with a vacuum venting valve to quickly vent the system to atmospheric pressure. A shallow groove was machined and polished on the top surface of the base plate to provide seating for the bell jar.

A 0.89 m high bell jar with a rubber sealing gasket attached to its bottom sat on the machined groove on the top surface of the base plate. The temperature sensors of choice were bare cylindrical 4 wire Resistance Temperature Detector, RTD, elements 1.5 mm in diameter and 25 mm long. A total of 10 RTDs (5 RTDs in the hot metering block and 5 RTDs in the cold metering block) were inserted in through holes drilled in the metering blocks, 10 mm apart. A solid model of the apparatus and an image of the apparatus after assembly are shown in Figures 6.2 and 6.3, respectively.

The RTDs were connected in series and excited with a 25 μA supplied from a National Instrument data acquisition board. The same board also measured voltage drop across every RTD and automatically converted electrical measurements into corresponding temperature value. Near the bottom of the hot metering block, four through holes arranged in a 2 by 2 matrix housed cylindrical cartridge heaters capable of a maximum output of 400 watts. The heaters were wired such that upper 2 heaters heated the metering blocks while the lower two heaters acted as guard heaters. Two extra RTDs

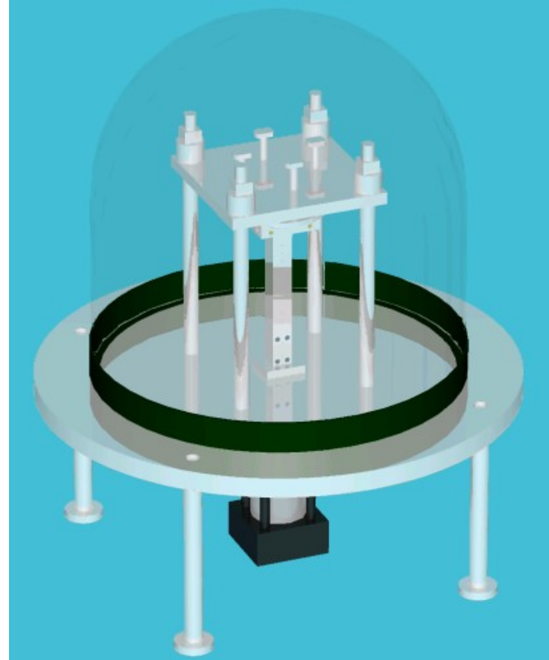


Figure 6.2 - Solid model of apparatus

Figure 6.3 - Apparatus after assembly

were placed in between the upper and lower rows of heaters to balance heat flow. Two zero voltage cross fired heater controllers regulated heat flow to upper and lower heaters independently. A 4 to 20 mA signal from a second National Instrument data acquisition and control board controlled the power output from the heater controllers. Another 4 to 20 mA signal controlled air pressure output from a pressure regulator that supplied air to the pneumatic actuator, thus controlling axial force applied on the metering blocks and the sample.

The data acquisition system also collected force readings from the load cell, vacuum pressure from a vacuum gauge fitted to the vacuum line and inlet and exit cooling water temperature from two NPT threaded RTDs mounted on cooling serpentine. Figure 6.4 shows details of components used in data acquisition and control.

Preliminary test runs revealed that the bare RTD elements are too fragile and can not be safely inserted into their designated holes in the metering blocks. They were especially vulnerable to fracture at the transition joint connecting the RTD element to the extension wires. To strengthen the transition joint, an aluminum sleeve was inserted to cover the joint and underfill material was dispensed to fill the tight clearance between the joint and the sleeve. The modification proved to be effective in eliminating transition joint fracture. Vacuum grade thermal grease was used to minimize contact resistance between the metering blocks and the RTD elements.

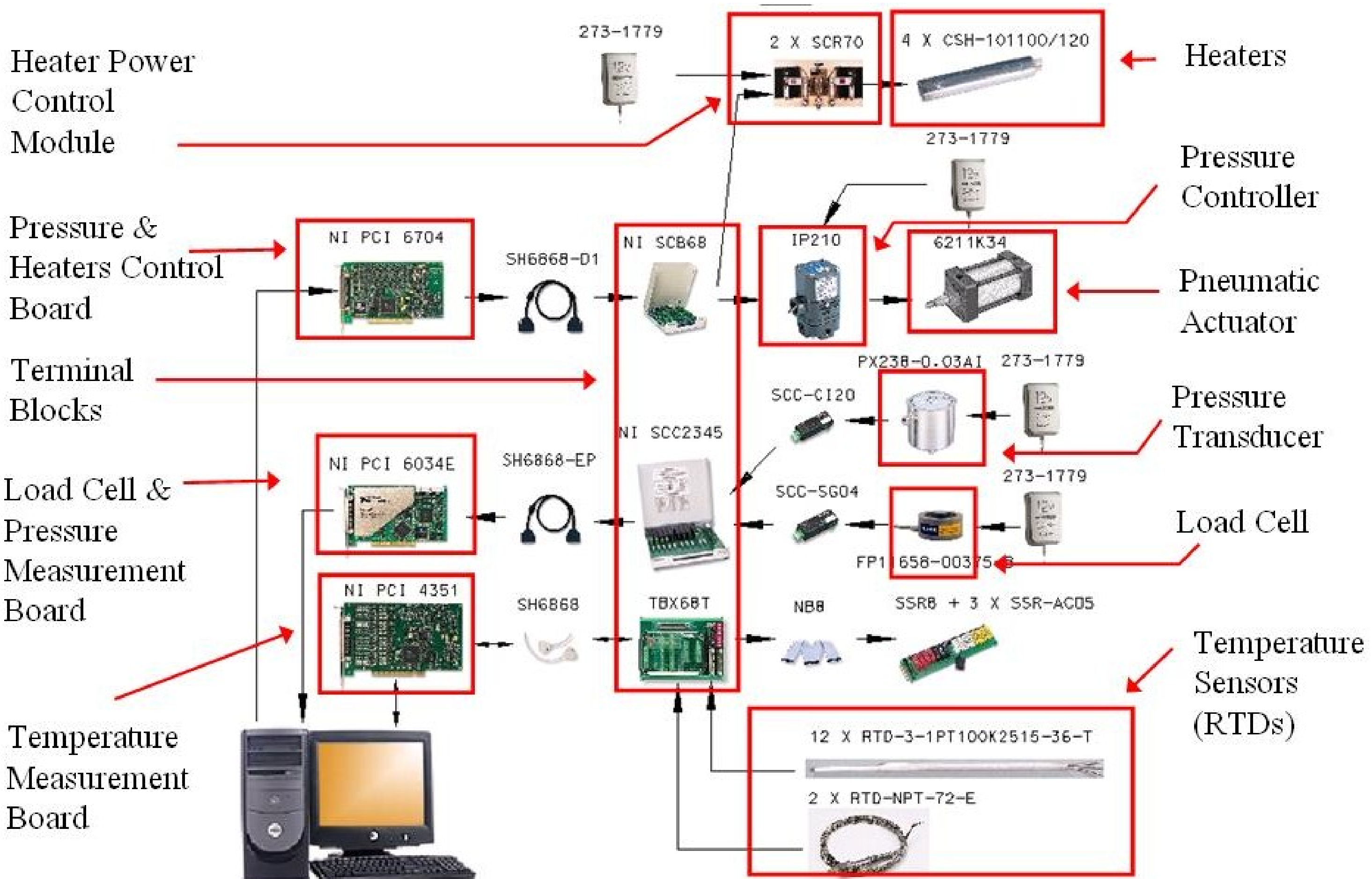


Figure 6.4 - Data acquisition and control diagram

6.4 Metering Blocks Calibration

Metering blocks thermal conductivity had to be accurately evaluated since heat flow and temperature gradient calculations depended on it. The metering blocks material had a nominal thermal conductivity of 121 [W/(m·K)]. To verify the accuracy of that value, the apparatus heaters were disconnected from the heater AC controllers and hooked to two DC power supplies. Each DC power supply powered one row of heaters.

The upper two heaters were used to heat the metering blocks while the other two lower heaters functioned as guard heaters. To begin the calibration process, the vacuum pump was started and pressure inside the bell jar was monitored until it fell below 3 mTorr. Then, by adjusting power output levels of the DC power supplies, a zero temperature difference was achieved between the two RTDs located between the upper and lower theaters sets. The zero temperature difference meant that all the heat generated in the upper heater sets would pass through the metering blocks towards the cooling serpentine. The values of upper heater's current and voltage drop were measured using a 6 digits multi-meter and the amount of heat generation was calculated according to:

$$Q = V \times I \qquad \text{(Eq. 6.3)}$$

where:

Q = Heat flowing through the system [W]

V = Voltage drop across the heaters [V]

I = Current flowing through the heaters [A]

Temperature measurements of the RTDs were recorded and fitted to a linear equation using least square error method. Using the best fit slope and heat flow values, the thermal conductivity of the metering blocks was calculated. The metering blocks

thermal conductivity was found to be 133 W/(m·K) which was higher than the documented value of 121 W/(m·K). Experimental measurements used for evaluating metering blocks thermal conductivity are listed in Table 6.1

6.5 Evaluation of Sample Contact Resistance

To evaluate the contact resistance between the sample and metering blocks, two 25 by 25 mm copper samples of 5 mm and 10 mm thickness were tested. Copper was selected as the sample material because it would be a good indicator of device measurement accuracy due to its low thermal resistance. Since both samples were of the same material and varied only in thickness, thermal resistance of the 10 mm sample should be double that of the 5 mm sample if thermal contact resistance was negligible. However, since thermal resistance is usually of considerable value, it can not be overlooked and needs to be evaluated.

The relation between the thermal resistances of the two samples can be written as:

$$R_{th_10mm} = 2R_{th_5mm} \qquad \text{(Eq. 6.4)}$$

where:

$$R_{th_10mm} + R_C = \frac{\Delta T_{10}}{Q_{10}} \qquad \text{(Eq. 6.5)}$$

$$R_{th_5mm} + R_C = \frac{\Delta T_5}{Q_5} \qquad \text{(Eq. 6.6)}$$

and where:

R_{th_10mm} = Thermal resistance of 10 mm sample

R_{th_5mm} = Thermal resistance of 5 mm sample

Table 6.1 - Measurements used to calculate thermal conductivity of metering blocks

Heater Voltage Drop	41.375 V
Heater Current	0.55562 A
Guard RTD #1	67.4 ºC
Guard RTD #2	67.4 ºC
Metering Block RTD #1	29.56 ºC
Metering Block RTD #2	32.37 ºC
Metering Block RTD #3	35.2 ºC
Metering Block RTD #4	37.92 ºC
Metering Block RTD #5	40.76 ºC
Best Fit Slope	279.56 ºC/m
Cross Sectional Area	625×10^{-6} m^2

R_C = Thermal contact resistance

ΔT_{10} = Measured temperature drop across 10 mm sample

ΔT_5 = Measured temperature drop across 5 mm sample

Q_{10} = Measured heat flow through 10 mm sample

Q_5 = Measured heat flow through 5 mm sample

Multiplying Eq. 6.6 by 2 gives

$$2R_{th_5mm} + 2R_C = 2\frac{\Delta T_5}{Q_5} \qquad \text{(Eq. 6.7)}$$

Substituting for $2R_{th_5mm}$ with R_{th_10mm}, Eq. 6.7 becomes

$$R_{th_10mm} + 2R_C = 2\frac{\Delta T_5}{Q_5} \qquad \text{(Eq. 6.8)}$$

Subtracting Eq. 6.5 from Eq. 6.8 yields:

$$R_C = 2\frac{\Delta T_5}{Q_5} - \frac{\Delta T_{10}}{Q_{10}} \qquad \text{(Eq. 6.9)}$$

By repeating measurements for the 10 mm and 5 mm samples under different axial loads, it was be possible to generate calibration curves that were used to account for contact resistance for different samples under different axial loads. The tests were preformed for both samples under vacuum less than 3 mTorr. The applied axial force varied from 890 to 3114 N with an approximate step size of 222 N. At every step the heat flow through the sample and temperature drop across the sample were calculated. The average sample temperature through the test was kept at 50 $\pm$ 0.1 ºC.

Measurements used to calculate thermal contact resistance are listed in Tables 6.2 and 6.3. Due to difference in calculated heat flow values between the cold and hot

Table 6.2 - Measurements used to calculate contact resistance (5 mm thick sample)

Force [N]	Q [W] Hot Block	Q [W] Cold Block	Q [W] Average	ΔT [K] Sample	Mean Sample Temperature [C]
890	27.02	27.32	27.17	4	50.02
1134	27.11	27.4	27.26	3.73	49.97
1357	27.1	27.52	27.31	3.64	50.04
1579	27.29	27.5	27.4	3.53	50
1802	27.44	27.61	27.53	3.45	50.05
2015	27.5	27.58	27.54	3.38	50.01
2282	27.38	27.74	27.56	3.29	50.06
2464	27.49	27.71	27.6	3.25	50.06
2691	27.46	27.78	27.62	3.19	50.05
2918	27.45	27.79	27.62	3.12	50.03
3114	27.72	27.9	27.81	3.05	50.05

Table 6.3 - Measurements used to calculate contact resistance (10 mm thick sample)

Force [N]	Q [W] Hot Block	Q [W] Cold Block	Q [W] Average	ΔT [K] Sample	Mean Sample Temperature [C]
890	26.88	27.21	27.05	4.18	50.03
1223	27.23	27.29	27.26	3.98	50.01
1348	27.07	27.41	27.24	3.92	50.03
1601	27.15	27.49	27.32	3.8	50.05
1788	27.34	27.48	27.41	3.75	50.05
2024	27.25	27.61	27.43	3.65	50.09
2251	27.32	27.61	27.47	3.6	50.06
2460	27.23	27.58	27.41	3.56	50.02
2673	27.23	27.55	27.39	3.53	50.04
2918	27.26	27.62	27.44	3.49	50.07
3132	27.13	27.66	27.4	3.44	50.07

metering blocks values, the average of the two metering blocks was used. However the at any given step, the mismatch between the two metering blocks did not exceed 2%. Thermal resistance versus axial force data was fitted with exponential equation of the form:

$$R_{th} = ae^{bF} + c \qquad \text{(Eq. 6.9)}$$

The correlation coefficients for the 5 mm sample were:

$a = 0.080158$ K/W $\qquad b = -6.750824E-4$ 1/N $\qquad c = 0.101625$ K/W

The correlation coefficients for the 10 mm sample were:

$a = 0.072374$ K/W $\qquad b = -8.731265E-4$ 1/N $\qquad c = 0.121281$ K/W

Measured $\frac{\Delta T}{Q}$ values and the corresponding best fit curves are shown in Figure 6.5. Substituting with best fit equations in Eq. 6.9

$$R_c = 2\left(0.080158\, e^{-6.750824\, E-4F} + 0.101625\right) - \left(0.072374\, e^{-8.731265\, E-4F} + 0.121281\right) \text{ K/W}$$

Rearranging:

$$R_c = 0.160316e^{-6.750824E-4F} - 0.072374e^{-8.731265E-4F} + 0.081969 \text{ K/W} \qquad \text{(Eq. 6.10)}$$

By taking the limit as the axial force goes to infinity, the amount of permanent contact resistance was calculated.

$$R_c = \lim_{F \to \infty} \left(0.160316e^{-6.750824E-4F} - 0.072374e^{-8.731265E-4F} + 0.081969\right) = 0.081969 \text{ K/W}$$

A plot of contact resistance versus axial force is shown in Figure 6.6. To calculate the thermal resistance of the 5mm sample, R_{th_10mm} was substituted with $2R_{th_5mm}$ in equation 6.5.

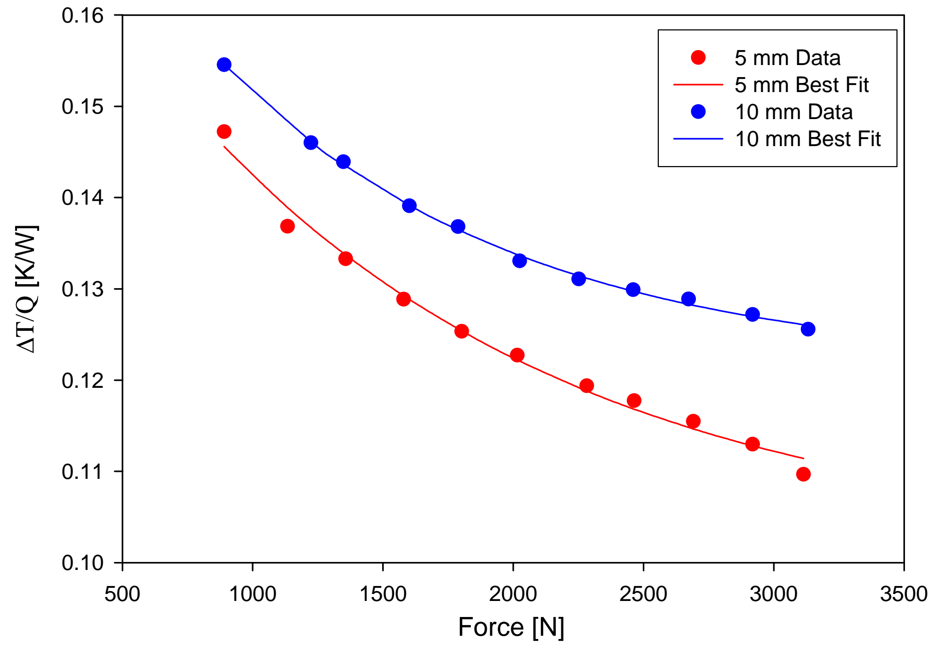


Figure 6.5 - Thermal resistance measurements of 5 and 10 mm copper samples

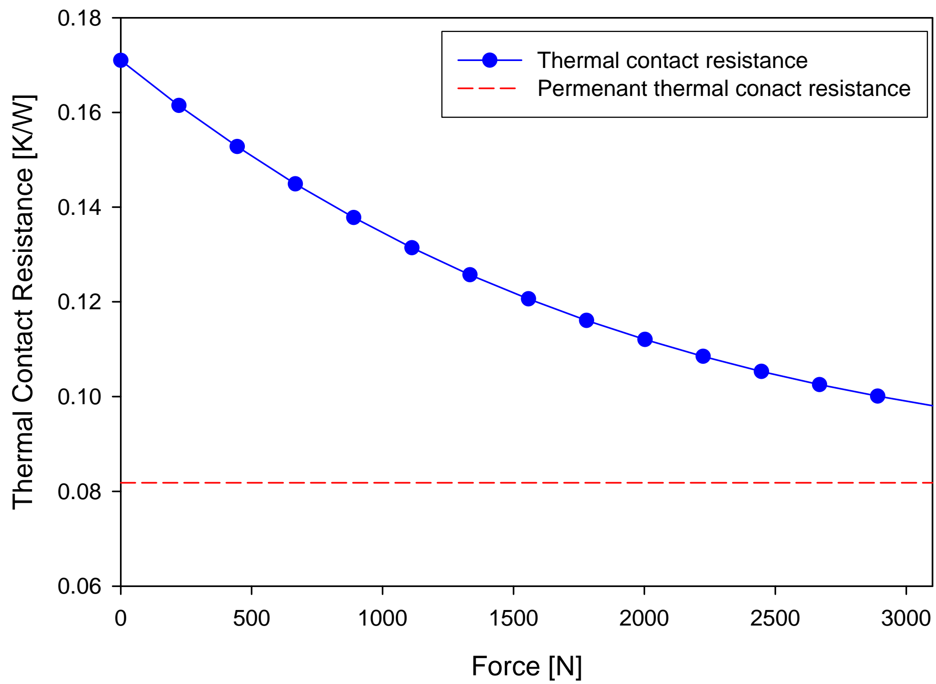


Figure 6.6 - Calculated contact resistance as a function of axial force

$$2R_{th_5mm} + R_C = \frac{\Delta T_{10}}{Q_{10}} \qquad \text{(Eq. 6.11)}$$

Subtracting Eq. 6.6 from Eq. 6.11 and taking the limit as the force goes to infinity yields:

$$R_{th_5mm} = \lim_{F\to\infty}\left(\left(0.072374e^{-8.731265E-4F} + 0.121281\right) - \left(0.080158e^{-6.750824E-4F} + 0.101625\right)\right)$$

$$R_{th_5mm} = 0.121281 - 0.101625 = 0.019656 \text{ K/W}$$

The conductivity of the copper material was calculated according to:

$$k = \frac{L_5}{AR_{th_5mm}} = \frac{5E-3}{(625E-6)(0.019656)} = 407 \text{ W/(m·K)}$$

The calculated conductivity of the copper material was 5.7% higher than the reference value of 385 W/(m·K). A heat flow of 30 W passing through a 5 mm thick sample with a 385 W/(m·K) thermal conductivity would cause a 0.62 ºC drop across the sample. The same heat flow passing through a similar sample with a 407 W/(m·K) thermal conductivity would cause a 0.59 ºC drop across the sample. That meant that the 5.7% thermal conductivity measurement discrepancy was equivalent to a temperature measurement error of only 0.03 ºC. It would be expected that measurement accuracy should improve significantly for samples whose thermal resistance are higher than that of copper sample.

6.6 Modification of Temperature Sensors.

Although bare RTD elements proved to be a good choice from measurement accuracy standpoint, they were extremely fragile. RTD elements needed to be replaced repeatedly to the extent that RTD fracturing imposed a serious impediment to practical use of the apparatus. RTD elements were fractured due to deformation of their respective

holes under axial force. It was clear that modifications of RTD element were needed in order to ensure continuous reliable performance of the apparatus.

The modifications had to satisfy several objectives. They were:

1. Provide protection to RTD elements.
2. Provide good contact between the sensor and the metering blocks
3. Overall thermal resistance of the sensor should be as close as possible to that of the metering blocks to maximize measurements accuracy.

Protection of RTD elements may be achieved by encasing them in metallic sheaths. A thin underfill layer would bond the RTD to the sheath as well as to function as a protective cushion for the RTD due to its relatively low stiffness. A solid model representation of proposed modifications is shown in Figure 6.7. By machining the outer diameter of the sheath to a slightly oversized dimension than that of the holes in the metering blocks, a tight fit and better contact would be achieved between the metering blocks and the sensors.

A 2-D half symmetry parametric finite element model was introduced that would help identify the optimum dimensions and sheath material that would satisfy the design requirements. The model was meshed with 18960 quad elements and 19609 nodes. Detail of the finite element model is shown in Figure 6.8. Material properties of RTD material was assumed to be that of 98% pure Alumina based on information supplied from the RTDs vendor. All material properties used were extracted from www.matewb.com, except for underfill material.

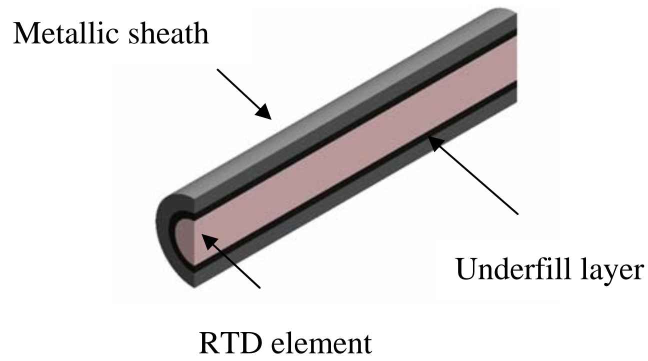


Figure 6.7 - Proposed modifications for bare RTD elements

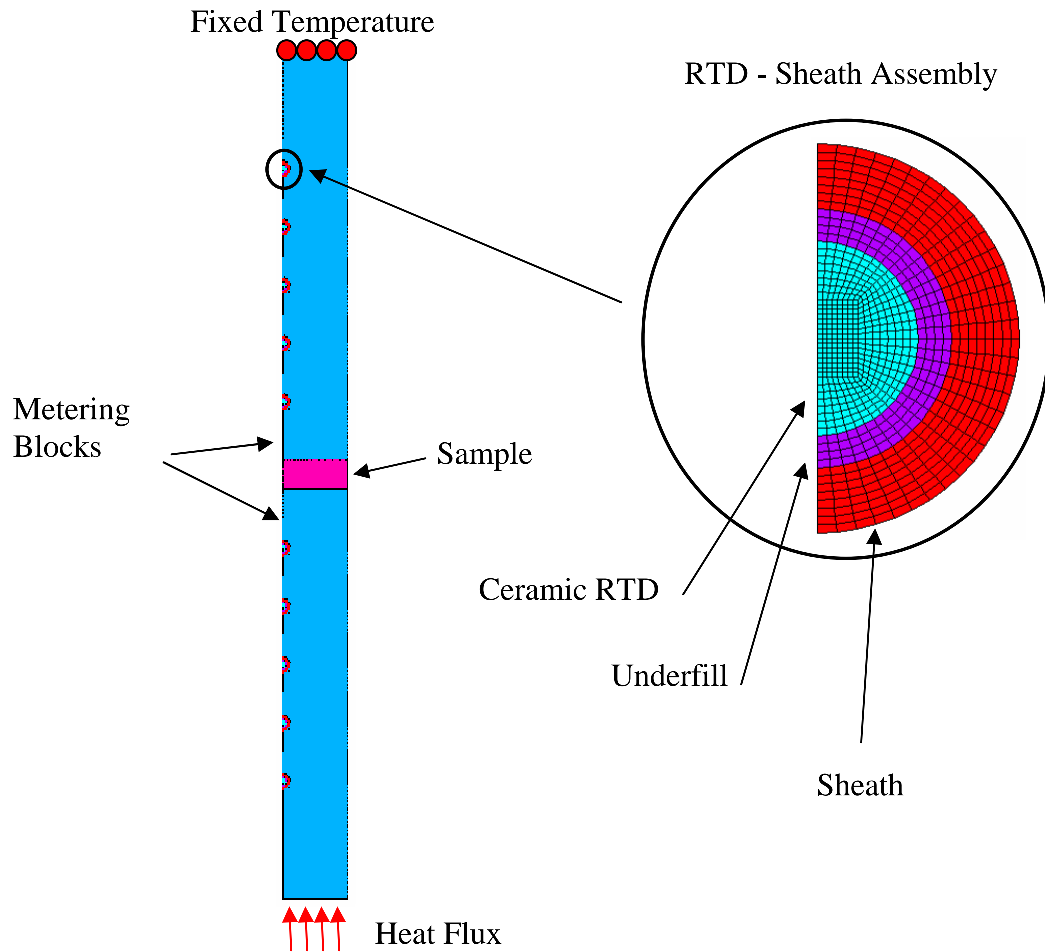


Figure 6.8 - Finite element model detail

The thermal conductivity and thermal expansion coefficient of the underfill were obtained from vendor data sheet; Young's modulus data was obtained from CAVE (Center for Advance Vehicle Electronics at Auburn University) testing data. Material properties used in finite element model are shown in Table 6.4.

An optimization analysis was preformed using the finite element model using the design variables sweep technique. Sheath material, sheath thickness, underfill thickness were used as the input variables for the optimization analysis. For every design variable a search range was defined. The search ranges were 0.5 to 385 W/(m·K), 0.1 to 2 mm and 0.25 to 0.5 mm for sheath thermal conductivity, sheath thickness, and underfill thickness respectively.

Using temperature distribution in RTD elements obtained from the finite element solution, sample thermal conductivity was calculated using the same approach used in experimental measurements. The objective function of the optimization analysis was set to minimize the difference between the calculated thermal conductivity of the sample and the actual value defined in the model.

The first design optimization run using aluminum as the metering block did not identify a practical choice for the sheath material that would satisfy design requirements. Optimization results indicated that sheath material thermal conductivity would need to be higher than 385 W/(m·K) (the set upper search limit of the optimization algorithm). That was due to the fact that aluminum had a relatively high thermal conductivity and the need for sheath material thermal conductivity to be higher than that of the metering blocks material to compensate for the low thermal conductivity of the ceramic RTD and the underfill layer. Rerunning the optimization analysis using stainless 304 for the metering

blocks material proved to be successful. Although stainless steel metering blocks would require higher heat flow to maintain the average sample temperature around 50 ºC, that should not be a problem for the 400 watts capacity of the apparatus heaters.

The optimization results were:

Underfill Thickness: 0.25 mm

Sheath Thickness: 0.52222 mm

Sheath Conductivity: 38 W/(m·K)

Conducting material property search in www.matweb.com for a thermal conductivity of 38 W/(m·K) revealed that the Toughmet alloy (77% Cu, 15% Ni, 8% Sn) had a thermal conductivity value of 38 W/(m·K) and good machinability. Since there would be a practical limit on the degree of accuracy to which the sheath thickness can be machined, the sheath thickness was selected to be 0.52 mm. Reviewing FEA results using the parameters values proposed by the optimization analysis confirmed that RTD elements were effectively sampling the correct temperature readings. For a sample of 5 mm thickness and 385 W/(m·K), the FEA model predicted a measurement of 387.75 W/(m·K) , an error of only 0.7%. Finite elements results showing temperature distribution in one of the RTDs is shown in Figure 6.9.

6.7 Structural Analysis of RTD Assembly

An interference fit would be the best solution to maintain good contact between the RTD assembly and the metering blocks. The assembly process would be conducted by heating the metering blocks and then inserting the oversized RTD assemblies. After cooling down, a compressive stress should guarantee permanent contact between the

Table 6.4 - Material properties used in finite element analysis

	Elastic Modulus GPa	Poisson's Ratio	Thermal Conductivity W/(m·K)	CTE 1/K
Ceramic	370E9	0.22	30 @ 20 ºC. 26 @ 100 ºC.	7.6×10^{-6}
Underfill	4.76@ 25 ºC. 4.29@ 50 ºC. 3.8@ 75 ºC. 3.11@ 100 ºC. 1.32@ 125 ºC.	0.3	0.38	35×10^{-6}
Metering Blocks	195	0.29	16.2 @ 0 to100 ºC 21.5 @ 500 ºC	17.3×10^{-6}

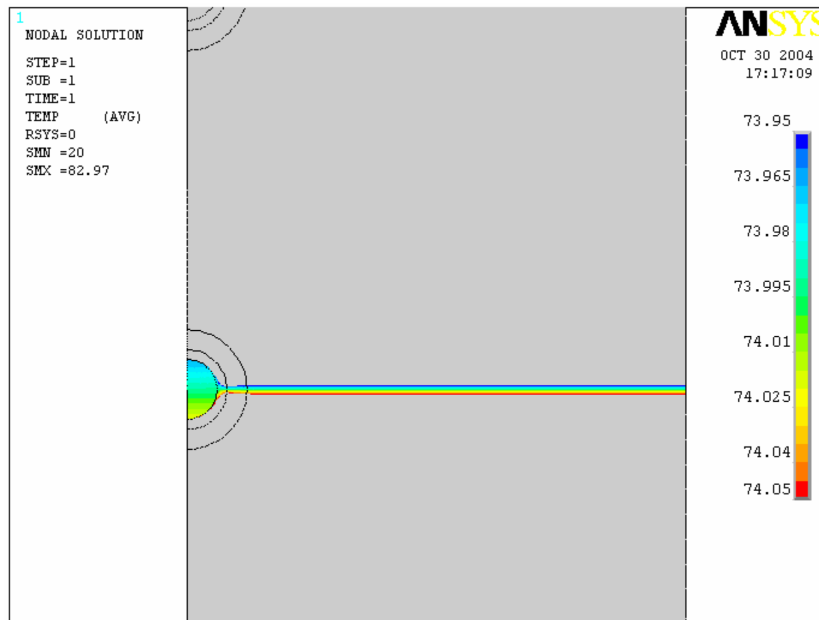


Figure 6.9 - Temperature distribution in RTD and metering block

(Model Parts in gray color are outside the legend temperature limits)

RTD assemblies and the metering block. The challenge would be to select the amount of interference required to enforce contact while not loading the RTD elements with high stress values that might cause fracture during the assembly process.

To investigate the accepted level of interference, a structural analysis was conducted by changing element types from thermal to structural in the thermal FEA model. To simulate the interference fit between the sheath and metering blocks, a free stress state was modeled while maintaining metering blocks temperature at 200 ºC and 20 ºC for the RTD assemblies. The metering blocks were then loaded with a temperature of 20 ºC. The effect of the cooling process was checked and found to be equivalent to a 10 micron interference fit.

The associated maximum compressive stress in the RTD element was found to be 72 MPa. The maximum allowable compressive stress listed in www.mateb.com was 2700 MPa, which indicated that stress levels associated with the assembly process should not cause fracture of the RTD elements. Third principal stress distribution in RTD assembly is shown in Figure 6.10. To simulate the net effect of metering blocks holes expansion and interference fit on the contact status while taking experimental measurements, the structural model was subsequently loaded with the temperature profile obtained from the thermal run as well as an axial load of 3 MPa.

Simulation results indicate that RTD assembly would maintain contact with the metering blocks under a 148 MPa compressive stress during experimental measurements. Radial stress distribution during experimental measurements is shown in Figure 6.11.

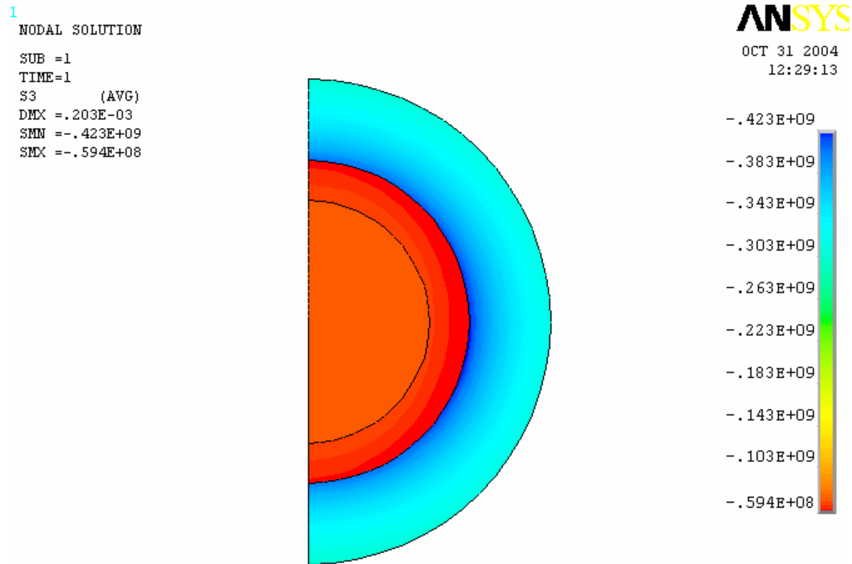


Figure 6.10 - Third principal stress in RTD assembly during assembly

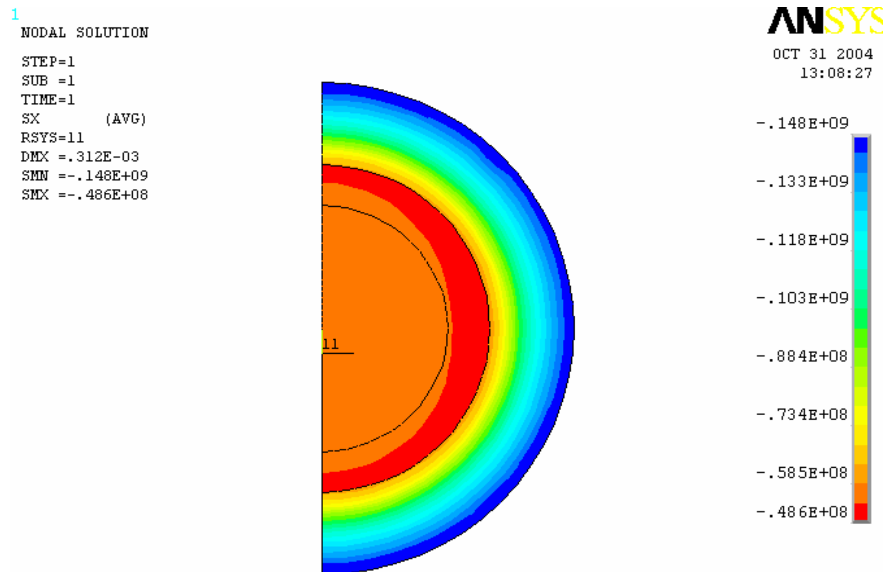


Figure 6.11 - Radial Stress in RTD assembly during experimental measurements

CHAPTER 7

SUMMARY AND CONCLUSION

A new automated system for measuring thermal resistance of plastic Ball Grid Array packages was built. The system used P-N diodes integrated into die surface as temperature sensor devices. The new system included a special module for calibration of the temperature sensing diodes. The automated system was capable of conducting calibration, experimental measurement and report generation with minimal user interaction. The testing apparatus used a stream of water from a water chiller to maintain the back surface of test boards at a constant temperature. The cooling water temperature was continuously monitored using K type thermocouples. Thermal resistance measurements were conducted by heating the die surface using surface heaters integrated into test packages die surface and recording die surface temperature, cooling water temperature and heater power at steady state condition.

Using the mentioned system, the impact of several package, board and assembly parameters on thermal performance was investigated. The investigated parameters were use of underfill, use of thermal balls, die size, number of perimeter balls and thermal via geometry. For every test parameters combination, 4 identical packages were tested. The test samples included packages underfilled with three different types of underfill.

Other tested packages were not underfilled to be used as basis of comparison. Evaluation of the effect of using thermal balls was preformed by removing all 16 thermal balls from some of the package and comparing their thermal performance to similar packages with thermal balls. The effect of die size and number of number of perimeter balls was quantified by testing two different packages with different die size and different number of perimeter balls. Two different thermal vias were fabricated into test boards and their impact on thermal performance was evaluated. Thermal via type #1 was fabricated as a set of intersecting copper traces while thermal via type two was fabricated as a solid square copper slab. Both designs connected thermal balls to a set of plated trough holes which were in turn connected to copper ground plane buried inside the PCB. The test matrix consisted of 32 test boards and 96 packages.

Experimental measurements proved that using underfill can significantly reduce thermal resistance. A drop of thermal resistance between 8% and 45% was observed due to the use of underfill depending on package configuration. Removal of thermal balls caused an increase in thermal resistance as low as 12% and as high as 85% depending on package configuration. Packages with larger die size constantly exhibited better thermal performance. Packages fitted with the smaller die showed up to 37% higher thermal resistance than packages fitted with the larger die. That may be attributed to the fact that large dies had more than double the projected surface area of the smaller dies.

Packages fitted with the small dies had more 48 perimeter balls than the packages fitted with the large dies which meant a 33% increase in the cross sectional area of perimeter balls. However that extra area of the relatively high conductive solder did not help to enhance thermal performance to match that of the packages fitted with the large

dies, which may attributed to the relatively remote distance of the perimeter balls from the die where heat was generated.

The solid copper slab design proved to be better than the intersected copper traces design. Packages mounted on the solid copper thermal vias had up to 9% less thermal resistance when compared to similar packages mounted on the intersected copper traces thermal vias. The best thermal performance was observed in package that had the large dies, had underfill, had thermal balls and were mounted on the solid copper slab via. Thermal performance of packages with the smaller die was more sensitive to the use of thermal balls than the use of underfill. The converse was true for package fitted with the large dies.

After performing thermal resistance measurements for all packages, they were placed in an oven and thermally cycled between -40 and 125 ºC to investigate the impact of thermal cycling on thermal resistance. The oven cycle duration was 90 minutes. Thermal cycles consisted of 15 minute ramps and 30 minutes dwells at the lower and upper temperature extremes.

The first 500 thermal cycles revealed no noticeable change in thermal performance for all BGA Packages. Major changes appeared at 750 cycles for BGA #1 with no underfill/with thermal balls as a continuous gradual increase of thermal resistance. At 1250 thermal cycles thermal resistance increased from for 23.9 K/W at 0 cycles to 30.5 K/W (28% increase) for BGA #1/Via #1. Similarly, for BGA #1/Via #2 thermal resistance increased from for 22.7 K/W at 0 cycles to 26.4 K/W (16% increase). After 1250 cycles most diodes and heaters have failed for that package type. This early failure was expected due to no use of underfill as well as the large die size of BGA #1.

After 750 cycles BGA #1 with no underfill and no thermal balls started showing a continuous increase of thermal resistance from for 36.3 K/W at 0 cycles to 43.1 K/W (19% increase).

Thermal finite element simulation model for transient and steady state conditions were introduced to help understand heat flow patterns inside BGA packages. Finite element models were created using auto meshing of solid models of different packages. A total of 16 different models were created covering every study parameters combination. Simulation results were in agreement with experimental measurements. The difference between simulation results and experimental measurement varied between 0% and 12%. Transient numerical simulation models proved that packages with the least thermal resistance would be the first to reach steady state condition by up to 25 seconds.

Correlation between solder joints cracking due to thermal cycling and degradation of thermal performance was investigated with the help of structural numerical simulation. A fully parameterized BGA finite element model was developed using Ansys parametric development language (APDL) which helped cut down model generation time from days to less than one hour. The structural model predicted the number of thermal cycles to crack initiation in solder balls under thermal cycling loads. The predicted number of thermal cycles was in the vicinity of the number of thermal cycles where an increase of thermal resistance was observed experimentally.

A new apparatus for measuring thin components used in electronic packaging was designed, manufactured and tested. The apparatus was designed according to ASTM standard D5470-95 guidelines. Measurements were performed by inserting thin samples of 25 x 25mm cross-section between long slender metering blocks of similar cross

section. The metering blocks were made from Aluminum 2024-T3. One of the free ends of the metering blocks was heated using a set of cartridge heaters while the opposite free end on the second metering block was cooled using a serpentine drawing water from a water chiller. Five bare RTDs (Resistance temperature detector) were inserted in equi-spaced through holes in the hot metering block. The cold metering block was fitted with a similar number of RTDs. Axial force from a pneumatic actuator was applied on the metering blocks and the sample sandwiched between them to minimize contact resistance. The amount of axial force applied was measured using an inline load cell. Temperature measurements were performed in a vacuum environment of less than 3 mTorr to minimize heat loss to the environment. The testing process was fully automated from a PC through a set of data acquisition and control boards.

Thermal conductivity of the metering blocks was checked using 2 DC power supplies to power the cartridge heaters and was found to be 133 W/(m·K). The amount of power supplied from the heaters was calculated by measuring temperature distribution of the metering blocks using the RTDs. Temperature of the upper and lower sample surfaces were calculated by linear extrapolation of the metering blocks temperatures.

By conducting measurements on 2 copper samples of 5 mm and 10 mm, the relation between the applied axial force and contact resistance between the sample and the metering blocks was established. The contact resistance was found to be of the form:

$$R_C = 0.16029e^{-2.996004E-3F} - 0.072434e^{-3.891367E-3F} + 0.08183$$

Thermal conductivity of the copper samples was also calculated and found to be 405.2 W/(m·K), which was 5.2% more than the reference value of 385 W/(m·K). The thermal conductivity measurement error was equivalent to a temperature measurement

error of 0.0311. It would be expected that higher accuracy of thermal conductivity measurement would be achieved for samples with less thermal conductivity than copper.

Although bare RTD elements provided accurate temperature measurement, their fragility was an obstacle to continual use of the apparatus. A proposed modification that would help protect the RTD elements was introduced. The propose modification would shield the RTD element with a metal sheath, bonding between the RTD element and the sheath would be achieved by using a thin underfill layer. A thermal numerical optimization simulation was preformed to select the optimum dimensions and sheath material that would maximize measurement accuracy. No possible solution was found for the aluminum metering blocks. Rerunning the analysis for a stainless steel metering blocks proved to be successful. The optimum dimensions were 0.25 mm for the underfill layer thickness and 0.52 mm for the metallic sheath thickness. The analysis was also solved for the thermal conductivity of the sheath material and was found to be 38 W/mK.

A material property search was conducted to find such material. The Toughmet alloy (77% Cu, 15% Ni, 8% Sn) was found to have a thermal conductivity of 38 W/mK and good machinability. A structural analysis was also preformed to investigate the possibility of using interference fit between the new RTD assembly and the metering blocks to enhance contact between the RTD assembly and the metering blocks. Simulation results indicated that 10 micron interference fit between the RTD assembly and metering blocks should maintain good contact between the RTD assembly and the metering block. Simulation results also indicated the compressive stresses associated with the interference fit were not expected to cause fracture of the RTD elements.

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APPENDIX A

Sample Diode Calibration Report

Diode calibration for Board No. 1
Test started on Aug 9/02 - 02:13
Start temperature: 30 [C] End temperature: 50 [C]
Step: 5 [C] Dwell: 10 [Sec.] Current: 500 [U Amp.]
Diode coefficients:
-1.704E-03
.747191
-1.699E-03
.746975
-1.702E-03
.747118
-1.755E-03
.738808
-1.711E-03
.745888
-1.709E-03
.745753
-1.709E-03
.745768
-1.739E-03
.735667
Test Details:

Temp.	Diode #1	Diode #2	Diode #3	Diode #4	Diode #5	Diode #6	Diode #7	Diode #8
30.1	.747191	.746975	.747118	.738808	.745888	.745753	.745768	.735667
35.1	.738844	.738696	.738794	.730021	.737464	.737362	.737367	.727151
40	.730445	.730315	.730422	.721392	.729022	.728925	.728916	.71857
45	.721948	.721841	.721916	.712714	.720498	.720412	.720399	.709919
50.1	.713118	.713005	.713093	.703682	.711686	.711598	.711614	.70095

Calibration ended successfully on Aug 9 02 02:33

APPENDIX B

Sample Thermal Resistance Report

Thermal BGA Test Results - Board No. 1

Test Started on 08 27 02 - 16 53

Sampling Points: 8

Max Standard Deviation: .01

Test Packages: BGA#1_1, BGA#2_1, BGA#2_2, BGA#1_2

BGA#1_1 Package Data:

Underfill: #1

Power Start: 0.1 [W]

Power Step: 0.1 [W]

Power End: 1 [W]

Fractured Balls: None

BGA#1_1 Test Started on 08 27 02 - 16 53

BGA#1_1 Test Data

Set Power [W]	T1 [ºC]	T2 [ºC]	T3 [ºC]	Cooling Temperature [ºC]	Actual Power [W]	Standard Deviation [ºC]	Thermal Resistance [K/W]
0.1	23.71	23.93	24.29	23.57	0.101	N/A	N/A
0.1	24.96	24.9	25.08	23.5	0.101	N/A	N/A
0.1	25.34	25.24	25.39	23.58	0.101	N/A	N/A
0.1	25.54	25.43	25.57	23.56	0.101	N/A	N/A
0.1	25.65	25.52	25.65	23.56	0.101	N/A	N/A
0.1	25.71	25.58	25.71	23.53	0.101	N/A	N/A
0.1	25.75	25.62	25.75	23.53	0.101	N/A	N/A
0.1	25.77	25.64	25.76	23.51	0.101	0.60	N/A
0.1	25.79	25.66	25.76	23.55	0.101	0.26	N/A
0.1	25.8	25.66	25.78	23.94	0.101	0.15	N/A
0.1	25.8	25.67	25.79	23.53	0.101	0.09	N/A

0.1	25.8	25.67	25.77	23.53	0.101	0.05	N/A
0.1	25.81	25.68	25.77	23.54	0.101	0.03	N/A
0.1	25.8	25.65	25.79	23.55	0.101	0.02	N/A
0.1	25.81	25.67	25.79	23.52	0.101	0.01	22.03
0.2	26.18	26.39	26.78	23.47	0.208	N/A	N/A
0.2	27.51	27.41	27.63	23.51	0.203	N/A	N/A
0.2	27.88	27.75	27.93	23.5	0.203	N/A	N/A
0.2	28.06	27.92	28.08	23.59	0.203	N/A	N/A
0.2	28.18	28.04	28.19	23.51	0.203	N/A	N/A
0.2	28.23	28.08	28.23	23.55	0.203	N/A	N/A
0.2	28.28	28.12	28.26	23.51	0.203	N/A	N/A
0.2	28.3	28.15	28.29	23.54	0.203	0.61	N/A
0.2	28.31	28.15	28.32	23.54	0.203	0.26	N/A
0.2	28.32	28.17	28.31	23.57	0.203	0.15	N/A
0.2	28.34	28.17	28.32	23.55	0.203	0.09	N/A
0.2	28.35	28.19	28.32	23.52	0.203	0.06	N/A
0.2	28.35	28.18	28.32	23.49	0.203	0.04	N/A
0.2	28.34	28.19	28.33	23.52	0.203	0.02	N/A
0.2	28.35	28.18	28.32	23.48	0.203	0.01	N/A
0.2	28.35	28.18	28.32	23.57	0.203	0.01	23.22
0.3	28.69	28.87	29.29	23.53	0.305	N/A	N/A
0.3	30.04	29.93	30.17	23.48	0.305	N/A	N/A
0.3	30.45	30.31	30.51	23.49	0.306	N/A	N/A
0.3	30.66	30.5	30.69	23.49	0.306	N/A	N/A
0.3	30.77	30.61	30.79	23.55	0.306	N/A	N/A
0.3	30.86	30.68	30.83	23.52	0.306	N/A	N/A
0.3	30.9	30.7	30.88	23.5	0.306	N/A	N/A
0.3	30.92	30.74	30.9	23.56	0.306	0.65	N/A
0.3	30.94	30.75	30.92	23.47	0.306	0.28	N/A
0.3	30.95	30.75	30.92	23.5	0.306	0.16	N/A
0.3	30.95	30.75	30.92	23.48	0.306	0.09	N/A
0.3	30.94	30.75	30.92	23.49	0.306	0.05	N/A
0.3	30.95	30.76	30.93	23.54	0.306	0.03	N/A
0.3	30.96	30.76	30.93	23.51	0.306	0.02	N/A
0.3	30.96	30.78	30.94	23.54	0.306	0.01	N/A
0.3	30.95	30.77	30.94	23.56	0.306	0.01	23.96

0.4	31.3	31.41	31.83	23.5	0.403	N/A	N/A
0.4	32.53	32.4	32.63	23.52	0.404	N/A	N/A
0.4	32.92	32.73	32.96	23.77	0.404	N/A	N/A
0.4	33.15	33.05	33.13	23.98	0.404	N/A	N/A
0.4	33.26	33.16	33.23	23.53	0.404	N/A	N/A
0.4	33.28	33.08	33.27	23.54	0.404	N/A	N/A
0.4	33.32	33.1	33.3	23.47	0.404	N/A	N/A
0.4	33.34	33.13	33.34	23.52	0.404	0.61	N/A
0.4	33.35	33.14	33.33	23.54	0.404	0.27	N/A
0.4	33.37	33.16	33.35	23.55	0.404	0.14	N/A
0.4	33.38	33.16	33.35	23.5	0.404	0.06	N/A
0.4	33.38	33.17	33.36	23.49	0.404	0.04	N/A
0.4	33.38	33.16	33.35	23.51	0.404	0.03	N/A
0.4	33.39	33.17	33.36	23.49	0.404	0.02	N/A
0.4	33.39	33.17	33.36	23.48	0.404	0.01	N/A
0.4	33.39	33.18	33.36	23.51	0.404	0.01	24.23
0.5	33.74	33.86	34.33	23.5	0.505	N/A	N/A
0.5	35.06	34.91	35.17	23.49	0.506	N/A	N/A
0.5	35.47	35.28	35.52	23.47	0.506	N/A	N/A
0.5	35.67	35.46	35.85	23.54	0.506	N/A	N/A
0.5	35.8	35.58	35.81	23.5	0.506	N/A	N/A
0.5	35.86	35.64	35.86	23.57	0.506	N/A	N/A
0.5	35.92	35.68	35.9	23.48	0.506	N/A	N/A
0.5	35.95	35.7	35.92	23.48	0.506	0.64	N/A
0.5	35.96	35.72	35.93	23.47	0.506	0.28	N/A
0.5	35.97	35.73	35.95	23.48	0.506	0.15	N/A
0.5	35.97	35.74	35.94	23.53	0.506	0.08	N/A
0.5	35.98	35.74	35.95	23.49	0.506	0.06	N/A
0.5	35.98	35.74	35.95	23.5	0.506	0.04	N/A
0.5	35.98	35.74	35.96	23.5	0.506	0.02	N/A
0.5	35.98	35.75	35.96	23.55	0.506	0.02	N/A
0.5	35.99	35.76	35.96	23.54	0.506	0.01	N/A
0.5	36	35.75	35.97	23.5	0.506	0.01	N/A
0.5	36	35.76	35.97	23.5	0.506	0.01	N/A
0.5	36	35.77	35.98	23.52	0.506	0.01	24.48
0.6	36.37	36.46	36.96	23.52	0.610	N/A	N/A

0.6	37.68	37.47	37.76	23.5	0.601	N/A	N/A
0.6	37.99	37.75	38.02	23.48	0.602	N/A	N/A
0.6	38.17	37.93	38.17	23.55	0.602	N/A	N/A
0.6	38.27	38.02	38.25	23.53	0.602	N/A	N/A
0.6	38.34	38.08	38.31	23.5	0.602	N/A	N/A
0.6	38.37	38.11	38.36	23.49	0.602	N/A	N/A
0.6	38.39	38.14	38.38	23.5	0.602	0.57	N/A
0.6	38.4	38.14	38.38	23.49	0.602	0.23	N/A
0.6	38.41	38.16	38.4	23.48	0.602	0.14	N/A
0.6	38.42	38.15	38.39	23.49	0.602	0.08	N/A
0.6	38.42	38.15	38.39	23.49	0.602	0.05	N/A
0.6	38.41	38.16	38.4	23.54	0.602	0.03	N/A
0.6	38.42	38.16	38.4	23.48	0.602	0.02	N/A
0.6	38.43	38.16	38.4	23.47	0.602	0.01	24.67
0.7	38.79	38.86	39.38	23.47	0.709	N/A	N/A
0.7	40.14	39.94	40.28	23.52	0.710	N/A	N/A
0.7	40.56	40.32	40.63	23.52	0.711	N/A	N/A
0.7	40.79	40.52	40.81	23.49	0.711	N/A	N/A
0.7	40.91	40.64	40.92	23.52	0.711	N/A	N/A
0.7	40.99	40.71	40.99	23.51	0.711	N/A	N/A
0.7	41.03	40.74	41.02	23.47	0.711	N/A	N/A
0.7	41.06	40.78	41.03	23.52	0.712	0.66	N/A
0.7	41.07	40.79	41.07	23.53	0.712	0.30	N/A
0.7	41.09	40.81	41.06	23.52	0.712	0.17	N/A
0.7	41.1	40.8	41.08	23.47	0.712	0.10	N/A
0.7	41.1	40.8	41.08	23.55	0.712	0.06	N/A
0.7	41.11	40.83	41.08	23.51	0.712	0.04	N/A
0.7	41.11	40.82	41.09	23.56	0.712	0.03	N/A
0.7	41.12	40.83	41.1	23.49	0.712	0.02	N/A
0.7	41.12	40.82	41.1	23.52	0.712	0.01	N/A
0.7	41.11	40.81	41.09	23.52	0.712	0.01	24.58
0.8	41.47	41.51	42.07	23.48	0.814	N/A	N/A
0.8	42.76	42.5	42.85	23.54	0.804	N/A	N/A
0.8	43.06	42.78	43.1	23.47	0.805	N/A	N/A
0.8	43.23	42.93	43.25	23.5	0.805	N/A	N/A
0.8	43.34	43.02	43.33	23.46	0.805	N/A	N/A

0.8	43.39	43.08	43.38	23.5	0.805	N/A	N/A
0.8	43.43	43.12	43.43	23.5	0.805	N/A	N/A
0.8	43.46	43.15	43.45	23.48	0.805	0.56	N/A
0.8	43.47	43.16	43.46	23.51	0.805	0.23	N/A
0.8	43.48	43.16	43.58	23.55	0.805	0.14	N/A
0.8	43.48	43.17	43.45	23.52	0.805	0.09	N/A
0.8	43.48	43.17	43.47	23.56	0.805	0.06	N/A
0.8	43.5	43.18	43.48	23.49	0.805	0.04	N/A
0.8	43.51	43.19	43.49	23.5	0.805	0.03	N/A
0.8	43.51	43.2	43.48	23.54	0.805	0.02	N/A
0.8	43.51	43.18	43.48	23.51	0.805	0.02	N/A
0.8	43.52	43.2	43.5	23.52	0.805	0.01	N/A
0.8	43.52	43.19	43.49	23.5	0.805	0.01	N/A
0.8	43.52	43.21	43.48	23.49	0.805	0.01	24.72
0.9	43.84	43.84	44.41	23.55	0.903	N/A	N/A
0.9	45.13	44.86	45.26	23.49	0.904	N/A	N/A
0.9	45.53	45.22	45.59	23.55	0.905	N/A	N/A
0.9	45.75	45.41	45.76	23.49	0.905	N/A	N/A
0.9	45.86	45.52	45.88	23.56	0.905	N/A	N/A
0.9	45.94	45.6	45.94	23.52	0.905	N/A	N/A
0.9	45.98	45.64	45.99	23.52	0.905	N/A	N/A
0.9	46.02	45.68	46.01	23.51	0.905	0.63	N/A
0.9	46.04	45.7	46.03	23.53	0.905	0.29	N/A
0.9	46.04	45.7	46.03	23.51	0.905	0.17	N/A
0.9	46.05	45.71	46.04	23.57	0.905	0.10	N/A
0.9	46.06	45.72	46.05	23.5	0.905	0.07	N/A
0.9	46.06	45.72	46.05	23.51	0.905	0.04	N/A
0.9	46.07	45.72	46.05	23.51	0.905	0.03	N/A
0.9	46.07	45.73	46.06	23.54	0.905	0.02	N/A
0.9	46.07	45.72	46.06	23.49	0.905	0.01	N/A
0.9	46.07	45.73	46.06	23.54	0.905	0.01	24.76
1	46.43	46.42	47.02	23.51	1.015	N/A	N/A
1	47.78	47.5	47.94	23.58	1.016	N/A	N/A
1	48.23	47.89	48.29	23.53	1.017	N/A	N/A
1	48.41	48.01	48.39	23.53	1.005	N/A	N/A
1	48.43	48.1	48.47	23.51	1.017	N/A	N/A

1	48.58	48.16	48.51	23.48	1.005	N/A	N/A
1	48.49	48.12	48.45	23.55	1.005	N/A	N/A
1	48.47	48.1	48.46	23.56	1.005	0.61	N/A
1	48.49	48.11	48.47	23.5	1.005	0.22	N/A
1	48.48	48.1	48.46	23.56	1.005	0.08	N/A
1	48.48	48.11	48.47	23.54	1.005	0.04	N/A
1	48.47	48.1	48.46	23.57	1.005	0.03	N/A
1	48.49	48.11	48.44	23.54	1.005	0.02	N/A
1	48.49	48.11	48.47	23.53	1.005	0.01	24.70

BGA#1_1 Thermal Resistance = 25.0891 [K/W]

BGA#1_1 Test Ended on 08 27 02 - 17 07

BGA#2_1 Package Data:

Underfill: #1

Power Start: .1 [W]

Power Step: .1 [W]

Power End: 1 [W]

Fractured Balls: None

BGA#2_1 Test Started on 08 27 02 - 17 07

BGA#2_1 Test Data:

Set Power [W]	T1 [ºC]	Cooling Temperature [ºC]	Actual Power [W]	Standard Deviation [ºC]	Thermal Resistance [K/W]
0.1	25.78	23.46	0.098	N/A	N/A
0.1	26.87	23.46	0.103	N/A	N/A
0.1	27.19	23.5	0.103	N/A	N/A

0.1	27.31	23.42	0.103	N/A	N/A
0.1	27.38	23.44	0.103	N/A	N/A
0.1	27.42	23.44	0.103	N/A	N/A
0.1	27.45	23.47	0.103	N/A	N/A
0.1	27.47	23.45	0.103	0.57	N/A
0.1	27.48	23.43	0.103	0.21	N/A
0.1	27.48	23.46	0.103	0.10	N/A
0.1	27.49	23.46	0.103	0.06	N/A
0.1	27.5	23.46	0.103	0.04	N/A
0.1	27.5	23.46	0.103	0.03	N/A
0.1	27.5	23.45	0.103	0.02	N/A
0.1	27.5	23.45	0.103	0.01	N/A
0.1	27.5	23.5	0.103	0.01	38.80
0.2	28.4	23.45	0.207	N/A	N/A
0.2	29.65	23.47	0.207	N/A	N/A
0.2	29.93	23.49	0.207	N/A	N/A
0.2	30.05	23.49	0.207	N/A	N/A
0.2	30.12	23.47	0.207	N/A	N/A
0.2	30.16	23.48	0.207	N/A	N/A
0.2	30.19	23.48	0.207	N/A	N/A
0.2	30.2	23.48	0.207	0.61	N/A
0.2	30.22	23.46	0.207	0.19	N/A
0.2	30.22	23.47	0.207	0.10	N/A
0.2	30.22	23.44	0.207	0.06	N/A
0.2	30.22	23.49	0.207	0.04	N/A
0.2	30.22	23.47	0.207	0.02	N/A
0.2	30.23	23.43	0.207	0.01	N/A
0.2	30.23	23.45	0.207	0.01	32.80
0.3	31.11	23.41	0.305	N/A	N/A
0.3	32.34	23.49	0.305	N/A	N/A
0.3	32.61	23.47	0.305	N/A	N/A
0.3	32.74	23.48	0.305	N/A	N/A
0.3	32.8	23.49	0.305	N/A	N/A
0.3	32.84	23.5	0.305	N/A	N/A
0.3	32.87	23.48	0.305	N/A	N/A
0.3	32.89	23.45	0.305	0.60	N/A

0.3	32.89	23.49	0.305	0.19	N/A
0.3	32.9	23.49	0.305	0.10	N/A
0.3	32.91	23.48	0.305	0.06	N/A
0.3	32.91	23.5	0.305	0.04	N/A
0.3	32.91	23.45	0.305	0.02	N/A
0.3	32.91	23.48	0.305	0.02	N/A
0.3	32.91	23.48	0.305	0.01	30.93
0.4	33.77	23.48	0.406	N/A	N/A
0.4	34.98	23.46	0.406	N/A	N/A
0.4	35.25	23.46	0.406	N/A	N/A
0.4	35.37	23.48	0.406	N/A	N/A
0.4	35.44	23.5	0.406	N/A	N/A
0.4	35.48	23.46	0.406	N/A	N/A
0.4	35.5	23.52	0.406	N/A	N/A
0.4	35.51	23.52	0.406	0.59	N/A
0.4	35.53	23.47	0.406	0.19	N/A
0.4	35.53	23.47	0.406	0.10	N/A
0.4	35.53	23.48	0.406	0.06	N/A
0.4	35.54	23.47	0.406	0.03	N/A
0.4	35.54	23.46	0.406	0.02	N/A
0.4	35.54	23.46	0.406	0.02	N/A
0.4	35.54	23.47	0.406	0.01	N/A
0.4	35.54	23.46	0.406	0.01	29.73
0.5	36.51	23.49	0.516	N/A	N/A
0.5	37.77	23.47	0.504	N/A	N/A
0.5	37.92	23.5	0.504	N/A	N/A
0.5	38.03	23.53	0.504	N/A	N/A
0.5	38.09	23.48	0.504	N/A	N/A
0.5	38.13	23.53	0.504	N/A	N/A
0.5	38.15	23.49	0.504	N/A	N/A
0.5	38.16	23.49	0.504	0.56	N/A
0.5	38.17	23.47	0.504	0.14	N/A
0.5	38.18	23.48	0.504	0.09	N/A
0.5	38.19	23.51	0.504	0.05	N/A
0.5	38.19	23.51	0.504	0.03	N/A
0.5	38.2	23.52	0.504	0.02	N/A

0.5	38.2	23.5	0.504	0.02	N/A
0.5	38.2	23.51	0.504	0.02	N/A
0.5	38.2	23.51	0.504	0.01	N/A
0.5	38.21	23.51	0.504	0.01	29.12
0.6	39.18	23.5	0.614	N/A	N/A
0.6	40.44	23.48	0.601	N/A	N/A
0.6	40.59	23.52	0.602	N/A	N/A
0.6	40.69	23.5	0.601	N/A	N/A
0.6	40.74	23.53	0.602	N/A	N/A
0.6	40.78	23.53	0.602	N/A	N/A
0.6	40.8	23.49	0.602	N/A	N/A
0.6	40.82	23.51	0.602	0.55	N/A
0.6	40.83	23.51	0.602	0.14	N/A
0.6	40.83	23.52	0.602	0.08	N/A
0.6	40.84	23.5	0.602	0.05	N/A
0.6	40.84	23.48	0.602	0.04	N/A
0.6	40.84	23.52	0.602	0.02	N/A
0.6	40.84	23.54	0.602	0.01	N/A
0.6	40.84	23.5	0.602	0.01	28.84
0.7	41.77	23.54	0.707	N/A	N/A
0.7	43.09	23.51	0.707	N/A	N/A
0.7	43.39	23.51	0.707	N/A	N/A
0.7	43.52	23.53	0.707	N/A	N/A
0.7	43.59	23.52	0.707	N/A	N/A
0.7	43.64	23.54	0.707	N/A	N/A
0.7	43.67	23.51	0.707	N/A	N/A
0.7	43.69	23.52	0.707	0.65	N/A
0.7	43.7	23.51	0.707	0.21	N/A
0.7	43.71	23.56	0.707	0.11	N/A
0.7	43.72	23.52	0.707	0.07	N/A
0.7	43.72	23.5	0.707	0.05	N/A
0.7	43.72	23.56	0.707	0.03	N/A
0.7	43.73	23.52	0.707	0.02	N/A
0.7	43.73	23.54	0.707	0.01	N/A
0.7	43.73	23.51	0.707	0.01	N/A
0.7	43.73	23.51	0.707	0.01	28.59

0.8	44.61	23.53	0.807	N/A	N/A
0.8	45.88	23.55	0.807	N/A	N/A
0.8	46.17	23.48	0.808	N/A	N/A
0.8	46.29	23.51	0.808	N/A	N/A
0.8	46.36	23.55	0.808	N/A	N/A
0.8	46.41	23.54	0.808	N/A	N/A
0.8	46.44	23.53	0.808	N/A	N/A
0.8	46.46	23.54	0.808	0.62	N/A
0.8	46.47	23.55	0.808	0.20	N/A
0.8	46.48	23.52	0.808	0.11	N/A
0.8	46.49	23.56	0.808	0.07	N/A
0.8	46.49	23.53	0.808	0.05	N/A
0.8	46.5	23.55	0.808	0.03	N/A
0.8	46.5	23.53	0.808	0.02	N/A
0.8	46.5	23.54	0.808	0.02	N/A
0.8	46.5	23.52	0.808	0.01	N/A
0.8	46.51	23.53	0.808	0.01	28.45
0.9	47.29	23.55	0.905	N/A	N/A
0.9	48.43	23.54	0.906	N/A	N/A
0.9	48.68	23.55	0.906	N/A	N/A
0.9	48.8	23.53	0.906	N/A	N/A
0.9	48.86	23.56	0.906	N/A	N/A
0.9	48.9	23.53	0.906	N/A	N/A
0.9	48.93	23.54	0.906	N/A	N/A
0.9	48.94	23.56	0.906	0.56	N/A
0.9	48.95	23.56	0.906	0.18	N/A
0.9	48.96	23.56	0.906	0.10	N/A
0.9	48.97	23.56	0.906	0.06	N/A
0.9	48.98	23.54	0.906	0.04	N/A
0.9	48.98	23.53	0.906	0.03	N/A
0.9	48.97	23.55	0.906	0.02	N/A
0.9	48.98	23.55	0.906	0.02	N/A
0.9	48.98	23.55	0.906	0.01	N/A
0.9	48.97	23.57	0.906	0.01	28.04
1	49.97	23.55	1.019	N/A	N/A
1	51.25	23.55	1.003	N/A	N/A

1	51.37	23.56	1.003	N/A	N/A
1	51.46	23.57	1.003	N/A	N/A
1	51.53	23.55	1.003	N/A	N/A
1	51.56	23.59	1.003	N/A	N/A
1	51.59	23.58	1.003	N/A	N/A
1	51.6	23.55	1.003	0.55	N/A
1	51.61	23.53	1.003	0.13	N/A
1	51.62	23.55	1.003	0.09	N/A
1	51.62	23.53	1.003	0.06	N/A
1	51.63	23.53	1.003	0.03	N/A
1	51.63	23.54	1.003	0.02	N/A
1	51.64	23.58	1.003	0.02	N/A
1	51.64	23.56	1.003	0.01	N/A
1	51.64	23.53	1.003	0.01	N/A
1	51.64	23.56	1.003	0.01	28.00

BGA#2_1 Thermal Resistance = 26.7658 [W/K]

BGA#2_1 Test Ended on 08 27 02 - 17 18

BGA#2_2 Package Data:

Underfill: #1

Power Start: .1 [W]

Power Step: .1 [W]

Power End: 1 [W]

Fractured Balls: None

BGA#2_2 Test Started on 08 27 02 - 17 18

BGA#2_2 Test Data:

Set Power [W]	T1 [ºC]	Cooling Temperature [ºC]	Actual Power [W]	Standard Deviation [ºC]	Thermal Resistance [K/W]
0.1	24.28	23.5	0.102	N/A	N/A
0.1	25.28	23.5	0.102	N/A	N/A
0.1	25.5	23.5	0.102	N/A	N/A
0.1	25.59	23.5	0.102	N/A	N/A
0.1	25.65	23.5	0.102	N/A	N/A
0.1	25.68	23.4	0.102	N/A	N/A
0.1	25.7	23.5	0.102	N/A	N/A
0.1	25.72	23.5	0.102	0.49	N/A
0.1	25.72	23.5	0.102	0.15	N/A
0.1	25.73	23.5	0.102	0.08	N/A
0.1	25.73	23.5	0.102	0.05	N/A
0.1	25.73	23.5	0.102	0.03	N/A
0.1	25.73	23.4	0.102	0.02	N/A
0.1	25.73	23.5	0.102	0.01	N/A
0.1	25.74	23.4	0.102	0.01	23.09
0.2	26.59	23.5	0.204	N/A	N/A
0.2	27.73	23.5	0.204	N/A	N/A
0.2	27.96	23.5	0.204	N/A	N/A
0.2	28.06	23.5	0.204	N/A	N/A
0.2	28.11	23.4	0.204	N/A	N/A
0.2	28.15	23.5	0.204	N/A	N/A
0.2	28.17	23.5	0.204	N/A	N/A
0.2	28.18	23.4	0.204	0.54	N/A
0.2	28.19	23.4	0.204	0.16	N/A
0.2	28.19	23.4	0.204	0.08	N/A
0.2	28.2	23.5	0.204	0.05	N/A
0.2	28.2	23.5	0.204	0.03	N/A
0.2	28.2	23.5	0.204	0.02	N/A
0.2	28.2	23.5	0.204	0.01	N/A
0.2	28.21	23.5	0.204	0.01	23.20
0.3	29.12	23.5	0.309	N/A	N/A
0.3	30.26	23.5	0.300	N/A	N/A
0.3	30.41	23.5	0.300	N/A	N/A

0.3	30.5	23.5	0.300	N/A	N/A
0.3	30.54	23.5	0.300	N/A	N/A
0.3	30.57	23.5	0.300	N/A	N/A
0.3	30.59	23.4	0.300	N/A	N/A
0.3	30.6	23.5	0.300	0.50	N/A
0.3	30.61	23.4	0.300	0.12	N/A
0.3	30.62	23.5	0.300	0.07	N/A
0.3	30.62	23.5	0.300	0.04	N/A
0.3	30.63	23.4	0.300	0.03	N/A
0.3	30.63	23.5	0.300	0.02	N/A
0.3	30.63	23.5	0.300	0.02	N/A
0.3	30.63	23.5	0.300	0.01	N/A
0.3	30.63	23.5	0.300	0.01	23.78
0.4	31.54	23.5	0.405	N/A	N/A
0.4	32.74	23.5	0.405	N/A	N/A
0.4	32.99	23.5	0.405	N/A	N/A
0.4	33.09	23.5	0.405	N/A	N/A
0.4	33.14	23.5	0.405	N/A	N/A
0.4	33.18	23.5	0.405	N/A	N/A
0.4	33.2	23.5	0.405	N/A	N/A
0.4	33.21	23.5	0.405	0.57	N/A
0.4	33.22	23.5	0.405	0.16	N/A
0.4	33.23	23.4	0.405	0.08	N/A
0.4	33.23	23.5	0.405	0.05	N/A
0.4	33.24	23.5	0.405	0.03	N/A
0.4	33.24	23.5	0.405	0.02	N/A
0.4	33.24	23.5	0.405	0.02	N/A
0.4	33.24	23.5	0.405	0.01	N/A
0.4	33.25	23.5	0.405	0.01	24.08
0.5	34.09	23.5	0.508	N/A	N/A
0.5	35.22	23.5	0.508	N/A	N/A
0.5	35.45	23.4	0.509	N/A	N/A
0.5	35.55	23.5	0.509	N/A	N/A
0.5	35.6	23.4	0.509	N/A	N/A
0.5	35.63	23.5	0.509	N/A	N/A
0.5	35.66	23.4	0.509	N/A	N/A

0.5	35.67	23.5	0.509	0.53	N/A
0.5	35.68	23.5	0.509	0.16	N/A
0.5	35.68	23.5	0.509	0.08	N/A
0.5	35.69	23.5	0.509	0.05	N/A
0.5	35.69	23.5	0.509	0.03	N/A
0.5	35.69	23.5	0.509	0.02	N/A
0.5	35.7	23.5	0.509	0.01	N/A
0.5	35.7	23.5	0.509	0.01	N/A
0.5	35.7	23.5	0.509	0.01	23.93
0.6	36.53	23.5	0.605	N/A	N/A
0.6	37.65	23.5	0.605	N/A	N/A
0.6	37.87	24	0.605	N/A	N/A
0.6	37.97	23.5	0.605	N/A	N/A
0.6	38.02	23.5	0.605	N/A	N/A
0.6	38.05	23.5	0.605	N/A	N/A
0.6	38.07	23.5	0.605	N/A	N/A
0.6	38.08	23.5	0.605	0.53	N/A
0.6	38.09	23.5	0.605	0.15	N/A
0.6	38.1	23.5	0.605	0.08	N/A
0.6	38.1	23.5	0.605	0.05	N/A
0.6	38.1	23.5	0.605	0.03	N/A
0.6	38.11	23.5	0.605	0.02	N/A
0.6	38.1	23.4	0.605	0.01	N/A
0.6	38.1	23.5	0.605	0.01	24.20
0.7	39.01	23.4	0.710	N/A	N/A
0.7	40.22	23.5	0.710	N/A	N/A
0.7	40.47	23.5	0.710	N/A	N/A
0.7	40.58	23.5	0.710	N/A	N/A
0.7	40.63	23.5	0.710	N/A	N/A
0.7	40.67	23.5	0.710	N/A	N/A
0.7	40.7	23.5	0.710	N/A	N/A
0.7	40.71	23.5	0.710	0.57	N/A
0.7	40.72	23.5	0.710	0.17	N/A
0.7	40.73	23.5	0.710	0.09	N/A
0.7	40.73	23.5	0.710	0.05	N/A
0.7	40.73	23.5	0.710	0.04	N/A

0.7	40.73	23.5	0.710	0.02	N/A
0.7	40.73	23.4	0.710	0.01	N/A
0.7	40.73	23.5	0.710	0.01	24.29
0.8	41.59	23.5	0.816	N/A	N/A
0.8	42.72	23.5	0.816	N/A	N/A
0.8	42.95	23.5	0.816	N/A	N/A
0.8	43.05	23.4	0.816	N/A	N/A
0.8	43.11	23.5	0.809	N/A	N/A
0.8	43.03	23.5	0.795	N/A	N/A
0.8	42.9	23.5	0.795	N/A	N/A
0.8	42.88	23.5	0.795	0.50	N/A
0.8	42.87	23.5	0.795	0.12	N/A
0.8	42.87	23.5	0.795	0.09	N/A
0.8	42.87	23.4	0.795	0.10	N/A
0.8	42.87	23.5	0.795	0.09	N/A
0.8	42.87	23.6	0.795	0.06	N/A
0.8	42.87	23.5	0.795	0.01	N/A
0.8	42.87	23.5	0.795	0.00	24.34
0.9	43.76	23.5	0.906	N/A	N/A
0.9	44.97	23.5	0.899	N/A	N/A
0.9	45.22	23.5	0.907	N/A	N/A
0.9	45.32	23.5	0.907	N/A	N/A
0.9	45.38	23.4	0.907	N/A	N/A
0.9	45.41	23.5	0.899	N/A	N/A
0.9	45.44	23.5	0.907	N/A	N/A
0.9	45.45	23.5	0.900	0.57	N/A
0.9	45.46	23.5	0.907	0.17	N/A
0.9	45.47	23.5	0.907	0.09	N/A
0.9	45.47	23.5	0.907	0.05	N/A
0.9	45.47	23.5	0.900	0.03	N/A
0.9	45.47	23.5	0.907	0.02	N/A
0.9	45.47	23.5	0.907	0.01	N/A
0.9	45.48	23.5	0.900	0.01	24.45
1	46.44	23.5	1.019	N/A	N/A
1	47.61	23.5	1.003	N/A	N/A
1	47.68	23.5	1.003	N/A	N/A

1	47.75	23.5	1.003	N/A	N/A
1	47.8	23.5	1.003	N/A	N/A
1	47.83	23.5	1.003	N/A	N/A
1	47.86	23.5	1.003	N/A	N/A
1	47.87	23.5	1.003	0.48	N/A
1	47.88	23.6	1.003	0.10	N/A
1	47.88	23.5	1.003	0.07	N/A
1	47.88	23.5	1.003	0.05	N/A
1	47.88	23.6	1.003	0.03	N/A
1	47.89	23.5	1.003	0.02	N/A
1	47.89	23.4	1.003	0.01	24.40

BGA#2_2 Thermal Resistance = 24.6336 [W/K]

BGA#2_2 Test Ended on 08 27 02 - 17 29

BGA#1_2 Package Data:

Underfil1: #1

Power Start: .1 [W]

Power Step: .1 [W]

Power End: 1 [W]

Fractured Balls: None

BGA#1_2 Test Started on 08 27 02 - 17 29

BGA#1_2 Test Data:

Set Power [W]	T1 [ºC]	T2 [ºC]	T3 [ºC]	Cooling Temperature [ºC]	Actual Power [W]r	Standard Deviation [ºC]	Thermal Resistance [K/W]
0.1	23.61	23.93	24.21	23.93	0.101	N/A	N/A
0.1	24.78	24.82	24.94	23.75	0.105	N/A	N/A
0.1	25.14	25.13	25.21	23.77	0.105	N/A	N/A
0.1	25.3	25.28	25.34	23.5	0.105	N/A	N/A

0.1	25.38	25.35	25.4	23.76	0.105	N/A	N/A
0.1	25.43	25.39	25.44	23.79	0.105	N/A	N/A
0.1	25.45	25.41	25.46	23.61	0.105	N/A	N/A
0.1	25.47	25.42	25.47	23.75	0.105	0.52	N/A
0.1	25.47	25.43	25.48	23.77	0.105	0.21	N/A
0.1	25.48	25.44	25.48	23.5	0.105	0.11	N/A
0.1	25.47	25.41	25.44	23.79	0.101	0.06	N/A
0.1	25.44	25.41	25.46	23.52	0.105	0.03	N/A
0.1	25.47	25.43	25.48	23.75	0.105	0.02	N/A
0.1	25.48	25.44	25.49	23.76	0.105	0.02	N/A
0.1	25.48	25.44	25.48	23.77	0.105	0.02	N/A
0.1	25.48	25.44	25.49	23.56	0.105	0.02	N/A
0.1	25.48	25.44	25.49	23.79	0.105	0.02	N/A
0.1	25.48	25.44	25.49	23.76	0.105	0.02	N/A
0.1	25.48	25.44	25.49	23.77	0.105	0.01	N/A
0.1	25.48	25.44	25.49	23.76	0.105	0.00	16.32
0.2	25.91	26.22	26.54	23.58	0.201	N/A	N/A
0.2	27.09	27.1	27.24	23.76	0.202	N/A	N/A
0.2	27.42	27.39	27.48	23.59	0.202	N/A	N/A
0.2	27.57	27.53	27.6	23.8	0.202	N/A	N/A
0.2	27.65	27.6	27.67	23.61	0.202	N/A	N/A
0.2	27.7	27.64	27.71	23.78	0.202	N/A	N/A
0.2	27.72	27.66	27.73	23.76	0.202	N/A	N/A
0.2	27.73	27.67	27.74	23.46	0.202	0.51	N/A
0.2	27.74	27.68	27.74	23.77	0.202	0.20	N/A
0.2	27.74	27.69	27.75	23.51	0.202	0.10	N/A
0.2	27.74	27.69	27.75	23.8	0.202	0.06	N/A
0.2	27.75	27.68	27.75	23.75	0.202	0.03	N/A
0.2	27.75	27.68	27.75	23.75	0.202	0.02	N/A
0.2	27.74	27.68	27.75	23.73	0.202	0.01	N/A
0.2	27.74	27.68	27.75	23.77	0.202	0.01	19.59
0.3	28.18	28.47	28.81	23.58	0.302	N/A	N/A
0.3	29.37	29.36	29.51	23.8	0.302	N/A	N/A
0.3	29.7	29.65	29.76	23.77	0.302	N/A	N/A
0.3	29.86	29.8	29.89	23.55	0.302	N/A	N/A
0.3	29.94	29.87	29.95	23.76	0.303	N/A	N/A

0.3	29.98	29.91	29.99	23.79	0.303	N/A	N/A
0.3	30	29.92	30	23.57	0.303	N/A	N/A
0.3	30.01	29.93	30.01	23.74	0.303	0.51	N/A
0.3	30.02	29.94	30.02	23.48	0.303	0.20	N/A
0.3	30.03	29.94	30.02	23.74	0.303	0.10	N/A
0.3	30.03	29.95	30.03	23.49	0.303	0.05	N/A
0.3	30.03	29.95	30.03	23.77	0.303	0.03	N/A
0.3	30.03	29.95	30.03	23.59	0.303	0.01	N/A
0.3	30.03	29.95	30.03	23.77	0.303	0.01	20.62
0.4	30.49	30.78	31.13	23.5	0.405	N/A	N/A
0.4	31.73	31.7	31.87	23.56	0.405	N/A	N/A
0.4	32.08	32.01	32.14	23.77	0.409	N/A	N/A
0.4	32.24	32.16	32.27	23.79	0.406	N/A	N/A
0.4	32.3	32.18	32.27	23.78	0.399	N/A	N/A
0.4	32.27	32.16	32.26	23.79	0.399	N/A	N/A
0.4	32.27	32.17	32.27	23.76	0.399	N/A	N/A
0.4	32.28	32.17	32.27	23.52	0.399	0.50	N/A
0.4	32.28	32.18	32.27	23.77	0.399	0.17	N/A
0.4	32.28	32.18	32.27	23.5	0.399	0.06	N/A
0.4	32.28	32.18	32.27	23.48	0.399	0.01	21.99
0.5	32.72	32.98	33.36	23.75	0.503	N/A	N/A
0.5	33.96	33.91	34.09	23.51	0.504	N/A	N/A
0.5	34.31	34.22	34.36	23.8	0.504	N/A	N/A
0.5	34.48	34.36	34.49	23.78	0.504	N/A	N/A
0.5	34.56	34.44	34.56	23.76	0.504	N/A	N/A
0.5	34.61	34.48	34.6	23.77	0.504	N/A	N/A
0.5	34.63	34.51	34.63	23.78	0.504	N/A	N/A
0.5	34.65	34.52	34.64	23.77	0.504	0.54	N/A
0.5	34.66	34.53	34.65	23.53	0.504	0.21	N/A
0.5	34.66	34.54	34.65	23.78	0.504	0.11	N/A
0.5	34.67	34.54	34.65	23.55	0.504	0.06	N/A
0.5	34.67	34.54	34.65	23.75	0.504	0.04	N/A
0.5	34.67	34.54	34.65	23.49	0.504	0.02	N/A
0.5	34.67	34.54	34.65	23.48	0.504	0.01	N/A
0.5	34.67	34.54	34.66	23.48	0.504	0.01	22.10
0.6	35.13	35.38	35.78	23.58	0.608	N/A	N/A

0.6	36.37	36.27	36.45	23.77	0.600	N/A	N/A
0.6	36.63	36.51	36.67	23.58	0.601	N/A	N/A
0.6	36.77	36.64	36.78	23.54	0.601	N/A	N/A
0.6	36.85	36.71	36.84	23.75	0.601	N/A	N/A
0.6	36.89	36.74	36.88	23.75	0.601	N/A	N/A
0.6	36.91	36.76	36.89	23.79	0.601	N/A	N/A
0.6	36.92	36.77	36.9	23.77	0.601	0.49	N/A
0.6	36.93	36.78	36.92	23.75	0.601	0.18	N/A
0.6	36.94	36.79	36.92	23.6	0.601	0.10	N/A
0.6	36.94	36.79	36.92	23.78	0.601	0.05	N/A
0.6	36.95	36.79	36.92	23.8	0.601	0.03	N/A
0.6	36.95	36.8	36.93	23.75	0.601	0.02	N/A
0.6	36.95	36.8	36.93	23.51	0.601	0.01	N/A
0.6	36.95	36.8	36.93	23.49	0.601	0.01	N/A
0.6	36.95	36.79	36.92	23.59	0.601	0.01	22.13
0.7	37.4	37.62	38.04	23.78	0.705	N/A	N/A
0.7	38.63	38.5	38.69	23.78	0.696	N/A	N/A
0.7	38.87	38.73	38.9	23.77	0.696	N/A	N/A
0.7	39.01	38.85	39.02	23.74	0.696	N/A	N/A
0.7	39.09	38.91	39.07	23.61	0.696	N/A	N/A
0.7	39.12	38.95	39.1	23.77	0.697	N/A	N/A
0.7	39.15	38.97	39.12	23.77	0.697	N/A	N/A
0.7	39.16	38.99	39.14	23.77	0.697	0.48	N/A
0.7	39.17	39	39.14	23.59	0.697	0.17	N/A
0.7	39.18	39	39.15	23.8	0.697	0.10	N/A
0.7	39.18	39.01	39.15	23.77	0.697	0.05	N/A
0.7	39.18	39.01	39.15	23.53	0.697	0.03	N/A
0.7	39.19	39	39.16	23.79	0.697	0.02	N/A
0.7	39.19	39.01	39.16	23.57	0.697	0.01	N/A
0.7	39.19	39.01	39.16	23.78	0.697	0.01	22.02
0.8	39.63	39.82	40.25	23.5	0.804	N/A	N/A
0.8	40.88	40.77	41	23.77	0.804	N/A	N/A
0.8	41.25	41.08	41.28	23.58	0.805	N/A	N/A
0.8	41.42	41.24	41.42	23.78	0.805	N/A	N/A
0.8	41.51	41.32	41.49	23.76	0.805	N/A	N/A
0.8	41.56	41.36	41.53	23.77	0.805	N/A	N/A

0.8	41.59	41.39	41.56	23.77	0.805	N/A	N/A
0.8	41.6	41.4	41.57	23.48	0.805	0.55	N/A
0.8	41.62	41.41	41.58	23.49	0.805	0.22	N/A
0.8	41.62	41.42	41.59	23.51	0.805	0.12	N/A
0.8	41.63	41.42	41.59	23.51	0.805	0.07	N/A
0.8	41.63	41.43	41.59	23.49	0.805	0.04	N/A
0.8	41.63	41.43	41.59	23.76	0.805	0.03	N/A
0.8	41.63	41.43	41.6	23.53	0.805	0.02	N/A
0.8	41.64	41.44	41.6	23.51	0.805	0.01	N/A
0.8	41.64	41.44	41.6	23.49	0.805	0.01	22.44
0.9	42.06	42.21	42.65	23.51	0.904	N/A	N/A
0.9	43.27	43.12	43.38	23.61	0.905	N/A	N/A
0.9	43.62	43.43	43.65	23.75	0.905	N/A	N/A
0.9	43.79	43.58	43.78	23.75	0.906	N/A	N/A
0.9	43.87	43.66	43.85	23.74	0.906	N/A	N/A
0.9	43.93	43.7	43.89	23.6	0.906	N/A	N/A
0.9	43.95	43.73	43.92	23.76	0.906	N/A	N/A
0.9	43.97	43.74	43.93	23.76	0.906	0.53	N/A
0.9	43.98	43.75	43.94	23.75	0.906	0.22	N/A
0.9	43.98	43.75	43.94	23.75	0.906	0.12	N/A
0.9	43.99	43.76	43.94	23.48	0.906	0.07	N/A
0.9	43.99	43.76	43.95	23.74	0.906	0.04	N/A
0.9	43.99	43.76	43.95	23.6	0.906	0.02	N/A
0.9	44	43.76	43.95	23.77	0.906	0.02	N/A
0.9	44	43.77	43.96	23.5	0.906	0.01	N/A
0.9	44	43.77	43.95	23.78	0.906	0.01	22.22
1	44.45	44.59	45.07	23.78	1.011	N/A	N/A
1	45.69	45.48	45.72	23.55	1.006	N/A	N/A
1	45.97	45.79	46.06	23.75	1.013	N/A	N/A
1	46.21	45.93	46.13	23.76	1.007	N/A	N/A
1	46.2	45.94	46.15	23.77	1.007	N/A	N/A
1	46.21	45.96	46.17	23.74	1.007	N/A	N/A
1	46.22	45.96	46.17	23.74	1.001	0.49	N/A
1	46.22	45.96	46.17	23.78	1.007	0.17	N/A
1	46.23	45.97	46.18	23.76	1.007	0.06	N/A
1	46.23	45.97	46.18	23.74	1.007	0.02	N/A

1	46.24	45.98	46.18	23.78	1.007	0.02	N/A
1	46.24	45.98	46.19	23.5	1.007	0.01	N/A
1	46.25	45.99	46.19	23.49	1.001	0.01	N/A
1	46.25	45.99	46.2	23.51	1.007	0.01	N/A
1	46.25	45.99	46.2	23.76	1.007	0.01	N/A
1	46.26	45.99	46.2	23.77	1.007	0.01	22.22

BGA#1_2 Thermal Resistance = 23.0286 [W/K]

BGA#1_2 Test Ended on 08 27 02 - 17 44

APPENDIX C

Thermal Resistance Measurements at 0 Cycles

Packages with Thermal Balls

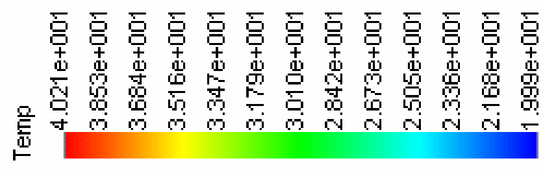
		Board #1	Board #2	Board #3	Board #4	Average	Standard Deviation
No Underfill	BGA #1/Via #1	23.47	24.75	23.48	24.08	23.94	0.61
	BGA #1/Via #2	22.82	22.91	21.54	23.60	22.72	0.86
	BGA #2/Via #1	27.41	30.24	26.50	27.53	27.92	1.62
	BGA #2/Via #2	25.34	27.54	24.78	25.02	25.67	1.27
Underfill #1	BGA #1/Via #1	17.63	19.32	18.76	18.86	18.64	0.72
	BGA #1/Via #2	17.68	18.05	18.35	18.24	18.08	0.29
	BGA #2/Via #1	26.09	25.53	26.54	25.98	26.04	0.41
	BGA #2/Via #2	23.76	23.76	24.38	24.16	24.01	0.31
Underfill #2	BGA #1/Via #1	18.09	18.40	18.96	18.85	18.74	0.30
	BGA #1/Via #2	17.71	17.27	17.63	17.64	17.57	0.20
	BGA #2/Via #1	25.40	25.89	25.22	24.72	25.31	0.48
	BGA #2/Via #2	23.19	23.42	23.28	23.97	23.56	0.36
Underfill #3	BGA #1/Via #1	19.13	18.93	18.59	18.59	18.70	0.19
	BGA #1/Via #2	17.51	18.10	17.73	18.31	17.91	0.36
	BGA #2/Via #1	25.08	25.04	25.06	24.85	25.01	0.11
	BGA #2/Via #2	22.98	23.45	23.84	22.89	23.39	0.48

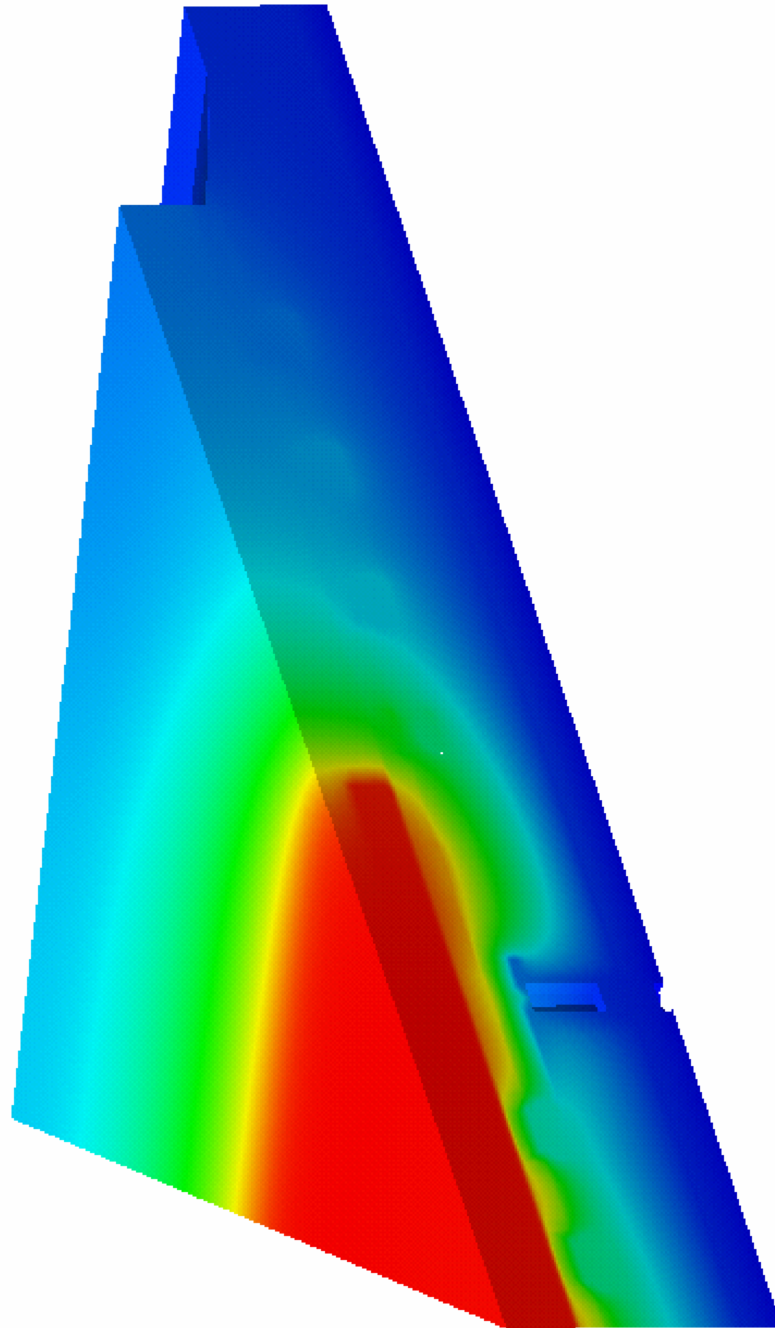
Packages without Thermal Balls

		Board #1	Board #2	Board #3	Board #4	Average	Standard Deviation
No Underfill	BGA #1/Via #2	36.37	34.62	36.65	37.40	36.26	1.18
	BGA #2/Via #2	47.44	46.98	47.66	48.38	47.62	0.58
Underfill #1	BGA #1/Via #2	19.72	19.70	19.85	20.08	19.84	0.18
	BGA #2/Via #2	29.60	29.90	29.88	30.33	29.93	0.30
Underfill #2	BGA #1/Via #2	19.71	19.36	19.97	19.83	19.72	0.26
	BGA #2/Via #2	29.49	28.93	29.11	N/A	29.18	0.13
Underfill #3	BGA #1/Via #2	20.64	20.71	20.74	21.12	20.80	0.22
	BGA #2/Via #2	31.19	30.94	30.29	30.82	30.81	0.34

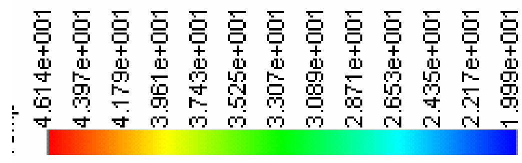
APPENDIX D

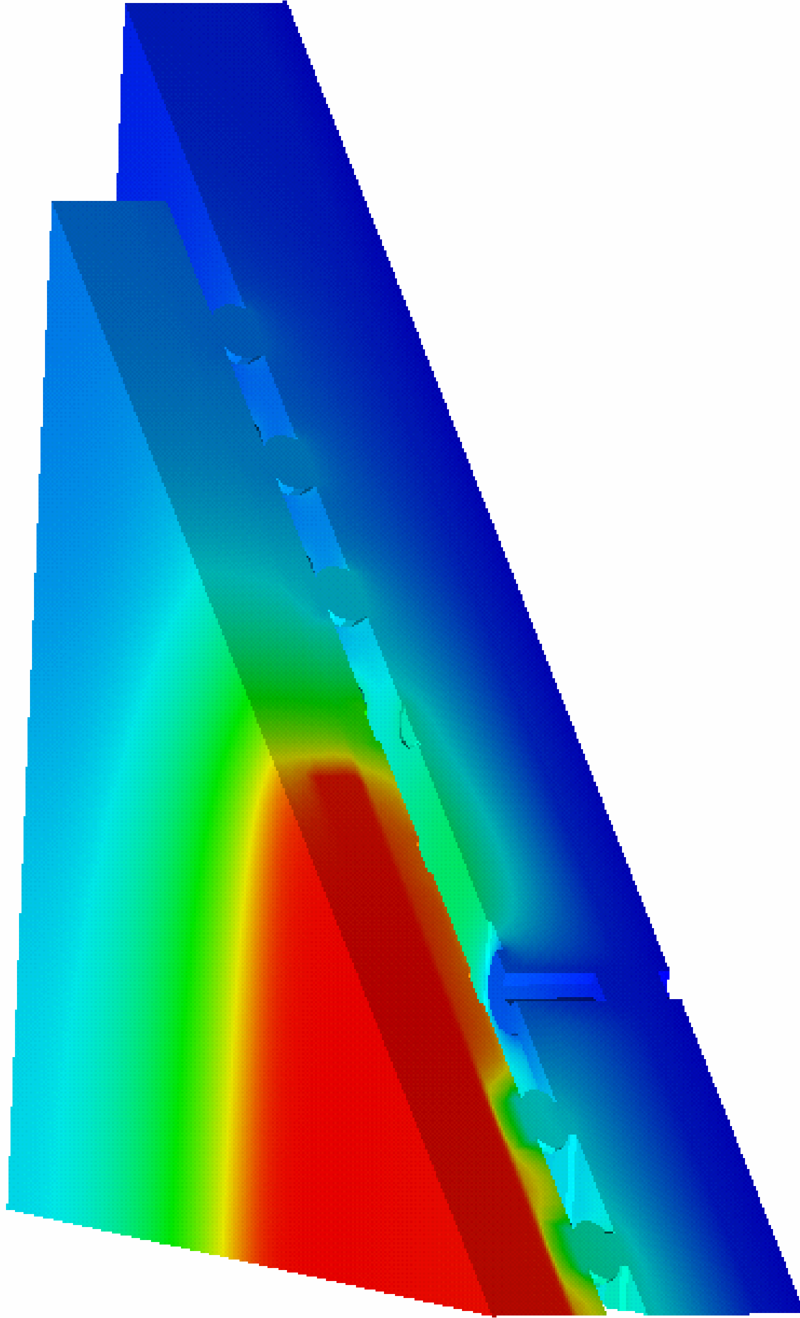
Numerical Simulation Temperature Distributions [ºC]



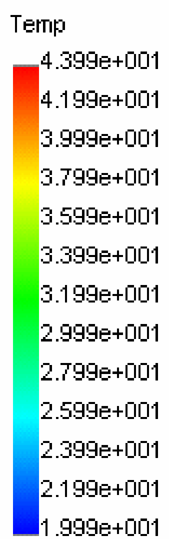


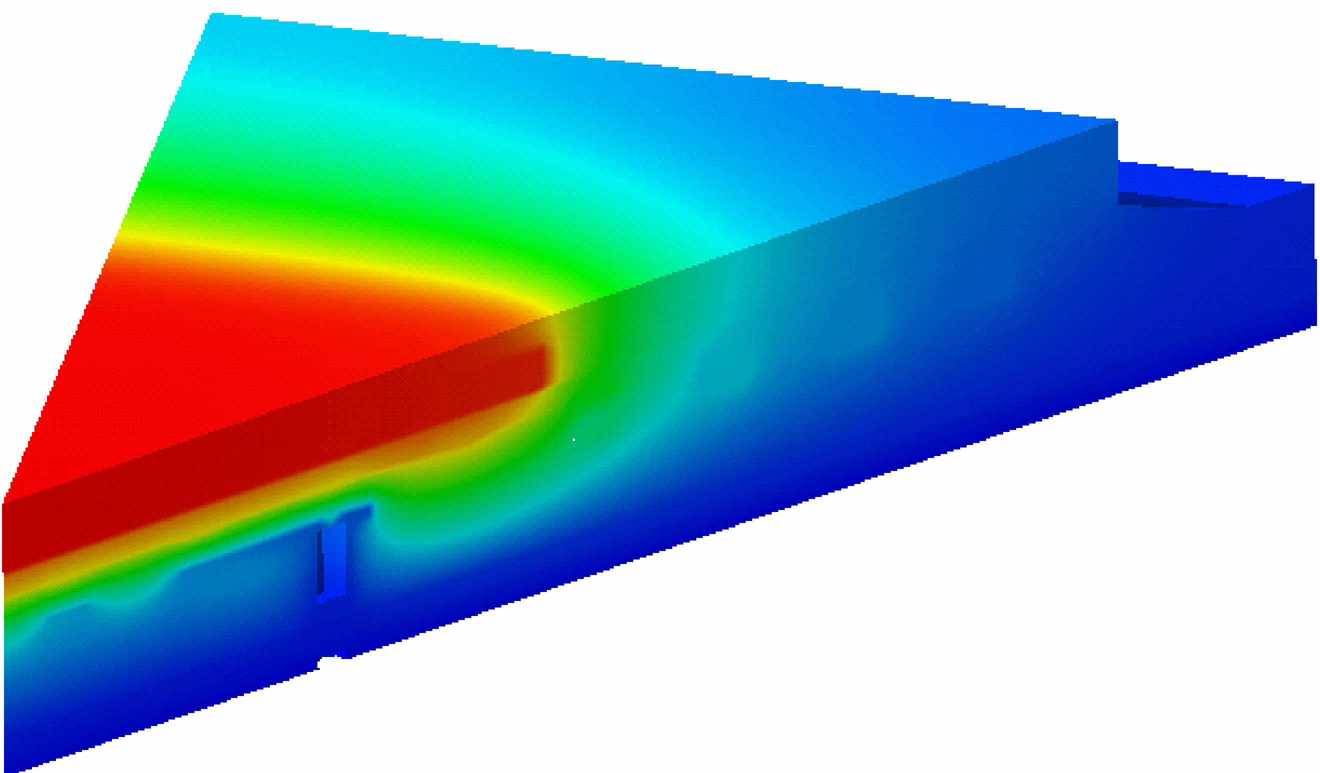
BGA #1 / Via #1 / With Underfill / With Thermal Balls



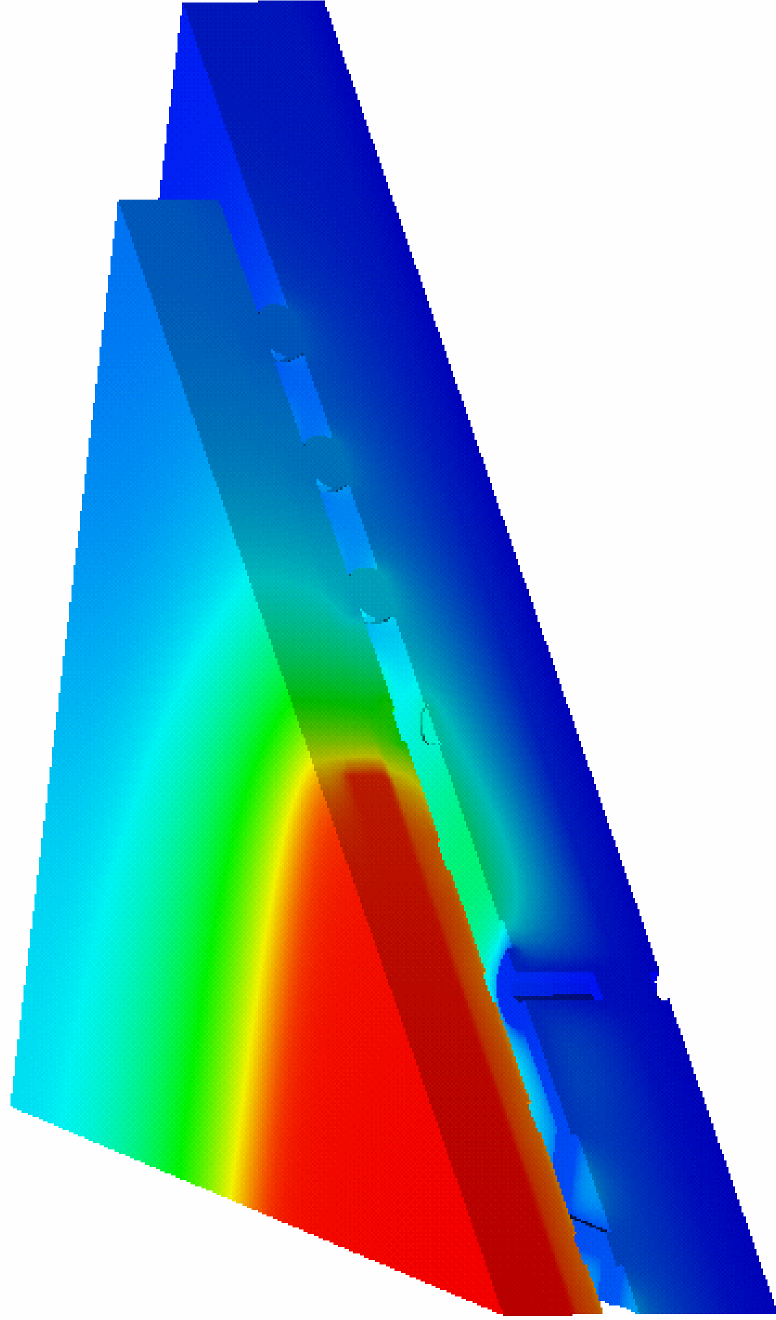


BGA #1 / Via #1 / Without Underfill / With Thermal Balls

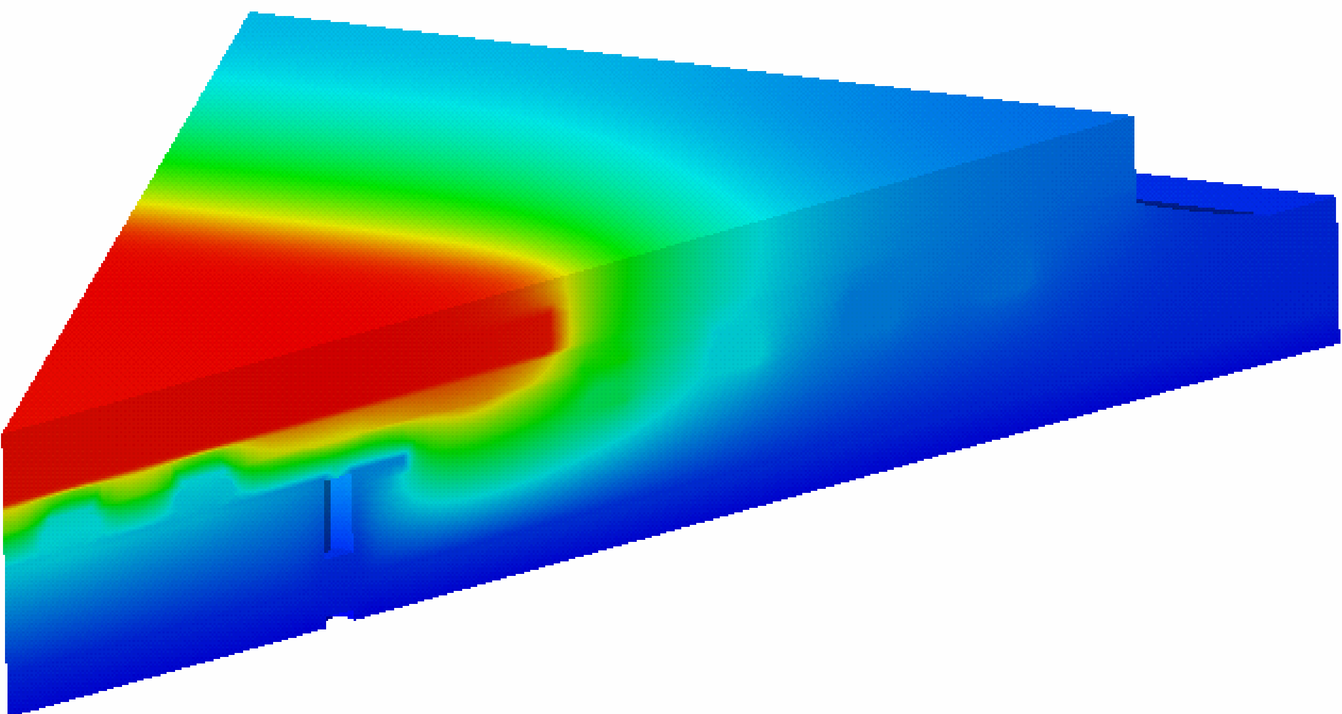


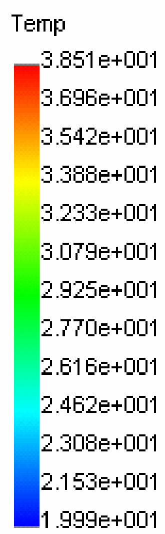


BGA #1 / Via #1 / With Underfill / Without Thermal Balls



BGA #1 / Via #1 / Without Underfill / Without Thermal Balls





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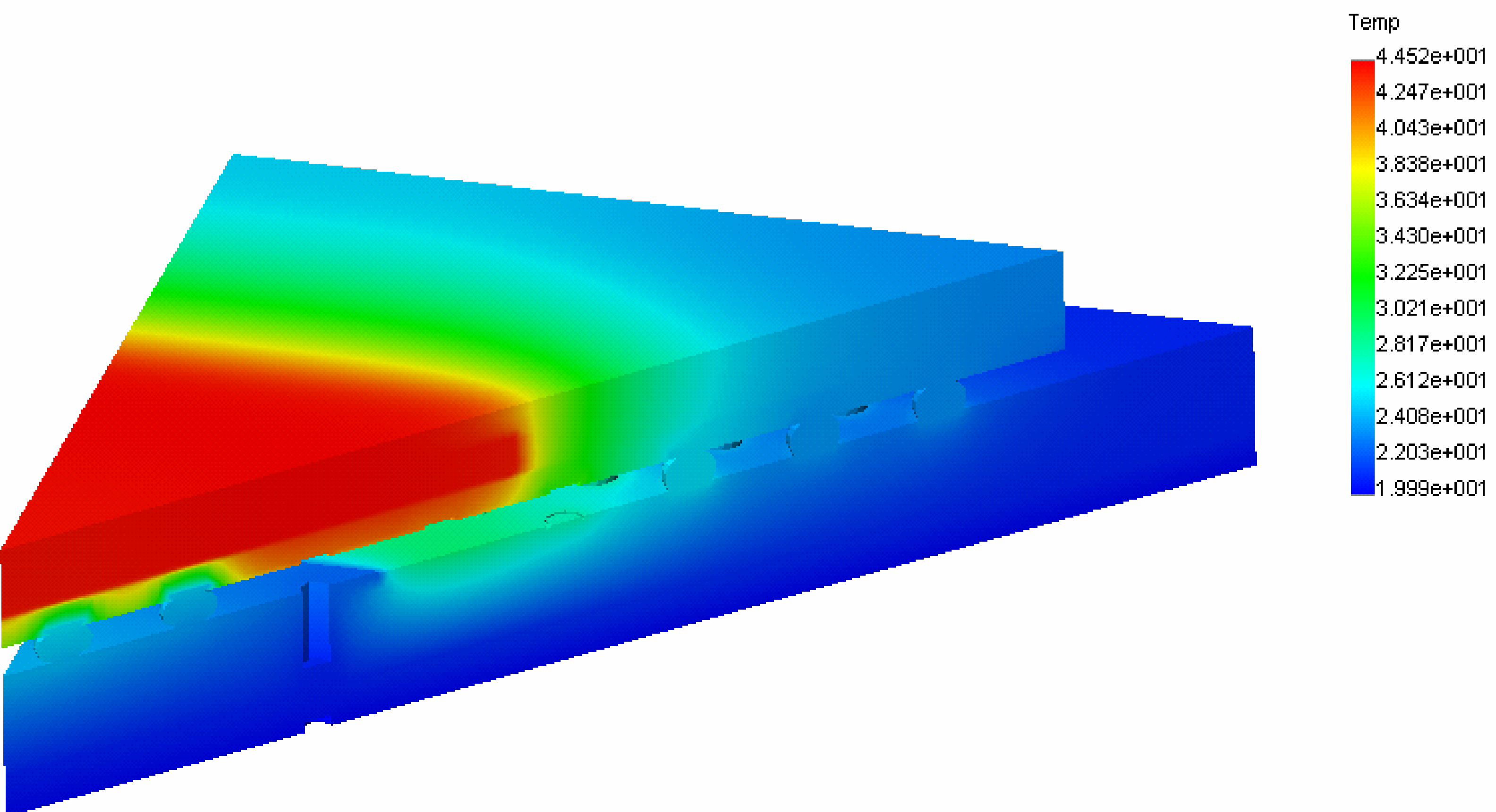

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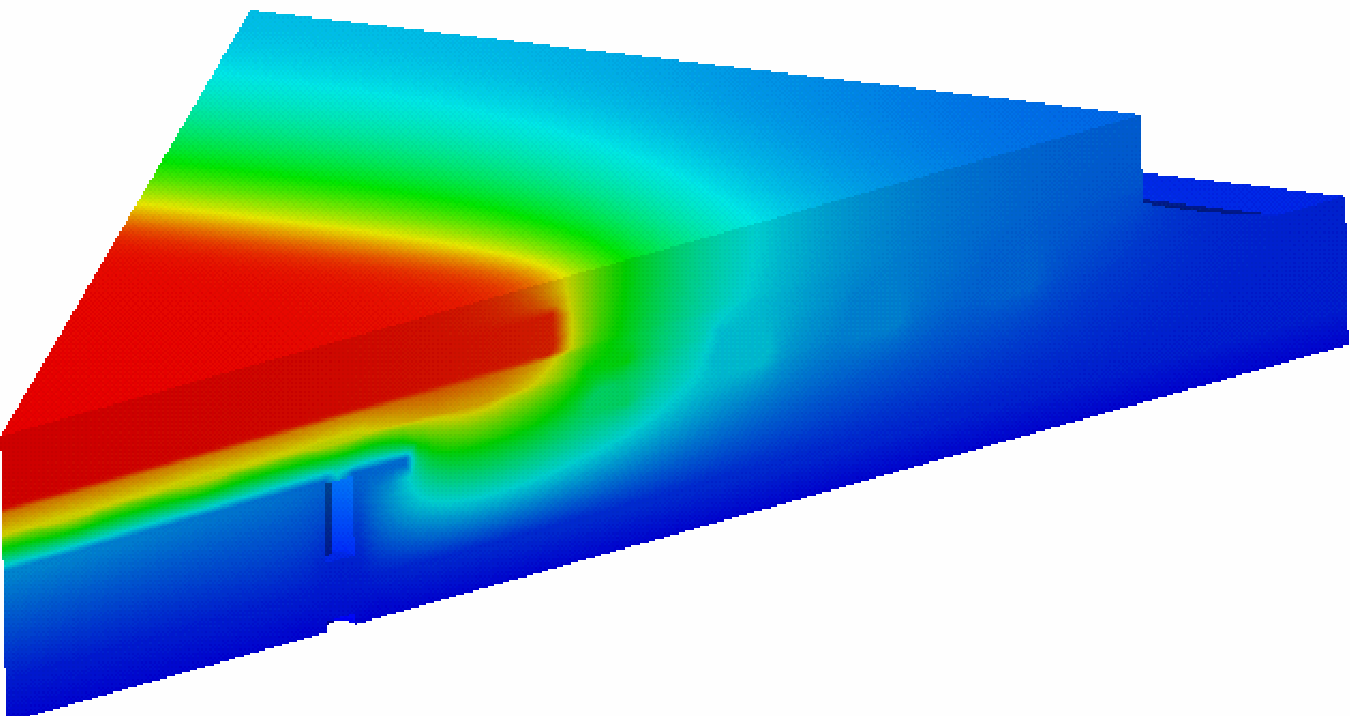

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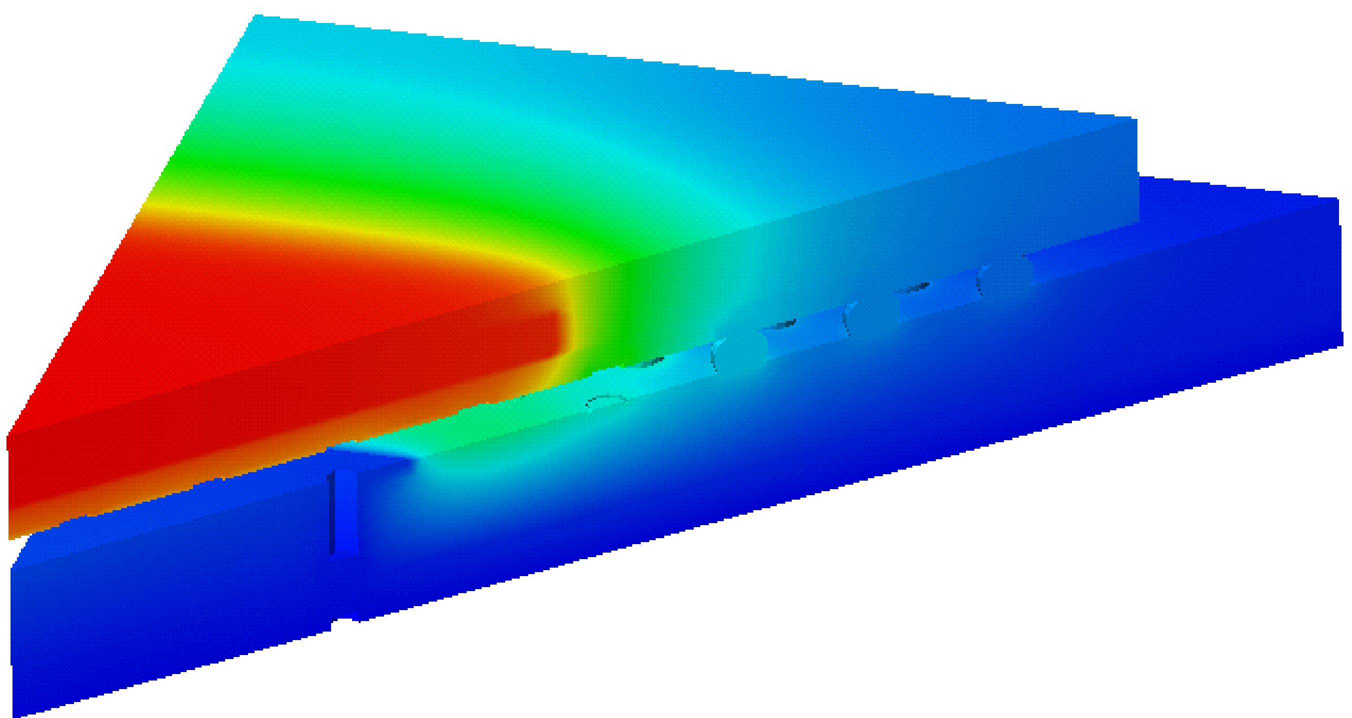

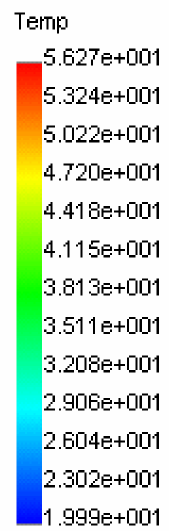

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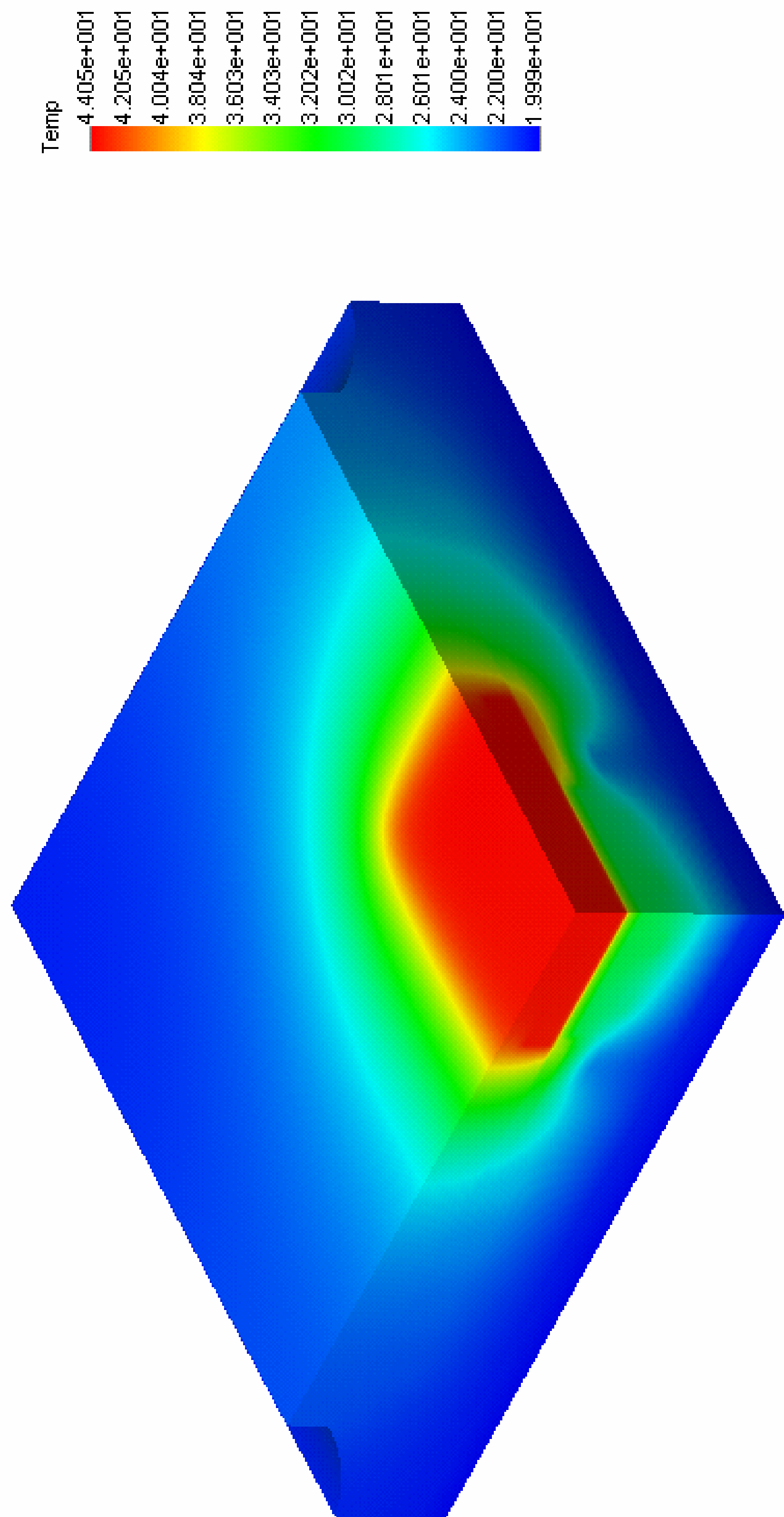

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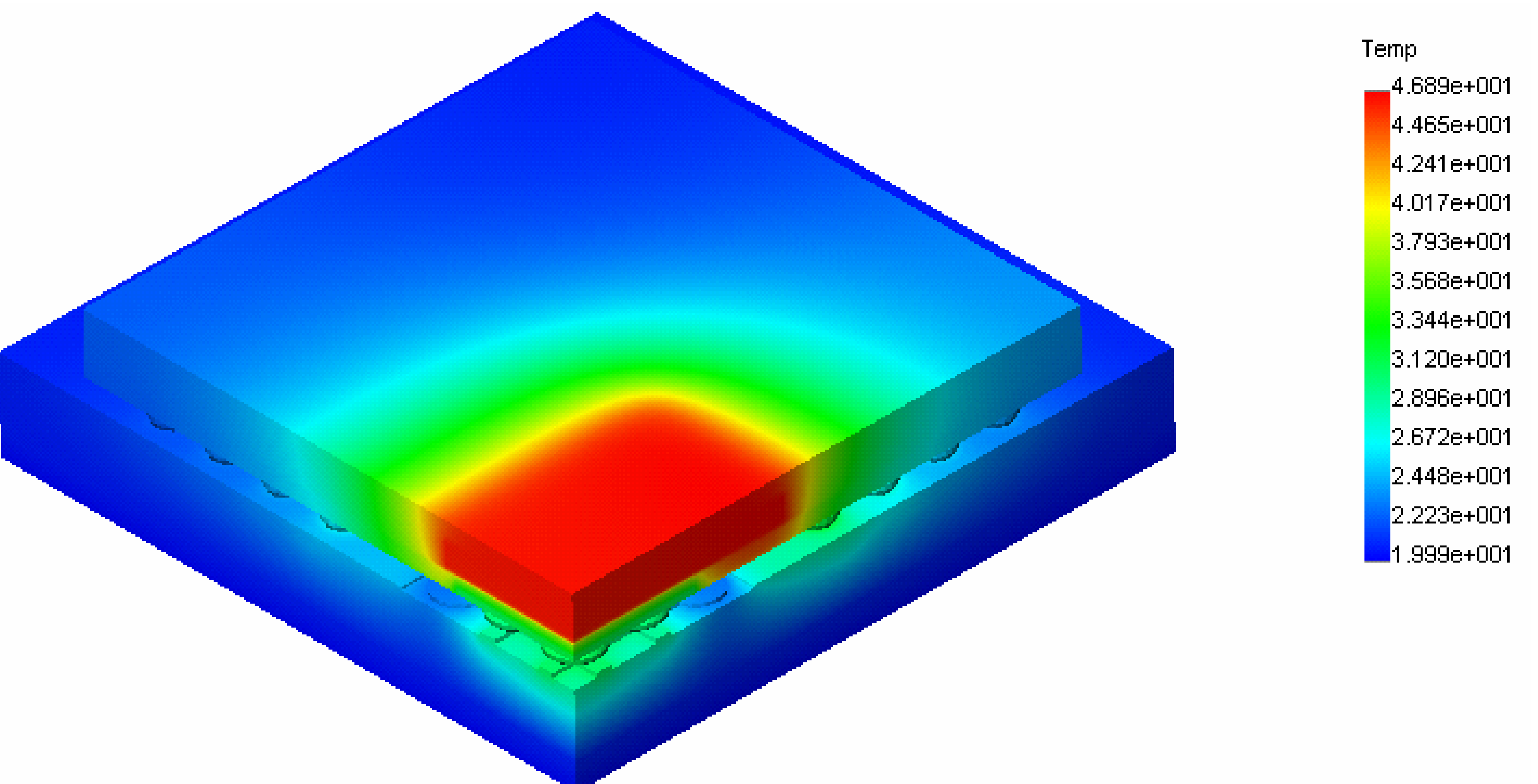

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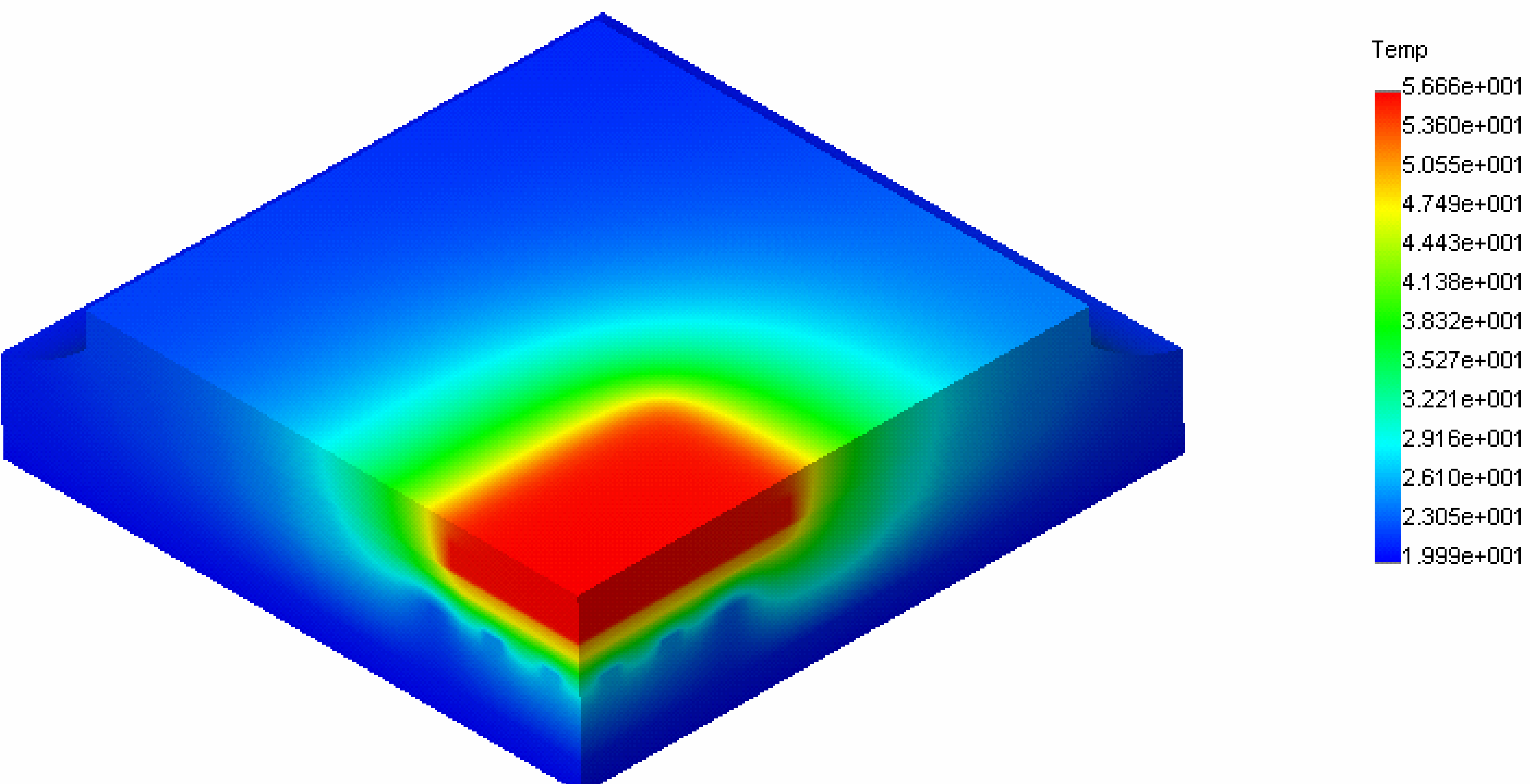

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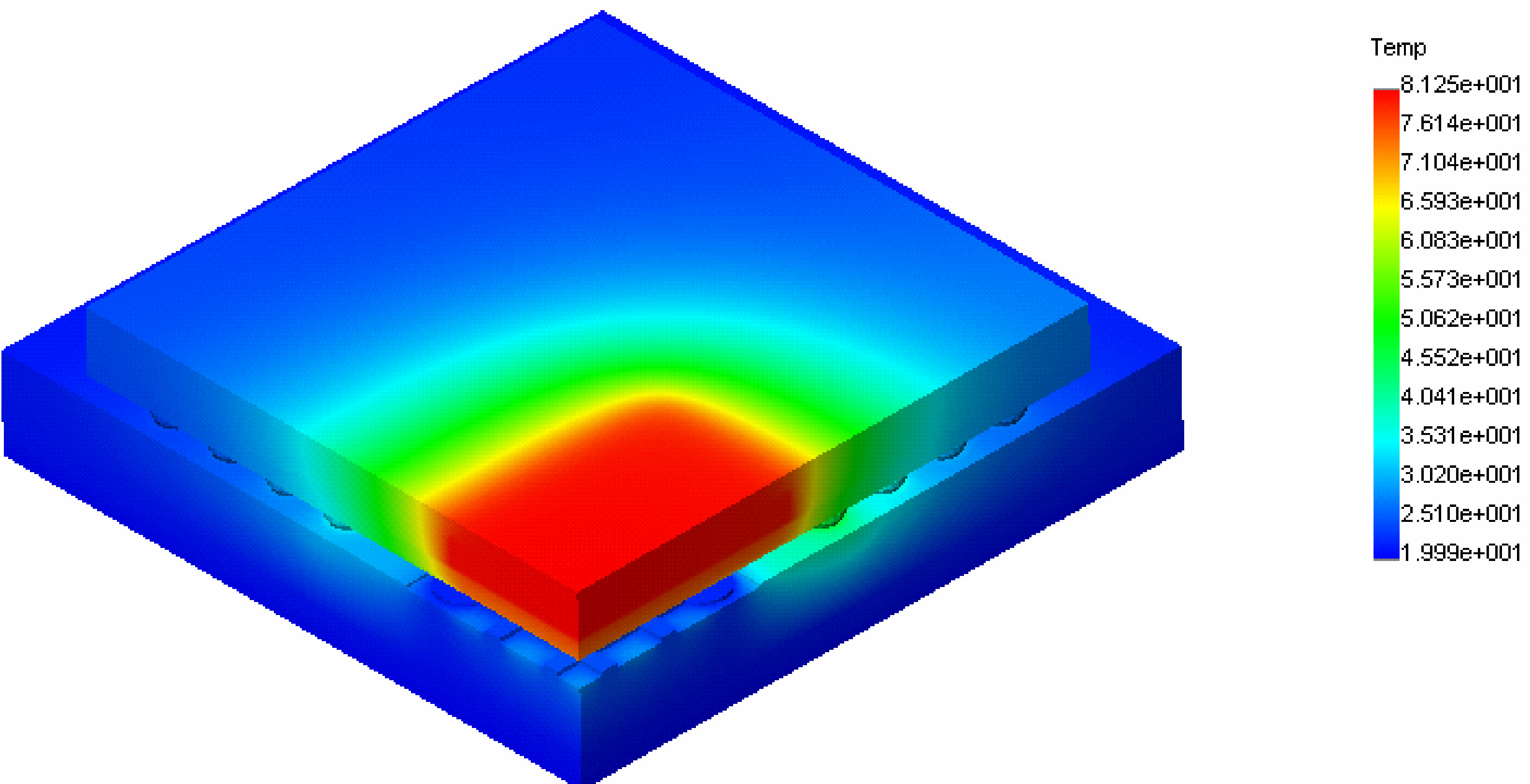

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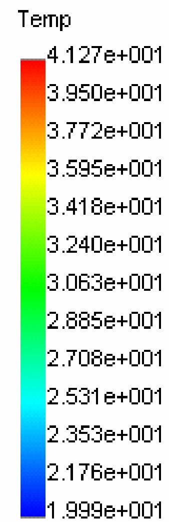
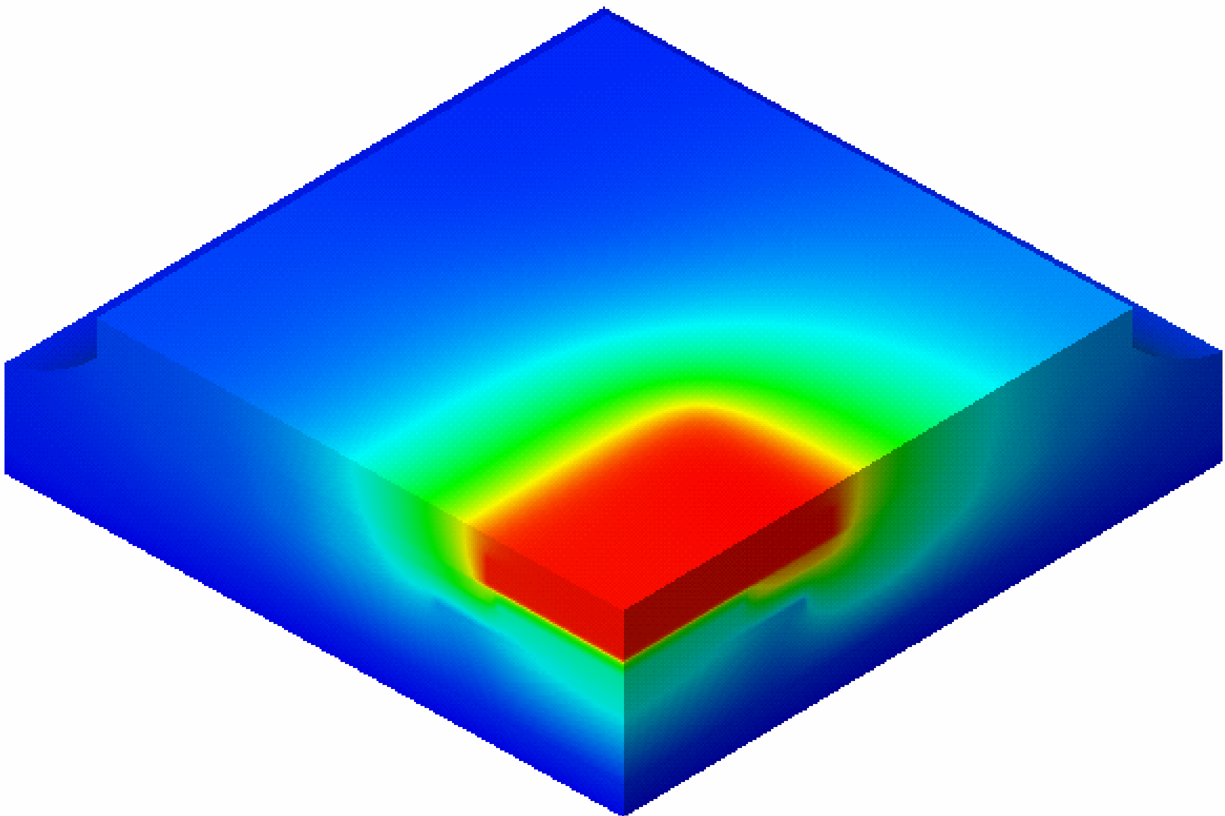
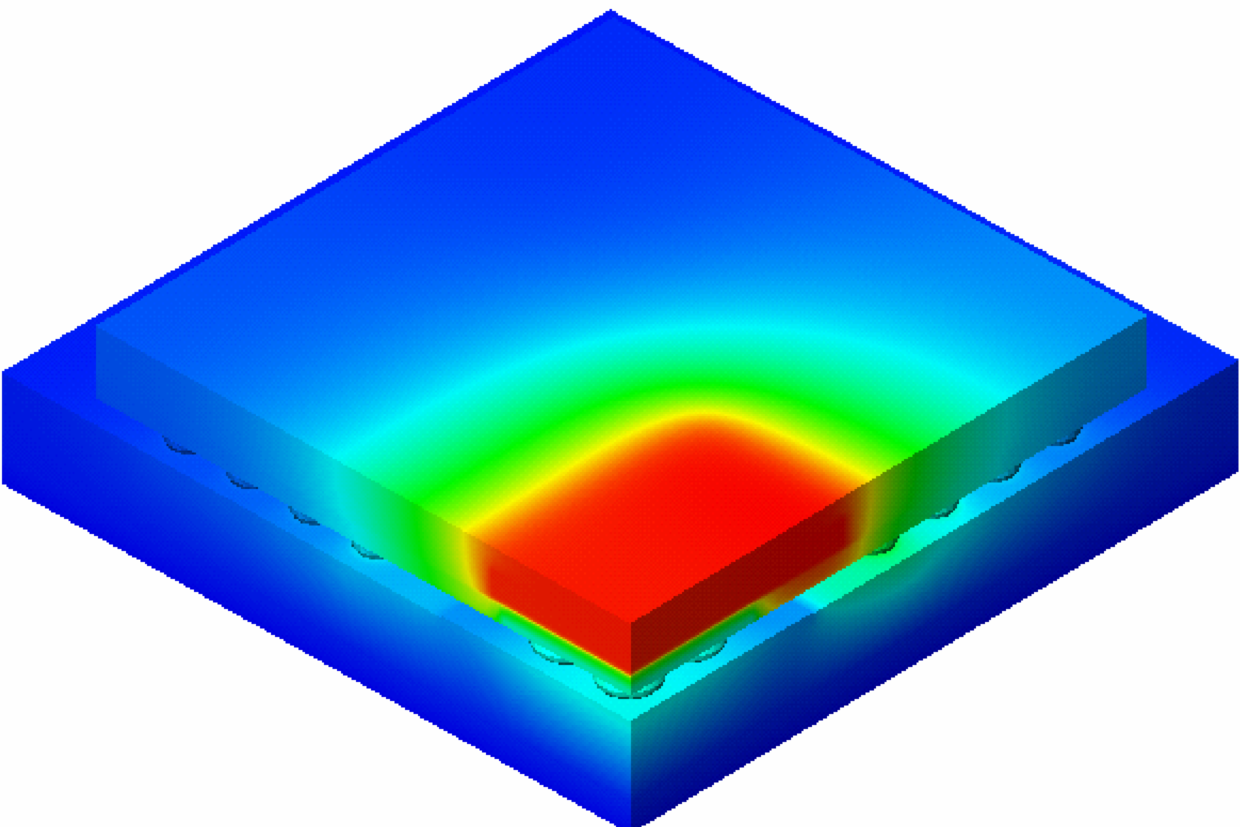
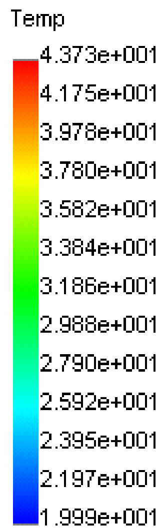


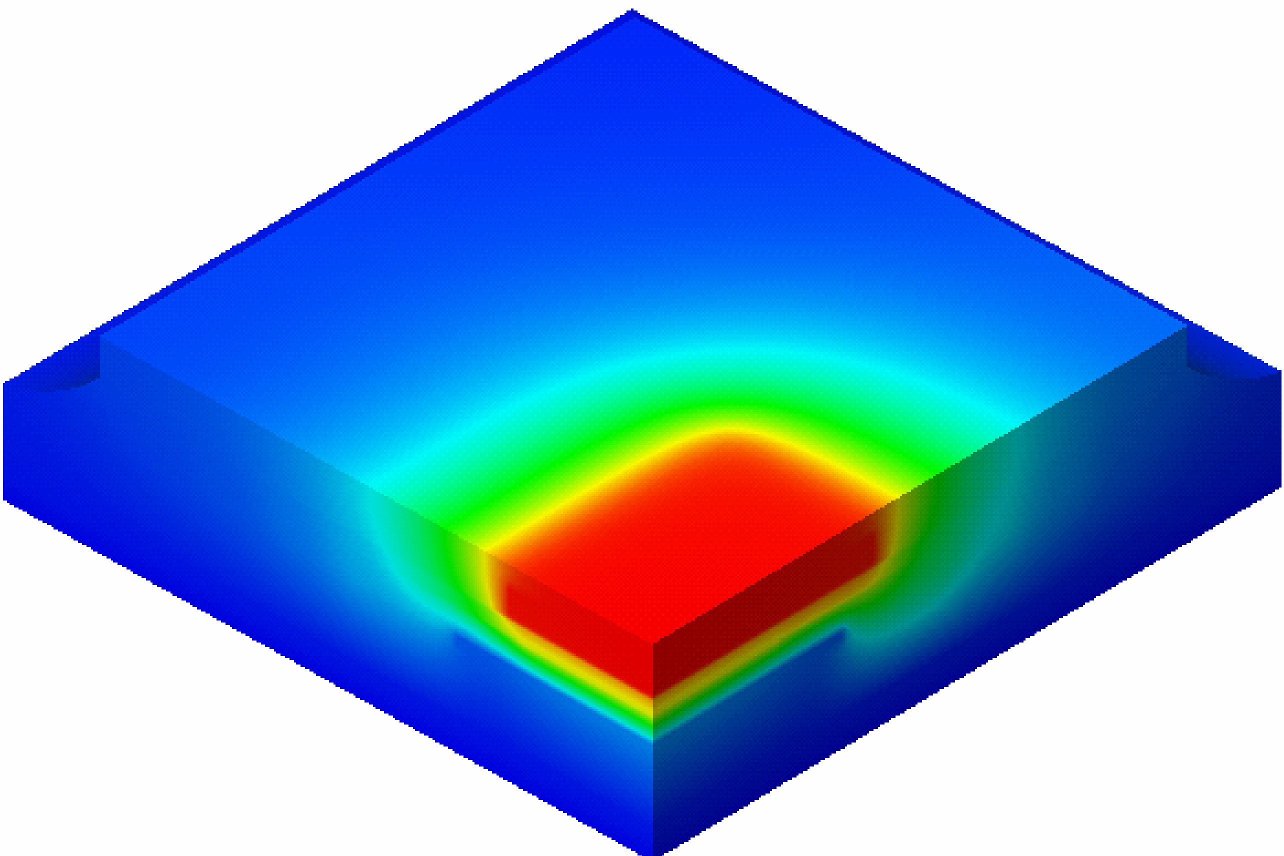


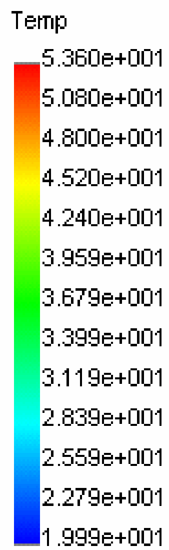
BGA #2 / Via #2 / With Underfill / With Thermal Balls





BGA #2 / Via #2 / Without Underfill / With Thermal Balls





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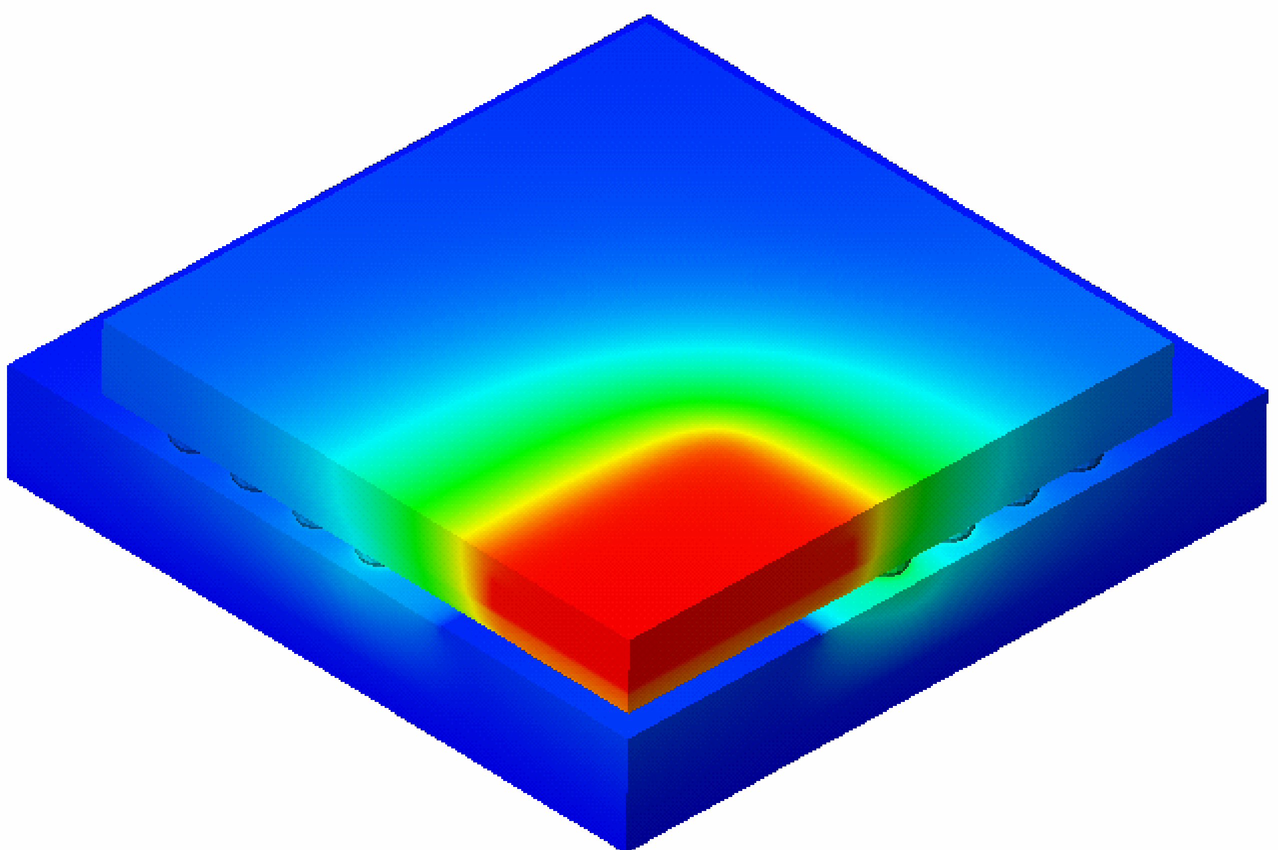

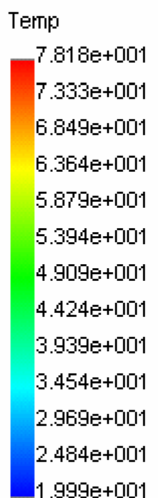

BGA #2 / Via #2 / Without Underfill / Without Thermal Balls