Silicon Carbide/Aluminum Oxide Field-Effect Transistors

by

Isanka Udayani Jayawardhena

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Approved by

Sarit Dhar, Chair, Associate Professor of Physics
Ayayi C. Ahyi, Chair, Associate Research Professor of Physics
Minseo Park, Professor of Physics
Marcelo A. Kuroda, Assistant Professor of Physics
Michael Gramlich, Assistant Professor of Physics
Leonard C. Feldman, Distinguished Professor Emeritus of Physics and Astronomy, Material Science and Engineering, Rutgers University
Willis E. Hames, Professor of Geology

Abstract

4H-Silicon Carbide is a wide band gap semiconductor with attractive physical properties for high power, high-frequency devices, and electronics that operate under harsh environments that are not accessible to conventional silicon devices. A significant challenge in 4H-SiC metal oxide semiconductor field-effect transistors (MOSFETs) is the poor channel conductance due to the trapping of carriers by high-density of near-interface traps at the 4H-SiC/SiO_2 interface. Many trap passivation methods have been researched as a solution and currently, nitridation of the interface via processes such as nitric oxide (NO) annealing is the most reliable approach. The nitrided SiO_2/4H-SiC interfaces are still far from ideal and alternate approaches are desirable. One such approach is the deposition of high-k dielectrics which has added advantages over conventional SiO_2. Among these alternative dielectrics, atomic layer deposition (ALD) of Al_2O_3 has shown promising results in the literature. The focus of this thesis is the study of ALD Al_2O_3/4H-SiC interfaces using systematic process variations, device fabrication and electrical characterization.

Among the electrical characterization methods used to evaluate interface trap densities (D_{it}), constant capacitance deep level transient spectroscopy (CCDLTS) is a method capable of differentiating trap types in MOS devices. Two signature near interface oxide traps named O1 and O2 are typically detected for the SiO_2/4H-SiC interfaces by CCDLTS. In this work, for the first time, it was found that such traps are absent in Al_2O_3/4H-SiC interfaces formed on the H-terminated 4H-SiC surface. This strongly indicates that the O1 and O2 traps are inherent to SiO_2/4H-SiC interfaces. This result motivated further investigation where a systematic study of the effect of 4H-SiC surface treatments prior to the deposition of Al_2O_3 by ALD was conducted. This is the first comprehensive study where Al_2O_3/4H-SiC MOSFETs were fabricated to analyze the dependence of the channel mobility on the surface treatments. Among the studied surface

treatments, H_2 annealing at high temperature prior to ALD was found to result in reduced D_{it} and impressive channel mobility along with improved stability for the Al_2O_3/4H-SiC MOS devices. The most likely reason for this is that H_2 annealing results in a Si-H terminated 4H-SiC surface, which in turn leads to a more uniform nucleation of the ALD Al_2O_3 thin film, resulting in a better SiC/Al_2O_3 interface. In addition, it was also found that similar to SiO_2/4H-SiC, nitridation of the Al_2O_3/4H-SiC interface results in trap passivation and possible surface doping by N. In this work, interfacial nitridation was carried out by performing sacrificial oxidation of SiC in NO. This results in a sub-nm thick SiON layer on top of SiC and subsequent H_2 annealing of this surface prior to Al_2O_3 deposition leads to further improvements. Al_2O_3/4H-SiC MOSFETs fabricated with this process resulted in peak field-effect mobility of 52 cm^2/Vs which is 2x higher channel electron mobility compared to conventional nitrided SiO_2/4H-SiC MOSFETs. The channel mobility results in this work are very encouraging for the application of ALD Al_2O_3 on SiC from the point of view from channel conductance. However, it was observed that the large dielectric leakage currents associated with the defects in the bulk of the ALD thin films is the biggest challenge that need to be overcome. In this work, it was conclusively demonstrated that 4H-SiC surface treatments prior to ALD are key to the optimization of MOS interfaces using deposited dielectrics. The Hydrogen and Nitrogen based surface treatments developed in this work can be applied to other deposited dielectrics in the future as well.

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Chapter 1

Introduction

Electronics has changed the world and we strongly depend on it in the 21st century. Nowadays from daily household items to transportation, power distribution, robotics, medicine, automation, telecommunication, space exploration, almost every field is based on electronics, and the requirements are growing at fast pace. Power electronics can be described as one of the key elements of modern technology. The invention of microelectronics started a new era in electronics by opening a vast area of opportunities to create compact, reliable, and power-efficient new devices at a low cost. Thus, the world has become faster, efficient, connected, and more capable than ever before in history.

According to Gartner [1], global semiconductor revenue will reach about $400 billion in 2020. That is about 2x growth in just 12 years [2]. In 1950s semiconductor power devices started serving silicon as the base material. Even today, Si is dominating the industry as the main semiconductor manufacturing material [3]–[5]. However, since around 2010 Moore's law predictions are deviating from the actual manufacturing industry, calling for new inventions in microelectronics. Silicon is reaching its maximum possible capabilities in performance; especially in the high power electronics area due to its inherent material properties [3]. This has led to the idea of using wide bandgap semiconductors such as Silicon carbide or Gallium nitride [6], fulfilling the requirement of greater power efficiency. In addition to that, they are compact and lighter with the capability of usage in harsh environments [5].

1.1. Wide band gap semiconductors and power electronics

Power electronics, or the conversion of electric power using power semiconductor devices, is a concept introduced by Newall in 1973 [7]. But the power electronics efficiency is limited by the performance of the semiconductor materials they are manufactured with. Power devices are used in many aspects in different voltage regions as well as in different environments. Figure 1.1 shows the major applications of power devices in many different areas.

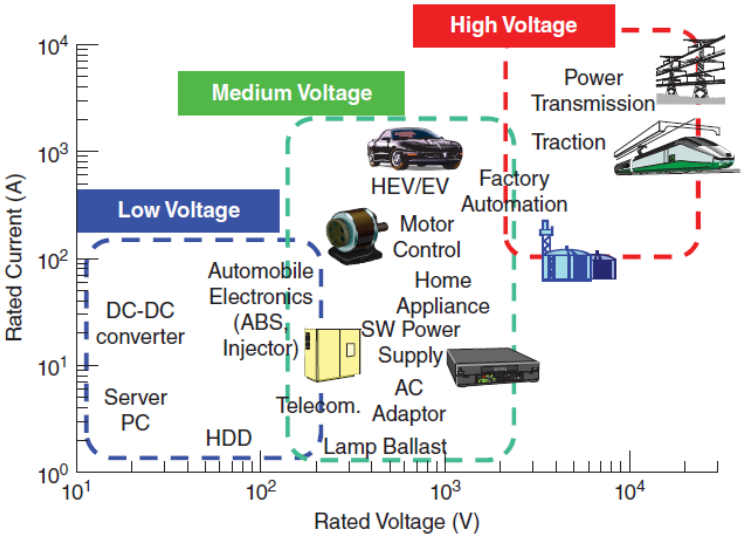

Figure 1.1: Power device application in general areas [3].

Si power devices performance has been drastically improved by developing power MOSFET (Metal-oxide-semiconductor field-effect transistor) and IGBT (Insulated Gate Bipolar Transistors), and in low-voltage and medium- voltage regions Si performs extremely well. In the high-voltage region, wide band gap semiconductors such as SiC and GaN exhibit more advantages than Si due to their physical properties as reflected by their higher figures of merit as in Figure 1.2. These semiconductors have a bandgap of 2-4 eV (forbidden bandgap). Currently SiC dominates the high voltage (1200 V and above) high power application area due

to its low level of defect density and high thermal conductivity. GaN with higher band gap dominates the mid 650 to 900 V range at high power due to the high carrier mobility of the high-electron-mobility transistors (HEMTs) and so far has been prevented to reign at higher voltages due to the absence of low defect GaN wafers. Si cannot compete with these wide bandgap materials especially at high switching frequencies [8-9]. Table 1.1 shows several wide band gap material properties in comparison with Si.

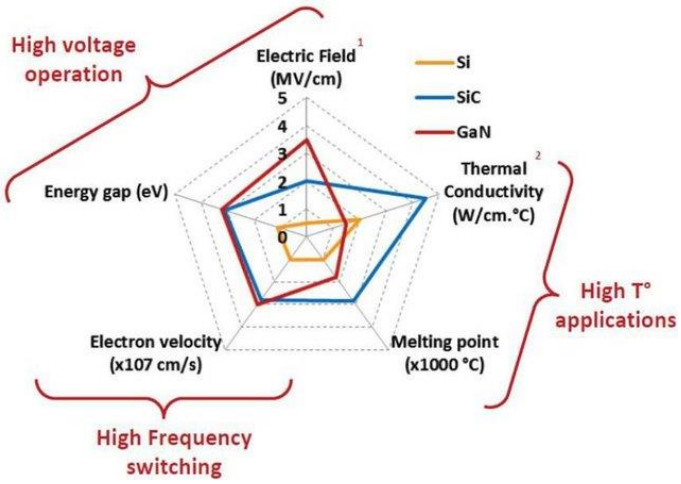

Figure 1.2: Comparison of figures of merit of Si, SiC, and GaN [8]

Table 1.1: Comparison of properties of several wide bandgap semiconductor materials [3], [6].

Properties	Si	4H-SiC	GaAs	GaN
Crystal structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy gap E_g (eV)	1.12	3.26	1.43	3.50
Electron mobility μ_n (cm^2/V.s)	1400	1000	8500	1250
Hole mobility μ_p (cm^2/V.s)	600	100	400	200
Relative dielectric constant ε_r	11.8	9.7	12.8	9.5
Electric breakdown field (MV/cm)	0.3	2.5	0.4	3.3
Thermal conductivity (W/cm°C)	1.5	4.9	0.5	1.3
Average density (g/cm^3)	2.33	3.21	5.32	6.15
Baliga's figure of Merit ($\varepsilon_s \mu_n E_c^3$)	1	317	15	870

Baliga's figure of merit (BFOM) [2] for power devices is an indicator of the impact of the semiconductor material properties on the resistance of the drift region, and a measure of power-handling capability (W/cm^2) of a power device compared to Si. It is derived from the definition of specific resistance of the ideal drift region $R_{On\text{-}ideal}$ where ε_S is the dielectric constant of the semiconductor, μ_n is the electron mobility, E_C is the critical electric field for the semiconductor breakdown and B_V is the desired breakdown voltage [2].

$$BFOM = \varepsilon_S \mu_n E_C^3 = \frac{4{B_V}^2}{R_{on-ideal}} \tag{1.1}$$

As shown in figure 1.3, a significant reduction of the ideal specific on-resistance for SiC devices over Si devices is predicted. Based on these considerations, the silicon carbide power device development took place. Pioneering work on SiC-based power devices was done in 1989 by Baliga [2], [3] and in the next decade, SiC Schottky diodes, MOSFETs, IGBTs, and Hybrid modules were commercially fabricated. By today 4H-SiC is the most advanced wide band gap semiconductor with excellent performance and enough capabilities to grow further.

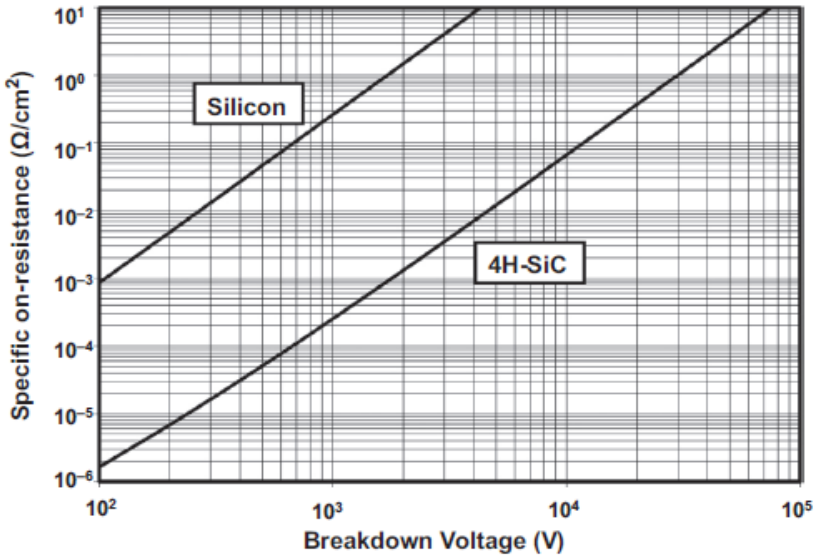

Figure 1.3: Ideal specific on-resistance for SiC compared to Si [2]

1.2. Properties of SiC

Silicon carbide or carborundum is a compound semiconductor of 50% silicon and 50% carbon. It is a rare mineral that was discovered when accidently grown by Edward G. Acheson in the 1890s while attempting to produce artificial diamonds [10]. Both Si and C atoms are tetravalent elements and they covalently bond pairing with sp^3 hybrid orbits to form SiC crystal.

1.2.1. Crystal structure

SiC can adopt different crystal structures without changes in chemical composition. The variation in the occupied sites along the c-axis in a hexagonal closed-packed system results in different SiC polytypes. SiC crystallizes in more than 200 polytypes. But mainly there are 3 types of polytypes that are relevant in semiconductor technology. As shown in Figure 1.4, they are 3C-SiC, 4H-SiC, and 6H- SiC where C- stands for cubic, and H- stands for hexagonal structures. Polytypes are represented by the number of Si-C bilayers in the unit cell and the crystal system. Here A, B, and C are the potentially occupied sites in the hexagonal closed pack structure. In 3C-SiC, ABCABC repeating sequence is followed while in 4H-SiC, and 6H-SiC, ABCB (or ABAC), and ABCACB sequences are followed, respectively.

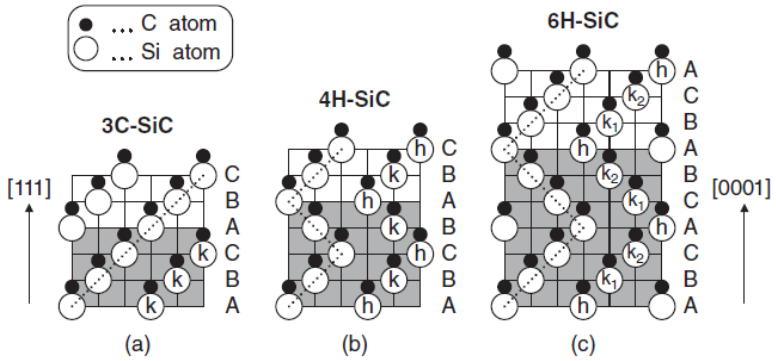

Figure 1.4: Schematic structures of (a) 3C-SiC, (b) 4H-SiC and (c) 6H-SiC polytypes (Si: opened circles, closed circled: C atoms)

The variation of major physical properties of major polytypes compared to Si is shown in Table 1.2 [3], [11]. Since 4H-SiC band gap and breakdown field strength are the largest compared to other polytypes it is considered more favorable for power electronics applications [2].

Table 1.2: Table of physical properties of major SiC polytypes (*perpendicular to the c-axis,+ parallel to the c-axis) compared to Si [3], [6]

Property	Si	3C-SiC	4H-SiC	6H-SiC
Band gap (eV) at RT	1.12	2.36	3.26	3.02
Breakdown field (MV/cm)*	0.3	1.5	2.3	1.7
Breakdown field (MV/cm)+		1.4	2.8	3.0
Bulk electron mobility (cm^2/Vs)*	1350	1000	1020	450
Bulk electron mobility (cm^2/Vs)+		1000	1200	100
Hall mobility * (cm^2/Vs) at RT	480	80	120	80
Thermal conductivity (W/cmK)	1.5	4.9	4.9	4.9
Dielectric constant*	11.8	9.7	9.7	9.7
Electron affinity (eV)	4.05	3.8	3.1	3.3

As shown in figure 1.5, mainly there are mainly 2 types of lattice sites in above polytypes as hexagonal and cubic denoted by “h” and “k” cites.

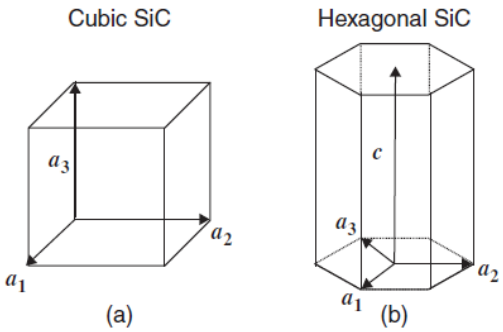

Figure 1.5: Primitive cells and fundamental translation vectors of (a) cubic (b) hexagonal SiC

The stability varies among the SiC polytypes. 4H-SiC and 6H-SiC are popular in applications and 3C-SiC is an unstable polytype that can be converted into hexagonal polytypes at a high temperature. But the thermal expansion coefficients of different SiC polytypes are similar to each other.

1.2.2. Electrical properties

All the SiC polytypes have indirect band structures. The effective mass of electrons are also strongly dependent on the polytype, but the hole effective mass is almost independent of the polytype [12]. The band gap of each polytype also increases monotonically with the increasing hexagonality and the band gap dependency on temperature as shown in Figure 1.6. Because of the thermal expansion, with increasing temperature, the band gap decreases. Also, band gap depends on the doping density as shown in Figure 1.7 for both p-type and n-type 4H-SiC, as well as for other polytypes.

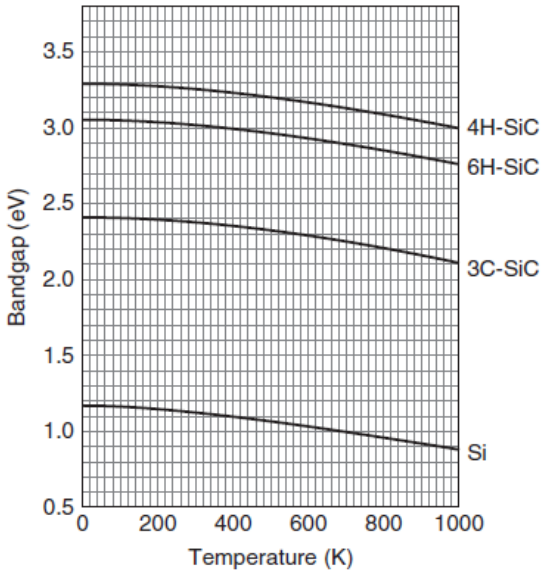

Figure 1.6: Temperature dependence of bandgap for SiC polytypes [3], [13].

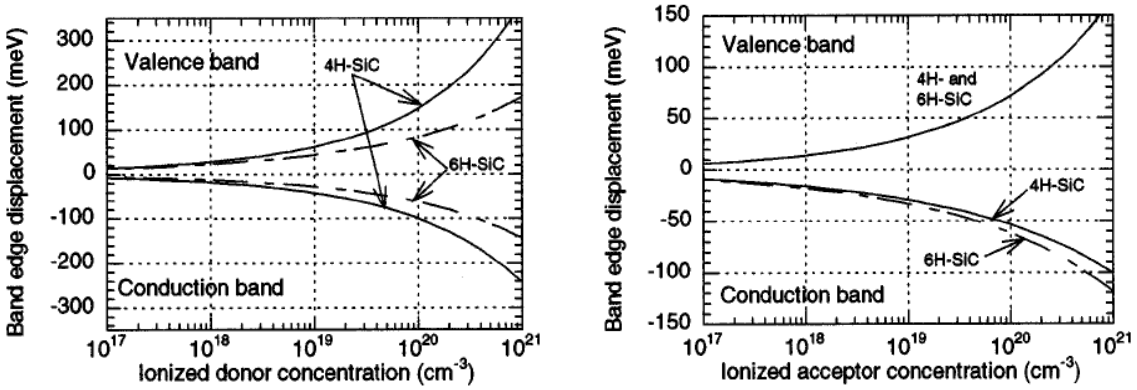

Figure 1.7: Conduction and valence band displacements for n-type and p-type SiC [14]

Normally, for n-type doping of 4H-SiC, nitrogen or phosphorus is used, while for p-type doping Aluminum is used. The free carrier density variations with temperature for n-type and p-type doped (using N and Al) 4H-SiC is shown in Figure 1.8.

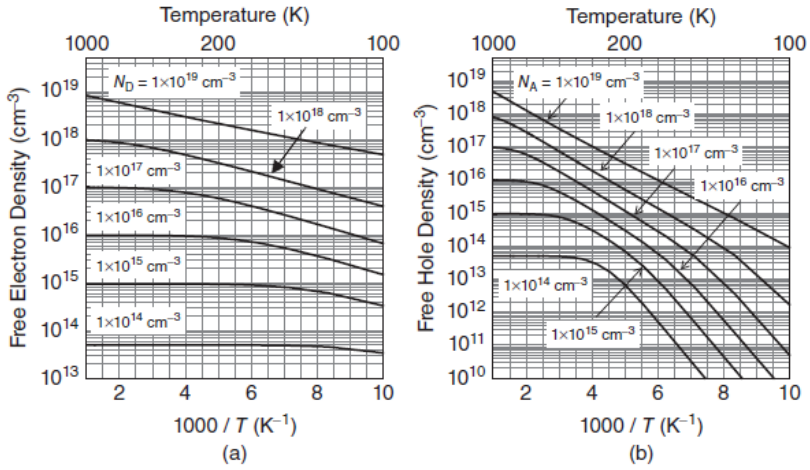

Figure 1.8: Arrhenius plots of the free carrier density of nitrogen-doped (left) and aluminum-doped (right) 4H-SiC [14].

1.2.3. SiC bulk and epitaxial growth

For device fabrications, SiC wafers are mainly produced by SiC bulk growth via the seeded sublimation method. This is also known as the physical vapor transport method. SiC powder made

by the Acheson process is used as the source material [3]. By heating the powder at a high temperature of about 2500 ˚C, SiC seed crystals are formed. Tairov and Tsvetkov [15] developed the seeded sublimation method. There, SiC source (SiC powder) is placed at the bottom of a cylindrical graphite crucible, and the SiC seed crystal is kept near the top lid of the crucible. Then the crucible is heated up to 2300-2400 ˚C controlling both thermodynamics and kinetics to grow high-quality SiC boule crystals. 6H-, 4H-, and 15R- SiC polytypes are formed around this temperature. 4H-SiC is formed at a relatively low temperature and low-pressure conditions compared to 6H polytype. The preferred polytype also can be formed by impurity incorporation. During SiC boule crystals formation many defects such as extended defects and point defects can be introduced. Micropipes, threading screw dislocations, threading edge dislocations, and basal plane dislocations are some of the extended defects observed in SiC. Over the past years, many improvements have been made to SiC wafer quality during production [3].

SiC n-type doping is performed by introducing nitrogen gas into the growth ambient by adding aluminum to the SiC source, p-type doping is performed. SiC boules are cylindrical shape and the diameter is usually 4,6 or 8 inches. After the crystallographic orientations of the boules are determined by X-ray diffraction, they are sliced into thin wafers and polished and cleaned. The quality, including flatness, sub-surface dislocations, and residual stress of wafer surface after the polishing, is critical for high-quality epitaxial growth.

For desired doping density and thicknesses of active layers of SiC, epitaxial growth is essential. Homoepitaxial growth technology via chemical vapor deposition (CVD) is used for this as the standard method. In-situ n-type doping is gained by introducing N_2; for p-type doping the addition of a small amount of trimethylaluminum ($Al(CH_3)_3$) is used during CVD growth. Different types of epitaxial defects also can be present. Extended defects such as surface morphological defects,

micropipes, dislocations (TSD, TED, BPD), interface dislocations, in-growth stacking faults, and point defects/deep levels are few of them [3].

1.3. Dielectrics

1.3.1. SiO_2 for 4H-SiC MOSFETs

One special trait both Si and SiC have in common is the native oxide, SiO_2. For MOS device fabrication, SiO_2 can be grown via thermal oxidation, wet oxidation, or plasma oxidation processes. The oxidation rates and surface chemistry are highly dependent on the SiC wafer orientation. Also, the thermal oxidation of SiC is not fully understood and considerably more complicated than Si. Thermal oxidation of SiC can be expressed by; [3], [16].

$$SiC + 1.5\ O_2 \leftrightarrow SiO_2 + CO \tag{1.2}$$

Compared to Si oxidation, in SiC the out-diffusion of CO gas is critical. The extra C involved in the oxidation could affect the oxide/semiconductor surface. It is believed that the oxide is not completely free of C, and C atoms remain near the oxide/SiC interface [17] leading to C related defects such as C-dangling bonds, C-interstitials, and C- dimers. Figure 1.9 shows a TEM image of the (0001) 4H-SiC/thermal oxide MOS structure and shows that the intensity profiles of Si, C, and O signals vary over the distance via EELS measurements. Although in TEM image a transition layer is not observed, in EELS spectra a transition layer of about 2 nm can be observed around the interface.

The specific defects introduced into the interface and oxide, during oxidation are not yet clearly identified. However possible defects are suggested to be O vacancies/interstitials, Si interstitials in addition to the C- related bonds [18]. Due to the lattice mismatch of SiC and SiO_2, stress or strain can be also be generated near the interface [19]. Through the first-principle study, Ono et al. [20] have shown that CO_2 molecules are the most preferential species at the initial stage of

oxidation, while CO emission becomes favorable as the SiO_2 layer grows. All these kinetics of the oxidation reaction may influence the oxide quality as well as the interface trap densities which will in return directly influence MOS device performance.

The oxidation thickness is highly dependent on the oxidation temperature. It varies depending on wafer orientation [16], [21] as shown in Figure 1.10.

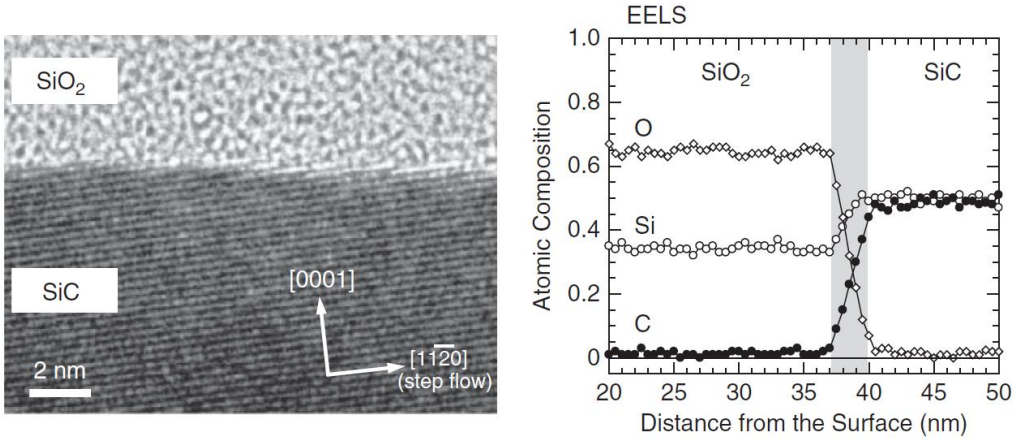

Figure 1.9: Typical cross-sectional TEM image (left) and Si, O, and C signals in EELS measurements on (0001) 4H-SiC with thermal oxide grown at 1300 ˚C [3].

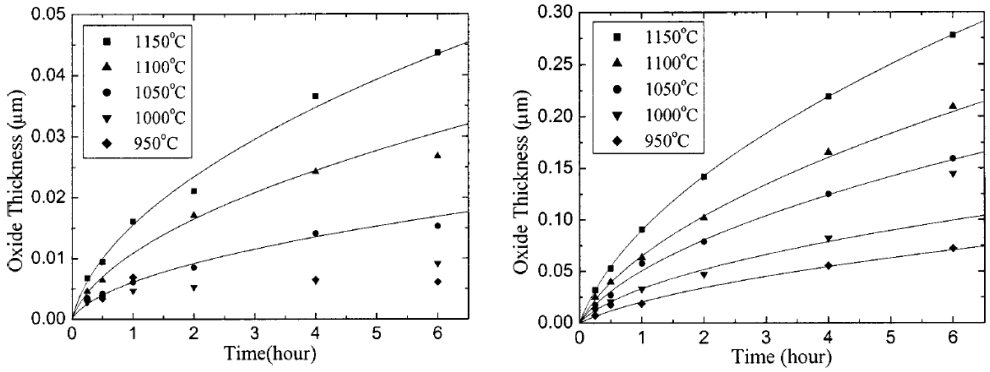

Figure 1.10: Oxidation thickness as a function of temperature and time for (0001) Si terminated (left) and (000-1) C terminated (right) 4H-SiC [16].

SiO_2/4H-SiC MOSFETs made with thermally grown SiO_2 exhibit channel mobility close to 10 $cm^2V^{-1}s^{-1}$. Compared to the bulk channel mobility of ~ 800 $cm^2V^{-1}s^{-1}$ this value is drastically low. It is believed that interface defects formed during oxidation contribute majorly to this phenomenon. Compared to Si/SiO_2 interface, in SiC/SiO_2 interface much higher interface trap densities are observed. These traps correspond to dangling bonds, C- clusters, and near interface defects located closer to the dielectric/semiconductor interface. Especially near the band edges, this trap density population is extremely high. These traps can limit channel conductance in MOSFETs and drastically affect MOS device performance in SiC/SiO_2 devices. Figure 1.11 shows the schematic representation of the density of states at the SiC/SiO_2 interface of different SiC polytypes.

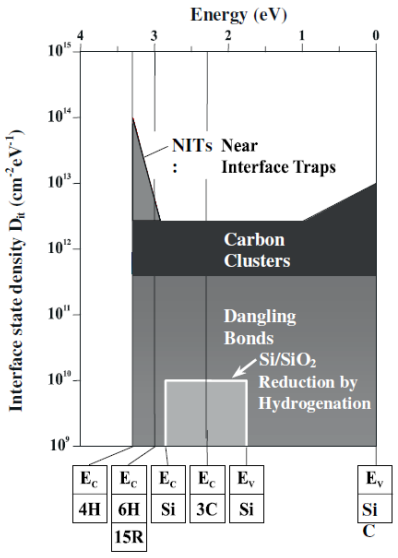

Figure 1.11: Schematic representation of the density of states at the SiC/SiO_2 interface of different SiC polytypes [22]

Many studies have evidenced that passivation methods or post oxidation annealing help to overcome this challenge. Among them nitridation via NO/ N_2O [23]–[25], H_2 annealing [26]–[28],

Phosphosilicate (PSG) [29], [30] or Borosilicate glass (BSG) incorporation [31], [32], have led to excellent channel mobility and stability improvements.

Out of the above passivation methods, NO annealing is considered as the most reliable and commercially preferable method for SiO_2/4H-SiC MOS devices. The effect of nitridation of SiC devices has been widely studied. While many possible strategies have been proposed, the exact interface chemistry resulting from nitridation and exact defect types passivated during nitridation remain less understood. Even with nitridation, MOSFET channel mobility can be improved up to about 30-50 $cm^2V^{-1}s^{-1}$[3], that is ~5% of the SiC bulk mobility. This is a limitation to overcome in order to unlock the total potential of SiC. Therefore, a more suitable passivation method than nitridation remains to be found

1.3.2. Replacing SiO_2 with alternative high-k dielectrics: Al_2O_3

Considering the pros and cons of using SiO_2 as a suitable dielectric with passivation methods to improve device performance, another promising approach for optimizing SiC device performance is using an alternative dielectric. Especially, if the chosen dielectric is a high-k dielectric, there are many added advantages compared to SiO_2, such as lower operating electric field for turn on, the lower electric field in the oxide in the high voltage 'blocking' or 'off' state, and lower channel resistance. High-k materials have a higher dielectric constant compared to SiO_2 (k=3.9) and Al_2O_3, HfO_2, ZrO_2, and TiO_2 are few of the examples for high-k materials [33]. By replacing SiO_2 with a high-k dielectric, it enables to use of physically thicker oxide to gain equivalent capacitance. This could lead to a reduction of leakage problems associated with thin SiO_2 layers. These advantages can be realized if and only if the dielectric has low bulk defect density and forms a stable interface with SiC. It is also expected to have better channel mobility than standard nitrided SiO_2. Additionally, an appropriate band-offset with 4H-SiC should be maintained for MOS device

performance. Figure 1.12 shows the plot of alternative dielectrics with their band gaps and dielectric constants. Among the possible dielectrics to be used with 4H-SiC, Al_2O_3 [34]–[38] has shown excellent channel mobilities and device performance. In addition, AlON [39], [40], HfO_2 [41]–[44] have also shown promising results for 4H-SiC MOS devices.

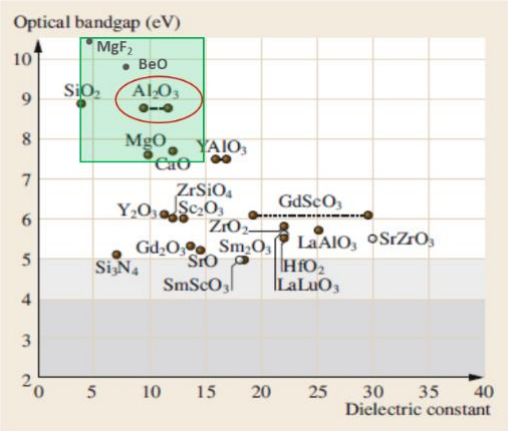

Figure 1.12: Adapted plot of dielectric constant vs. optical bandgaps of alternative dielectrics [45]

It was observed that many studies related to high-k dielectrics employ a stacked dielectric approach, by inserting a thin SiO_2 layer between the semiconductor and high-k dielectric for device performance improvements. However, there is no consensus on a specific preferred method for Al_2O_3 deposition resulting in high-performance MOS devices. Although Al_2O_3 has been widely studied, still nitrided SiO_2 dominates in performance. Some drawbacks of Al_2O_3 MOS devices have been reported such as gate leakage issues and device instability. If these could be overcome, it would be possible for using Al_2O_3 in commercial applications in the future.

1.3.3. Status of MOSFET mobilities of 4H-SiC with SiO_2 and Al_2O_3

4H-SiC MOSFET channel conductance improvements have gained the attention of many researchers in the field and has achieved a notable success over the past years. A considerable amount of research has been done aiming at the improvement of MOSFET channel electron

mobility focusing on different passivation methods, alternative dielectrics, employing different 4H-SiC wafer orientations, different oxidation conditions, using a buried channel, or using counter doping to improve device performance. Table 1.3 shows selected MOSFET peak channel mobilities μ_{FE} for (0001) Si-face 4H-SiC from literature.

Table 1.3: Some recently reported (0001) 4H-SiC MOSFET channel mobilities prepared with different approaches of dielectrics.

Year	Dielectric	Doping concentration (cm^{-3})	μ_{FE} ($cm^2V^{-1}s^{-1}$)	Reference
2001	Dry SiO_2	8×10^{16}	5	[46]
2001	NO annealed (1175 ˚C 2hr) dry SiO_2	8×10^{16}	37	[46]
2001	Thermal oxide+buried channel	5×10^{15}	140	[47]
2008	Al_2O_3+thin oxide layer	7.6×10^{15}	284	[34]
2009	NO annealed SiO_2+Al_2O_3+buried channel	-	106	[48]
2010	SiO_2+AlON	-	26.9	[49]
2013	Thermal oxide+PSG	8.3×10^{15}	80	[50]
2017	Thermal oxide with BSG+Sb	1×10^{16}	180	[51]
2018	Al_2O_3+thin oxide layer	5.3×10^{15}	125	[52]

In most of these studies, SiO_2 remains as part of the dielectric stack in some form for MOSFETs for improved device performance. Thus, the interface of oxide/semiconductor remains somewhat the same, although there is an involvement of high-k dielectric. It is clear that in all of these studies the common factor is the interface manipulation or interface chemistry change. As a result, channel

mobility changes have been observed; since the reported values are field-effect mobilities, effective mobility/Hall mobility should be greater than these values. Although the cleanliness of 4H-SiC is considered during these fabrications, a systematic study on the effect of 4H-SiC surface treatments prior to dielectric deposition is not presently reported, especially in devices [3].

1.3.4. Atomic layer deposition (ALD) of Al_2O_3

Atomic layer deposition is used to deposit material on top of substrates through self-limiting chemical reactions using gaseous precursors to the desired species. They are called self-limiting reactions as the reactions automatically stop when all the available surface functional groups are reacted with the gas-phase reactant. Depending on the material to be deposited, precursors and deposition ambient, precursor purging time durations, and temperature are optimized in a system such that, during one ALD cycle, a monolayer of material is deposited. Typically, one ALD cycle results in one atomic layer of Al_2O_3 about 0.5-1.5 Å thick [53]. Until the desired thickness is reached, the number of deposition cycles are repeated. In ALD, these precursors are alternatively added into the system and never present simultaneously as in chemical vapor deposition. ALD is a deposition yielding very uniform and precise thin films. There are two main deposition types for Al_2O_3; thermal deposition and plasma deposition. The thermal deposition is done at temperatures typically around 150-400 ˚C. The quality of thin-film can highly depend on various factors such as deposition temperature [54] and deposition system type. The plasma ALD can yield improved film quality with lower impurity levels due to the increased reactivity of precursors, but the plasma ALD equipment is more complex as a plasma source is incorporated. Compared to PECVD and PVD, ALD has several benefits. The excellent uniformity, ability to use over large substrates, relatively low substrate temperature, and the ability for reaching desired multilayer thickness are few of these benefits [55].

An ALD cycle consists of four steps as following [56]:

Step 1: Introducing the first precursor to the reactor chamber

Step 2: Purged by the flow of inert gas (usually N_2)

Step 3: Introducing the second precursor into the reactor chamber

Step 4: Purged by inert gas (usually N_2)

For standard ALD Al_2O_3, trimethyl-aluminum ($Al(CH_3)_3$)/TMA is used as the metal precursor and H_2O is often used as the oxidant precursor. Ozone (O_3) can be used as the oxidant in both thermal and plasma ALD [57]. In this work, TMA and H_2O were used at 200℃ using N_2 as the carrier gas. The growth mechanism of Al_2O_3 is shown in Figure 1.13. The initial substrate surface is hydroxylated and in the first half cycle, a short pulse of TMA is introduced in the chamber and reacts with the -OH groups on the substrate surface, while -CH_3 bonds remain exposed on the surface. Then the purge pulse removes any remaining TMA gas from the chamber. Next, an H_2O pulse is introduced that replaces -CH_3 bonds with -OH bonds on the surface. This changes the surface from methyl-terminated to hydroxyl-terminated. The final purge pulse removes remaining non-reactive H_2O from the chamber and the cycle completes with the formation of one monolayer of Al_2O_3. With the next TMA pulse, the second cycle starts. [53], [58-60]. The two reactions that take place during the deposition are as follows:

$$Al - OH^* + Al(CH_3)_3(g) \rightarrow AlO - Al(CH_3)_2{}^* + CH_4(g)$$

$$AlO - Al(CH_3)_2{}^* + H_2O(g) \rightarrow AlOAl(OH)^* + 2CH_4(g) \quad (1.3)$$

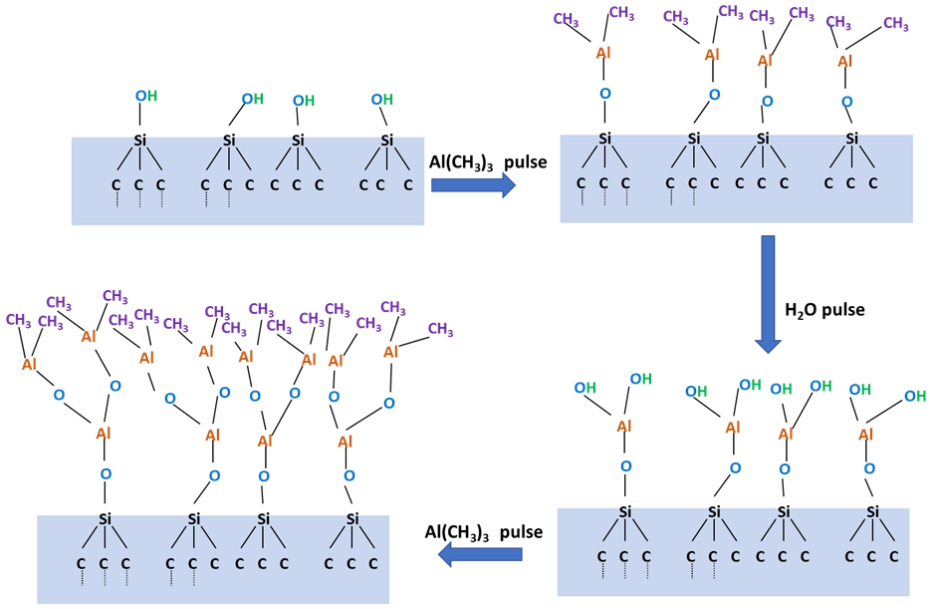

Figure 1.13: Atomic layer deposition of Al_2O_3 with TMA and H_2O as precursors.

Usually, at 200 ˚C, the thermal ALD Al_2O_3 system will deposit ~1Å/cycle on the SiC substrate. Considering the cyclical nature of the ALD process where every new layer relies on the previous, the surface termination of the initial surface is very important. If the substrate is uniformly nucleated into -OH terminated surface prior to the first TMA pulse, and the substrate is contamination minimized and defect minimized, the SiC/Al_2O_3 interface will a smoother structure. The MOSFET device channel will be formed below this interface and the defects near the interface will directly influence the channel conductance and thus the device performance.

1.4. The motivation for the dissertation work

1.4.1. CCDLTS analysis of SiO_2 and Al_2O_3 4H-SiC MOS devices

The study of interface trap densities is essential for understanding and optimizing of 4H-SiC MOSFETs [61]. While the simultaneous high-low method, conductance method, Terman method, C-ψ_S method [62], and Gray-Brown technique [63] provide information on total trap densities for

a given energy range of the band gap, the information of contributions of each trap type is missing in that data. Although we would see trap density reductions due to different passivation methods, it is important to understand which specific trap types contribute to the channel conductance reduction. That is where the need for Constant capacitance deep level transient spectroscopy (CCDLTS) [64]–[67] becomes vital. CCDLTS can be used to identify different trap types in MOS devices and quantify trap energies, trap cross-section areas, and trap densities for each trap type. In addition, these studies are extremely helpful for theoretical modeling of MOS interface chemistry.

In this study, we have studied different MOS interfaces by changing dielectrics (SiO_2 and Al_2O_3), 4H-SiC wafer orientation, 4H-SiC epitaxial doping concentrations, and various passivation methods. This information helps us understanding MOS interface similarities and differences, especially in the O1 and O2 [68] trap densities.

1.4.2. Study of 4H-SiC surface treatments on MOSFETs with deposited Aluminum oxide

During thermal oxidation, top 4H-SiC layers are consumed for oxidation and thus the SiC/dielectric interface moves towards the semiconductor. At the end of oxidation, the original 4H-SiC top surface will not be the same as the interface. However, for deposited oxides this is different. Oxide deposition will start on the 4H-SiC top surface and thus that surface is converted into the semiconductor/oxide interface at the end of the deposition. As mentioned in earlier sections, the surface chemistry of this interface directly affects the device performance.

Therefore, it opens up the question: how important is the 4H-SiC pre-deposition surface terminations via surface treatments in the determination of MOSFET performance? To our knowledge, no systematic study has been done. Some studies mention that surface treatments like

H_2 annealing [69], [70], growing a thin oxide prior to ALD [34], [37], [52], [71], and N_2 conditioning [72] result in better device performances where the top SiC surface is modified prior to ALD and gains device improvements or promising results.

The goal of this research work was to identify the effect of 4H-SiC surface treatments/surface terminations on Al_2O_3/4H-SiC MOS interface defect densities as well as MOSFET channel mobilities. Understanding the effect of 4H-SiC surface treatments will help identify steps where process development needs to be done for SiC electronic device fabrications.

Al_2O_3 is a widely studied dielectric. If we can build a methodology to optimize the 4H-SiC top surface suitable for Al_2O_3, that process could be used for other deposited dielectrics as well. Thus, in addition to the study of Al_2O_3/4H-SiC MOS devices, this study builds a platform that can be used for newly deposited dielectrics to be tested.

1.5. Thesis Outline

In chapter 2, the fundamentals of MOS device physics with electrostatics is discussed for quantifying and understanding the MOS devices are explained. This chapter contains the technical background for the analysis of chapter 3 and 4.

In chapter 3, the nature of 4H-SiC interface traps in SiO_2 and Al_2O_3 was studied using constant capacitance deep level transient spectroscopy. Near interface, trap types are quantitatively studied for various SiO_2/4H-SiC surfaces, and Al_2O_3/4H-SiC are compared.

In chapter 4, a rigorous systematic study of 4H-SiC surface treatments prior to ALD is discussed in detail with device fabrications and characterization aspects. MOS capacitor characterizations and MOSFET channel mobilities are presented with a comparison of SiO_2 and Al_2O_3.

In chapter 5, conclusions and suggestions for future work are described based on studies presented in chapters 3 and 4.

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Chapter 2

Fundamentals of device physics and characterization

The Metal-Oxide-Semiconductor (MOS) structure was first proposed by Moll, Pfann and Garrett in 1959 [1]. In 1960 the Si-SiO_2 based metal-oxide-semiconductor field-effect transistor (MOSFET) was first reported by Kahng and Atalla [2]. Following that, commercial MOSFETs produced by Fairchild Semiconductor and by RCA became available in 1964. The two-terminal MOS capacitor is the simplest and structural heart of MOS devices which can be undoubtedly named as the core structure of modern-day microelectronics [3]. The reliability and stability of all semiconductor devices are intimately related to the semiconductor surface. To study that, the MOS structure has been thoroughly used over the years. For process development as well as device fabrications and characterizations, it is essential to understand MOS fundamentals. In this chapter, the physics behind the MOS capacitor and MOSFET is discussed in detail. In addition, electrical and physical characterization methods applied for MOS devices are described with the theory behind each experimental technique.

2.1. MOS Fundamentals

2.1.1. MOS capacitor – Ideal structure and electrostatics

MOS capacitor is a two-terminal device composed of a thin dielectric layer sandwiched between a semiconductor substrate with back ohmic contact and a top gate metal layer as in Figure 2.1. Normally, the back contact is grounded, and the voltage is applied to the metal gate. Ideal MOS structure would have the following explicit properties [3];

1. The metallic gate is sufficiently thick so that it can be considered as an equipotential region
2. The oxide is a perfect insulator with no current flowing through the oxide layer under all static bias conditions
3. There are no charge centers located in oxide or oxide/semiconductor interface
4. The semiconductor is uniformly doped and sufficiently thick
5. An ohmic contact is established between the semiconductor and the back contact
6. All variables are taken to be one-dimensional parameters in x-direction as in Figure 1.

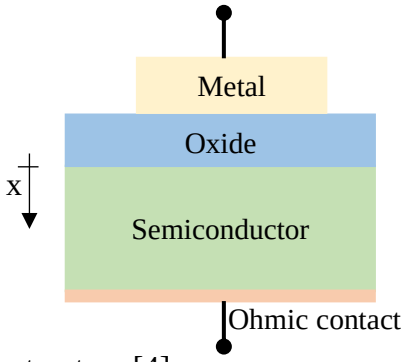

Figure 2.1: MOS capacitor structure [4]

The energy band diagrams are convenient aids in visualizing the operation of MOS devices under static biasing conditions [1], [5]. In addition, block charge diagrams can indicate information on approximate charge distributions inside a MOS structure. The ideal MOS structure for zero bias gate voltage V_G=0 is shown in Figure 2.2. Here, the energy difference between the metal work function ϕ_m and the semiconductor work function ϕ_s is zero. i.e. ϕ_{ms}=0. For n-type MOS capacitor

$$\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} - \psi_B\right) = 0 \qquad (2.1)$$

Where χ is the semiconductor electron affinity, E_g is the bandgap, ψ_B is the potential barrier between the metal and the insulator, and ψ_B is the potential difference between the Fermi level E_F and intrinsic Fermi level E_i. This is the *flat band condition,* where the bands are flat in the energy band diagram. In other words, the ideal band diagram should be in flat-band condition when no

bias is applied or at zero bias condition. There are no charges or electric fields anywhere in the metal-vacuum semiconductor system.

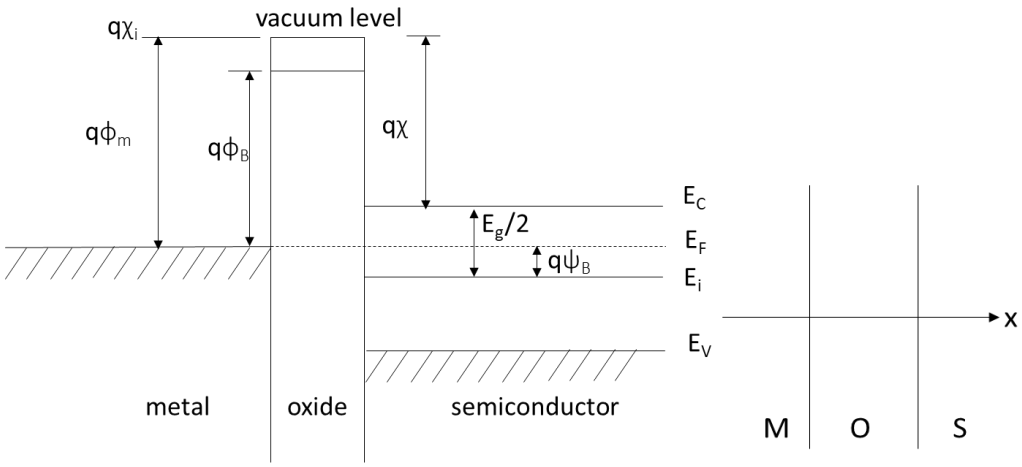

Figure 2.2: Energy band diagram of the ideal n-MOS capacitor at flat band condition at V_G=0 (left). Block charge diagram of MOS system at flat-band condition (right)

Figure 2.3 shows the band alignments of 4H-SiC with SiO_2 and Al_2O_3.Compared to SiO_2, a slightly lower semiconductor/oxide barrier height is present for Al_2O_3.

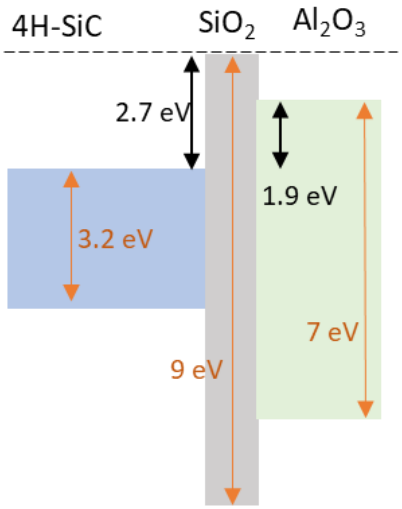

Figure 2.3: Band alignment diagram for the 4H-SiC, SiO_2 and Al_2O_3 [6]

When an ideal MOS capacitor is biased, bending of the energy bands occurs. Specific biasing regions can be distinguished such as accumulation, depletion, and inversion as a result of the continuity of the Fermi level across the MOS system. Band bending does not occur in the metal as it is an equipotential region [4], [7].

Here, electrostatic relationships for n-type semiconductor MOS devices are described, and these relationships can be applied for p-type MOS capacitors by considering reversed polarity. For an n-MOS capacitor, when a positive bias is applied to the gate metal; the application of $V_G>0$ lowers E_F in the metal relative to the E_F in the semiconductor results in a positive slope of the energy band in the semiconductor and the insulator as in Figure 2.4. This is called *accumulation* state where majority carrier concentration is larger near the oxide/semiconductor interface than in the bulk of the semiconductor.

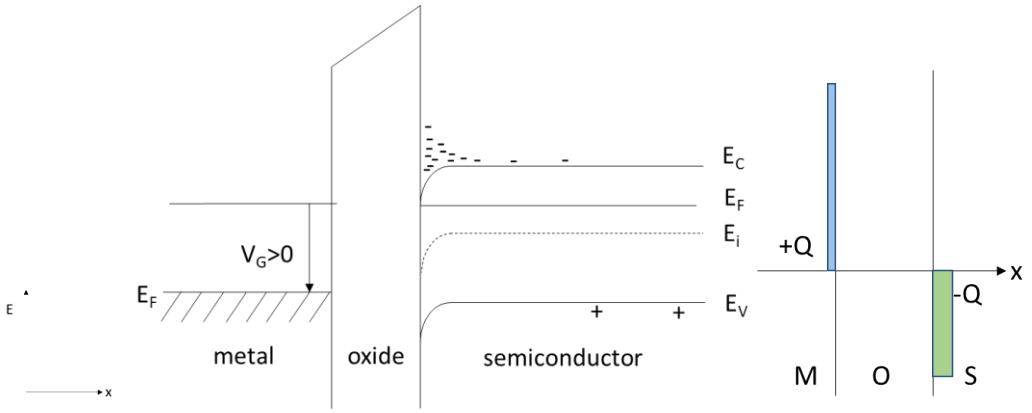

Figure 2.4: Energy band diagram of the n-MOS system at accumulation (left). Block charge diagram of MOS system at accumulation (right)

Next, for an n-MOS capacitor when a small negative bias is applied to the gate metal; the application of $V_G<0$ results in a small raise in E_F in the metal relative to the E_F in the semiconductor. This results in a negative slope of the energy band in the semiconductor and the

insulator as in Figure 2.5. This is called *depletion* state where majority carrier concentration is depleted near the oxide/semiconductor interface rather than in the bulk of the semiconductor or the background doping concentration.

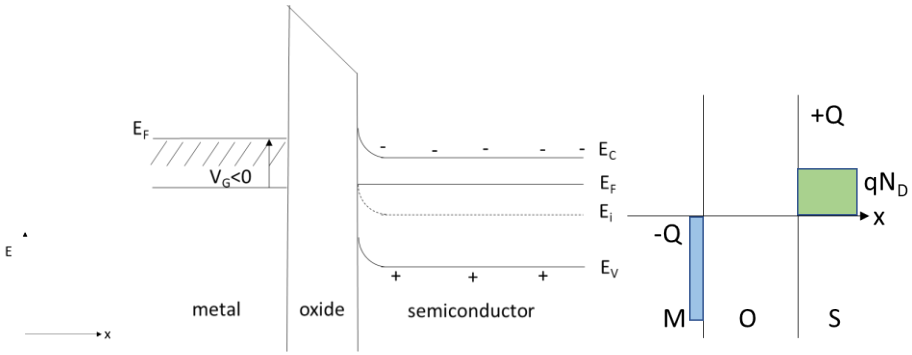

Figure 2.5: Energy band diagram of n-MOS system at depletion (left). Block charge diagram of MOS system at depletion (right)

As the next stage, for an n-MOS capacitor a larger negative bias is applied to the gate metal. The application of large $V_G<0$ results in a larger increase in E_F in the metal relative to the E_F in the semiconductor. This results in a steeper negative slope of the energy band in the semiconductor and the insulator as in Figure 2.6. This is called the *inversion* state where minority hole concentration at the surface exceeds majority electron concentration.

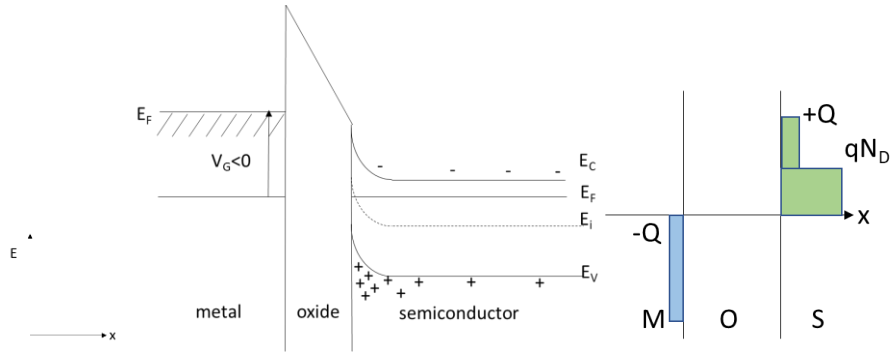

Figure 2.6: Energy band diagram of n-MOS system at inversion (left). Block charge diagram of MOS system at inversion (right)

At each bias condition, different surface potentials are created due to the difference in charges. The relationships between surface potential, space charge, and electric field can be derived for different bias regions in order to understand capacitance-voltage characteristics of MOS devices. The potential $\psi_{(x)}$ is measured with respect to the intrinsic Fermi level E_i of the bulk semiconductor where $\psi_{(x=\infty)}=0$. The semiconductor surface potential is then given by ψ_S

$$\psi_S = \frac{1}{q}\big(E_i(x = bulk) - E_i(x = 0)\big) \tag{2.2}$$

For equilibrium density of electrons and holes being n_o and p_o; the electron and hole concentrations are then given by

$$n = n_0 exp(q\psi/kT)$$

$$p = p_0 exp(-q\psi/kT) \tag{2.3}$$

at the surface, electron, and hole carrier densities respectively n_S and p_S can be written as

$$n_s = n_0 exp(q\psi_S/kT)$$

$$p_s = p_0 exp(-q\psi_S/kT) \tag{2.4}$$

depending on the surface potential, ψ_S; specific biasing conditions can be differentiated as follows for n-MOS capacitor;

$\psi_S > 0$: Accumulation of electrons (band bend downward)

$\psi_S = 0$: Flat-band condition

$\psi_B < \psi_S < 0$: Depletion of electrons (band bend upward)

$\psi_B = \psi_S$: Midgap with $n_i = n_s = p_s$

$2\psi_B = \psi_S$: Inversion when $p_s = N_D$

$2\psi_B > \psi_S$: Strong inversion $p_s > N_D$

The relationship between the electric field (ξ) and the potential ψ can be obtained by one-dimensional Poisson equation.

$$\frac{d^2\psi}{dx^2} = -\frac{\rho(x)}{\varepsilon_S} \tag{2.5}$$

where ε_S is the permittivity of the semiconductor and $\rho(x)$ is the total space charge density given by (N_D^+, N_A^- are the ionized donor and accepter densities)

$$\rho(x) = q\,(N_D^+ - N_A^- + p - n) \tag{2.6}$$

By considering charge neutrality in the bulk and solving Poisson equation, electric field at the surface can be determined as

$$\xi = \pm\frac{\sqrt{2kT}}{qL_D}F\left(q\psi_S/kT\,, \frac{n_0}{p_0}\right) \tag{2.7}$$

$$F\left(q\psi_S/kT\,, \frac{n_0}{p_0}\right) = \sqrt{\left[(e^{-q\psi_S/kT} + q\psi_S/kT - 1) + \frac{n_0}{p_0}(e^{q\psi_S/kT} - q\psi_S/kT - 1)\right]}$$

where L_D is the Debye length for majority carriers given by

$$L_D = \sqrt{\frac{kT\varepsilon_S}{q^2 p_o}} \tag{2.8}$$

In addition, the space charge per unit area Q_s required to produce this field can be determined by applying Gauss's law as following.

$$Q_S = -\varepsilon_S\xi = \mp\frac{\sqrt{2kT\varepsilon_S}}{qL_D}F\left(q\psi_S/kT\,, \frac{n_0}{p_0}\right) \tag{2.9}$$

In response to a small a.c. voltage applied in addition to a static d.c. voltage, the differential capacitance of the semiconductor depletion layer C_S can be written as

$$C_S = \frac{\partial Q_S}{\partial \psi_S} = \frac{\varepsilon_S}{\sqrt{2}L_D}\left[\frac{1 - e^{-q\psi_S/kT} + \left(\frac{n}{p}\right)\left(e^{q\psi_S/kT} - 1\right)}{F\left(q\psi_S/kT\,, \frac{n_0}{p_0}\right)}\right] \tag{2.10}$$

At flat-band condition, the differential capacitance can be found by setting ψ_S=0

$$C_{S(flat\ band)} = \frac{\varepsilon_S}{L_D} \tag{2.11}$$

Figure 2.7 shows the capacitance vs. voltage diagram for a n-type MOS capacitor. The flat band voltage (V_{fb}) separates the accumulation region from depletion region and the threshold voltage (V_{th}) separates the depletion and the inversion regions.

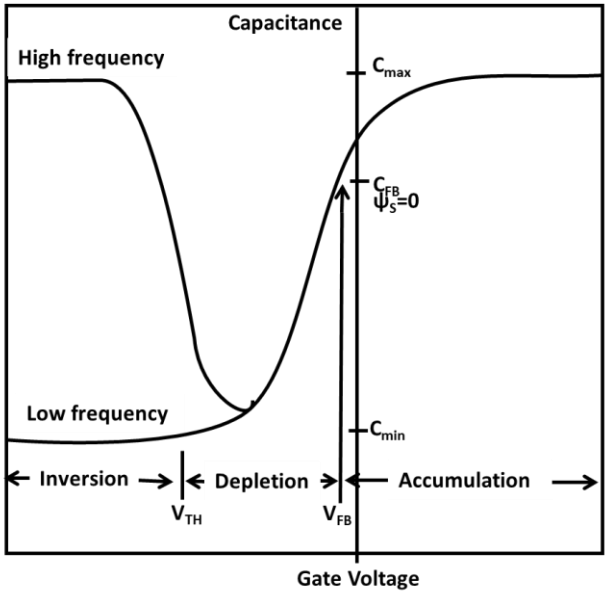

Figure 2.7: Capacitance vs. voltage diagram for a n-type MOS capacitor

When a dc bias V_G is applied to the gate metal, that applied voltage will partly appear across the oxide and partly across the semiconductor. Thus,

$$V_G = V_{ox} + \psi_S + \psi_{ms} \tag{2.12}$$

Where V_{ox} and ψ_S are the potential across the oxide and surface potential. In the absence of work function difference $\psi_{ms} = 0$; This simplifies to

$$V_G = V_{ox} + \psi_S \tag{2.13}$$

Also, by considering the electric field across the oxide width t_{ox};

$$V_{ox} = \xi_{ox} t_{ox} = \frac{|Q_S| t_{ox}}{\varepsilon_{ox}} \tag{2.14}$$

Then, the overall capacitance of the MOS system will be the addition of oxide capacitance C_{ox} and the semiconductor space charge region capacitance C_S as shown in Figure 2.8.

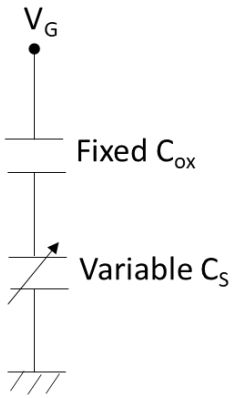

Figure 2.8: Equivalent circuit for the overall capacitance of the MOS system

Then the total capacitance of the system C can be expressed as

$$C = \frac{C_{ox}C_S}{C_{ox} + C_S} \tag{2.15}$$

At flat-band condition, the total capacitance will be C_{FB} and V_G=V_{FB} where

$$C_{FB} = \frac{C_{ox}\,\varepsilon_S/L_D}{C_{ox} + \varepsilon_S/L_D} \tag{2.16}$$

Thus, experimentally for an applied gate voltage of V_G across a MOS system.

$$V_G - V_{FB} = V_{ox} + \psi_S \tag{2.17}$$

At accumulation total capacitance is dominated by C_{ox} , therefore

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.18}$$

At depletion, the total capacitance is given by

$$C = \frac{C_{ox}\,\varepsilon_S/x_D}{C_{ox} + \varepsilon_S/x_D} \tag{2.19}$$

Where x_D is the depletion width defined as

$$x_D = \sqrt{\frac{2\varepsilon_S|\psi_S|}{qN_D}} \tag{2.20}$$

At strong inversion, $\psi_S = 2\psi_B$ condition is satisfied and the number of holes in the inversion layer will be equal to the number of ionized donors. Thus, at this moment depletion layer width reaches the maximum value of $x_{D(\max)}$

$$x_{D(\max)} = \sqrt{\frac{4\varepsilon_S|\psi_B|}{qN_D}} \tag{2.21}$$

2.1.2. n-channel lateral MOSFET

There are two major classes of transistors, as field-effect transistors (FETs) and bipolar junction transistors (BJTs), based on physics on operational mechanisms. Although the FET was invented first, BJTs predominated for many years. However, currently, FETs have surpassed BJTs in many areas due to the fabrication ease and performance in most electronic circuits. In FETs, the electric field across the gate (G) structure affects the flow of current between the other two terminals (i.e. source (S) and drain (D)). The type of FET is defined primarily by the structure of the gate and the mechanism used to apply the field [8]. Over time, the FET structure has commonly become known as Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [3].

MOSFET is a four-terminal device with gate, source, drain, and body. Often substrate/body is connected to the source and considered as a three-terminal device. Current in a MOSFET is dominated by carriers of one polarity only, and thus it is a unipolar device. In n-channel MOSFET, electrons act as the majority carrier. The basic structure of a n-channel MOSFET is shown in Figure 2.9 [1], [4] ,[8–10] .

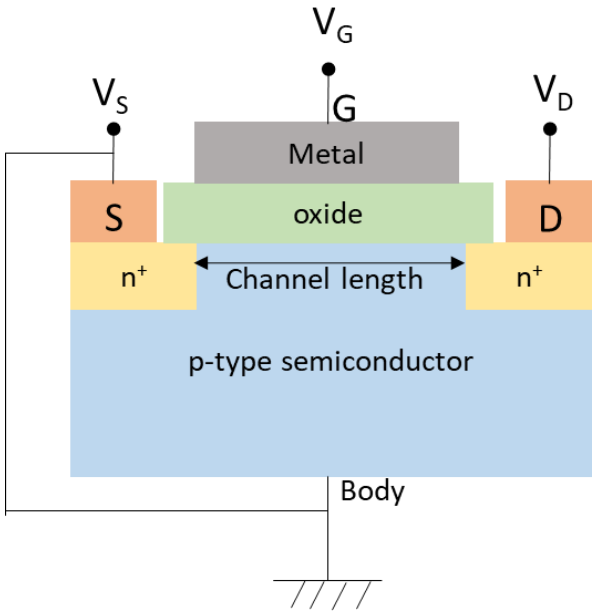

Figure 2.9: Schematic diagram of an n-channel MOSFET

When the gate is zero biased (V_G=0), the source (S) to drain (D) electrodes corresponds to two p-n junctions connected back-to-back. The only current that can flow between S and D is the reverse leakage current. With a sufficiently large positive gate bias (V_G>0), a surface inversion layer is formed at the semiconductor oxide interface which will act as a conducting channel. The conductance of this channel can be controlled by V_G [1]. The onset of strong inversion is defined in terms of the threshold voltage V_T applied at the gate.

When a gate voltage V_G (>V_T) is applied to a MOSFET, the uniform current along the channel I_D can be derived as

$$I_D = -\frac{W\mu_N}{L}\int_{V_S}^{V_D} Q_N(V_R)dV_R \qquad (2.22)$$

where μ_N is the electron mobility in the inversion layer and W and L are the width and length of the channel respectively.

A relationship between inversion charge Q_N and V_R can be obtained by delta-depletion approximation as

$$Q_N = -C_{OX}(V_G - V_T) \tag{2.23}$$

Where threshold voltage V_T is given by

$$V_T = V_{fb} + 2\psi_F + V_R + \sqrt{2V_0(2\psi_F + V_R)} \tag{2.24}$$

while the term V_0 is a constant determined by the doping and oxide thickness and has the units of volts. Thus, Q_N can be rewritten as

$$Q_N = -C_{OX}\left[V_G - V_{fb} - 2\psi_F - V_R - \sqrt{2V_0(2\psi_F + V_R)}\right] \tag{2.25}$$

Now, the MOSFET current-voltage relationship can be obtained as (using 2.26 and 2.23)

$$I_D = -\frac{C_{OX}W\mu_N}{L}\left\{(V_G - V_{fb} - 2\psi_F - V_S)V_{DS} - \frac{1}{2}V_{DS}^2 - \frac{2}{3}\sqrt{2V_0}(2\psi_F + V_S + V_{DS})^{\frac{3}{2}} - (2\psi_F + V_S)^{\frac{3}{2}}\right\} \tag{2.26}$$

In which $V_{DS} = V_D - V_S$

When the source is grounded (V_S=0), this relationship can be simplified and the familiar equation for the MOSFET can be written as

$$I_D = -\frac{C_{OX}W\mu_N}{L}\left\{(V_G - V_T)V_{DS} - \frac{1}{2}V_{DS}^2\right\} \tag{2.27}$$

As V_{DS} increases, drain voltage can result in pinch-off (i.e. channel thickness becoming negligibly small as the gate to substrate potential at the drain is smaller than threshold) , and charge in the inversion layer at the drain become zero.

Then saturation drain voltage can be written as

$$V_{D,saturation} = \left(V_G - V_{fb} - 2\psi_F - V_S\right) + V_0 - \sqrt{{V_0}^2 + 2V_0(V_G - V_{FB})} \tag{2.28}$$

The on-resistance R_{ON} at low drain voltages is also an important parameter as the power MOSFET operates in the 'on' state. The specific on-resistance of the MOSFET is given as

$$R_{ON} = \frac{L}{C_{OX}\mu_N W(V_G - V_T)} \tag{2.29}$$

2.1.3. MOSFET mobility

When a voltage V_G is applied to the gate causing an inversion at the semiconductor surface and a small V_D is applied to the drain, the current will flow from source to drain through the channel. Then the channel will have some resistance and the drain current I_d will be proportional to the drain voltage V_D. As long as this proportionality is held, that area is called the linear region. As this V_D is increased, eventually it will reach pinch-off point where channel depth reduces to zero. From that point onward I_d will remain essentially the same; this region is called the saturation region. Figure 2.10 shows the drain characteristics of a MOSFET based on the applied gate voltage.

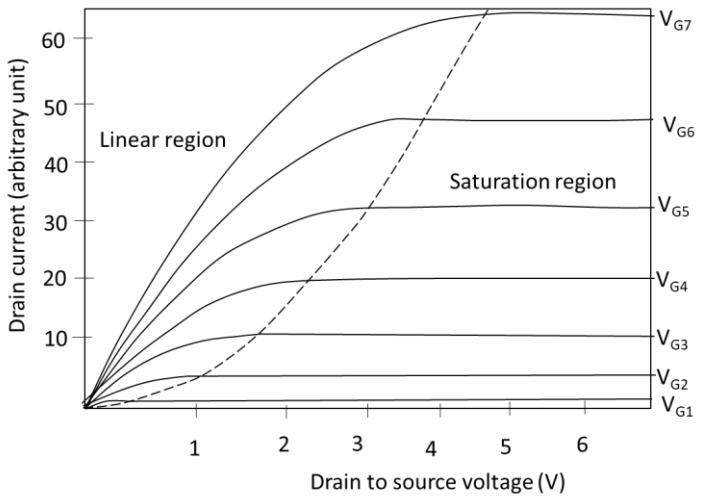

Figure 2.10: Drain characteristics of a MOSFET

Field-effect mobility

Channel conductance is given by

$$g = \frac{W}{L}\int \sigma(x)dx \tag{2.30}$$

Where σ is the conductivity of the channel due to electrons.

For the case of small V_D i.e. in the linear region of the MOSFET, for $V_D << (V_G - V_T)$, using equation (2.28)

$$I_D = \frac{C_{OX} W \mu_N}{L} [(V_G - V_T) V_{DS}] \tag{2.31}$$

Where are L, W and C_{ox} are MOSFET gate length, width, oxide capacitance respectively and V_T is

$$V_T = 2\psi_B + \frac{\sqrt{2 \in_S qN_A(2\psi_F)}}{C_{ox}} \tag{2.32}$$

By plotting I_d vs. V_G, the V_T can be obtained from the linearly extrapolated value at the V_G axis.

In the linear region transconductance, g_m can be defined as

$$g_m = \frac{\partial I_d}{\partial V_G} | V_{D=constant} = \frac{C_{OX} W \mu_{FE} V_{DS}}{L} \tag{2.33}$$

Where μ_{FE} is the Field-effect mobility

$$\mu_{FE} = \frac{L g_m}{C_{OX} W V_{DS}} \tag{2.34}$$

Differently, the field-effect mobility can be expressed as

$$\mu_{FE} = \frac{\mu_{real}}{1 + \frac{q^2 D_{it}(E_F)}{C_{inv}}} \tag{2.35}$$

where $D_{it}(E_F)$ is the interface state density at a Fermi level and C_{inv} is the differential capacitance of the inversion layer. Thus, the estimated channel mobility is underestimated compared to the real channel mobility by the conductance method because of the interface trapping issue. μ_{real} can be determined by MOS-Hall effect measurements, by directly determining the sheet density of mobile carriers as a function of gate bias [11].

Effective mobility

Another measure associated with MOSFET channel conductance is effective mobility μ_{eff}, in which drain current is considered as a combination of drift and diffusion currents as [7];

$$I_D = \frac{W\mu_{eff}Q_nV_{DS}}{L} - \frac{W\mu_{eff}kT}{q}\frac{dQ_n}{dx} \tag{2.36}$$

where Q_n is the mobile channel charge density. Usually μ_{eff} is measured at lower V_{DS}. Then channel charge is more uniform and allows the second term in the equation to be considered negligible. Then μ_{eff} can be determined as

$$\mu_{eff} = \frac{g_dL}{WQ_n} \tag{2.37}$$

Where

$$g_d = \frac{\partial I_d}{\partial V_D}|V_{GS=constant} \tag{2.38}$$

To determine Q_n there are two approaches.

(a) Using mobile channel charge density approximation as $Q_n = C_{OX}(V_{GS} - V_T)$, but this approximation has some deficiencies.

(b) The better approach is the direct measurement of Q_n from capacitance measurements solving $Q_n = \int_{-\infty}^{V_{GS}} C_{GS}d\,V_{GS}$; but still in the sub-threshold region where $V_{GS} < V_T$ the drain current is mainly due to diffusion and the validity of μ_{eff} (defined as above) is questionable. Also, capacitance should be measured at high frequency to avoid the interface trap contribution in the capacitive component [7].

Hall mobility

The total density of induced electrons in a MOSFET is given by [1], [11]

$$n_{total} = n_{mobile} + n_{trap} \tag{2.39}$$

Where n_{mobile}, n_{trap} are the densities of mobile electrons and electrons trapped at interface states respectively. Then the calculated mobility μ_{ch} is related to the real mobility μ_{real} as

$$\mu_{ch} = \mu_{real} \frac{n_{mobile}}{n_{mobile} + n_{trap}} \tag{2.40}$$

The real mobility of mobile electrons can be extracted by MOS-Hall effect measurements. In addition to μ_{real}, the total density of induced electrons and real mobile electron density also can be determined using Hall measurements.

In Hall measurements, a magnetic field B is applied perpendicular to the direction of current flow in a MOSFET as shown in Figure 2.11

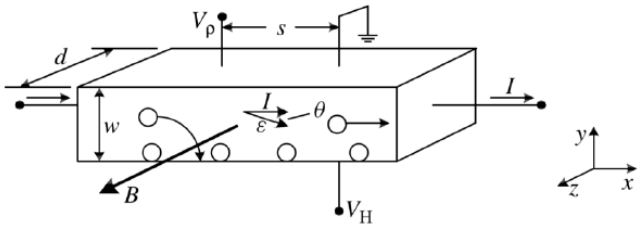

Figure 2.11: Schematic of Hall measurement setup for a p-type semiconductor [7]

For a p-type semiconductor, the motion of holes can then be written as a combination of electric force and Lorentz force

$$F = q(E + v \times B) \tag{2.41}$$

Then the Hall coefficient R_H is defined as

$$R_H = \frac{dV_H}{BI} \tag{2.42}$$

Where $V_H = E_y d$ and then Hall mobility is computed as

$$\mu_{Hall} = \frac{R_H}{\rho} \tag{2.43}$$

Where resistivity $\rho = \frac{wdV_\rho}{sI}$ where w, d, s are semiconductor parameters shown in the Figure 2.11. Hall mobility measurements are vital for building theoretical models related to channel conductance and identifying the effect of interface defects in MOSFETs as the real channel mobility is only obtained via this method.

2.1.4. Mobility limiting mechanisms

For SiC, n-channel conductance is mainly limited especially by high density shallow interface states near the conduction band edge as trapping results in lower than ideal carrier concentration. But, the channel mobility in 4H-SiC MOSFETs is more complicated than in Si. In addition to Coulomb scattering from charged traps, surface roughness and large fluctuation of surface potential can also affect channel mobility. In general, 4H-SiC MOSFETs often show negative correlation between the channel mobility and the threshold voltages determined by linear extrapolation of the I_d-V_g curves as in Figure 2.12.

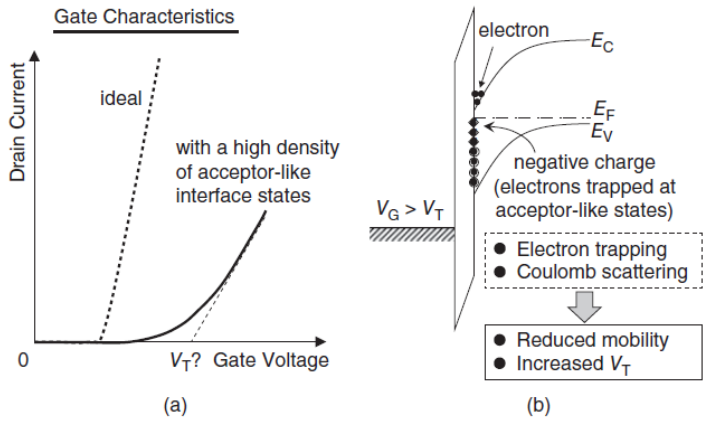

Figure 2.12: Effect of interface trap densities in channel mobility and threshold voltage. (a) Degradation of gate characteristics due to a high density of interface states, (b) major limiting factors of channel mobility in 4H-SiC MOSFETs [11].

Channel mobility decreases when threshold voltage is increased. When the interface trap density near the conduction band is increasing, more electrons will be trapped in the interface leading to a decrease in the drain current and a gradual increase of the threshold voltage. However, more fundamental studies are needed to relate interface defects and carrier transport properties in the inversion layers.

The electron mobility μ_N in the inversion layer of a (0001) 4H-SiC MOSFET is only about 5-10% of the bulk mobility [11]. Electron mobility in the inversion layer is limited by several mechanisms including: 1. surface-phonon scattering, 2. Coulomb scattering, and 3. surface roughness scattering. Resulting carrier mobility is inversely proportional to the total scattering rates from different mechanisms and by Matthiessen's rule, resultant mobility μ_N can be written as [11]

$$\frac{1}{\mu_N} = \frac{1}{\mu_B} + \frac{1}{\mu_P} + \frac{1}{\mu_C} + \frac{1}{\mu_S} \tag{2.44}$$

where μ_B is the mobility of electrons in the bulk semiconductor, μ_P is the mobility limitation by surface phonon scattering, μ_C is the mobility limitation by Coulomb scattering, and μ_S is the mobility limitation by surface roughness scattering. There are several reasons for Coulomb scattering such as ionized impurities or charges at or near the MOS interface. Surface roughness scattering can be aroused by structural and stoichiometric disorders at the interface.

Noguchi et al. [12] have recently investigated the effect of each scattering mechanism on Si-face NO annealed 4H-SiC/SiO_2 MOSFETs using Hall mobility measurements as

$$\frac{1}{\mu_{Hall}} = \frac{1}{\mu_P} + \frac{1}{\mu_C} + \frac{1}{\mu_S} \tag{2.45}$$

According to their findings, dominant limiting factors of inversion layer mobility in Si-face 4H-SiC were concluded as Coulomb and phonon scattering only. The contribution of surface roughness scattering was negligible even at higher electric fields as shown in Figure 2.13.

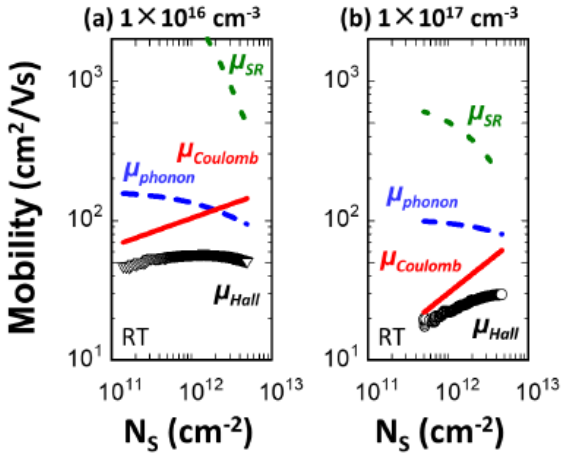

Figure 2.13: Dominant limiting factors of inversion layer mobility in nitrided Si-face 4H-SiC was found to be mainly coulomb and phonon scatterings [12]

2.2. Interface trap characterization

2.2.1. Interface trap fundamentals

There are four main types of charge in the oxide-semiconductor system as shown in Figure 2.14 They include 1. fixed interface charge (Q_f), 2. oxide-trapped charge (Q_{ot}), 3. Interface trapped charge (Q_{it}) and 4. mobile charge (Q_m) with corresponding trap numerical trap densities (units: cm^{-2}), N_f, N_{ot}, N_{it} and N_m respectively. Q_f is considered to be located within a thin layer away from the interface while Q_{ot} is both negative and positive traps located throughout the oxide. Q_{it} is located directly at the interface and Q_m is usually from contaminations (alkali-metal ions) that are readily absorbed into the oxide [10], [13]. Interface trapped charges (Q_{it}) are also called interface states, fast states, or surface states and they exist within the forbidden gap due to the interruption of the periodic lattice structure. Q_{it} can be either donor or acceptor like.

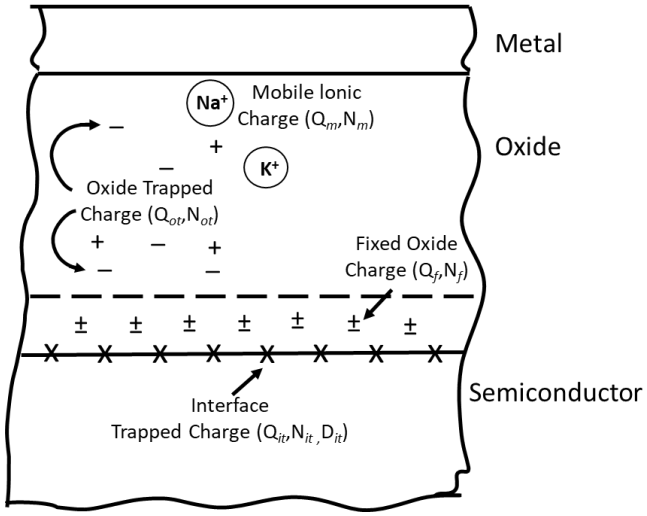

Figure 2.14: Various oxide charges in the MOS system [1]

Acceptor like interface traps are in the upper half of the bandgap and donor like type traps are located in the lower half of the bandgap. A trap is considered a donor type if it can become neutral or positive by donating an electron. An acceptor type is defined as a trap capable of accepting an electron and become negative or neutral. When a voltage is applied/light is illuminated/or the sample is heated or cooled, interface trap levels move up or down with the valance and the conduction bands while the Fermi level remain fixed [1]. Interface states are distributed with density D_{it} (units: $cm^{-2}eV^{-1}$) within the forbidden-gaps energies as in Figure 2.15.

For WBG materials like SiC, electrons trapped at deep acceptor levels act as if they were "negative fixed charges" while holes trapped at deep interface states behave as if they were "positive fixed charges". On SiC (0001), the interface state density increases in an exponential manner toward the conduction band edge. Due to this rapid increment with increasing energy levels, the interface state density near the band edge is very high for 4H-SiC (0001). In n-channel MOSFETs, when electrons in the inversion layer get trapped in these interface states, they become almost immobile. The trapped electrons can act as Coulomb scattering centers as well. Therefore, the acceptor-like states

near the conduction band edge are affecting n-channel mobility. This results in poor channel mobility (5–8 $cm^2V^{-1}s^{-1}$ for as oxidized samples) for 4H-SiC(0001) MOSFETs [11].

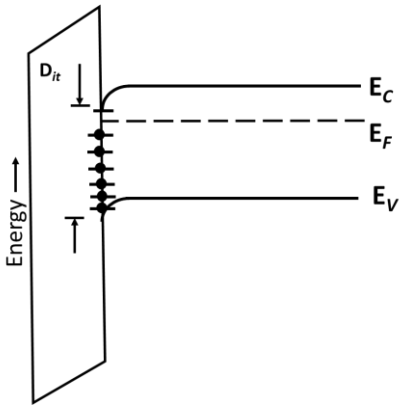

Figure 2.15: Energy levels at the oxide/semiconductor interface showing D_{it} within the forbidden energy gap for n-type MOS device at accumulation. Lines with balls indicate filled interface traps and hollow lines represent unoccupied traps [1].

Interface traps are positive or negative charges, introduced by structural defects, oxidation-induced defects, metal impurities, or other defects caused by radiation or similar bond-breaking processes. Many types of interface traps have been proposed or identified for the SiO_2/SiC interface. Few of them are Si interstitials, Carbon dimers, and Oxygen vacancies [11]. Electrical characterization methods such as simultaneous high-low capacitance-voltage measurements, Gray-Brown technique, Constant capacitance deep level transient spectroscopy can quantitatively determine interface trap densities. These methods are extensively used in this dissertation work and are therefore discussed next.

2.2.2. Simultaneous high-low frequency capacitance-voltage method

The simultaneous high-low frequency method is a common interface trapped charge measurement method developed by Berglund [14]. The method compares CV curves of high and low frequencies

measured at every dc bias point simultaneously. The low- and high- frequency CV measurements are performed in the quasi-static mode and at frequencies between 100 kHz-1 MHz, respectively. The two main assumptions considered are that the interface states completely respond during a low-frequency or quasi-static measurement and do not respond at all for high-frequency measurement. Considering the interface trapped charge, the total capacitance at depletion will be the addition of semiconductor capacitance (C_s) and capacitance due to interface traps (C_{it}) in series with oxide capacitance (C_{ox}) as shown in Figure 2.16 [4], [11], [13].

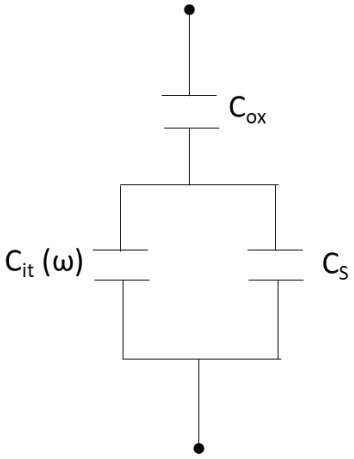

Figure 2.16: Equivalent circuit for overall capacitance with interface traps response

Total capacitance at low frequency/quasi-static mode C_{LF} will be

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_S + C_{it}} \tag{2.46}$$

But C_{it} will not contribute (C_{it}=0) to the total capacitance at high -frequency mode (C_{HF}) and

$$\frac{1}{C_{HF}} = \frac{1}{C_{ox}} + \frac{1}{C_S} \tag{2.47}$$

C_{it} can be expressed as

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right]^{-1} \tag{2.48}$$

C_{it} can be related to interface trap density by $D_{it}=C_{it}/q^2$ and D_{it} is given by

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{C_{LF}/C_{ox}}{1 - C_{LF}/C_{ox}} - \frac{C_{HF}/C_{ox}}{1 - C_{HF}/C_{ox}}\right) \tag{2.49}$$

But in reality, for WBG SiC the quasi-static capacitance does not detect traps with slow emission rates while high-frequency capacitance may include traps with fast emission rates. Therefore, the interface trap density D_{it} obtained by the simultaneous high-low CV method underestimates actual interface trap densities. But this can be corrected to some extent by measuring capacitance over a wider temperature range such that to obtain faster trap densities at low temperature and slow trap densities at high temperature. D_{it} extracted from the simultaneous high-low method is valid accurately for a limited energy range when used on SiC. For room temperature measurements it is about 0.2 eV-0.6 eV below the conduction band edge. Trap energies are extracted by using the surface potential ψ_S, bulk potential ψ_B and the band gap E_g of the semiconductor.

$$E_C - E = \frac{E_g}{2} + \psi_S - \psi_B \tag{2.50}$$

Apart from D_{it}, other important parameters like oxide capacitance C_{ox}, oxide thickness t_{ox}, Doping concentrations N_D/N_A, and flat band voltage V_{fb} also can be extracted by capacitance-voltage measurements.

2.2.3. C-ψ_s method

As it was mentioned in the previous section, the simultaneous high-low capacitance technique underestimates D_{it}. Especially for SiC, D_{it} near the conduction band edge or the shallow region is much higher is responsible for low channel mobility. Therefore, it is essential to determine shallow D_{it}. Yoshioka et al. [11], [15] proposed a method called "C-ψ_s Method" to accurately determine the surface potential based on the depletion capacitance and to evaluate D_{it} by determining theoretical capacitance in SiC MOS devices.

Surface potential ψ_S is first calculated using:

$$\psi_S(V_G) = \int \left(1 - C_{QS}/C_{ox}\right) dV_G + \bar{A} \tag{2.51}$$

In which constant $\bar{A}$ is determined by plotting $\frac{1}{(C_S+C_{it})^2}$ vs ψ_S and extrapolating

$$\frac{1}{(C_S + C_{it})^2} = \frac{2\psi_S}{A^2 \varepsilon q N_D} \tag{2.52}$$

Where C_S is the semiconductor capacitance, C_{it} is the interface state capacitance, A is the area of the gate electrode, ε is the semiconductor dielectric constant and N_D is the donor concentration in the n-type SiC.

After ψ_S is extracted, theoretical semiconductor capacitance can be determined as follows

$$C_{s,theory}(\psi_S) = \frac{AqN_D\left|\left(exp(q\psi_S/kT)\right) - 1\right|}{\sqrt{\frac{2kTN_D}{\varepsilon}\left[\left(exp(q\psi_S/kT)\right) - (q\psi_S/kT) - 1\right]}} \tag{2.53}$$

Then D_{it} is evaluated as

$$D_{it} = \frac{(C_S + C_{it})_{QS} - C_{s,theory}}{Aq^2} \tag{2.54}$$

This D_{it} includes fast interface states without frequency limit and this method only requires a low frequency/quasi-static capacitance-voltage measurement. But since this method highly depends on the accuracy of the surface potential as does the high-low method, if the doping density varies along with the depth, the determined D_{it} will have an associated error.

2.2.4. Gray-Brown technique

Gray et al. [16] proposed a measurement method to determine the change in surface charge by obtaining flat band voltages at two different temperatures (300 K and 77 K). Following that, shallow trap densities (D_{it} << 0.2 eV below conduction band for 4H-SiC) can be extracted for MOS capacitors by comparing CV measurements obtained at room temperature and low temperature [17]. The reduction of temperature causes bulk Fermi level to shift closer to conduction band edge,

results in a change in occupancy of interface traps. As a result of this, CV shift/V_{fb} shift is observed. Using Gray-Brown technique, the density of interface states (N_{it}) can be determined by

$$N_{it} = \frac{C_{ox}}{Aq}\left(V_{fb(T1)} - V_{fb(T2)}\right) \tag{2.55}$$

where $V_{fb(T1)}$ and $V_{fb(T2)}$ are the flat band voltages at given two different temperatures. C_{ox} is the oxide capacitance and A is the area of the MOS capacitor.

Figure 2.17 shows 1 MHz frequency CV curves obtained at 298 K and 77 K for NO annealed SiO_2/4H-SiC MOS capacitor. For this temperature range N_{it} can be calculated from ~E_c-0.05 eV to E_c-0.2 eV [17] from the conduction band edge of 4H-SiC. Over the simultaneous high-low method, the Gray-Brown method gives additional information, especially on shallow trap densities. This region is extremely important to analyze as high D_{it} near the conduction band edge is responsible for 4H-SiC poor channel mobility [18].

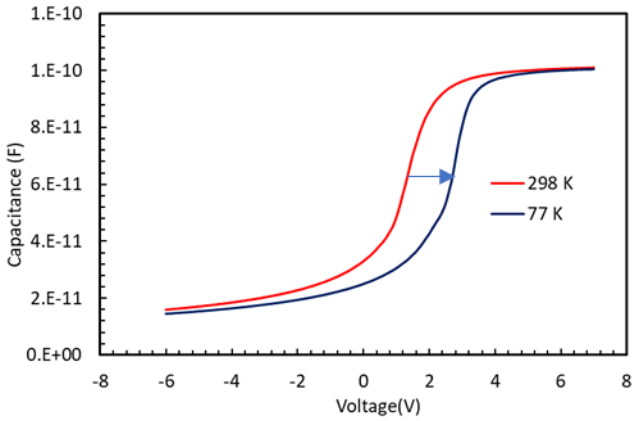

Figure 2.17:1 MHz frequency CV curves obtained at 298 K and 77 K for NO annealed SiO_2/4H-SiC MOS capacitor

2.2.5. Constant capacitance deep level transient spectroscopy (CCDLTS)

Constant capacitance deep level transient spectroscopy (CCDLTS) [19] can be used to analyze and differentiate interface trap levels or defects in the MOS structure. While all the above discussed

measurement techniques provide information on trap densities in a specific part of the energy bandgap, CCDLTS, proposed by Johnson et al. [20], [21] can identify the energy levels and trap cross-sections separately for each trap type. This is useful in understanding interface chemistry and chemical bonding nature of the interface to explain reasons for interface defects. It also is important for understanding how these defects can affect channel mobilities and performance of MOSFETs. Basically, temperature dependent emission activation energies can be obtained via emission rates using CCDLTS technique for characterization of 4H-SiC MOS interfaces.

The CCDLTS technique is derived from the DLTS technique [22]. Through a feedback loop circuit, the MOS device is held at a constant capacitance C_P biased at depletion throughout the measurement while the device is pulsed by a bias voltage from depletion to accumulation as shown in Figure 2.18.

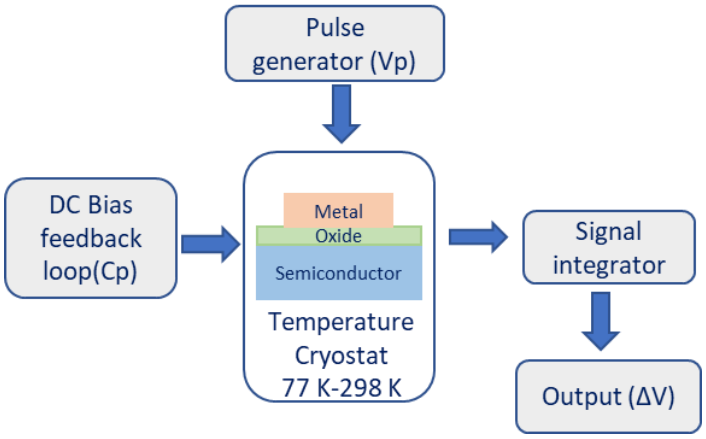

Figure 2.18: Schematic of the basic CCDLTS setup

The voltage pulse will result in charging and discharging; thus, electron capture, and emission will take place in trap levels. Meanwhile, the pulsing will be continuously carried out for a range of temperatures (from 77 K to 298 K for most of our analysis). Since the MOS device is held at constant capacitance, when charging and discharging occurs a transient signal will be generated

(at each temperature) that can be measured as a CCDLTS signal (ΔV). This signal will be maximized at some temperature depending on the emission activation energy of the trap. Each peak in the spectrum would represent a specific trap type.

In a MOS capacitor, the gate voltage or the pulse voltage V_P will drive the MOS device from depletion to accumulation, and interface states are populated with the electron (majority carries) as shown in Figure 2.19. When the device is returned to the deep depletion state, interface states will be in a non-equilibrium state with trapped charge and they will relax by thermal emission of electrons to the conduction band.

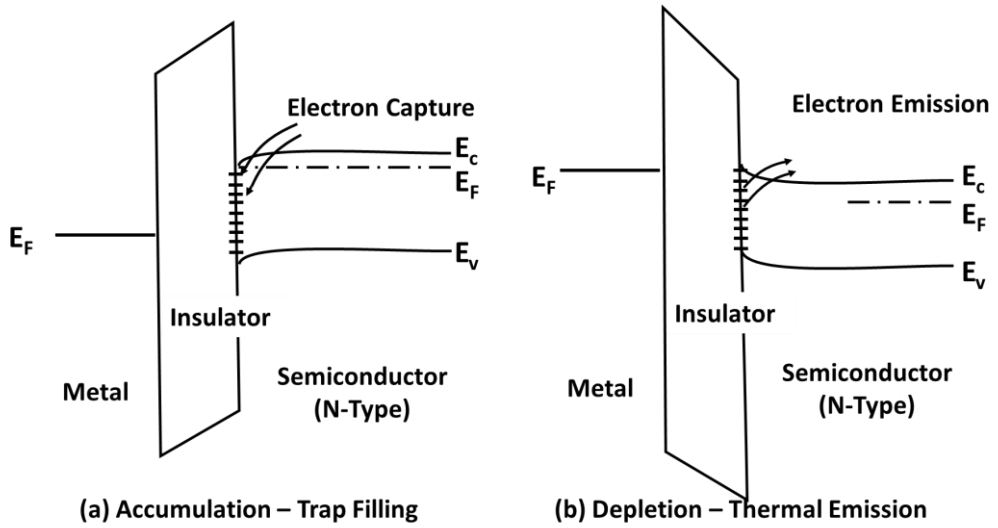

Figure 2.19: Energy band diagram for n-type MOS device for (a) trap filling at accumulation (b) trap emission at depletion bias [21]

Experimentally, the device is biased in depletion as shown in Figure 2.20 with capacitance C_{hf} and gate bias V_{dc}. Then the pulse V_p (usually 25 ms width) is applied driving the device into accumulation and then at the end of the pulse, the device returns back to depletion but not to the exact previous state as the non-equilibrium occurred due to interface traps. The CCDLTS signal [$\Delta V=V(t_1)-V(t_2)$] is measured by forming the difference of gate voltages at two delay times t_1 and

t_2 (with t_2=2.5 t_1) after the charging pulse as in Figure 2.21. Experimentally t_1 and t_2 can be changed by changing spectrometer rate windows (τ^{-1}_{max}) or the initial delays (ID) of the setup. The CCDLTS signal will be maximized when the trap emission rate, e_n matches the spectrometer rate window (τ^{-1}_{max}).

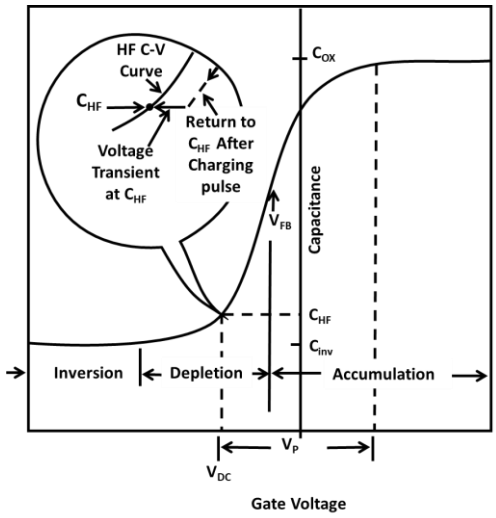

Figure 2.20: High-frequency CV characteristics of the MOS capacitor for pulsing during CCDLTS measurement [21]

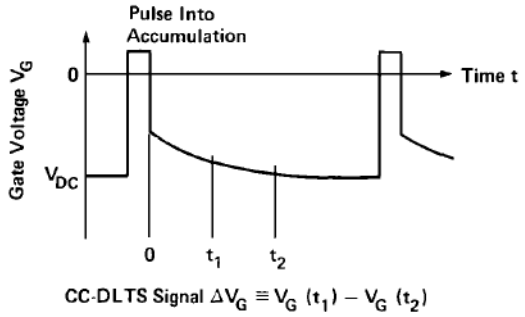

Figure 2.21: CCDLTS measurement during thermal emission of interface traps [21]

According to collision theory, molecules/species must collide to react. A reaction would occur when the minimum amount of energy required for that reaction is satisfied and this is called the activation energy. But the reaction rate is controlled by both activation energy and the temperature.

Arrhenius equation correlates rate constant of a reaction ($\bar{k}$), with activation energy (E_a) and temperature (T). F_0 is called the frequency factor which will depend on frequency of collisions and orientation of species during the collision and k is the Boltzmann constant.

$$\bar{k} = F_0 \exp\left(\frac{-E_a}{kT}\right) \tag{2.56}$$

For a specific reaction with a fixed activation energy, rate constant will be changed as temperature of the system change. Using Arrhenius relationship, activation energies of each trap type in MOS interfaces can be obtained using CCDLTS as the thermal emissions of electrons are measured by varying the temperature of the MOS system during measurements.

Electron emission rate e_n is given by:

$$e_n = \sigma_n v_n N_C \exp\left[-\frac{(E_c - E_T)}{kT}\right] \tag{2.57}$$

Where σ_n is the electron capture cross-section, $v_n = \sqrt{3kT/m^*}$ is the electron thermal energy, $N_C = 2(2\pi m^* kT/h^2)^{3/2}$ is the effective density of states in the semiconductor conduction band, E_c is the conduction band energy and E_T is the trap activation energy. Here $E_a = E_c - E_T$ and m* is the effective mass of the electron.

For different rate windows, CCDLTS spectrums are obtained, and thus the temperature of the peak position (T_0) of each spectrum is noted. Using the Arrhenius plot of ln (T_0^2/e_n) vs (1/ T_0), the trap activation energy (E_c-E_T) and the capture cross-section σ_n can be determined using slope and the intercept for each trap type for each corresponding peak.

The density of each interface trap type can also be determined by CCDLTS as [23];

$$N_{it} = \frac{3.C_{ox}.\Delta V(T_0).\Delta W}{q} \tag{2.58}$$

where C_{ox} is the oxide capacitance per unit area, $\Delta V(T_0)$ is the amplitude of the CCDLTS signal at peak temperature, and ΔW is the ratio of the integrated CCDLTS intensity over the measured temperature range to the integrated intensity of the CCDLTS signal. This technique has been extensively used in this dissertation as detailed in chapter 3.

2.3. Physical Analysis

In semiconductor device fabrications and characterizations, optical analysis is extremely important. Depending on the feature size and resolution, we can select between methods to do the optical analysis. During MOS device fabrications it is essential to do optical analysis in each step for alignments, to detect contaminations and for process optimization. But none of these, methods are useful to identify and characterize semiconductor/oxide interface defects we are interested in for our MOS devices which are at atomic/electronic level.

2.3.1. Optical Microscope

Most of the semiconductor device features are not clearly visible by the naked eye. A compound optical microscope is a useful equipment used during semiconductor device fabrications and characterizations for sample sizes of about 0.5 μm. Essential elements of the optical microscope are eyepiece, objective lenses, and illumination. Magnification can be changed by selecting between lenses of the compound microscope. Modern microscopes have six or more corrected compound lenses and basic microscope cane be enhanced by adding phase and differential interference contrast as well as polarizing filters. During mask alignment, lift-off, and after most of the MOSFET fabrication steps as well as characterization methods such as capacitance-voltage or current-voltage measurements and MOSFET measurements it is essential to use optical microscopy [24]. Some defects on the substrate can be seen through an optical microscope during device fabrication.

2.3.2. Digital microscope

While the optical microscope can be used to observe features in size of a few micrometers to above, to analyze smaller features, a digital microscope becomes much useful. With features such as 2D and 3D measurement tools, automatic edge detection, color, and contrast enhancements, a digital microscope helps during the semiconductor fabrication process. In addition to that, digital microscope is used to see defects, roughness, some contaminations, and features on substrate better than the compound optical microscope. But for identifying semiconductor or oxide defects in atomic size or nanometer level features this becomes useless.

2.3.3. Atomic Force Microscope

Scanning probe microscopy is a technique that uses a sharp tip to scan across a sample surface to obtain 2D or 3D images of a surface at a nanometer size resolution. Under extreme conditions 0.1 nm lateral resolution and 0.01 nm vertical resolution can be obtained using them. There are many scanning microscopy techniques such as Atomic force microscopy (AFM), Scanning tunneling microscopy (STM), Scanning capacitance microscopy (SCM), etc.

AFM was introduced to analyze the surface of insulating and conducting samples and operates by measuring the force between the probe and the sample. Figure 2.22 shows the main components of an AFM such as cantilever, piezo oscillator, laser diode, and photodiode. AFM can operate in several modes such as contact mode, non-contact mode or tapping mode depending on the contact of probe tip and sample. A topographical map of the sample surface can be generated, and feature dimensions can be measured with a high-resolution accuracy of nanometer size. In surface science and semiconductor microelectronics, AFM is extremely useful for sample topography analysis and precise thickness measurements. Some defects in the semiconductor substrate and dielectric also can be observed through AFM [25]. Especially AFM was used to measure thin oxide thicknesses

and surface roughness during the sample processing and sample preparation described in Chapter 4 in this dissertation.

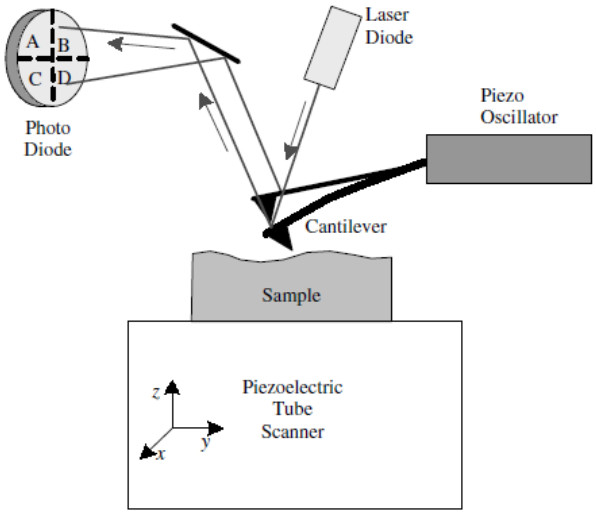

Figure 2.22: Schematic of the main components of AFM [25]

2.3.4. X-ray photoelectron spectroscopy (XPS)

For chemical surface information such as analyzing organics, polymers, and oxides, XPS is used. XPS is especially useful for understanding chemistry and mechanisms, for all elements except hydrogen and helium. Here energy shifts, due to changes in the chemical structure of the sample atoms or compounds, are used to obtain information about the surface. When photons of low energy (< 50 eV) are incident on the sample, they can eject electrons from the valance band and that effect is called ultraviolet photoelectron spectroscopy (UPS). As shown in Figure 2.23, there are three basic components of XPS, as X-ray source, spectrometer, and a high vacuum. Incident X-ray must be monochromatic light elements like Al or MG are common X-ray sources [26].

In XPS, photons that interact with core-level electrons are X-rays and for X-rays energies greater than the binding energy, electrons can be ejected from orbital with photoemission as shown in Figure 2.24. Measured energy of the emitted electron at the spectrometer E_{sp} can be expressed as

$$E_{sp} = h\upsilon - E_B - q\Phi_s \tag{2.59}$$

Where E_B is the binding energy, hυ is the energy of the primary X-rays, and ϕ_s is the work function of the spectrometer.

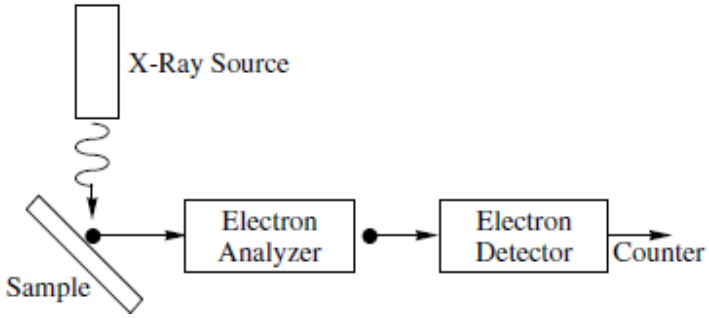

Figure 2.23: Schematic of XPS measurement [26]

By the location of energy peaks on XPS spectra, chemical compounds or elements are identified and the method is primarily for this purpose. In addition, density determination can be also performed and for that peak heights and peak areas can be used with correction factors. For oxide thickness measurements XPS can be used. In addition, Silicon suboxides can be also identified and thicknesses can be measured using XPS. Depth profiling is also possible by ion beam sputtering or sample tilting. Angle-resolved XPS (by angle tilting), the sample depth is λ sin θ where θ is the angle between the sample surface and the path of the emitted photoelectrons. The upper 0.5-5 nm of the surface of the sample can be analyzed through XPS [26] and this method can be used to identify the chemical nature and defects associated with the semiconductor/oxide interface when it comes to MOS physics characterization. In chapter 4 of this dissertation XPS was used to measure the ultra-thin oxide (SiO_x) layer thicknesses (<2nm).

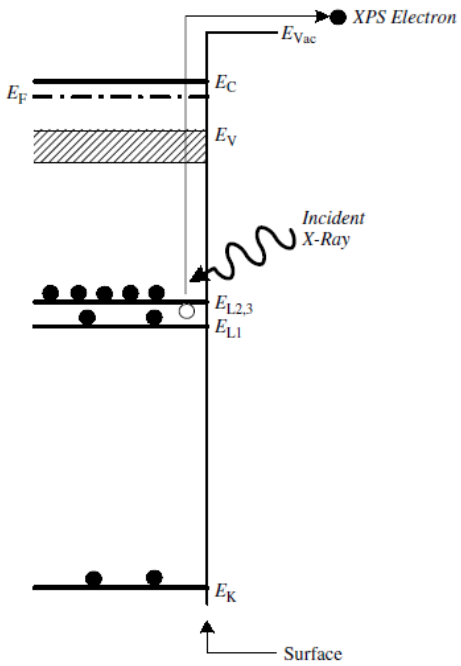

Figure 2.24: Electronic processes in XPS [26]

2.4 Summary

In this chapter, MOS device physics and important device parameters are introduced and discussed. Also, defects in MOS devices are discussed along with electrical characterization methods used for MOS devices such as simultaneous high-low capacitance method, C-ψ_s method, Gray-Brown technique, and constant capacitance deep level transient spectroscopy. Physical characterization methods such as microscopes, atomic force microscope, X-ray photoelectron spectroscopy used in microelectronics are also reviewed. In next two chapters, above mentioned MOS physics and electrical and optical characterizations are used extensively for 4H-SiC/dielectric MOS device characterizations and data interpretations. In order to optimize or improve MOSFET performance, these findings are extremely important. In microelectronics, this background knowledge helps understanding performances of devices made with semiconductor materials other than SiC as well.

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Chapter 3

Nature of 4H-SiC interface traps in SiO_2 and Al_2O_3 MOS devices: A comparison using CCDLTS

Electronic states/defects with energies lying close to the bottom of the conduction band or the top of the valance band in the semiconductor band gap are called the shallow donor or acceptor states. Other impurity atoms, intrinsic defects, and complexes of impurities and intrinsic defects in the gap away from the band edges are the deep levels usually are in bulk crystals [1]. Interface traps can be introduced to the semiconductor during thermal oxidation-like processes and drastically affect interface qualities and reflect in carrier transport. Therefore, differentiating these defects is extremely helpful for understanding and optimization of silicon carbide MOS devices. Constant capacitance deep level transient spectroscopy (CCDLTS) is an electrical characterization technique by which defects or trap types in MOS devices can be distinguished and quantified [2]. Among the other CV methods like simultaneous high-low capacitance CV method, C-ψ_s method [3] (described in chapter 2) or Terman method [4] provides information on total trap densities in a given trap energy range but would not provide information of different trap types, and CCDLTS is the method relevant for that. Using CCDLTS, interface trap energies, trap cross section areas as well as the density of each trap type can be obtained as mentioned in chapter 2.

3.1. Introduction

Lang [5] introduced the new technique DLTS in 1974 as a high-frequency capacitance transient thermal scanning method to be used to observe different kinds of electron or hole traps in semiconductors. First, n-GaAs was studied, and he identified three different shallow electron traps

with energies 0.08 eV, 0.17 eV, and 0.38 eV relative to the conduction band. An extension to DLTS was done by Lefevre et al. [6] in 1976 with improved sensitivity by double correlation and named this method as double correlation DLTS (DDLTS) and GaAs was analyzed. In 1979 Johnson et al. [2] proposed constant capacitance DLTS (CCDLTS) by analyzing bulk semiconductor defects for Si SBDs. They identified 4 distinct emission activation energies corresponding to trap energies measured relative to the Si conduction band minimum E_c using Arrhenius analysis of the trap emission rates as in Figure 3.1 [2]. In addition, special depth profiles for the defect levels was also carried out in this work.

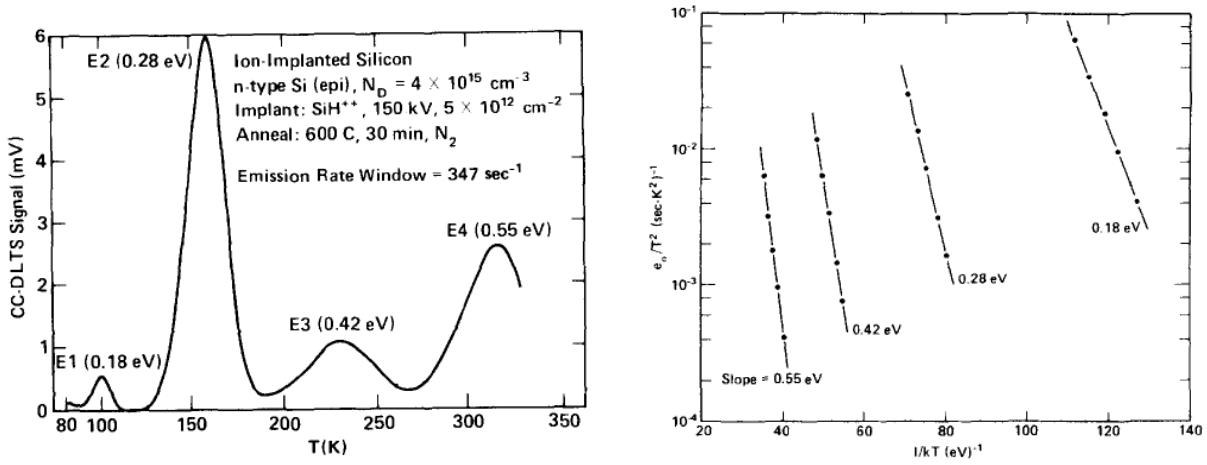

Figure 3.1: CCDLTS spectrum for Si Schottky-barrier diode (left). Arrhenius analysis of the four peaks in the CCDLTS spectrum (right) [2]

In 1982 Johnson measured semiconductor-insulator interface states and proposed MOS device characterization using CCDLTS. Si/SiO_2 interface defects were identified in this work and also the effect of H_2/N_2 anneal with trap passivation was observed compared to as-oxidized Si as in Figure 3.2. In addition to the identification of interface trap energies, and densities, he proposed the capture cross-section calculations using CCDLTS in this review [7].

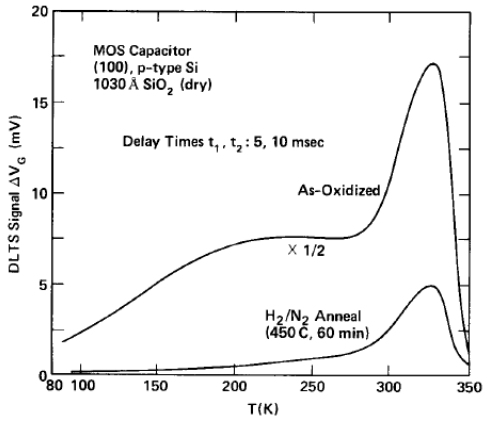

Figure 3.2: CCDLTS spectrum for as oxidized and annealed Si MOS capacitors [7].

In 2011 Basile et al. investigated n-type 4H and 6H-SiC MOS interfaces with CCDLTS technique. A series of nitrided SiO_2/SiC MOS capacitors were fabricated with dry oxidation followed by NO annealing. As in Figure 3.3 for the SiO_2/4H-SiC MOS interface, they identified two well-defined peaks with emission activation energies of 0.15 ± 0.05 eV and 0.39 ± 0.1 eV below the SiC conduction band and named them as O1 and O2 oxide traps, respectively [8].

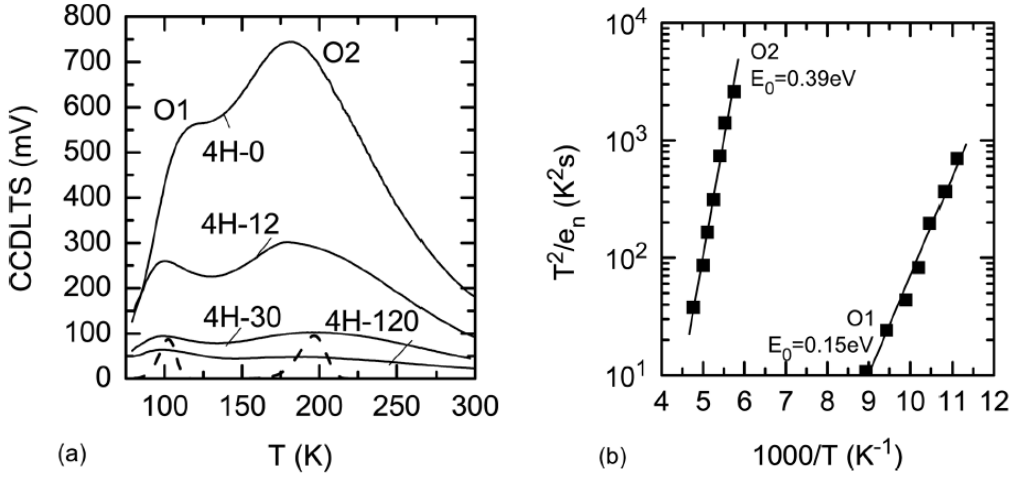

Figure 3.3: a) CCDLTS spectra for emission rate of 465 s^{-1} for as SiO_2/4H-SiC MOS capacitors with different NO anneal durations (constant capacitance 35 pF, and filling voltage of 16 V). b) Arrhenius plots for O1 and O2 peaks for the 4H-30 sample [8].

In addition, by comparing with theoretical ab initio calculations of interface traps by Knaup et al. [9], the detected O1 and O2 trap origins were assigned to be C-dimer on oxygen sites and Si-interstitials (Si_i) in SiO_2 in this work [8]. Figure 3.4 shows the C_o=C_o and Si_i formed in SiO_2 during the oxidation process and these defect densities were found to be reduced by introducing nitrogen by NO annealing by Basile et al.

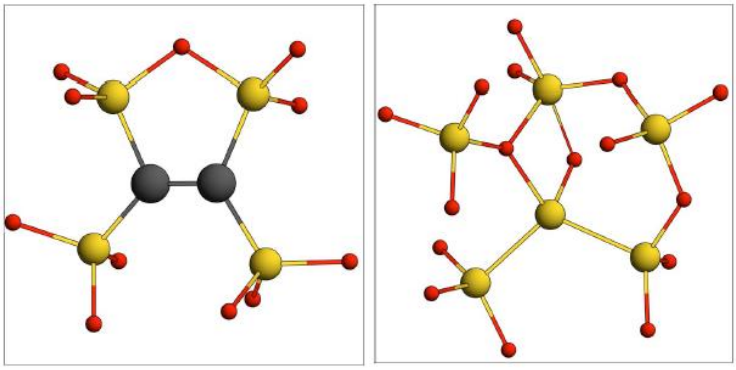

Figure 3.4: Carbon dimers substituted for O dimers in SiO_2 (suggested to be O1) in left. Interstitial Si in SiO_2 (suggested to be O2) in right. Si: larger yellow, O: smaller red, C: black spheres[9]

While simultaneous high-low CV method yields D_{it} for the 0.2 eV-0.6 eV region, Gray- Brown method and CCDLTS (77 K-298 K) yields D_{it} for ~0.05 eV-0.2 eV region below the E_c of SiC. Depending on the temperature range a particular CCDLTS system covers, this energy range can be changed. For a system in which lowest temperature achievable is 77 K (using liquid nitrogen), the closest it can reach is 0.1 eV below the conduction band of 4H-SiC which misses the information about shallower traps. This could be overcome by having a system in which achievable minimum temperature is less than 77 K.

3.2. Effect of trap passivation at SiO_2/4H-SiC interfaces in CCDLTS

The study of O1/O2 signature oxide traps in SiO_2/4H-SiC MOS devices is significant for understanding the correlation between shallow trap densities and the channel transport depending

on the trap passivation methods such as nitridation, phosphosilicate glass (PSG), or Borosilicate glass (BSG).

Basile et al. [8] investigated the 4H-SiC/SiO_2 interface by CCDLTS on O1/O2 trap characteristics and concluded that the O1 and O2 traps reside in the oxide layer, rather than at the interface. A significant finding of the study was the effect of nitridation by NO annealing. The density of the broad O1, O2 energy level distributions in the two hours NO annealed sample was reduced by about a factor of 10 compared to the as-oxidized sample as they reported. This study shows that O1 and O2 oxide traps are possible defects created during oxidation and they remain even after nitridation but in reduced amounts and do not completely vanish. Compared to as-oxidized SiO_2/4H-SiC MOSFET channel mobility, nitridation results in higher channel mobility [10] and one reason for that could be O1 and O2 trap density reduction.

Jayawardena et al. [11] investigated MOS capacitors with phosphosilicate glass (PSG)/ Phosphorus doped SiO_2 [12], [13] as the gate dielectric using CCDLTS. They observed the presence of the two broad O1 and O2 peaks but significantly less than NO annealed or as-oxidized MOS capacitors. With theoretical modeling, authors were able to suggest that the presence of P in the near- interfacial region reduces the stability of the O1 defect and reduces the density of O2 defect through network restructuring based on the criteria that O1 and O2 being C_o=C_o and Si_i in SiO_2 respectively.

These observations show that in as-oxidized, NO annealed as well as PSG incorporated SiO_2/4H-SiC MOS devices, O1 and O2 are signature defects detected by CCDLTS in 77 K-298 K temperature region which reflects ~0.05- 0.2 eV below the conduction band edge of 4H-SiC. Thus, information on these near-interface oxide interface traps is important to study especially to understand how they affect device channel mobilities or threshold voltage (V_{th}) instability.

Therefore, in this work we compared as-oxidized (Dry-ox) SiO_2, NO annealed (NO) SiO_2, Phosphosilicate glass (PSG) incorporated and Borosilicate glass (BSG) [14], [15] based 4H-SiC MOS capacitors with CCDLTS as shown in Table 3.1. MOS capacitors were fabricated using 5 mm×5 mm samples diced from 4° off-axis n-type 4H-SiC wafers with 10 μm epitaxial layers doped with nitrogen at ~2×10^{16} cm^{-3}. After standard RCA cleaning as in the appendix, dry thermal oxides were grown at 1150 °C. While one sample was kept as the reference dry-oxide sample, the second sample was annealed in NO at 1175 °C for 2 hours. The third sample was subjected to post oxidation annealing using a 3-inch B_2O_3 planar diffusion source (Techneglas, GS-139) for BSG formation. BSG formation was done in 2 steps; first the oxidized sample was placed facing the B_2O_3 source with an Ar flow of (50 sccm) and O_2 (5 sccm) at 950 °C for 30 min, second the B_2O_3 source was removed and the sample was kept in the same furnace for 2 hrs while flowing Ar at 950 °C for 2 hrs for diffusion purpose. All samples were patterned with circular Al gates via thermal evaporation as in appendix and colloidal silver paint was used as back contact. Data from Jayawardena et al. [11] was used for comparison with PSG in which similar substrates and fabrication conditions as above were used.

Table 3.1: MOS capacitors fabricated with different passivation methods

Sample	t_{ox}±2 (nm)	Processing
Dry-ox	62	Thermal oxidation 1150 °C 10 hr
NO	62	Thermal oxidation 1150 °C 10 hr+ NO 1175 °C 2 hr
PSG	66	Thermal oxidation 1150 °C 10 hr+ PSG (1100 °C in $POCl_3$+O_2+N_2 15 min)
BSG	86	Thermal oxidation 1150 °C 10 hr+ BSG (950 °C)

Simultaneous high-low capacitance-voltage measurements were carried out using 100 kHz and quasi-static CV measurements with a Keithley 590 CV analyzer at 298 K and D_{it} was extracted from 0.2 eV-0.6 eV below the conduction band edge as in Figure 3.5.

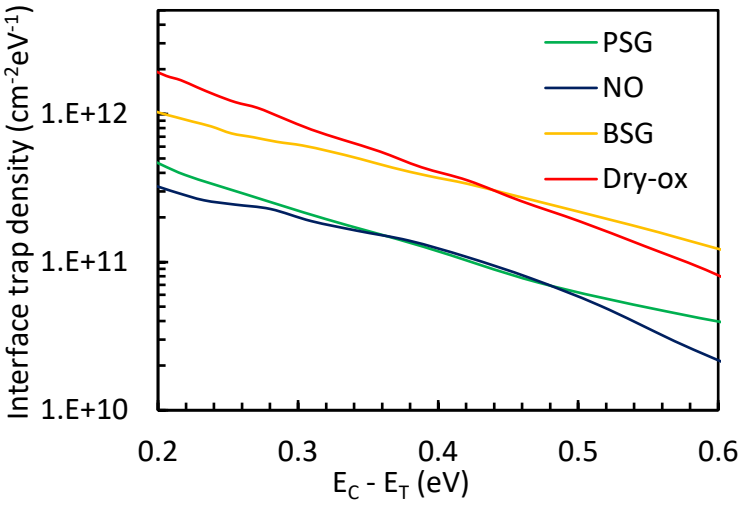

Figure 3.5: Interface trap density (D_{it}) extracted by simultaneous high-low capacitance-voltage method for MOS capacitors with different post oxidation annealing conditions.

Clearly, both BSG and PSG passivation results in lower D_{it} closer to the conduction band edge of 4H-SiC compared to dry-oxide sample and NO annealing yields the lowest D_{it} compared to all POA methods according to simultaneous high-low capacitance-voltage method.

Next CCDLTS analysis was performed maintaining constant capacitance of 37 pF biasing MOS capacitors in the deep depletion region. 25 ms pulse width filling pulse voltage V_p was changed from V_{fb} to V_{fb}+4 V in steps of 1 V. For all the samples, two broad peaks were visible. CCDLTS signal increased for all the samples when filling voltage V_p was increased. This should correspond to reaching near-interface oxide traps which are spatially located further deeper from the interface as V_p is increased. To compensate that, when the spectra are compared, the same V_p-V_{fb} was employed for different samples. Figure 3.6 shows the interface trap charges extracted by CCDLTS

signal for NO, PSG, and BSG passivated MOS capacitors compared to dry -oxidation for $V_p=V_{fb}+4$ V and for electron emission rate (e_n) of 46.5 s^{-1}.

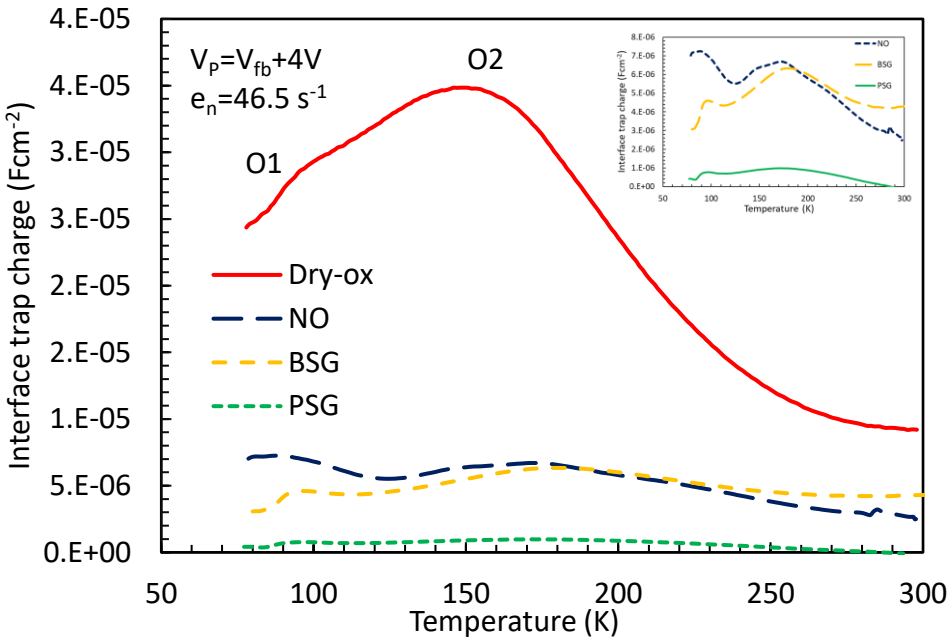

Figure 3.6: CCDLTS for samples with different passivation methods compared to dry oxidation. Inset shows magnified CCDLTS spectra for NO, PSG and BSG samples.

For different electron emission rates (e_n) of 4.65 s^{-1}, 11.6 s^{-1}, 23.2 s^{-1}, 46.5 s^{-1}, 116 s^{-1}, 232 $s^{-1,}$ and 465 s^{-1} CCDLTS spectra were obtained for $V_p=V_{fb}+4$ filling pulse by changing initial delays (ID) of the CCDLTS system in the temperature range of 77 K to 298 K. By finding the peak position temperature for each emission rate, Arrhenius analysis (as described in Chapter 2) was performed by plotting ln (T^2/e_n) vs 1000/T. Using this Arrhenius plot, trap activation energies (E_c-E_T) and trap cross-section areas (σ_n) were calculated for the observed two peaks. Trap activation energies confirmed that the two peaks visible in Dry-ox, NO, PSG and BSG samples were indeed O1 and O2 traps. For each trap type N_{it} was calculated using the equation 2.57 as in reference [8].

Broadening factor :ΔW was used as 4, 6 for O1 and O2 respectively as defined by Basile et al. [8]. Table 3.2 shows the quantitative analysis of trap activation energies, capture cross-sections, and trap densities for O1, O2 traps calculated for NO annealed (N- incorporated) SiO_2, PSG (P incorporated), and BSG (B incorporated) based 4H-SiC samples compared to MOS devices with dry oxidation (without any passivation).

Table 3.2: O1, O2 trap activation energies with standard deviation over several devices, capture cross-sections and trap densities obtained by CCDLTS for MOS capacitors fabricated with different passivation methods compared to dry oxidation [16] (error of σ_n is about two orders of magnitude)

Sample	O1 Trap			O2 Trap		
	E_c-E_T (eV)	σ_n (cm^2)	N_{it} (±10% cm^{-2})	E_c-E_T (eV)	σ_n (cm^2)	N_{it} (±10% cm^{-2})
Dry-Ox	0.15±0.05	1×10^{-15}	2.60×10^{12}	0.34±0.1	5×10^{-16}	1.77×10^{12}
NO	0.19±0.05	1×10^{-13}	1.88×10^{11}	0.35±0.1	1×10^{-14}	2.61×10^{11}
PSG	0.15±0.01	1×10^{-15}	3.12×10^{10}	0.38±0.01	7×10^{-13}	4.14×10^{11}
BSG	0.14±0.05	1×10^{-16}	1.35×10^{11}	0.33±0.1	2×10^{-15}	2.42×10^{11}

According to our observations, ‘O1’ and ‘O2’ are signature traps in thermal oxide/4H-SiC MOS interfaces regardless of the incorporated post oxidation passivation. None of these passivation methods could completely remove these signature traps although they could be significantly reduced.

It is a known fact that the channel mobility of n-channel 4H-SiC(0001) MOSFETs fabricated on lightly-doped p-type epilayers has been enhanced from a single digit (4–8 $cm^2V^{-1}s^{-1}$) for dry

oxides to 30 –52 $cm^2V^{-1}s^{-1}$ for NO-nitrided oxides [17]. In addition, $POCl_3$ anneal (PSG) and BSG incorporation improve channel mobility up to ~100 $cm^2V^{-1}s^{-1}$ for SiO_2/4H-SiC [12], [14], [15]. Clearly, O1 and O2 trap density reduction must influence channel mobility increment for these passivation methods. However many other possible reasons can affect channel mobility reduction for SiO_2/4H-SiC MOS devices other than O1, O2 oxide traps [18]. But, this CCDLTS result provides a solid ground to understand the common, interface chemistry and bonding nature shared by all these MOS interfaces.

3.3. Effect of wafer orientations with nitrided SiO_2/4H-SiC

Four major crystal planes in 4H-SiC are shown in Figure 3.7 [19] . These are the polar Si-face, C-face and non-polar, a-face and m-face. These wafer orientations demonstrate very different electrical properties when used in electronic structures.

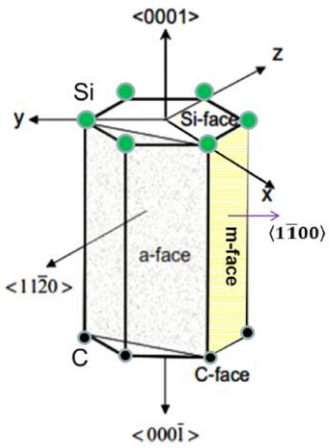

Figure 3.7: Crystal faces in 4H-SiC. The Si-face is terminated by Si atoms and C-face by C-atoms. A-face and m-face have equal number of Si and C atoms. (Si-large green balls, C-small black balls) [19]

While different crystal faces have different oxidation rates, their interface state distributions are also unique depending on wafer orientation. This may stem from the oxidation rate differences as well as the atomic structural differences such as C and Si atom ratios on the planes [17]. Figure 3.8 shows the interface state density distributions obtained for n-type 4H-SiC (0001) Si-face, (000-1) C-face, (11-20) a-face, and (1-100) m-face for dry oxidation.

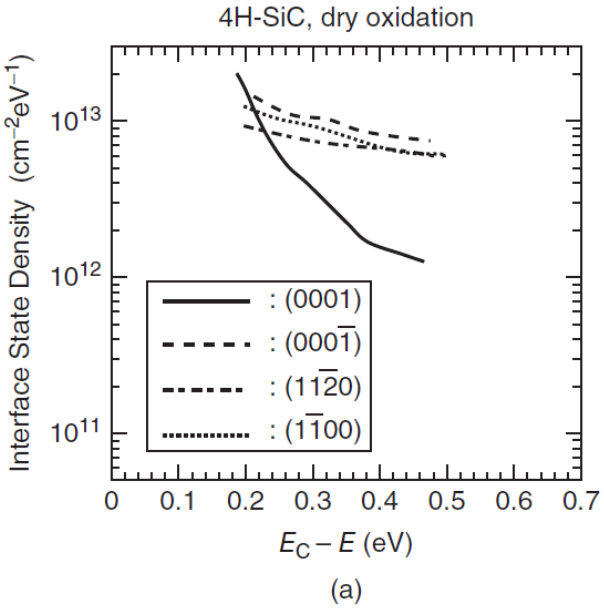

Figure 3.8: Interface state densities obtained by simultaneous high-low CV method for n-type 4H-SiC MOS capacitors prepared under dry oxidation using different wafer orientations [17].

Clearly, there is a dramatic contrast between Si-face and all other faces close to the conduction band edge as well as closer to midgap. The distributions of D_{it} towards the conduction band edge for non-standard C-, a- and m- faces are rather flat. Another fact to mention here is depending on post oxidation annealing conditions, different faces react differently resulting in various amounts of D_{it} reductions. Therefore, reported channel mobilities for these faces are also dramatically different as in Figure 3.9 [17].

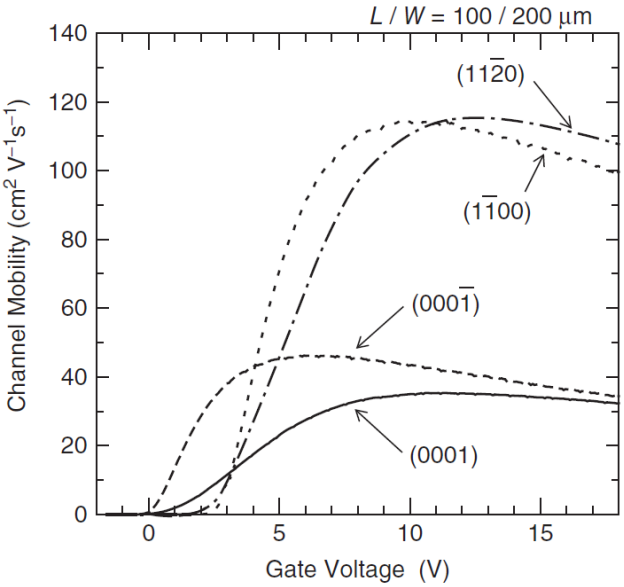

Figure 3.9: Field-effect mobility as a function of the gate voltage of n-channel MOSFETs fabricated on 4H-SiC (0001), (000-1), (11-20), and (1-100) with NO annealed SiO_2 [17].

To study the effect of wafer orientation, we studied polar (0001) Si-face (100% Si) and (000$\bar{1}$) C-face (100% C terminated), and non-polar (11$\bar{2}$0) a-face (50% Si, 50% C) oriented 4H-SiC using CCDLTS [20]. MOS capacitors were fabricated using 5 mm×5 mm samples diced from 4° off-axis n-type 4H-SiC wafers with different crystal orientations with 10 µm epitaxial layers doped with nitrogen at ~10^{16} cm^{-3}. After standard RCA cleaning as in the appendix, dry thermal oxides were grown at 1150 °C for different time intervals of 10 hr, 3 hr, and 1 hr yielding 62 nm, 54 nm, and 76 nm oxide thicknesses for Si-, a-, C- faces respectively. As in Table 3.3, for each split, while one sample was kept as the reference dry -oxide sample, a second sample was annealed in NO at 1175 °C for 2 hours. Al gates were patterned using e-beam deposition and colloidal silver paint was used as back contact.

Table 3.3: Sample matrix for n-type 4H-SiC MOS capacitors fabricated on Si-, C-, and a- face wafers with and without nitridation.

sample	t_{ox} ±2 (nm)	2 hr NO anneal	Avg. V_{fb}(V)
S1 (Si-face)	62	no	0.45±0.2
S2 (Si-face)	62	yes	-1.5±0.1
A1 (a-face)	54	no	8.4±0.3
A2 (a-face)	54	yes	1.3±0.1
C1 (C-face)	76	no	12.5±1.5
C2 (C-face)	76	yes	6.8±0.5

Simultaneous high-low CV measurements were carried out on all the samples. For Si face MOS capacitors, about 10x reduction of D_{it} was observed with nitridation compared to the as-oxidized sample. As-oxidized C- and a-face MOS capacitors barely accumulated and D_{it} calculation was difficult, but there was a considerable amount of difference between high and quasi-static CV curves indicating high D_{it}. With nitridation, C- and a-face MOS devices D_{it} was reduced compared to as oxidized samples. For all the wafer orientations V_{fb} was reduced when nitridation was involved due to possible negative charged trap reduction. Overall, a clear reduction of interface traps as well as slow traps closer to the valance band edge was observed for all 3 wafer orientations tested in this work. Interface state densities obtained by simultaneous high-low CV method for 2 hr NO annealed n-type 4H-SiC MOS capacitors S2, C2, and A2 are shown in Figure 3.10. Among them, Si face has the lowest D_{it} in the given energy range of 0.2-0.6 eV below the conduction band edge of 4H-SiC according to simultaneous high-low method. But this method underestimates trap densities closer to the conduction band edge of 4H-SiC. Next we calculated D_{it} for the same samples with C-ψ_s method [3], as in Figure 3.11. According to C- ψ_s method, D_{it} was less for C-

face compared to a- and Si-faces. C- ψ_s method can be used to evaluate D_{it} especially considering shallow traps energetically located closer to the conduction band edge with better accuracy compared to simultaneous high-low method. Thus, these results show that especially in Si- and a-faces more shallower traps are present which may affect channel transconductance compared to C-face.

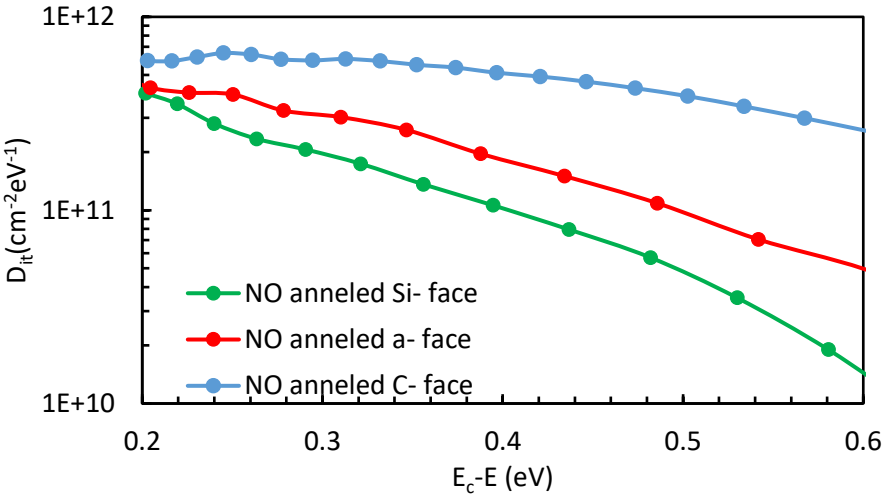

Figure 3.10: Interface state densities obtained by simultaneous high-low CV method for 2 hr NO annealed n-type 4H-SiC MOS capacitors with different wafer orientations

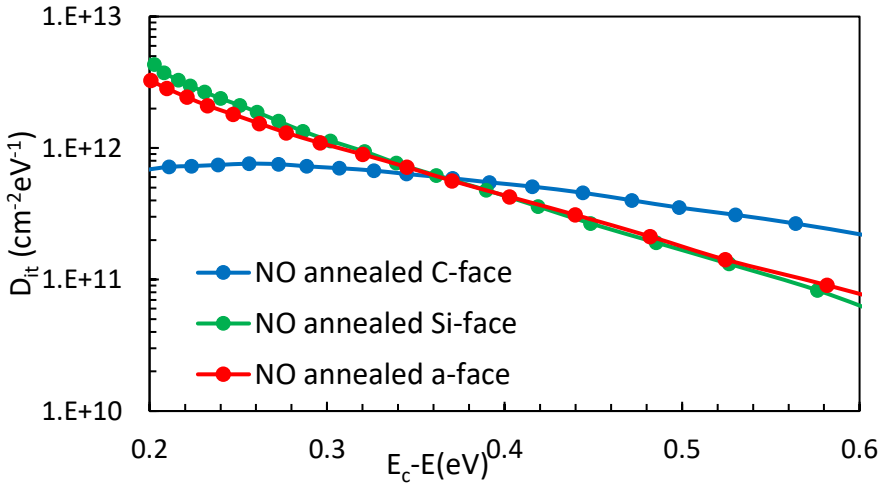

Figure 3.11: Interface state densities obtained by C-ψ_s method for 2 hr NO annealed n-type 4H-SiC MOS capacitors with different wafer orientations

Thus, it is essential to look at the shallow trap densities and trap types for these different wafer orientations as clearly, there can be a relationship between drastic differences of mobility observed for different wafer orientations. That is where the CCDLTS technique becomes useful.

We have already investigated and reported NO annealed Si-face 4H-SiC MOS interface traps detected by the CCDLTS technique in section 3.3. For the (0001) Si-face SiO_2/SiC interface, two types of NITs were detected by CCDLTS as described earlier [20].

CCDLTS analysis was performed on a-face and C- face NO annealed SiO_2/4H-SiC MOS capacitors maintaining constant capacitance biasing them in the deep depletion region. Filling pulse voltage V_p was changed from V_{fb} to V_{fb}+5 V in steps of 1 V and 25 ms pulse width. CCDLTS signal was also increased with filling pulse without saturation, indicating we are looking at traps inside the oxide and accessing traps away from the interface deeper into the oxide with higher V_p. For the a-face, two new peaks labeled as A1 and A2 were observed as in Figure 3.12.

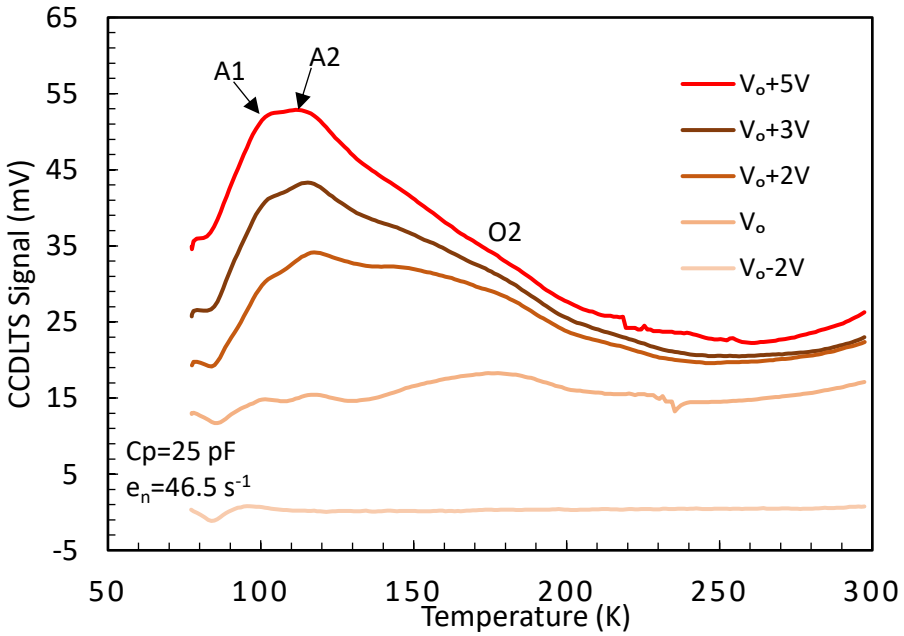

Figure 3.12: CCDLTS spectra for different filling voltages for NO annealed SiO_2/4H-SiC MOS capacitors fabricated on a-face 4H-SiC ($V_0 = V_{fb}$)

These traps were found to be in the same range as the O1 trap observed in Si-face when trap emission activation energy extracted from the measurements were compared as in Table 3.4. In addition, the O2 trap was also observed in a-face devices, but the quantitative analysis was difficult as the O2 signals were masked by the tails of the broad A1/A2 peaks for higher V_p. This was the first-time a-face 4H-SiC/SiO_2 interface was analyzed by CCDLTS. O2 (possible Si-interstitials in SiO_2) trap density is one of the main defect differences between nitrided Si- and a-face interfaces. For the C-face, no low-temperature peaks were detected as the signals from energetically deeper traps dominate the spectra masking possible shallow trap peaks. But even if there were O1/O2 traps in C-face devices, the trap charge density must be much less compared to Si- and a- face as in Figure 3.13 which shows the interface trap charges extracted by CCDLTS signal for A2 (NO annealed a-face SiO_2/4H-SiC) and C2 (NO annealed C-face SiO_2/4H-SiC) MOS capacitors compared to S2 (NO annealed Si-face SiO_2/4H-SiC).

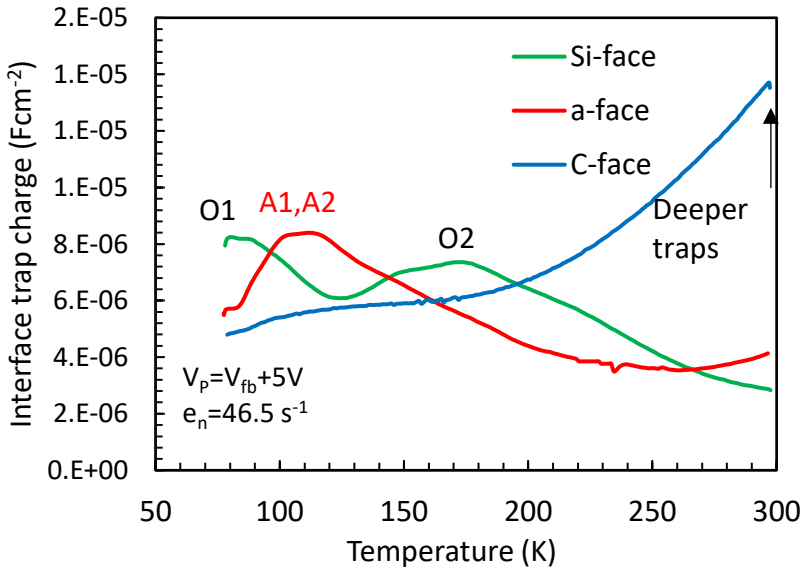

Figure 3.13: CCDLTS analysis for NO annealed SiO_2/4H-SiC MOS capacitors fabricated on different 4H-SiC wafer orientations for $V_p=V_{fb}+4$ V and electron emission rate (e_n) of 46.5 s^{-1}.[16]

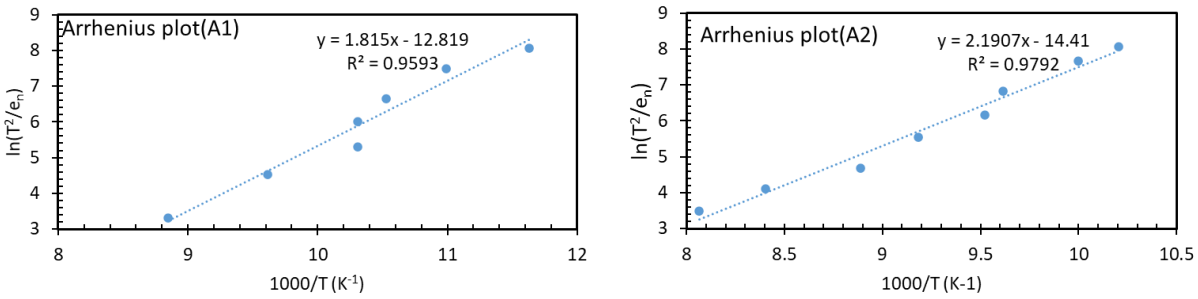

Figure 3.14: Arrhenius plots for A1 (left) and A2 (right) peaks detected by CCDLTS analysis NO annealed SiO_2/4H-SiC MOS capacitors fabricated on a-face 4H-SiC for $V_p=V_{fb}+5$ V

Table 3.4: Traps types, activation energies, cross-section areas and trap densities detected by CCDLTS for different wafer orientations of 4H-SiC/SiO_2 MOS capacitors with 2 hr NO annealing. The values are from three to five devices on each sample. The scatter in σ_n is about two orders of magnitude.

Sample	Trap type	E_c-E_T ±0.01 (eV)	σ_n (cm^2)	N_{it} ±10% (cm^{-2})
Si-face (S2)	O1	0.15	1×10^{-15}	2.2×10^{11}
	O2	0.35	3×10^{-14}	3.0×10^{11}
a-face (A2)	new A1	0.15	1×10^{-16}	2.3×10^{11}
	new A2	0.19	7×10^{-15}	2.3×10^{11}
	O2	Present but difficult to quantify as masked by A1, A2		
C-face (C2)	Difficult to quantify and deeper traps can be observed			

Hatayama et al. [21] have also studied C-face 4H-SiC with dry oxide SiO_2 MOS interface using CCDLTS. According to their findings, they have reported the presence of a trap named C1 with activation energy the same as O1 in C-face. They also have not observed O2 similar to our

observations. One main reason for the absence of C1 in our study can be due to different annealing conditions in the two works. While in our study we have performed NO annealing, Hatayama et al. have employed a combination of N_2O annealing and H_2 annealing together. It is possible that NO annealing suppresses the O1 trap completely but when N_2O annealing is performed in conjunction with H_2 annealing, the O1 trap remains in the interface. But regardless of the H_2 annealing, when nitrogen is incorporated into the interface, O2 found was found to be absent according to both studies implying passivation of Si-interstitials in SiO_2. In addition, they have observed O1 and O2 traps on Si-face dry oxides exposed to N_2O and H_2 annealing.

Dhar et al. [22] have calculated the areal ^{15}N density by Rutherford backscattering (RBS) for SiO_2/4H-SiC MOS capacitors with 1175 $^{\circ}$C 2 hr annealing in ^{15}NO prepared with different wafer oriented 4H-SiC. According to their findings, a- and C- faces have retained more than 2x of N concentration in the interface than Si-face after 2 hr NO annealing as in Figure 3.15. With the same NO annealing conditions (same temperature and same time duration) more nitrogen could have incorporated in a- and C- faces compared to Si-face. This could result in better passivation of Si-interstitials in SiO_2 ('O2' trap in CCDLTS spectrum) in a- and C- faces compared to Si-face as we observed in the CCDLTS study.

In this section, CCDLTS analysis of nitrided SiO_2/4H-SiC MOS interfaces on different wafer orientations was reported. The strong contrast of CCDLTS signatures from different crystal faces was observed and the highest O1, O2 trap densities were observed for Si-face, while lowest were observed for C-face. Thus C-dimers (O1) and Si- interstitial (O2) related trap densities are highest in Si face and lowest for C-face for MOS interfaces with 2hr NO annealed SiO_2/4H-SiC. C-dimers related trap densities were similar in Si- and a-faces. It can be concluded that depending on the wafer orientation, O1 and O2 trap densities are changing. These differences have possibly

contributed to the difference in D_{it} as well as different channel mobilities for different 4H-SiC wafer orientations.

3.4. Effect of epitaxial doping on nitrided SiO_2/4H-SiC

In section 3.2 and 3.3 standard NO annealed SiO_2/4H SiC MOS capacitor was considered as the reference sample. These devices were fabricated on Si-face (4° off-axis) n-type 4H–SiC wafers doped with nitrogen at $\sim 2\times10^{16}$ cm^{-3}. The CCDLTS spectrum of this sample is shown in Figure 3.15, in which 2 major peaks O1, O2 were detected as mentioned before. Other than the O1 and O2, two more peaks were barely visible in the spectrum but because they are broad, and not sharp enough, trap energy calculations were difficult.

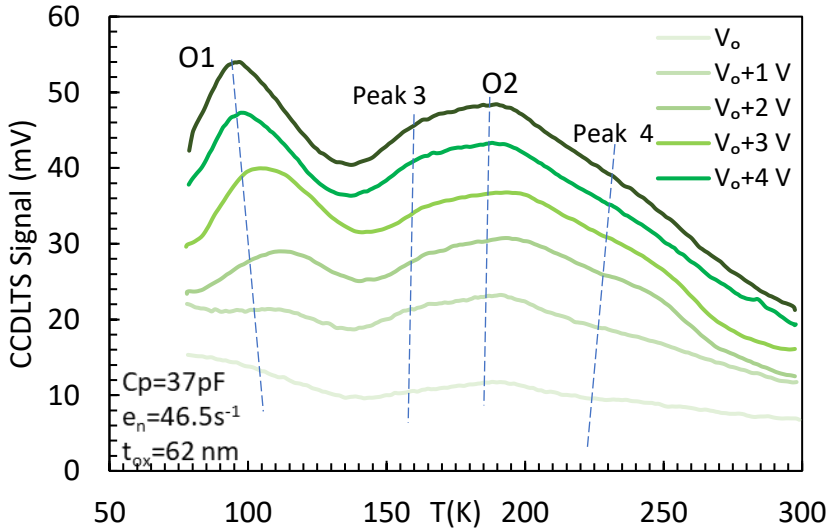

Figure 3.15: Series of CCDLTS spectra taken with increasing trap filling pulse voltages (V_P) in the temperature range 77 K-298 K on the NO annealed (1150 ˚C 2 hrs in O_2+ 1175 ˚C for 2hrs NO) SiO_2/(0001) 4H-SiC doped with nitrogen at $\sim 2\times10^{16}$ cm^{-3} [11]

Arrhenius analysis is valid only at clear peaks where the CCDLTS signal is maximized. A CCDLTS peak is generated when the emission rate of the traps, e_n, is equal to the spectrometer

rate window (τ^{-1}_{max}) [5]. The activation energies and the capture cross-sections can only be determined by generating the Arrhenius plot of $\ln(T^2/e_n)$ versus 1000/T, where T is the temperature of the CCDLTS peak maximum and e_n is the instrument rate window. Peak 3 and peak 4 are two more types of defects which are difficult to quantify as they are not sharp peaks.

Next, we investigated NO annealed SiO_2/4H SiC MOS capacitors fabricated on Si-face (4° off-axis) n-type 4H–SiC wafers doped with moderately higher nitrogen doping concentration at ~10^{17} cm^{-3}. NO annealed MOS capacitors were fabricated as described in section 3.2. The goal was to investigate the effect of doping concentration of the epitaxial layer on defects detected by CCDLTS. Figure 3.16 shows the CCDLTS spectra for increasing V_p for the sample with higher N doping concentration than the regular stand NO annealed sample. Obviously, three sharp peaks were visible for $V_p=V_{fb}+4$ filling voltage.

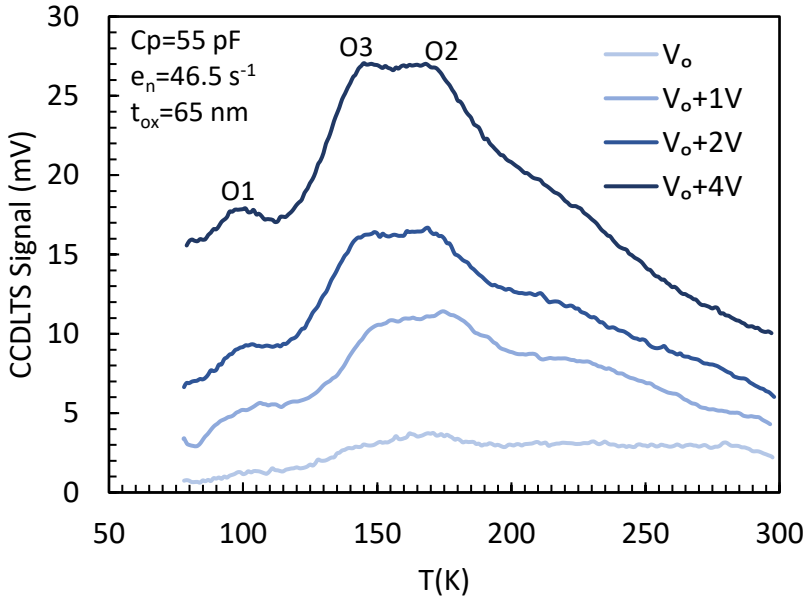

Figure 3.16: Series of CCDLTS spectra taken with increasing trap filling pulse voltages (V_P) in the temperature range 77 K-298 K on the NO annealed SiO_2/(0001) 4H-SiC doped with nitrogen at ~10^{17} cm^{-3} where $V_o=V_{fb}$

CCDLTS spectra were obtained for different rate windows/emission rates as in Figure 3.17. Arrhenius plots were obtained for detected peaks as shown in Figure 3.18 and trap activation energies, cross-section areas, as well as trap densities, were calculated as in Table 3.5.

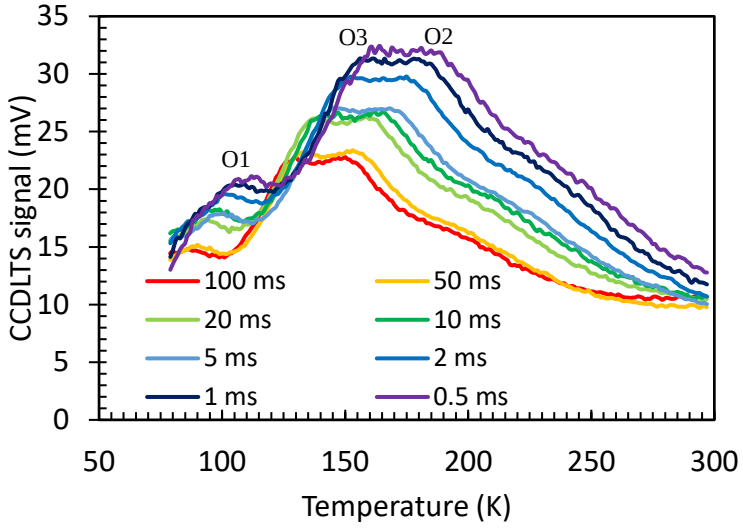

Figure 3.17: Series of CCDLTS spectra taken for different initial delays in the temperature range 77 K-298 K for $V_p=V_{fb}+4$ V on the NO annealed SiO_2/(0001) 4H-SiC doped with nitrogen at $\sim 10^{17}$ cm^{-3} keeping constant capacitance at 55 pF, t_{ox}=65 nm.

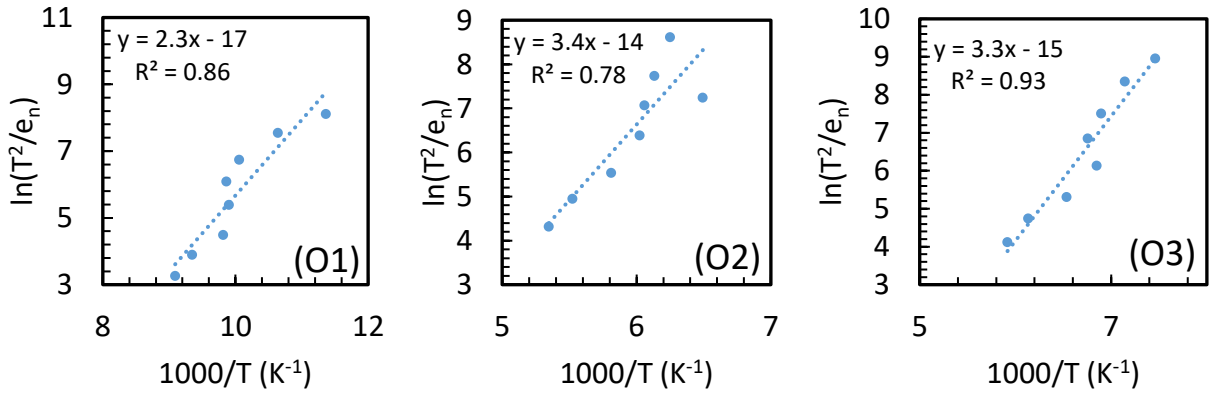

Figure 3.18: Arrhenius analysis of O1, O2 and O3 traps for $V_p=V_{fb}+4$V on the NO annealed SiO_2/ (0001) 4H-SiC doped with nitrogen at $\sim 10^{17}$ cm^{-3} for C_p=55 pF and $V_p= V_{fb}+4$ V

Table 3.5: Traps, cross-section areas and trap densities detected by CCDLTS for NO annealed SiO_2/(0001) 4H-SiC MOS capacitors doped with nitrogen. The values are from three to five devices on each sample. The scatter in σ_n is about two orders of magnitude.

Doping	Trap type	E_c-E_T ±0.03 (eV)	σ_n (cm^2)	N_{it} ±10% (cm^{-2})	Total N_{it} ±10% (cm^{-2})
1×10^{17} cm^{-3}	O1	0.17	1×10^{-14}	1.3×10^{11}	6.6×10^{11}
	O2	0.33	3×10^{-14}	2.8×10^{11}	
	new O3	0.26	1×10^{-15}	2.5×10^{11}	
2×10^{16} cm^{-3}	O1	0.15	1×10^{-15}	2.2×10^{11}	5.2×10^{11}
	O2	0.35	3×10^{-14}	3.0×10^{11}	

Other than the SiO_2/4H-SiC signature O1, O2 traps, we were able to clearly identify and calculate the new trap energy for the 3rd peak as 0.26±0.03 eV below the conduction band edge of 4H-SiC. The trap was labeled as "O3" and this is the possible "peak 3" which was difficult to quantify in the previous standard NO annealed SiO_2/ (0001) 4H-SiC MOS capacitors doped with nitrogen at $\sim2\times10^{16}$ cm^{-3}. With the increase of N-doping concentration, O3 became clearer and more highlighted in the CCDLTS spectrum imping O3 trap becomes more dominant in higher n-doped 4H-SiC samples.

When interface trap densities were compared for using simultaneous high-low method and C-ψ_s method, at E_c-E=0.2 eV; both have about similar D_{it} as shown in Figure 3.19. But clearly regardless of doping concentration, D_{it} near CB edge is higher when C-ψ_s method is used, compared to simultaneous high-low method. Only the CCDLTS spectra features were different (with clear O3 peak) when N- doping concentration in 4H-SiC was changed.

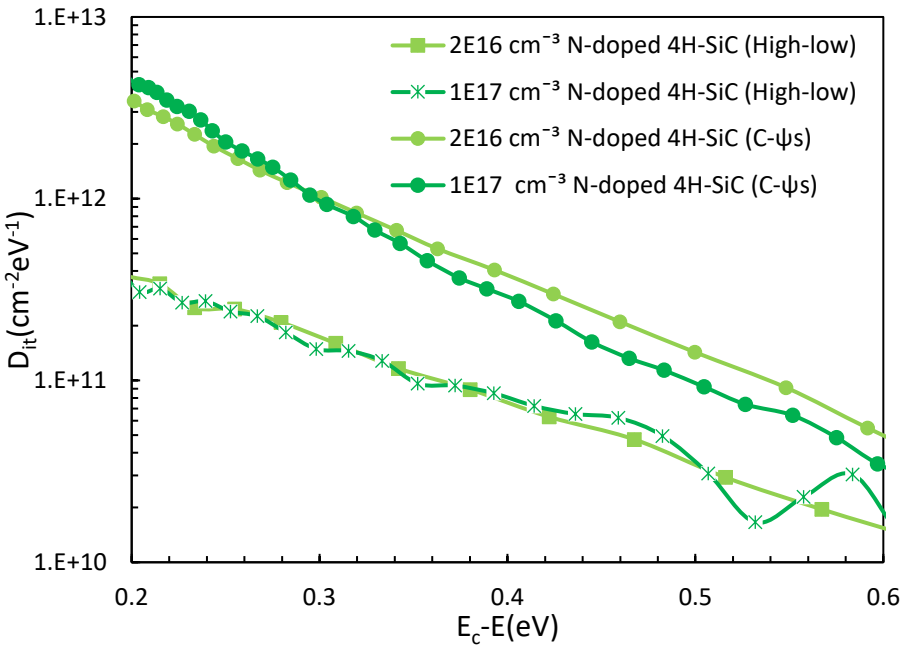

Figure 3.19: D_{it} extracted by simultaneous high-low method (High-low) and C-ψ_s method for NO annealed SiO_2/ (0001)4H-SiC MOS capacitors doped with different nitrogen concentrations.

The sharpening and dominative behavior of trap O3 in moderately higher n-doped 4H-SiC. The origin of O3 is unclear at the moment. Regardless of 4H-SiC doping concentration, O1 and O2 NITs are present in SiO_2/(0001) 4H-SiC MOS interfaces in about the same order of trap densities.

3.5. Absence of O1/O2 traps in H-terminated Al_2O_3/4H-SiC

In the previous sections of this chapter, we investigated SiO_2/4H-SiC interfaces under different post oxidation annealing conditions, with different 4H-SiC wafer orientations, and with different SiC doping conditions. Mainly two kinds of traps were detected, and they were suggested to be oxide traps in SiO_2 located near the oxide-semiconductor interface. Next, we studied the Al_2O_3/4H-SiC interface with the intention to see if we see any O1, O2 traps, and to get confirmed uniqueness of O1 and O2 for SiO_2 related interfaces [16]. For that, Al_2O_3/4H-SiC MOS capacitors were fabricated at Purdue University. For this work 1 cm×1 cm pieces diced from Si face (4° off-axis)

n-type 4H–SiC epitaxial wafers doped with nitrogen at ~10^{17} cm^{-3}. Prior to ALD, the samples were etched in hydrogen at 1600 °C [23] followed by annealing in hydrogen at 1000 °C [24], [25]. After the surface preparation, ~50 nm of Al_2O_3 was deposited by atomic layer deposition at 200 °C using Trimethylaluminum (TMA, $Al(CH_3)_3$) and H_2O as the precursors. Metal gates were formed with a Ti/Au stack and back-side contact colloidal silver paste was used. Simultaneous high-low frequency capacitance-voltage (CV) measurements at room temperature were performed, and D_{it} was calculated as in Figure 3.20. Compared to NO annealed SiO_2/4H-SiC, H_2 annealed Al_2O_3/4H-SiC D_{it} was in the same order of magnitude near the conduction band edge, but higher D_{it} was observed deeper in the gap according to the simultaneous high-low method. But with C-ψ_s analysis clearly trap densities closer to the 4H-SiC is lower for H-terminated Al_2O_3/4H-SiC interface than for nitrided SiO_2/4H-SiC interface.

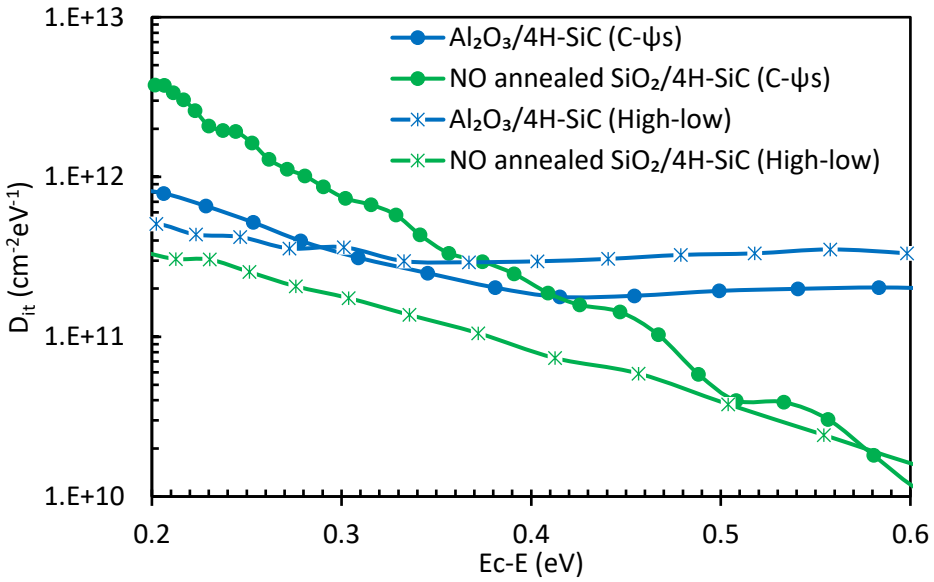

Figure 3.20: D_{it} extracted by simultaneous high-low method (High-low) and C-ψ_s method for H_2 etched and H_2 annealed Al_2O_3/4H-SiC MOS capacitor compared to NO annealed SiO_2/(0001) 4H-SiC MOS capacitors fabricated on ~10^{17} cm^{-3} n-doped 4H-SiC

Next, 1MHz capacitance-voltage (CV) measurements were performed at a range of temperatures from 77 K to 400 K as in Figure 3.21. Between 77 K- room temperature, CV curves were very stable. This may correspond to the presence of energetically deeper traps in Al_2O_3/4H-SiC interface. But when the temperature was increased from 298 K to 400 K, clear CV shifts to the positive voltages were observed. This implies increase of negative charges at higher temperatures above room temperature. By considering V_{fb} shifts between CV curves at 77 K and 298 K ΔN_{it} was calculated By Gray-Brown technique [26] and it was $(1.19\pm0.5) \times 10^{11}$ cm^{-2}. This ΔN_{it} is a measure of near-interface trap densities, energetically between ~0.05 eV to ~0.2 eV below the conduction band edge [27].

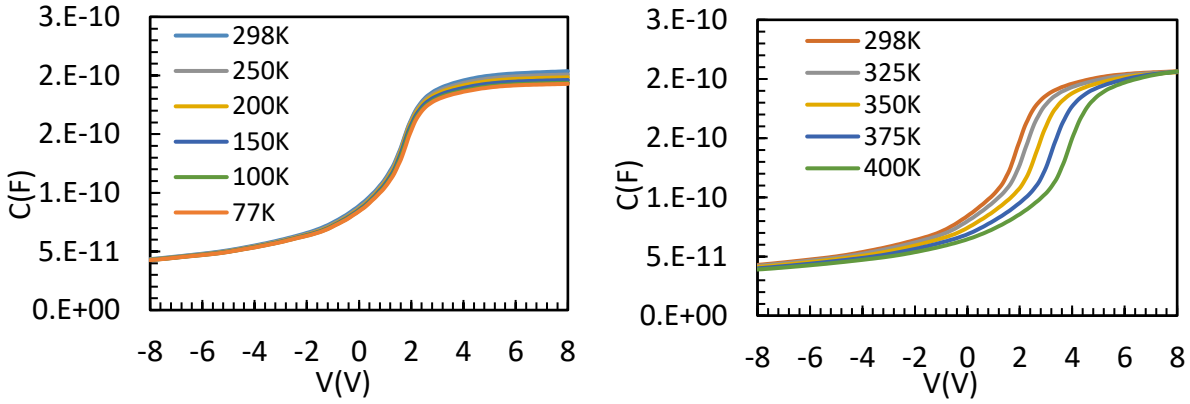

Figure 3.21: 1 MHz capacitance-voltage (CV) measurements performed from 77 K- 400 K region

CCDLTS was performed on three devices keeping the capacitance constant at 60 pF (deep depletion) for different emission rate windows. In addition, while keeping the emission rate window fixed, the pulse voltage (V_P) was changed from V_{fb}-2V to V_{fb}+5V. No peaks were observed in the temperature range of 77 K to 475 K but the CCLTS signal was slightly increased when the temperature was increased, indicating possible deep traps in valence band side. As shown in Figure 3.22 neither O1 nor O2 traps were present in the Al_2O_3/4H-SiC MOS devices fabricated

on H-terminated 4H-SiC. This is the first-time observation of the absence of O1 and O2 in the Al_2O_3/4H-SiC interface with H_2 treatment, strongly suggesting that the origin of the O1, O2 near interface oxide traps are inherent to the SiC/thermal SiO_2 interface.

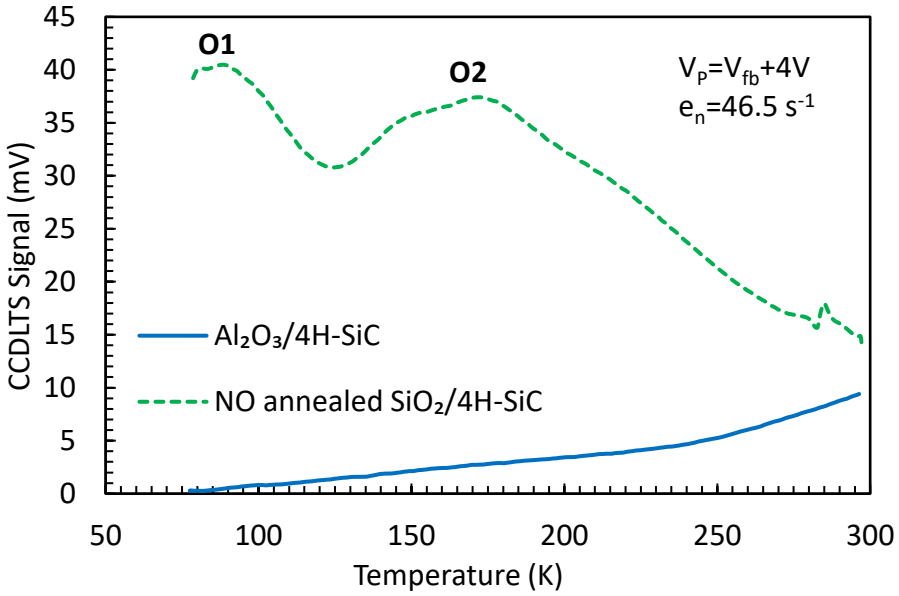

Figure 3.22: CCDLTS for 4H-SiC capacitors with ALD Al_2O_3 and NO annealed SiO_2 as gate dielectric. The ALD was performed after H_2 etch and H_2 annealing of the 4H-SiC [16]

3.6. Summary

'O1' and 'O2' are signature traps in SiO_2/4H-SiC MOS interfaces with emission activation energies of 0.15 ± 0.05 eV and 0.39 ± 0.1 eV below the SiC conduction band. The origin of these traps has been assigned to C-dimers on oxygen sites and Si- interstitials (Si_i) inside SiO_2 near the interface. Post oxidation passivation methods such as NO annealing, PSG or BSG incorporation do not completely remove these signature traps but can significantly reduce them. It is possible that O1 and O2 near interface oxide traps in SiC/thermal SiO_2 interface may affect the MOSFET channel conductance.

For different wafer orientations of 4H-SiC/nitrided SiO_2 MOS interfaces 'O1' and 'O2' trap densities are changing depending on the wafer orientation. While O1, O2 traps were observed for the (0001) Si-face, two new traps named A1, A2 were observed for the $(11\bar{2}0)$ a-face in the same energy range as O1. O2 was also present in a much lower concentration. For the $(000\bar{1})$ C-face, no low-temperature peaks including O1/O2 were detected as the signals from energetically deeper traps dominate the spectra and mask possible shallow trap peaks. According to the observed CCDLTS results for different wafer orientations, it is possible that, O1/O2 trap density differences in these wafer orientations has an impact on channel mobility variations between 4H-SiC wafer orientations.

As a result of different nitrogen doping concentrations in 4H-SiC, in addition to the typical O1 and O2 peaks, a clear 3rd peak (labeled O3) was observed for moderately higher N-doping concentration. The sharpening and dominative behavior of O3 in moderately higher n-doped 4H-SiC and the origin of O3 is unclear at the moment. Regardless of 4H-SiC doping concentration, O1 and O2 Near interface traps are present in SiO_2/(0001) 4H-SiC MOS interfaces in about the same order of trap densities.

Most importantly, neither O1 nor O2 traps were present in the Al_2O_3/4H-SiC MOS interface fabricated on H-terminated 4H-SiC, strongly suggesting for the first time that the origin of the O1, O2 near interface oxide traps are inherent to the SiC/thermal SiO_2 interface. CCDLTS analysis provides information on the identification of interface trap types, which may play an important role in defining the MOSFET channel conductance in the 4H-SiC/SiO_2 interface.

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Chapter 4

Effect of 4H-SiC surface treatments on Al_2O_3/4H-SiC MOS devices

During thermal oxidation of 4H-SiC as the oxide grows by the reaction of O_2 with SiC, the SiO_2/4H-SiC interface moves towards the semiconductor as the top layers of SiC converts into SiO_2. In contrast to that, for deposited dielectric thin films, the initial 4H-SiC surface bonds to the dielectric and becomes the final dielectric/semiconductor interface. Obtaining SiC surfaces with minimum electronic and structural defects is important especially for deposited dielectrics. As an alternative for SiO_2, as discussed in chapter 1, high-k dielectrics are attractive for improved power device applications. Among these materials, Al_2O_3 is the most widely studied dielectric with excellent reported SiC channel mobilities and low interface trap densities. In this work, a systematic study of 4H-SiC surface treatments prior to ALD is performed and their effects on interface trap densities and MOSFET channel mobilities are studied for Al_2O_3/4H-SiC interface. It is concluded that the surface termination of 4H-SiC is the key to obtain practical Al_2O_3/4H-SiC MOS devices using ALD Al_2O_3 with high channel electron mobilities compared to typical nitrided SiO_2. As mentioned in Chapter 3, we found that the O1, O2 inherent traps in SiO_2/4H-SiC, were absent in Al_2O_3/4H-SiC MOS devices fabricated on H-terminated 4H-SiC. This motivated to look into the effect of surface treatments of 4H-SiC on MOS interface trap densities. The proposed SiC surface treatments described in this study can be extended for other deposited high-k dielectric for better performance and characteristics of future SiC devices such as FETs for high-temperature CMOS technology.

In addition to that, the effect of each proposed surface treatment on 4H-SiC surface chemistry, oxide stability, gate leakage, high-temperature post-deposition annealing, temperature dependent performance of Al_2O_3/4H-SiC MOS devices are also discussed in detail. Finally, the relationships between channel mobility versus interface trap densities of SiO_2 and Al_2O_3 is also discussed.

4.1. Different surface treatments in (0001) 4H-SiC

To investigate the effect of surface treatments on n-4H-SiC/Al_2O_3, MOS capacitors and lateral MOSFETs were fabricated and electrical characterizations were performed. The surface treatments were done on (0001) Si-terminated 4° off-axis 4H-SiC surfaces after the standard RCA cleaning as described in the appendix and prior to ALD Al_2O_3 (Section 4.2 includes experimental details). The objective was to modify the Al_2O_3/4H-SiC interface based on approaches reported in the literature and optimization of the interface with low D_{it} and high channel mobility as well as to maintain good device stability with low dielectric leakage. In this section, reasons for choosing specific 4H-SiC surface treatment methods are discussed with existing experimental and theoretical research data. The main surface treatments discussed in subsections here are sacrificial oxidation in O_2, sacrificial oxidation in NO, growth of ultra-thin (<2nm) oxide, H_2 annealing, the combination of sacrificial oxidation in O_2 with H_2 annealing and the combination of sacrificial oxidation in NO with H_2 annealing.

4.1.1. Sacrificial oxidation in O_2

Before any surface treatment, an initial organic and RCA cleaning [1] was performed to remove particles, organic and ionic substances of the sample surface. Next, as the first surface treatment method, a dry thermal oxide, about 20 nm thick was grown at 1150 °C for 2 hours in pure O_2 and etched with 6:1 buffered oxide etch (BOE) prior to ALD. BOE is widely used both in Si and SiC device fabrication processes as an HF based etchant yielding better surfaces with uniformity. Dhar

et al. [2] reported HF etching of oxidized SiC yield hydrophilic surfaces which in contrast to the hydrophobic H-terminated surfaces resulting in oxidized Si surfaces. They also observed that the last monolayer of oxygen from the SiO_2 remains bonded to the SiC surface even after the HF etch. Therefore, these surfaces can be considered to be O-terminated or passivated by a layer of SiO_x or SiO_xC_y.

The surface properties of n- and p-type 4H-SiC has been conducted using X-ray photoelectron spectroscopy by Huang et al. [3] to observe the effect of such sacrificial oxidation. Figure 4.1 shows the Si2p, O1s, and C1s spectrum of n-and 4H-SiC surfaces respectively for before and after performing sacrificial oxidation. The basics of XPS have been discussed in Chapter 2 of this dissertation.

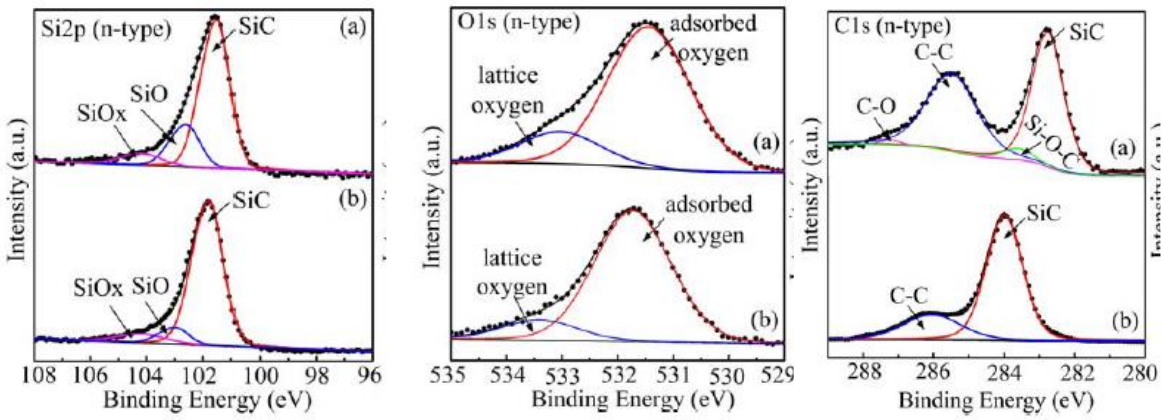

Figure 4.1: XPS analysis of Si2p, O1s and C1s spectrum of n-type (0001) 4H-SiC surfaces (a) before and (b) after the sacrificial oxidation [3]

They observed that for both n- and p-type SiC samples, a significant reduction of SiO_xC_y (silicon oxycarbides), lattice O (SiO_x), and C-C (carbon clusters) from the SiC surface after the sacrificial oxidation according to the XPS spectra. Also, Si-O-C (silicon oxycarbide) disappeared with sacrificial oxidation from the SiC top surface [3]. For the n-type sample, two surface defect centers

named H1 and H2 which were detected by DLTS were also completely removed by sacrificial oxidation. These H1 and H2 defects were suggested to be C-dimers and the trap energies were 0.68 and 1.55 eV below the E_c respectively. It was concluded that SiC sacrificial oxidation in O_2 reduces contamination and remove defects of both n- and p-type SiC.

Thus, these results indicate that the incorporation of sacrificial oxidation in O_2 prior to oxidation or oxide deposition is beneficial for a more uniform, defect passivated, and considerably stable dielectric/4H-SiC interface with and low D_{it} for device fabrication.

4.1.2. Sacrificial oxidation in NO

4.1.2.1. Nitrogen bonding and defect passivation on SiC surface

As the second surface treatment method, after initial cleaning of the sample, an oxide thin film was grown at 1175 °C for 2 hours in pure NO (ramping up/down the temperature from/to 900 °C in Ar) and etched with 6:1 buffered oxide etch (BOE) prior to ALD. The motivation behind the replacement of O_2 (as in the previous section) by NO for sacrificial oxide growth ambient was the incorporation of nitrogen at the interface to obtain a NO annealed like interface [4] with low D_{it} and high reliability. The treatment offers a way to deposit dielectrics on the nitrided surface. By this pre-treatment method, high-temperature exposure for nitridation is avoided on the ALD thin film, to protect it from crystallization described in chapter 4.

A similar approach has been experimented by Lichtenwalner et al. [5] when a thin (~1.5 nm) nitrided SiO_2 interface layer (without etching), formed in NO at 1175 °C and by depositing a 25 nm Al_2O_3 using ALD for fabricating a high (106 $cm^2/V \cdot s$) peak channel mobility MOSFET using 4H-SiC. In that case, a counter-doped channel was used to obtain the high mobility and the effect of nitridation of Al_2O_3 was not clear.

Shirasawa et al. [6] have discussed the formation of silicon oxynitride (SiON) epitaxial layer [7] by H_2 etching (1350 °C for 15 min) and subsequent N_2 anneal at 1350 °C. Authors have performed XPS and Low Energy Electron Diffraction (LEED) analysis and concluded that this SiON layer has an absence of dangling bonds as well as atomically abrupt and uniform interface with SiC. Based on their observations they have suggested an atomic-scale structural model in which N atoms are incorporated to form this interface [7].

Later, Xu et al. conducted XPS on HF etched NO annealed SiO_2 films on 4H-SiC to understand the N bonding nature and compared it with the SiO_2/Si interface [8]. According to the XPS results, they concluded that N is bound to SiC in a way it does not get removed by HF and stays at the surface of SiC layer by strong bonds. However, for Si, after the HF etch N1s signal has vanished. Figure 4.2 shows the nitrogen 1-s spectrum with possible peak assignments and predicts that a structure with 3 Si atoms bonded to one N atom dominates on the SiC surface after etching of NO annealed SiO_2.

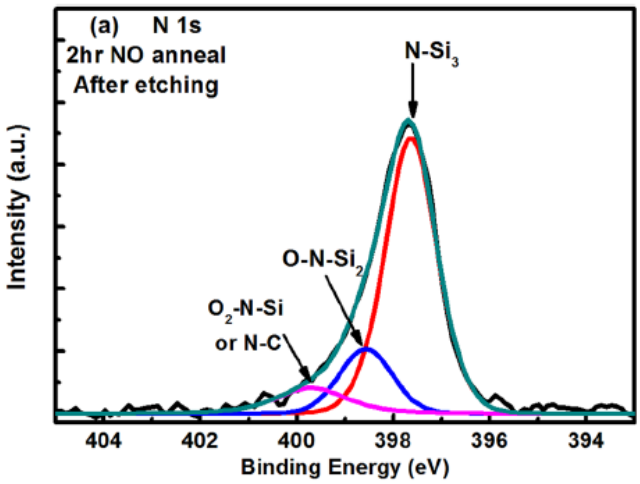

Figure 4.2: Nitrogen 1s spectrum with possible peak assignments [8].

Kosugi et al. have also reported that by investigation of nitrogen atomic profiles in the SiO_2/SiC interface by XPS measurements, a significant number of nitrogen atoms (areal density of 10^{14} cm^{-2}) remain fixed even after complete removal of the oxide layer by HF etch confirming Xu's observations [9]. As the composition of the interface is similar between SiO_2 annealed in NO and SiO_2 directly grown in NO, it is expected that the resulting surface after HF etching is very similar as well.

Xu et al. proposed two models for the thermodynamically stable Si_3N structures for N-incorporated SiC interfaces before etching as in Figure 4.4. By validating the experimental (XPS) data with theoretical density function theory calculations, they concluded that Model 2 is an attractive model for the Si-N-O interlayer with half monolayer coverage of nitrogen on the SiC surface. The interlayer was suggested to be related to rows of nitrogen atoms, each with silicon as the nearest neighbor with N, bonding directly to the Si atoms on SiC top layer. Carbon and Oxygen atoms were suggested to be the second nearest neighbors of nitrogen atoms as shown in Figure 4.3 [8].

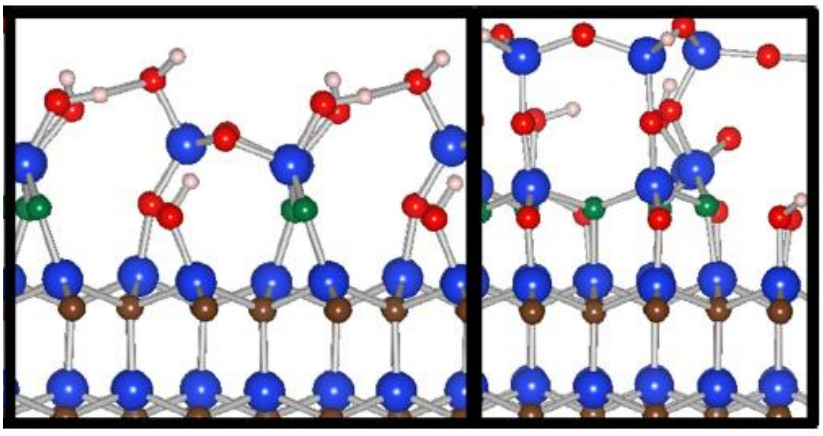

Figure 4.3: Models (Model 2:left, Model 3:right) for SiC/Oxynitride interfaces (before etching) with Si (blue), C (brown), N (green), O (red), and hydrogen (white) [8].

Therefore, it can be said that this interface is rich with nitrogen but still the presence of C and O related defects are to be expected from the structures on oxidation kinetics considerations [8]. This result predicts that the resulting Si-N-O molecular structure on the SiC surface after NO sacrificial oxidation.

Kosugi et al. [7] have also proposed that in the nitrided SiO_2/SiC interface, N atoms from a special chemical bond, so they become resistant to HF etching. The formation of a perfect epitaxial monolayer of silicon oxynitride (SiON) on (0001) 6H-SiC surfaces after nitridation agreed with Xu's proposed structure of Si-O-N like bonding nature in this study.

In addition, Umeda at al. has studied the nitrided SiO_2/SiC interface regions of n-channel lateral 4H-SiC MOSFETs using low-temperature electrically detected magnetic resonance (EDMR) spectroscopy and other related techniques. They have concluded that the nitrogen atoms have two primary behaviors at the SiO_2/4H-SiC interface, first being the removal of shallow interface states detectable at 20 K and secondly nitrogen acting as a dopant in the channel region, resulting in increased channel conductivity of SiC MOSFETs after post-nitridation annealing [9], [10].

Pitthan et al. [11] have incorporated nitrogen in different amounts into the SiO_2/4H-SiC interfaces and studied the resulting surface wettability to understand the nitrogen bonding behavior at the interface. They have observed that compared to a nitrogen-less surface, a nitrogen-rich surface is more hydrophobic. Also using the variation of surface chemistry with nitrogen coverage they were able to show that total surface energy has reduced when the N/O ratio is increased. With proportionality data, they concluded that simple atomic substitution of oxygen by nitrogen is impossible but instead, the presence of SiO_xN_y is a more acceptable model when it comes to nitrided SiO_2/4H-SiC interface bonding. The proposed bonding model is shown in Figure 4.4.

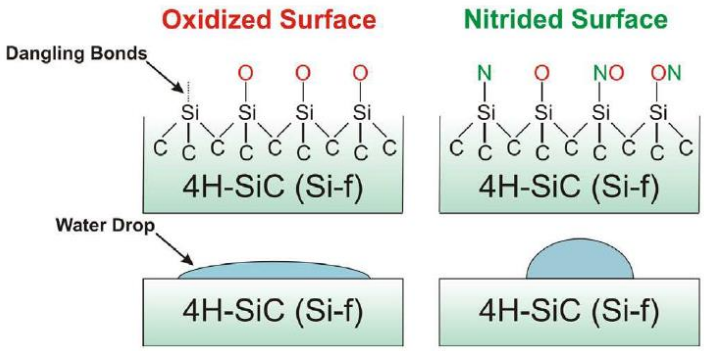

Figure 4.4: Representation of an oxidized (hydrophilic) and a nitrided (hydrophobic) SiC (Si-face) surface and their effects on a water drop [11].

In the latest finding Umeda et al. have studied the effect of NO annealing in SiO_2 by electrically detected magnetic resonance (EDMR). They have found that an intrinsic defect called "P_{bc} center" is formed when the dry oxidation occurs, and this defect is removed with NO passivation as well as H_2 passivation. P_{bc} center has been assigned to be a carbon-related interface defect and introducing nitrogen into the interface seems to passivate this trap consistent with the findings of Mori et al. [12].

4.1.2.2. Effect of surface nitridation on deposited SiO_2

Rozen et al. [13] have tried combining H_2 treatment/etch (at 1350 ˚C for 15 min at 700 Torr) and then N_2-conditioning [13] (at 1350 ˚C for15 min at 700 Torr in N_2) on 4H-SiC prior to high-temperature oxide SiO_2 deposition with LPCVD. Through N_2-conditioning as in Figure 4.5, they have tried to confine nitrogen to the interface prior to dielectric deposition. With XPS and SIMS analysis they have concluded that nitrogen resulting from N_2 conditioning is attached to Si atoms in the form of Si-N bonds as in Si_3N_4 and SiN_2O_2. Here authors have also mentioned the possibility of substitution of C by N at the interface by considering N/Si and C/Si ratios [13]. In this study H_2

treatment/etch seems to act more as a surface cleaning treatment rather than H-termination as described in detail in Shirasawa's [7] and Nakagawa's work [6] .

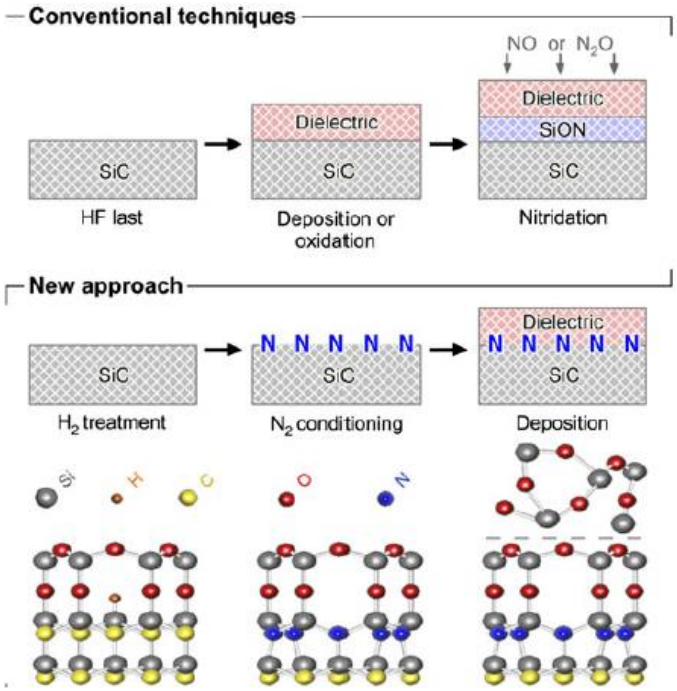

Figure 4.5: Schematic of SiO_2/4H-SiC stacks formed with gate dielectric deposition or oxidation followed by nitridation, and by N_2-conditioning approach followed by the gate dielectric deposition. The bottom drawings are corresponding to atomic configurations previously proposed [13].

Ramamurthy et al. [14] have demonstrated using SiON termination of 4H-SiC to be used with deposited SiO_2. Here they have performed 1500 ˚C H_2 etch to clean and gain atomically flat terraces on 4H-SiC followed by passivation anneal in nitrogen at 1350 ˚C for 15 min to form a stable SiON monolayer. Then SiO_2 was deposited by ALD. By fabrication of MOS capacitors using this method, they have demonstrated that via incorporation of N to the interface, a significant reduction in interface trap density has resulted.

Above mentioned studies suggest that the incorporation of Nitrogen into the SiC/dielectric interface results in defect passivated interface suitable for MOS devices. It can be proposed that sacrificial oxidation in NO prior to deposition of dielectrics results in a Si-N-O bonded SiON layer on top of 4H-SiC. It is possible that the N atoms can replace C sites and thus reduce C-related trap densities.

4.1.3. Insertion of ultra-thin oxide between 4H-SiC and Al_2O_3

Hatayama et al. [15] first reported the insertion of an ultrathin SiO_2 layer between Al_2O_3 and SiC to fabricate $Al_2O_3/SiO_2/SiC$ structures for the improvement of the channel mobility of MOSFETs. The ultra-thin interfacial SiO_2 layer was grown by thermal oxidation of SiC at low temperatures of 600˚C and 800 ˚C in that study.

Without the thin SiO_2 layer they have obtained 64 cm^2/Vs MOSFET peak channel mobility for Al_2O_3/4H-SiC structure (with sacrificial oxidation in O_2 prior to deposition of 70 nm MOCVD Al_2O_3). By insertion of 0.7 nm SiO_2 layer grown at 600 ˚C for 3 min, they have obtained $Al_2O_3/SiO_2/SiC$ structure which yielded an impressive 294 cm^2/Vs MOSFET peak channel mobility without any post-deposition/post metallization anneal. The peak value of the field-effect mobility was 200–300 cm^2/Vs when the SiO_2 layer thickness is less than 1.3 nm, but the interface properties degraded when the SiO_2 thickness was larger than 2 nm. They highlight that the precise thickness of the SiO_2 layer is extremely important for the channel mobility optimization. More importantly, they noted that the insertion of a SiO_2 layer was not effective for the suppression of the leakage current, suggesting that defects in the film are responsible for leakage currents [15].

Arith et al. [16] also reported a similar approach of MOSFETS with $Al_2O_3/SiO_2/SiC$ structure using the same SiO_2 thickness of 0.7 nm (as measured by XPS) and growth conditions as Hatayama with 40 nm ALD Al_2O_3 using TMA and H_2O as precursors. A post-deposition annealing in a

nitrogen ambient at 300 °C for 60 min was also carried out (which was absent in the Hatayama process) and they achieved a MOSFET peak channel mobility of 125 cm^2/Vs. Later using the same experimental conditions, Urresti et al. reported MOSFETs with peak effective mobility of 265 cm^2/Vs as in Figure 4.6 [17]. In addition, using n-, p-MOS capacitors they reported that D_{it} variations are extremely dependent on the interlayer SiO_2 thickness. Maintaining the thickness of 0.7 nm is highly critical to have the lowest D_{it} according to their studies as in Figure 4.8. The low D_{it} yielding thickness window was much narrow and as a result, similar MOSFET mobility variations were observed with interlayer thickness variations [16], [17].

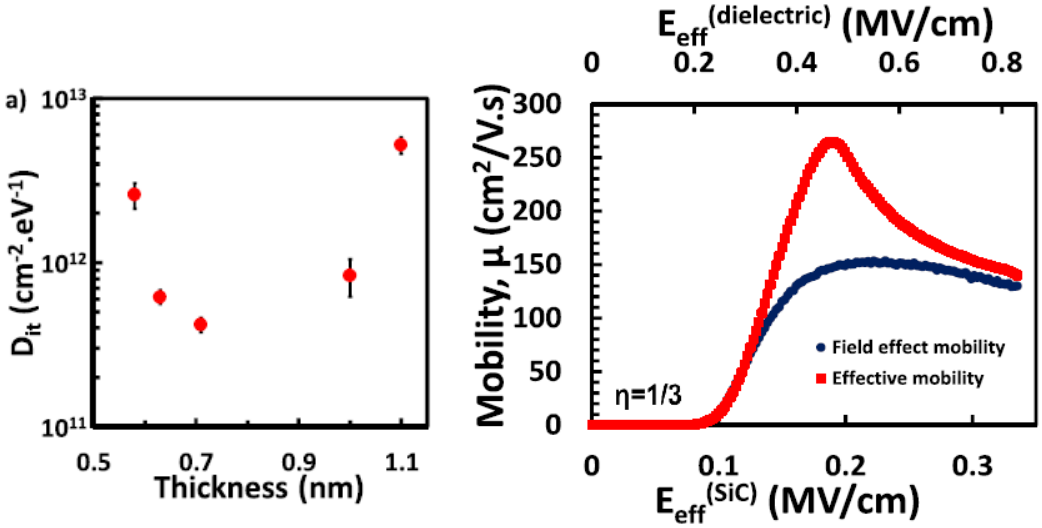

Figure 4.6: Variation of D_{it} with SiO_2 interlayer thickness (a) D_{it} extracted at $E - E_v = 0.2$ eV, for each capacitor as a function of the measured oxide thickness (left). Mobility as a function of increasing effective electric field E_{eff} in SiC resulting from the applied gate voltage (right) [17]

Both of these works have emphasized the criticalness of the interfacial SiO_2 thickness to be exactly 0.7 nm. A possible explanation of this specific thickness number was given by Muller et al. [18] by examining the SiO_2/Si system for Si power device fabrication. This was suggested by resolving the interfacial states that result from the spillover of the silicon-conduction band wavefunctions

into the oxide in SiO_2/Si structure. A fundamental limit of 0.7 nm (across 4 Si atoms) has been placed by the extent of these interfacial states on the thinnest usable SiO_2 gate dielectric thickness. They suggested that for a tunneling barrier to be formed, a minimum oxide thickness of 6λ (λ-decay length for the additional electronic states at the interface states) is needed where it is satisfied by 0.7 nm thick SiO_2 layer [18]. Experimentally, Hatayama, and Arith have observed this phenomenon that thickness increment results in a D_{it} increase, and as a result that, channel mobility has also decreased [15], [16].

However, fluctuations of ultra-thin oxide thickness from the critical value (even in 0.1 nm) had a drastic effect on the channel mobility. However, regenerating the exact process to get thickness condition would be difficult considering the type and nature of furnace, sample loading/unloading time, effect of humidity, ambient pressure, and as well as the thickness measurement methodology. Therefore, there is an inherent difficulty associated with these tight process windows for implementation.

By introducing an ultra-thin SiO_2 layer, several positive outcomes were expected. First, the SiO_2 layer would act as a barrier layer to avoid any undesirable chemical reaction of the SiC substrate during the Al_2O_3 deposition. Second, with a sufficiently thin SiO_2 layer, that the interface state density of the Al_2O_3/SiO_2/SiC structure would be lower than that of the Al_2O_3/SiC structure without the ultra-thin SiO_2 layer. Also, the inserted SiO_2 layer could possibly reduce the effect of Coulomb scattering from the fixed charges present in the Al_2O_3 film [15].

4.1.4. H_2 annealing

For any deposition process, the interface quality is strongly dependent on the properties of the substrate surface. Therefore, a surface preparation results in a high-quality surface which is stable and well passivated in an electronic and chemical sense. From Si, it is known that surface

hydrogenation is a suitable preparation method, which provides clean, unreconstructed, and chemically and electronically passivated surfaces [19]. As shown by Tsuchida et al. [20] H-termination of SiC can be obtained via H_2 annealing at a high temperature of 1000 ˚C for 15 min. The study was conducted by, comparing 6H-SiC surfaces before and after H_2 annealing by Fourier-transformed infrared attenuated total internal reflection (FTIR-ATR) technique. Before annealing, they have not observed any Si-H bond stretching vibrations from the SiC surface. Several kinds of Si-H stretching vibrations were observed from the 6H-SiC (0001) on-axis and perpendicular to the surface after the H_2 annealing under different temperature conditions ranging from 800 ˚C, 1000 ˚C, and 1100 ˚C. Also, they suggested that SiC (0001) prefers to form an intermediate oxide $Si_4C_{4-x}O_2$ with its =Si-O-Si= bonds as the first reaction product from a single Si-C double layer with molecular O_2 where O and C bonded to the Si atom. Hydrogenation of these intermediate oxides was proposed to produce Si-H bonds. At 1000 ˚C a single stretch mode with a narrow linewidth and the bond orientation has been observed in the FTIR-ATR spectrum suggesting that the Si-H bond observed at 2129 cm^{-1} is that of silicon monohydride in which three C atoms bonded to the Si atom. Also, the weak absorption band observed at 2156 cm^{-1} indicated residual surface defect modes such as D1 or T1 structures as in Figure 4.7 after H_2 annealing [20].

Tsuchida concludes in this work that Si-H bonds are formed perpendicular to the surface by removal of the oxide and ordering of the surface structure by H_2 annealing. In another study [21] Tsuchida et al. found that for C-face $(000\bar{1})$ 6H- SiC yields C-H stretching vibrations through H_2 annealing suggesting that atomic H has been absorbed on top sites of the Si- and C- face 6H-SiC. These results imply that via H-annealing, H atoms are incorporated into the interface creating Si-H bonds. This results in the removal or replacement of Si-, O- and C- related defects by uniform Si-H termination yielding a more uniform and ordered surface on the substrate.

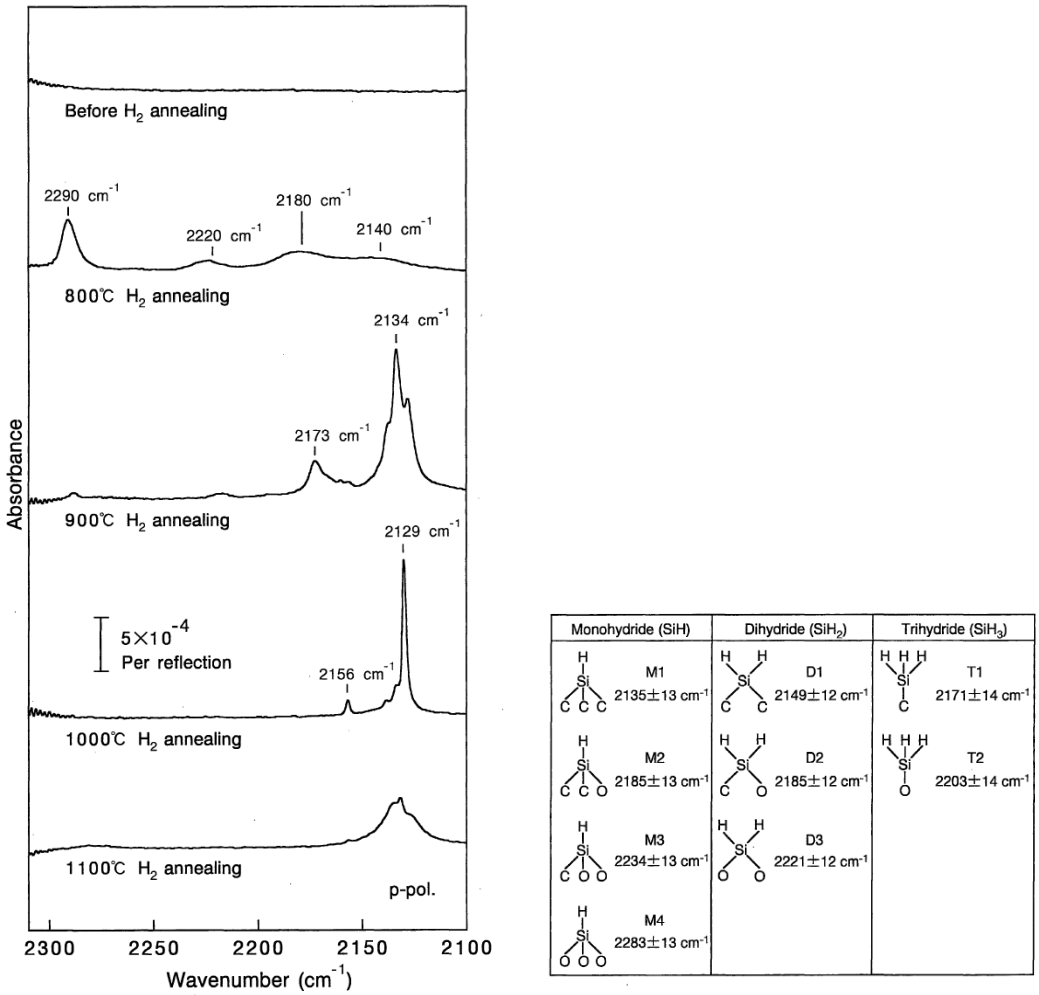

Figure 4.7: Si-H stretching vibrations from the 6H-SiC (0001) on- axis surfaces before and after H_2 annealing in the temperature range of 800-1100 ℃ for p-polarized light (left). Calculated frequency of the Si-H stretching vibrations (right) [20].

Another study by Tsuchida et al. [22] proves that Si-H modes yielded by H_2 annealing lose their sharp feature in the FTIR-ATR spectrum after four days of air exposure, but it was still visible. They have also confirmed that the H_2 treated (0001) surface with strong Si–H stretch modes showed excellent hydrophobic nature even after a short immersion in water, and the surface

became hydrophilic after the H_2O_2 treatment. This study highlights the reactiveness of H-terminated surfaces at the event of exposure to oxidants. For thermal ALD Al_2O_3 substrate surface must be initially -OH terminated, for uniform nucleation during the first deposition cycle of ALD. This study shows that Si-H bonds easily converts into Si-OH bonds which is the preferential surface for ALD.

Sieber et al. [23] have studied H_2 annealed 6H-SiC (0001) surfaces, where hydrogen was not detected by XPS or Low-energy electron diffraction (LEED) as the amount of H is undetectable through those methods. But when XPS spectra of the sample were compared before and after hydrogenation, they have observed that oxygen, fluorine, and hydrocarbon contaminations were removed after the H_2 anneal. LEED pattern has also shown that the surface is well ordered. Again, they prove that the H_2 annealed surface is monohydride Si-H terminated through FTIR-ATR analysis confirming Tsuchida's findings. But here, it =Si-(H_2) and -Si-(H_3) modes were also present in small amounts in the surface in addition to Si-H monohydrides after H_2 anneal.

By analyzing Si2p and C1s core level spectra, hydrogenation of the surface was found to be leading to a shift of core levels to lower binding energies by 0.4 eV. This shift has been assigned by authors as a result of the change in band bending at the surface such that the Fermi level E_F moves closer to its bulk position near the valence band maximum upon hydrogenation as in Figure 4.8. A similar shift in the opposite direction was observed on the n-type $(000\bar{1})$ surface as well. It has been observed that the hydrogen-terminated surfaces exhibit flat band conditions because states that tend to pin E_F near midgap have been effectively removed through hydrogenation. With these findings, Sieber at al. were able to show that hydrogenated Si- and C- face SiC surfaces are electronically and chemically passivated [23]. This result opens the path of using H_2 annealing in

power electronics applications as an interface passivation method via the surface treatment of 4H-SiC.

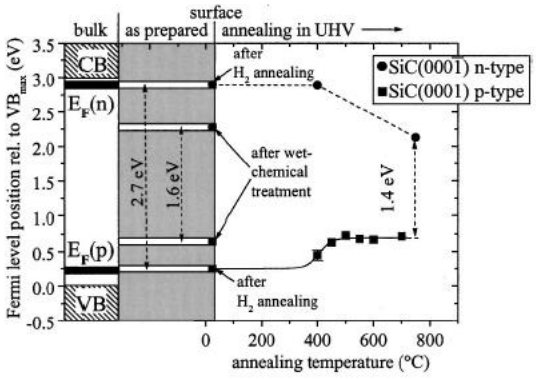

Figure 4.8: Surface Fermi level positions of p-type SiC (0001) and n-type SiC$(000\bar{1})$ as a function of surface preparation and annealing temperature [23].

As a result of these observations, Gao et al. [24] have studied deposited (ALCVD) Al_2O_3 with H_2O and TMA as precursors at 300 ˚C on H-terminated 6H-SiC (0001). H_2 anneal at 1000 ˚C for 15 min, has resulted in an H-terminated clean surface which is chemically inert up to 2 days. The XPS results indicated an atomically smooth and abrupt interface free of significant Si-suboxide and SiO_2 contributions. The Al_2O_3 layer was found to be connected to SiC by bridging oxygen to the Si atoms on the top layer of SiC.

Compared to the thermal oxides, a lower density of interface states, D_{it}, in the upper half the gap was observed by electrical measurements. They have demonstrated that Al_2O_3 provides energy barriers above 1.5 eV for electrons and holes for 4H-SiC for H-terminated SiC [24].

In addition to the above study, Seyller et al. [25] reported Si2p spectra with synchrotron XPS (SXPS) taken from an H-terminated 6H-SiC (0001) sample with an ultrathin (0.35 nm) layer of Al_2O_3 layer. Here, about a monolayer of Si^+ atoms were reported to form the link between the SiC

substrate and the Al_2O_3 overlayer via bridging oxygen atoms. A small component (less than 5% of a monolayer) of SiO_x indicated the presence of non-stoichiometric silicon oxide on the interface in addition to suggesting a small amount of substrate oxidation. The presence of approximately one monolayer of Si^+ and the tiny amount of higher oxidation state Si were mentioned as evidence for an abrupt interface between the Al_2O_3 and the underlying SiC (0001) substrate as a result of H-termination [25].

In summary, H_2 annealing of 4H-SiC results in a more uniform orderly structured Si-H terminated surface. Deposition of dielectrics on this surface can result in low D_{it}. Especially O and C related defect removal are possible by this process, which in turn, leads to improved ALD Al_2O_3/4H-SiC interfaces.

4.2. Experimental details of fabricated Al_2O_3/4H-SiC MOS capacitors

In this study, to investigate the effect of 4H-SiC surface treatments on MOS interfaces, MOS capacitors were fabricated with samples of ~5×5 mm^2 in size diced from Si face (4° off-axis) n-type 4H-SiC epitaxial wafers with 10 μm epitaxial layers doped at ~2×10^{16} cm^{-3} with nitrogen. After the initial standard RCA cleaning, different surface treatment processes were performed as in Table 4.1. Among the surface treatments:

- For sacrificial oxidation in O_2, samples were loaded at 900 ˚C in O_2 (T ramp-up rate 5˚C/ minute), oxide growth at 1150 ˚C for 2 hrs in O_2, and unloaded at 900 ˚C (T ramp-down rate 10˚C/min) in O_2.
- For sacrificial oxidation in NO, samples were loaded at 900 ˚C in Ar (T ramp-up rate 5˚C/ minute), oxide growth at 1175 ˚C for 2 hrs in NO, and unloaded at 900 ˚C (T ramp-down rate 10˚C/min) in Ar.

- For ultra-thin oxide growth, after the sacrificial oxide was etched, different temperatures (550 ˚C-700 ˚C) and time durations (3-10 minutes) were used targeting 0.7 nm thick oxide. Sample loading /unloading was done at the same temperature while pure O_2 was flowing.
- H_2 anneal was performed at 1000 ˚C in atmospheric pressure for 15 minutes and samples were unloaded at room temperature. Temperature ramp down was also in H_2 ambient and samples were unloaded at room temperature.

Table 4.1: 4H-SiC surface treatments prior to ALD Al_2O_3

Process	Surface treatment notation	Sacrificial oxide is grown and etched by 6:1 BOE (step 1)	H_2 anneal at 1000 ˚C(step 2)	Thin oxide growth prior to ALD (step 2)
1	Sac ox O_2	O_2 at 1150 ˚C 2hr	no	no
2	Sac ox NO	NO at 1175 ˚C 2hr	no	no
3	Ulta-thin SiO_x	O_2 at 1150 ˚C 2hr	no	O_2 at 550 ˚C-700 ˚C 3-10 min
4	H_2 anneal	no	yes	no
5	Sac ox O_2 + H_2 anneal	O_2 at 1150 ˚C 2hr	yes	no
6	Sac ox NO + H_2 anneal	NO at 1175 ˚C 2hr	yes	no

- The combination of the sacrificial oxidation and H_2 annealing was performed aiming for an additive effect. To that end, first, a sacrificial oxide was grown on n-4H-SiC at 1150 ˚C in pure O_2 for 2 hours and oxide was etched with BOE completely (5 min). Then 15 min 1000 ˚C H_2 anneal was performed and Al_2O_3 was deposited as described later in this chapter to create the dielectric/4H-SiC interface.

- Similarly, we combined sacrificial oxidation in NO with H_2 annealing. The aim was to see the effect of H-termination and N incorporation of the surface to achieve a further reduction of interface trap density. This was expected to yield H-terminated SiON layer on top of 4H-SiC. To this end, first, a sacrificial oxide was grown on n-4H-SiC at 1175 ˚C for 2 hours in pure NO, and oxide was etched with BOE (5 min) completely and followed by the H_2 annealing. Then, a 15 min 1000 ˚C H_2 annealing was performed and Al_2O_3 was deposited to create the dielectric/4H-SiC interface.

After surface treatments, thermal atomic layer deposition (ALD) was done as described in Chapter 1 in Purdue University, IN at 200 °C and a chamber pressure of 10^{-2} Torr, using Trimethylaluminum (TMA, $Al(CH_3)_3$) as the precursors and H_2O as the oxidizer to deposit ~33 nm of Al_2O_3 (except for the ultra-thin oxide approach in which thickness was ~40 nm). N_2 served as the carrier gas and pulse times were 0.06 s and 0.1 s respectively for the precursor and the oxidizer. The obtained thickness per cycle value of Al_2O_3 was 1.08 Å/cycle. About 100 nm thickness and 300 μm diameter aluminum circular metal gates were formed with mask alignment, photolithography, e-beam deposition, and lift-off process. (detailed process steps are given in the Appendix). After the removal of any residual oxide from the backside, the samples were then attached to copper plates using conducting silver paint to measure the electrical properties.

4.3. Band Alignments of ALD Al_2O_3 deposited on 4H-SiC

Several ~2 nm Al_2O_3 thin layers were deposited on the n-4H-SiC (0001) sample (with sacrificial oxidation in O_2+ H_2 anneal process) to obtain band alignment information of Al_2O_3/4H-SiC. X-ray photoelectron spectroscopy (XPS) and Reflection electron energy loss spectroscopy (REELS) was done as in Figure 4.9 by Rutgers University, NJ. Valence band maximum was obtained by

measuring the binding energy of least tightly bound electrons and the work function of Al_2O_3 was measured from lowest energy electrons that can be excited using an X-ray source of 1486.eV energy. Band gaps of Al_2O_3 and 4H-SiC were measured by REELS using 100 eV electrons. Then the band diagram for H_2 annealed 4H-SiC/Al_2O_3 was obtained as in Figure 4.10.

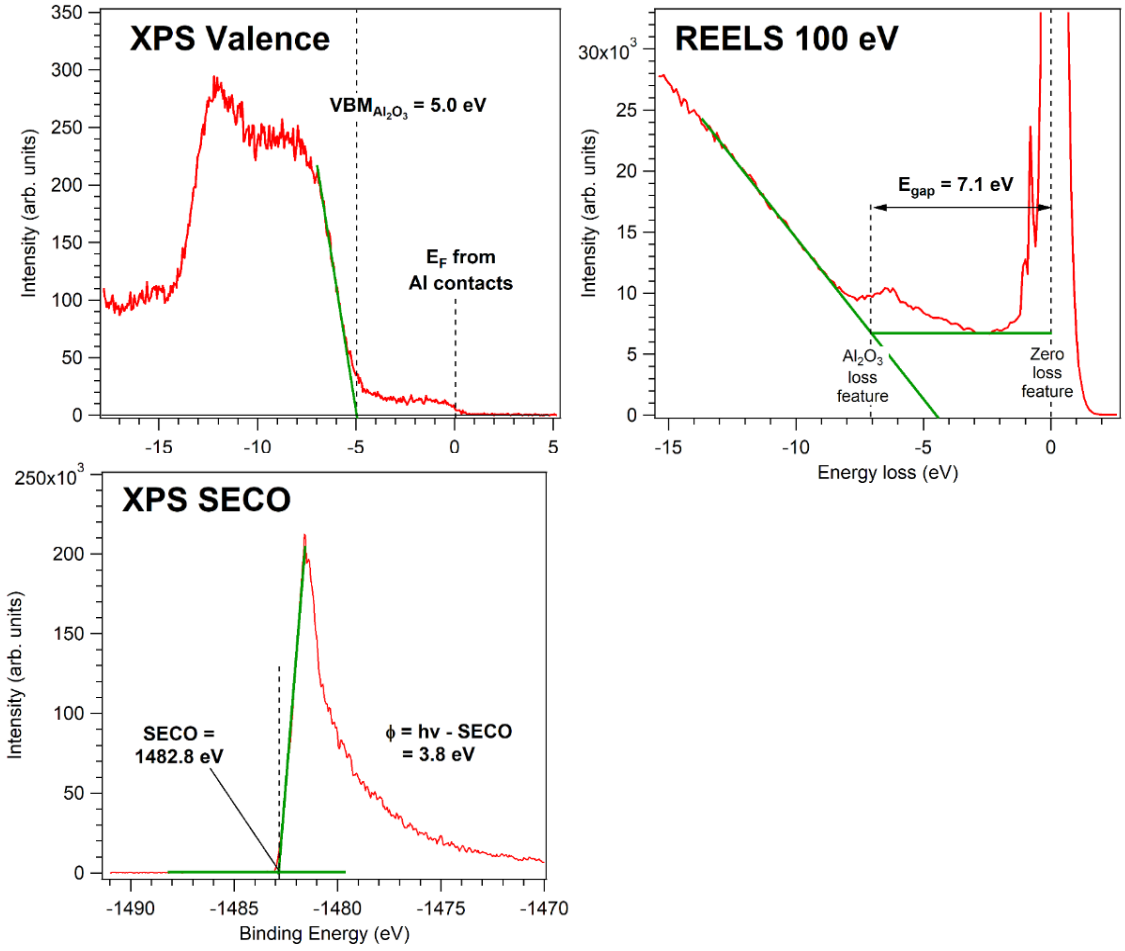

Figure 4.9: XPS and REELS measured for 4H-SiC/Al_2O_3 sample with sacrificial oxidation in O_2+H_2 annealing treatment prior to ALD. [Unpublished, Courtesy: Dr. Ryan Thorpe (Rutgers University)]

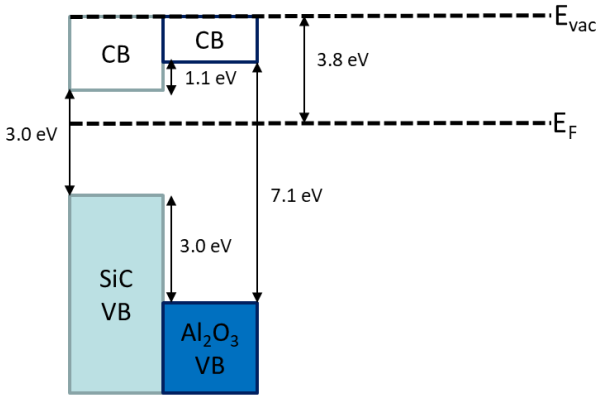

Figure 4.10: Energy band diagram for 4H-SiC/Al_2O_3 sample with sacrificial oxidation in O_2+H_2 annealing treatment prior to ALD. [Unpublished, Courtesy: Dr. Ryan Thorpe (Rutgers University)]

Compared to the energy band diagram of the ALCVD-deposited Al_2O_3 layer on 4H-SiC by Gao et al., slightly different band-offsets were observed. In our H_2 annealed 4H-SiC/Al_2O_3 sample valence and conduction band offsets were 3.0 eV and 1.1 eV respectively while in Gao's work they were reported to be more symmetric as 2.2 eV and 1.8 eV [24]. The differences in band offsets for different samples could be due to the surface preparation method as well as due to the deposited Al_2O_3 quality. But overall band diagram result implies that the Al_2O_3/4H-SiC interface satisfies a > 1eV band offset criteria to be used in device applications.

4.4. CV based trap characteristics of Al_2O_3/4H-SiC MOS capacitors

4.4.1. Effective interface charge density calculations

Using a Keithley 590 CV analyzer, 100 kHz capacitance-voltage (CV) measurements were performed at room temperature, sweeping the bias voltage from the accumulation to the inversion as in Figure 4.11. Effective interface charge densities (N_{eff}) corresponds to the charge present in the oxide or at the oxide-semiconductor interface under flat band condition. N_{eff} corresponding to the experimental flat band voltage from the ideal flat band voltage was calculated for each CV

curve and compared as in Figure 4.12. Ideal flat band voltage for MOS capacitors is defined as in equation 4.1 [26]

$$V_{fb} = \Phi_M - \Phi_S = \Phi_{MS} \tag{4.1}$$

where Φ_M and Φ_S are metal and semiconductor work functions.

Compared to the sacrificial oxidation in O_2/NO, H_2 annealing results in a clear left shift of the CV curves. This corresponds to the overall reduction of negative charges in the MOS capacitors. Insertion of ultra-thin SiO_x layer of 0.7 nm (fabricated at 650 ˚C for 5 min) also yielded low N_{eff}, compared to sacrificial oxidation only samples. But, sacrificial oxidation in NO+H_2 annealing yields the lowest negative N_{eff} associated MOS interface while the lowest N_{eff} was observed for the sacrificial oxidation in O_2+H_2 annealing process. While H_2 annealing reduces effective negative charges, it is possible that incorporation N results in the addition to positive changes to the interface via counter doping which would lead to an effective positive charge.

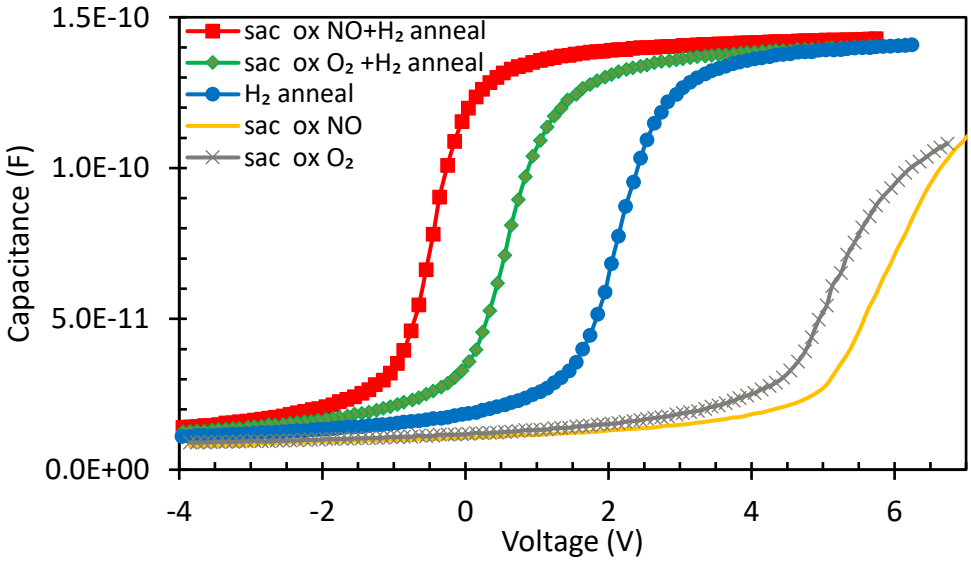

Figure 4.11: 100 kHz capacitance-voltage (CV) measurements for capacitors prepared under different 4H-SiC surface treatments

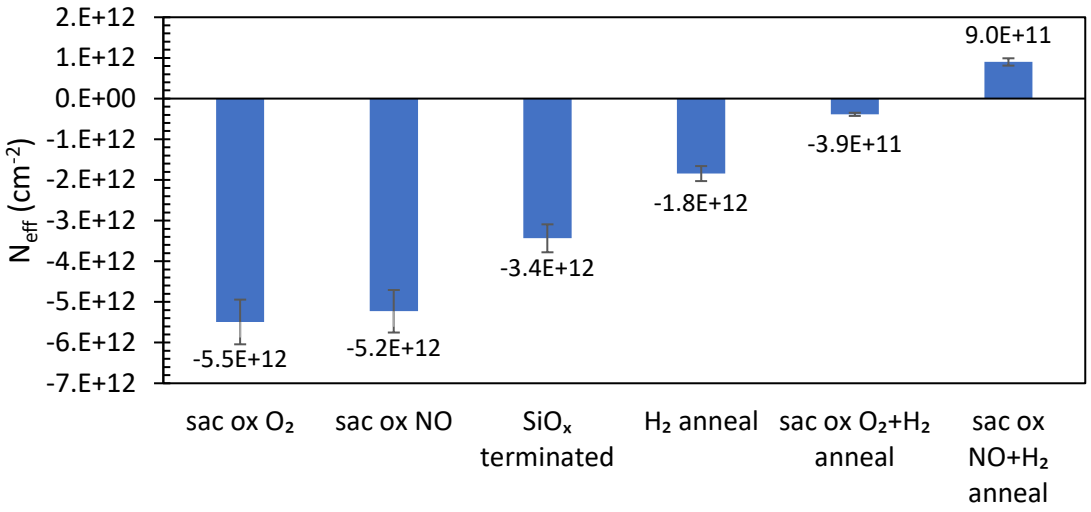

Figure 4.12: Effective interface charge densities (N_{eff}) under the flat-band condition and room temperature for Al_2O_3/4H-SiC MOS capacitors fabricated with different surface treatments.

4.4.2. Simultaneous high-low CV analysis

To investigate the effect of 4H-SiC surface treatments on interface trap densities, simultaneous high-low capacitance-voltage (CV) measurements were carried out on the MOS capacitors using 100 kHz and quasi-static CV measurements with a Keithley 590 CV analyzer at room temperature as in Figure 4.13.

Samples with only the sacrificial oxidation (O_2/NO), were barely able to withstand the positive accumulation voltage due to high dielectric leakage currents, and therefore interface trap densities (D_{it}) would not be obtained by high-low CV method due to large error. But qualitatively based on the dispersion of the high frequency and the quasi-static CV curves, a lower D_{it} can be observed for sacrificial oxidation in NO compared to sacrificial oxidation in O_2.

When H_2 annealing was used, a significant reduction in D_{it} was apparent as in Figure 4.14 with or without sacrificial oxidation. The lowest D_{it} near the conduction band edge was found to be in devices that were fabricated using a combination of sacrificial oxidation in NO and H_2 annealing.

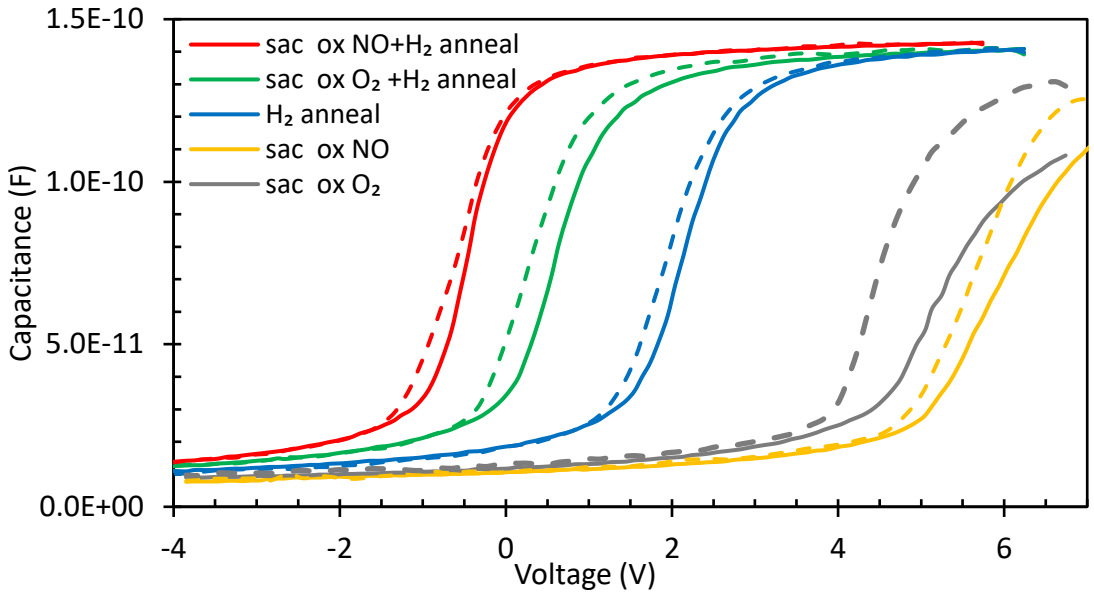

Figure 4.13: High-low CV measurements for capacitors (t_{ox}=33 nm) prepared under different 4H-SiC surface treatments at RT (solid line: CH-100 kHz high-frequency capacitance, dotted line: CQ- Quasistatic capacitance).

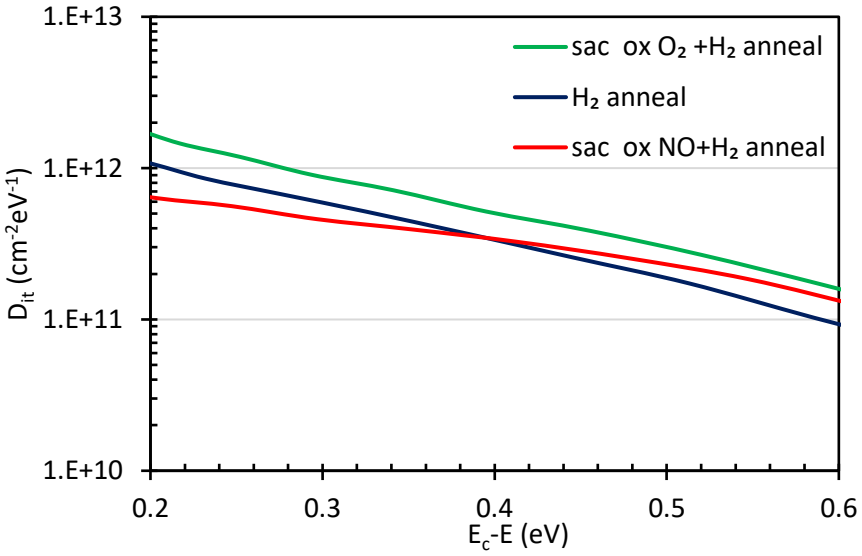

Figure 4.14: D_{it} extracted from high-low CV measurements for capacitors (t_{ox}=33 nm) prepared under different 4H-SiC surface treatments

Simultaneous high-low measurements done at room temperature evaluates D_{it} in E_c-E~0.2 to 0.6 eV range for samples with doping ~2×10^{16} cm^{-3}. This technique is not accurate close to the band-edge but provides a good relative comparison between different interfaces. But for MOSFET, traps closer to the conduction band edge have a huge impact on channel mobility. To analyze such shallow traps (E_c-E$\leq$ 0.2 eV), the Gray-Brown technique is used as described later.

But before that, the insertion of an ultra-thin oxide between 4H-SiC and Al_2O_3 prior to ALD is discussed further with simultaneous high-low method. Previous studies on Al_2O_3/4H-SiC MOS interfaces indicate the majority of the better devices/interfaces were fabricated via a stacked dielectric approach as described under section 4.1. Here we tried to reproduce this result by varying the SiO_2 thickness growth conditions as in Table 4.2 and used XPS to measure the interlayer thickness. (XPS measurements were carried out in Rutgers University, NJ, USA)

Table 4.2: 4H-SiC surface treatments prior to ALD Al_2O_3 (XPS thickness measured using $Si^{2+, 3+, 4+}$ intensities for wavelength λ = 3.7 nm) [unpublished, Courtesy: Dr. Ryan Thorpe (RU)]

Description	Thin oxide growth T/ ˚C	Thin oxide growth time/min	Interlayer (SiO_x) thickness (±10%)
RCA only	none	none	0.1
RCA + sac ox O_2	none	none	0.2
RCA + thin oxide	550	5	0.4
	600	5	0.4
	650	5	0.6
RCA + sac ox O_2+ thin oxide	600	3	0.3
	650	3	0.4
	700	3	0.4
	650	5	0.7
	650	10	0.8
	700	5	0.8

According to the obtained XPS results, the thin oxide was majorly silicon suboxides (Si^{+}, $Si^{2+,}$ and Si^{3+}) rather than Si^{4+} (SiO_2) as in Figure 4.15.

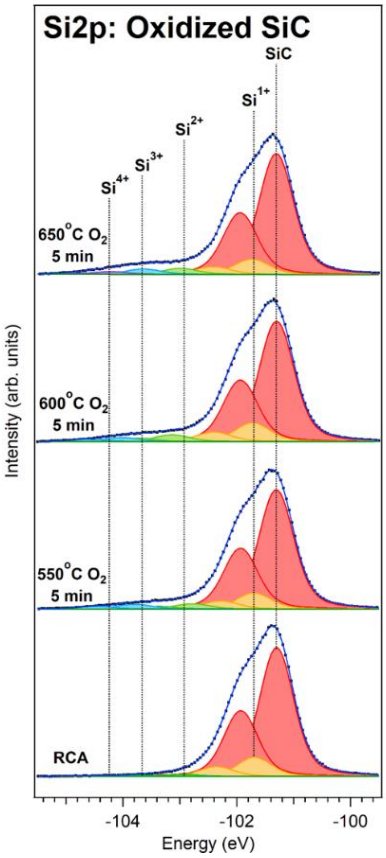

Figure 4.15: XPS spectrum for samples with grown SiO_x thin oxide under different conditions. [Unpublished, Courtesy: Dr. Ryan Thorpe (RU)]

On 4H-SiC samples prepared with the sacrificial oxidation on the O_2+thin SiO_x approach; 40 nm ALD Al_2O_3 was deposited and MOS capacitors were fabricated as in section 4.2. When high-low CV measurements were carried out on these samples, for any of the thin oxide growth conditions a D_{it} reduction was not observed. Figure 4.16 shows that compared to the sacrificial oxidation in O_2 when ultra-thin oxide was inserted the CV dispersion between high and low frequency became worse implying an increase of interface trap densities. In addition, a significant V_{fb} reduction

implying a negative N_{eff} reduction was observed when the SiO_x film growth temperature was increased from 550 ˚C to 650 ˚C. But for 700 ˚C again V_{fb} increased even more than the as-deposited sample. For all the oxidation conditions D_{it} remained high and similar.

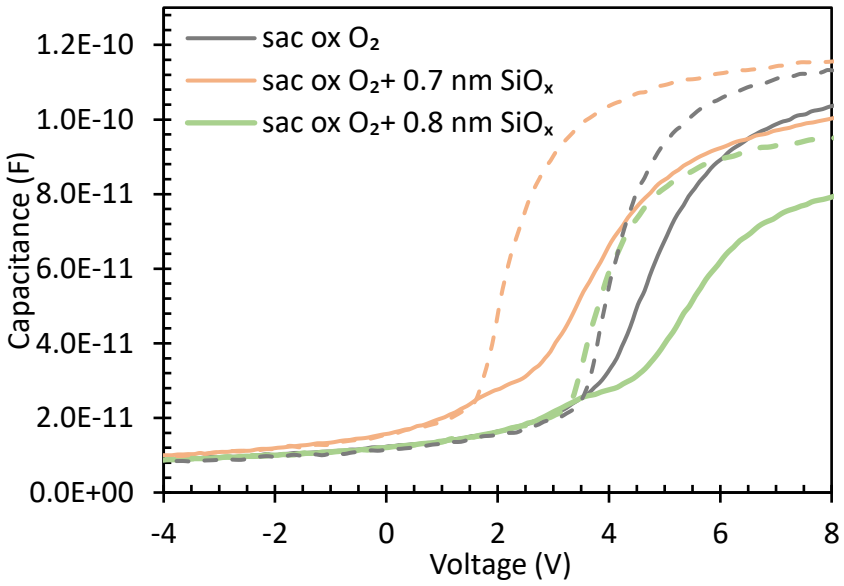

Figure 4.16: High-low CV measurements for capacitors (t_{ox}=40 nm) prepared by inserting an ultra-thin SiO_x layer compared to sacrificial oxidation only sample (solid line: CH-100 kHz high-frequency capacitance, dotted line: CQ- Quasistatic capacitance).

Therefore, the ultra-thin oxide approach was not selected for the fabrication of MOSFETs considering that any high D_{it} would result in poor device performance. This result contradicts reported works [15–17] and this may be due to the difficulty in obtaining the exact ultra-thin oxide thickness ~0.7 nm and the low D_{it} yielding thickness window was much narrow.

It can be concluded that out of all the surface treatments, the lowest D_{it} (for E_c-E=0.2 to 0.6 eV range) is yielded by a combination of sacrificial oxidation in NO and H_2 annealing by simultaneous high-low measurements at room temperature.

4.5. Device stability

CV hysteresis measurements were used to evaluate the defect device stability under bias. The phenomenon of large hysteresis and CV shifting is a critical issue for many deposited Al_2O_3/4H-SiC MOS devices prepared under various conditions in many reported studies. 100 kHz high-frequency cyclic CV measurements were carried out with a Keithley 590 CV analyzer at room temperature as in Figure 4.17. Depletion to accumulation (DA1: sweep 1), backward (AD2: sweep2), and forward (DA3: sweep3) slow measurements were performed in a timescale of seconds. Clearly, after the first bias sweep, CV curves shifted to the right in the next two consecutive sweeps implying that some energetically deep interface traps or bulk traps in the Al_2O_3 closer to the interface [27] get filled during the first sweep remained filled without emitting during subsequent measurements. Schiliro et al. have proposed calculating this slow oxide trap density (N_{ot}) using the shift between the forward and backward CV curves (ΔV_{fb}) [27]. Hydrogen annealing reduces this effect as evident from section 4.2.1. The hysteresis, as measured by the difference between the 2^{nd} and 3^{rd} sweeps was drastically reduced when sacrificial oxidation is done in NO or/and H_2 anneal was employed as a surface treatment step. The combination of sacrificial oxidation in NO with H_2 annealing yielded the lowest hysteresis out of all processes tested. MOS devices prepared with this surface treatment have promising behavior considering the stability of the devices. According to these results, it can be concluded that the main reason for hysteresis in the ALD Al_2O_3/4H-SiC MOS devices is the interface traps, which in turn relates to the termination of the 4H-SiC surface prior to ALD; rather than oxygen deficiencies in the ALD film.

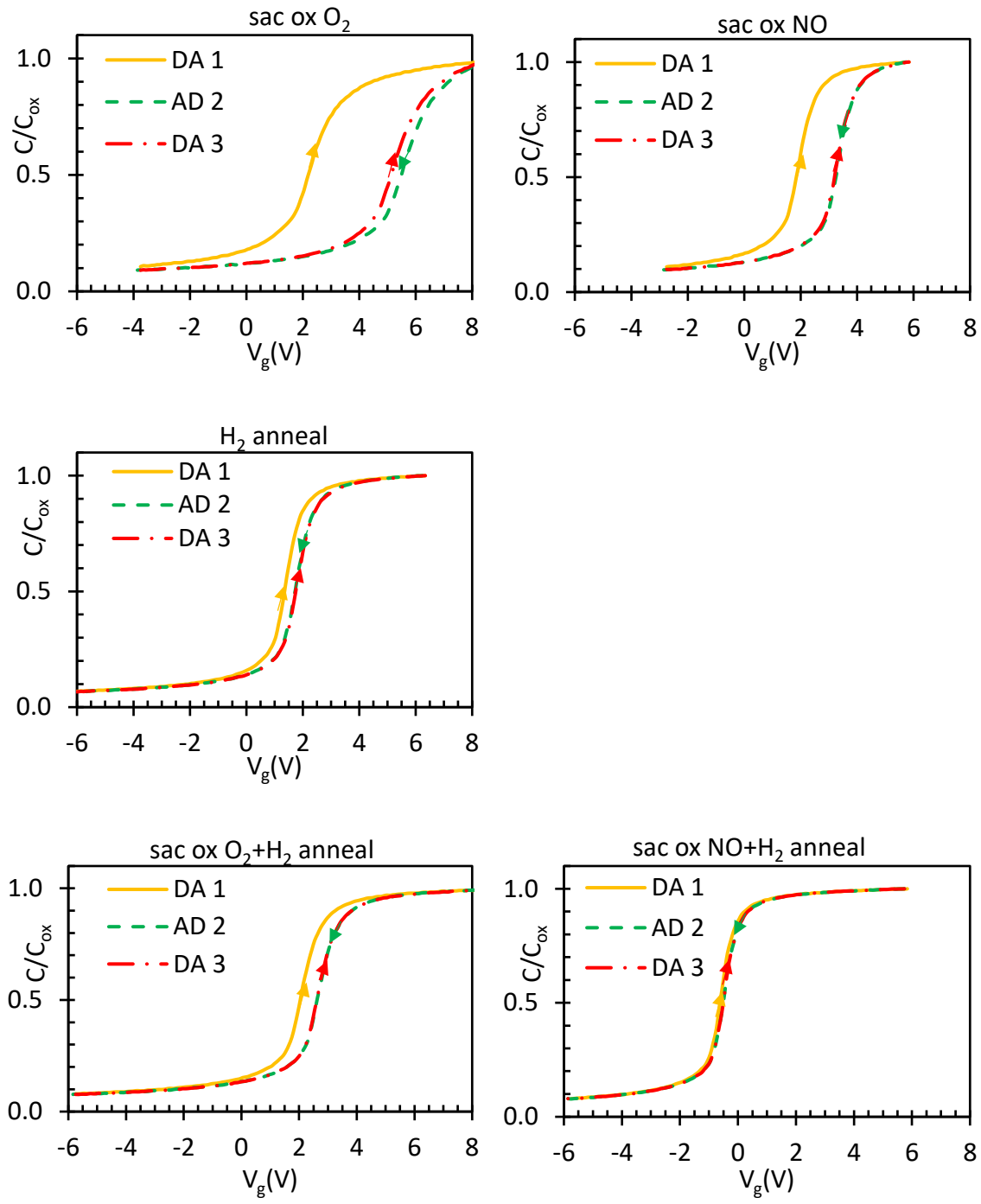

Figure 4.17: CV hysteresis obtained from Gray-Brown technique for Al_2O_3/4H-SiC MOS capacitors fabricated under different surface treatments where DA 1: depletion to accumulation sweep 1, AD 2: accumulation to depletion sweep 2, DA 3: depletion to accumulation sweep.

4.6. Dielectric leakage measurements

A challenging aspect to be carefully analyzed and improved for alternative dielectrics/4H-SiC MOS devices is oxide leakage. Depending on oxide deposition methods (thermal or plasma) and deposition conditions such as temperature and precursors (H_2O or Ozone), oxide quality can be different. But regardless of that, according to current-voltage (IV) measurements measured at room temperature using a Keithley 6517 electrometer/high resistance system, we observed that 4H-SiC surface treatments can affect and improve IV characteristics in MOS capacitors as in Figure 4.18. Especially compared to as-deposited samples, sacrificial oxidation prior to ALD of Al_2O_3 significantly improved device leakage as well as the device yield impressively. In addition, when leakage currents at 1 MV/cm electric field for Al_2O_3/4H-SiC MOS capacitors were compared for MOS capacitors prepared with different surface treatments, a clear difference of leakage current can be remarked and emphasized.

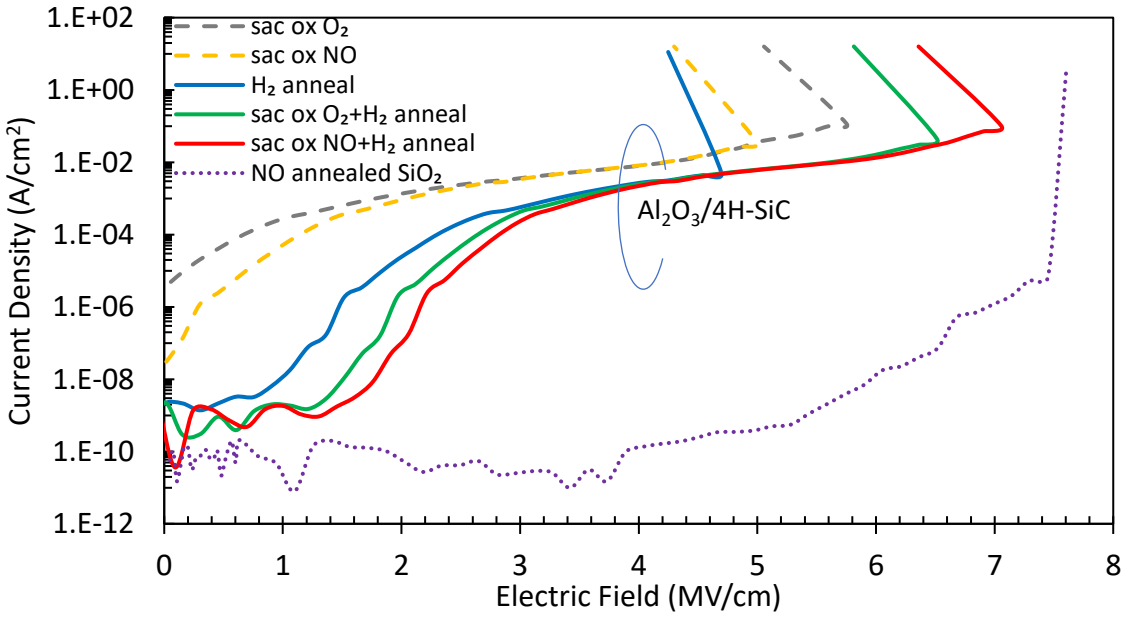

Figure 4.18: IV measurements performed on Al_2O_3/4H-SiC MOS capacitors prepared with different surface treatments. 2 hr NO annealed SiO_2/4H-SiC MOS capacitor IV data is for reference purpose.

While H_2 annealing seems to improve the oxide breakdown electric field, incorporating nitrogen also has the same effect. The highest oxide breakdown field was obtained for sacrificial oxidation in NO combined with the H_2 annealing. Apart from the lowest interface trap densities, this process results in the best leakage properties according to our device characterization. Nevertheless, Al_2O_3 MOS devices need to be improved in the oxide leakage aspect either through optimization of oxide deposition conditions or post-deposition anneal in the future for applying Al_2O_3 in device applications compared to SiO_2.

4.7. Effect of post-deposition annealing

Avice et al. [31] have studied ALD Al_2O_3/n-type 4H-SiC MOS capacitors with different PDA conditions in the Ar atmosphere from 100 to 1000 °C using durations between 1 and 3 h. According to their findings, the lowest V_{fb} and smallest CV hysteresis (i.e. lowest D_{it}) was observed for 1000 °C annealing in Ar for 3 hours. In addition, they have observed a N_{it} reduction after the PDA for the Ec-0.3 eV range implying a shallow trap density reduction [31]. By TEM investigations in combination with XPS, authors found that as-deposited ALD Al_2O_3 samples have a double interface created by an intermediate SiO_x suboxide layer and after 1000 °C annealing in Ar, this intermediate suboxide layer breaks up and transforms into SiO_2 islands which results in a rougher interface region [32]. Using XPS, Usman et al. have also shown that high-temperature post-deposition annealing of Al_2O_3/4H-SiC at 1000°C in N_2O results in forming a thin interfacial layer of SiO_2 between Al_2O_3 and SiC and this possibly results in improved interface properties of the system by reducing oxide charges, near-interface traps, and additional band offset to the dielectric system [33].

Here in this study, to investigate if post oxidation annealing (PDA) can help increase the oxide breakdown electric field or reduce leakage current and to check if the high temperature (900-1000

˚C) ohmic contact annealing can be carried out for Al_2O_3/4H-SiC MOSET fabrication, two MOS capacitors were tested. The first capacitor (labeled sample C1) was fabricated on standard RCA cleaned n-4H-SiC sample with sacrificial oxidation in O_2 and 40 nm ALD Al_2O_3 while on the second capacitor (labeled sample C2) sacrificial oxidation in O_2 combined with H_2 anneal was performed prior to ALD. The chosen PDA condition was 3 hr anneal in Ar at 1000 ˚C. Both MOS capacitors had ~100 nm e-beam deposited Al gates and back contact was silver paint. Here the main goal was to see the effect of PDA for samples with and without H-termination.

When we compared samples C1 and C2 with PDA condition proposed by Avice et al., we also observed a V_{fb} reduction and a D_{it} reduction for sample C1 after the PDA confirming the reference work. But, for sample C2 it was the opposite. For sample C2, where H_2 anneal was performed, we observed a V_{fb} increase as well as a D_{it} increase after the PDA as shown in Figure 4.19.

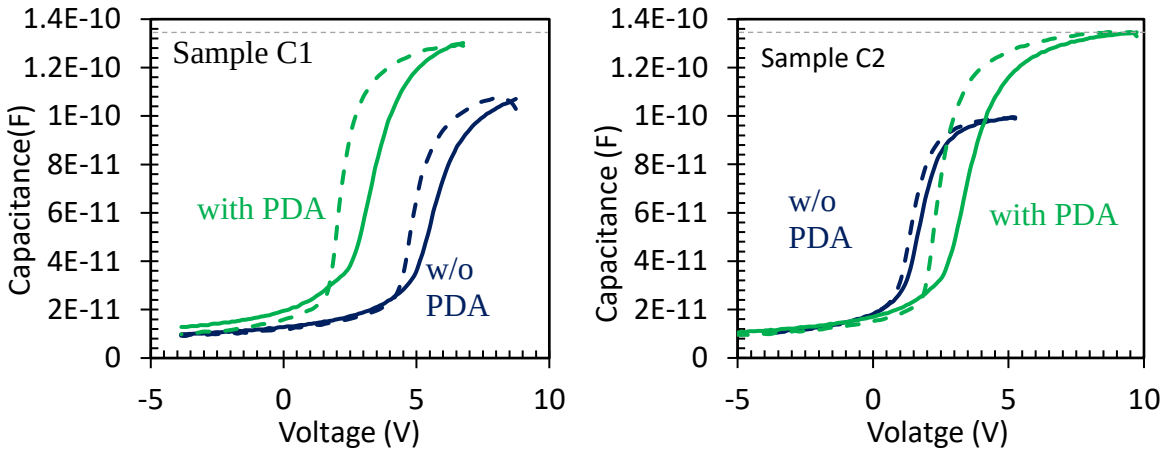

Figure 4.19: Effect of Post deposition anneal (PDA) on sacrificial oxidized in O_2 (left) and sacrificial oxidized in O_2+H_2 annealed (right) 4H-SiC/40 nm Al_2O_3 MOS capacitors by simultaneous high-low CV measurements where dotted lines represent adjusted quasistatic CV and solid lines represent adjusted 100 kHz high-frequency CV.

In addition to that, interestingly for both C1 and C2 capacitors after the 1000 °C PDA, oxide capacitance (C_{ox}) increment was observed. This is due to the phase change of Al_2O_3 from amorphous to polycrystalline phase [28-29] as in Figure 4.20 resulting in densification or a dielectric constant change. Corresponding to the oxide capacitance change we observed relative dielectric constant change from 7.45 to 10.1 proving the change of Al_2O_3 phase. As an alternative explanation, Zheng et al. have proposed that the diffusion of the excess oxygen in the as-deposited Al_2O_3 film into the Si(111) substrate during the high-temperature annealing accounts for the formation of SiO_2 between Al_2O_3/Si interface and thus results in a decrease in the film thickness of Al_2O_3 [30]. But in our case, considering the dielectric constants of SiO_2 (3.9) and Al_2O_3 (7-9), the idea of the formation of SiO_2 layer is not possible as the final oxide capacitance was greater after the PDA than that of before the PDA.

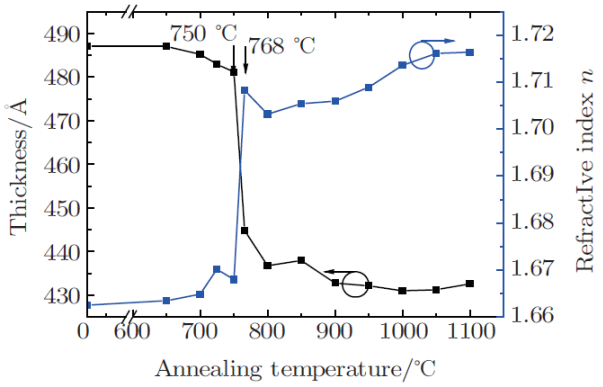

Figure 4.20: Phase change of Al_2O_3 from amorphous to crystalline(γ) by high-temperature annealing [29].

In summary, we observed that high-temperature PDA of Al_2O_3/4H-SiC MOS devices helps improve the electrical properties of as-deposited samples with sacrificial oxidation in O_2 as a surface treatment prior to ALD. However, for H_2 annealed 4H-SiC samples with deposited Al_2O_3, this PDA worsens interface properties. Therefore, exposing H_2 annealed 4H-SiC/Al_2O_3 MOS

interfaces should be avoided from exposure to high temperatures above ~750 °C around when the phase change occurs in Al_2O_3. Practical SiC MOSFETs require annealed ohmic contacts, which poses a problem for using low-temperature dielectrics such as ALD Al_2O_3.

4.8. Al_2O_3/4H-SiC MOSFET fabrication methods and process modifications

Although previous studies have shown some of the effects of proposed 4H-SiC surface treatments using MOS capacitors in regards to the interface trap densities, this is the first systematic study of Al_2O_3/4H-SiC MOSFETs on determining the effect of surface treatments of 4H-SiC on channel conductivity.

Long channel Al_2O_3/4H-SiC lateral MOSFETs (150 μm length x 290 μm width) were fabricated as in Figure 4.21, 1×0.5 mm^2 size (0001) 4H-SiC pieces with 4.4×10^{15} cm^{-3} epitaxial p-well channel regions. The source/drain regions were n+ doped with nitrogen dopant by ion implantation. Next, dopant activation annealing at 1650 °C was performed using a graphite carbon cap. After the carbon cap removal was done at 800 °C in O_2, standard RCA cleaning was performed. Then, different surface treatments as in Table 4.1 were carried out on MOSFET samples. Following that, ~33 nm of Al_2O_3 was deposited using ALD similar to the capacitor fabrication procedure. Finally, by mask alignment, photolithography, and e-beam deposition ~100 nm thickness Al and Ni gate and source/drain metals were patterned. For S/D area etch, 6:1 BOE dip was done for 1 min.

Detailed fabrication steps are included in the Appendix and MOSFET process flow shown in Figure 4.22. However, in this work, no ohmic contact annealing was performed as our goal was to investigate the channel mobility in long channel FETs, where contact resistance has a much smaller effect.

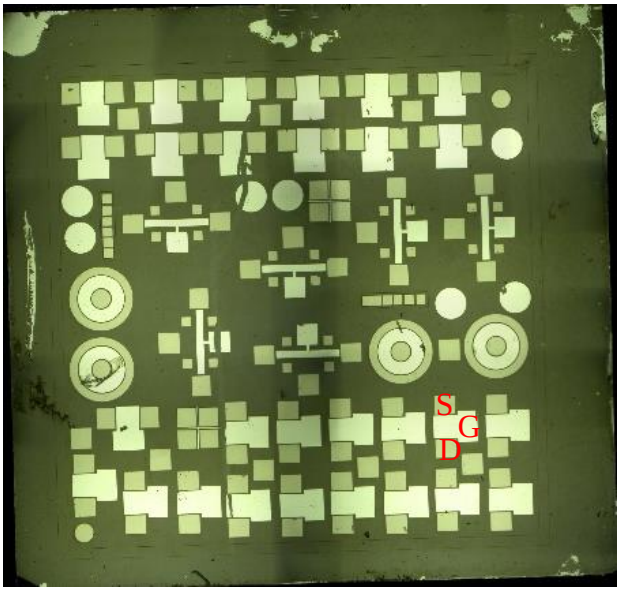

Figure 4.21: Al_2O_3/4H-SiC MOSFET sample top view after fabrication.

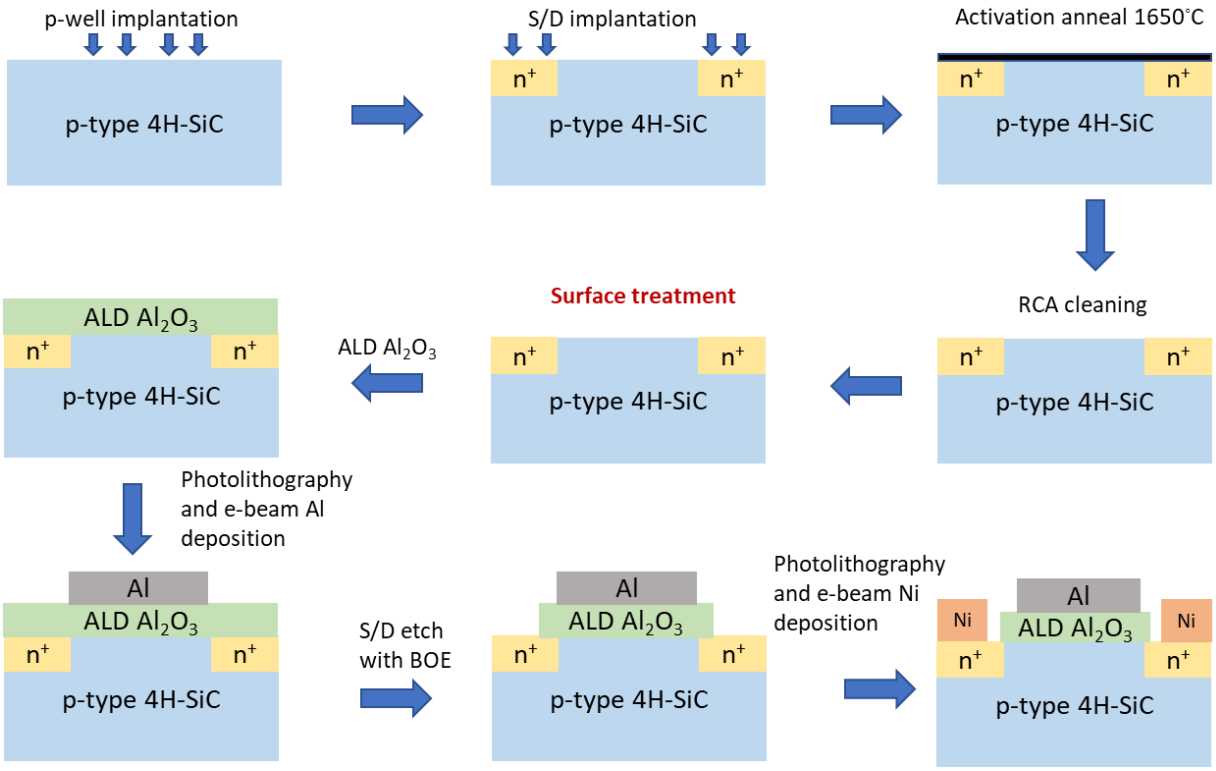

Figure 4.22: Al_2O_3/4H-SiC MOSFET process flow with different surface treatments as Table 4.1

4.9. Effect of 4H-SiC surface treatments on MOSFET Field-effect mobility

To investigate the effect of 4H-SiC surface treatments on Al_2O_3/4H-SiC MOSFET, transfer measurements (I_d-V_g) were carried out and μ_{FE} was extracted by the transconductance of drain current. Typical I_d-V_g measurements with a constant drain voltage of 25 mV at room temperature are shown in Figure 4.23.

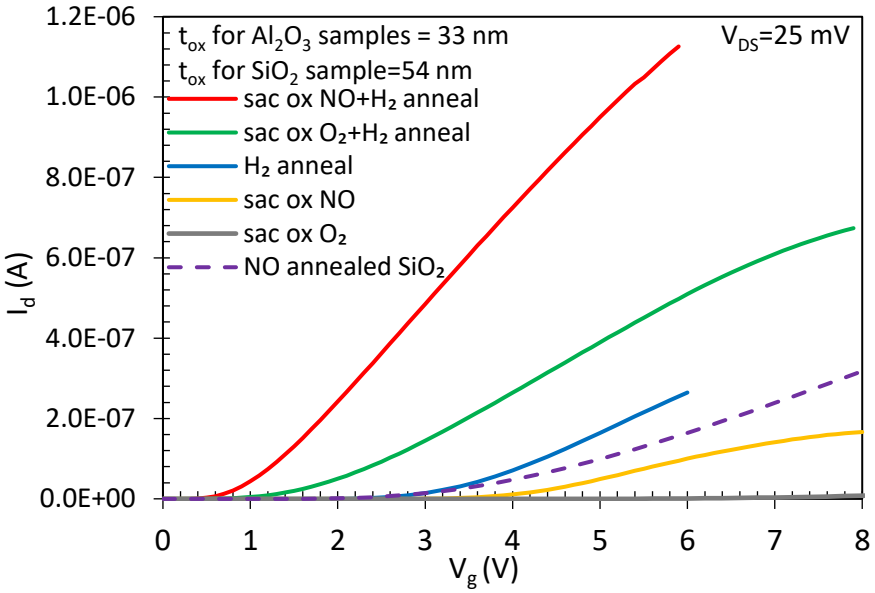

Figure 4.23: I_d-V_g for Al_2O_3/4H-SiC MOSFETs prepared with different surface treatments are compared with standard 2hr NO annealed SiO_2/4H-SiC MOSFET

The corresponding MOSFET field-effect mobilities are shown in Figure 4.24. For comparison purposes, a parallel MOSFET was also fabricated with 54 nm thermal SiO_2 grown at 1150 °C and subsequently, NO annealed at 1175 °C with the same lateral MOSFET structure and process flow. The results of this device are also shown in Figures 4.23 and 4.24.

Clearly, for Al_2O_3/4H-SiC MOSFET channel mobilities depends on 4H-SiC surface treatments according to these findings. Either for sacrificial oxidation in O_2/NO, when H_2 anneal is incorporated a significant channel mobility improvement was observed. Compared to sacrificial

oxidation in O_2, when it is replaced by NO; channel mobility increases further. The enhancement was highest when the H_2 annealing is applied to a nitrided surface. In this case, an impressive peak mobility of 52 $cm^2V^{-1}s^{-1}$ was obtained. It should be noted that this surpasses the standard NO annealed SiO_2/4H-SiC field-effect mobility. When sacrificial oxidation is done in NO, a sub-nm SiON structure formed on 4H-SiC as reported in Xu et al. [8]. When H_2 annealing is carried out on this surface a further reduction of interface trap densities was observed due to Si-H termination on the top layer of substrate (on top of SiON). This is the first observation where a nitrided surface was enhanced using H_2 anneal as a 4H-SiC surface preparation method for a deposited oxide.

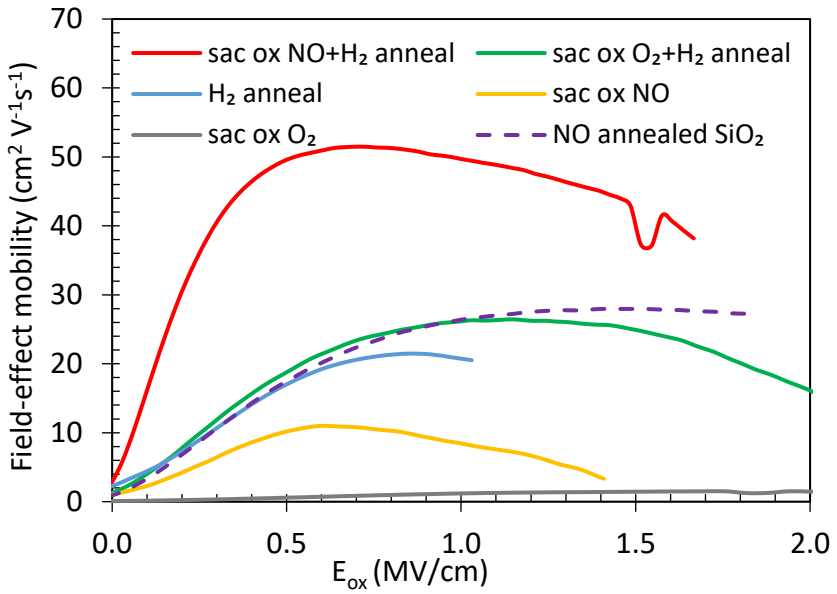

Figure 4.24: Field-effect mobilities for Al_2O_3/4H-SiC MOSFETs prepared with different surface treatments are compared with standard 2hr NO annealed SiO_2/4H-SiC MOSFET.

In parallel capacitors, we observed a D_{it} reduction with NO sacrificial oxidation and/or H_2 anneal. Here in MOSFETs, an inverse relationship trend was observed between channel mobility and D_{it} when all the surface treatments were compared. This relationship between field-effect mobility

and N_{it}/D_{it} also is a general inverse relationship for SiO_2/4H-SiC surfaces and according to these results, it seems valid for Al_2O_3/4H-SiC surfaces too. This relationship is discussed later in detail.

4.10. Trap analysis in MOSFETs using Gray-Brown method

To investigate the effect of 4H-SiC surface treatments on D_{it}, energetically between ~0.05 eV to ~0.2 eV below the conduction band edge [31], 100 kHz high-frequency capacitance-voltage (CV) measurements were carried out on MOS capacitors. For that, a Keithley 590 CV analyzer was used at room temperature (298 K) and low temperature (77 K) by submerging the capacitor in liquid nitrogen. Shallow near-interface trap density (ΔN_{it}) was calculated using equation 2.55 by considering flat-band voltage (V_{fb}) shifts in MOS capacitors and threshold voltage (V_{th}) shifts in MOSFETs at different temperatures.

Similarly, low-temperature I_d-V_g measurements were conducted to extract MOSFET mobility as in Figure 4.25 for the MOSFETs prepared with different surface treatments at 77 K compared to room temperature. MOSFET field-effect mobilities were extracted as in Figure 4.26 at 77 K.

Compared to 298 K MOSFET mobility, at low temperature 77 K; a clear mobility reduction was observed for all the Al_2O_3/4H-SiC MOSFETs prepared with different surface treatments prior to ALD as shown in Table 4.3. In addition, the threshold voltage V_{th} (extracted by linear extrapolation of the I_d-V_g curves) also higher at low temperature compared to room temperature for all Al_2O_3/4H-SiC MOSFETs. This is a result of trap limited /Coulomb limited mobility phenomena. However, nitrogen incorporated devices show a smaller reduction of channel mobility at low temperature compared to room temperature than non-nitrogen processes and this must be because nitrogen incorporation results in passivation of traps near the 4H-SiC conduction band edge.

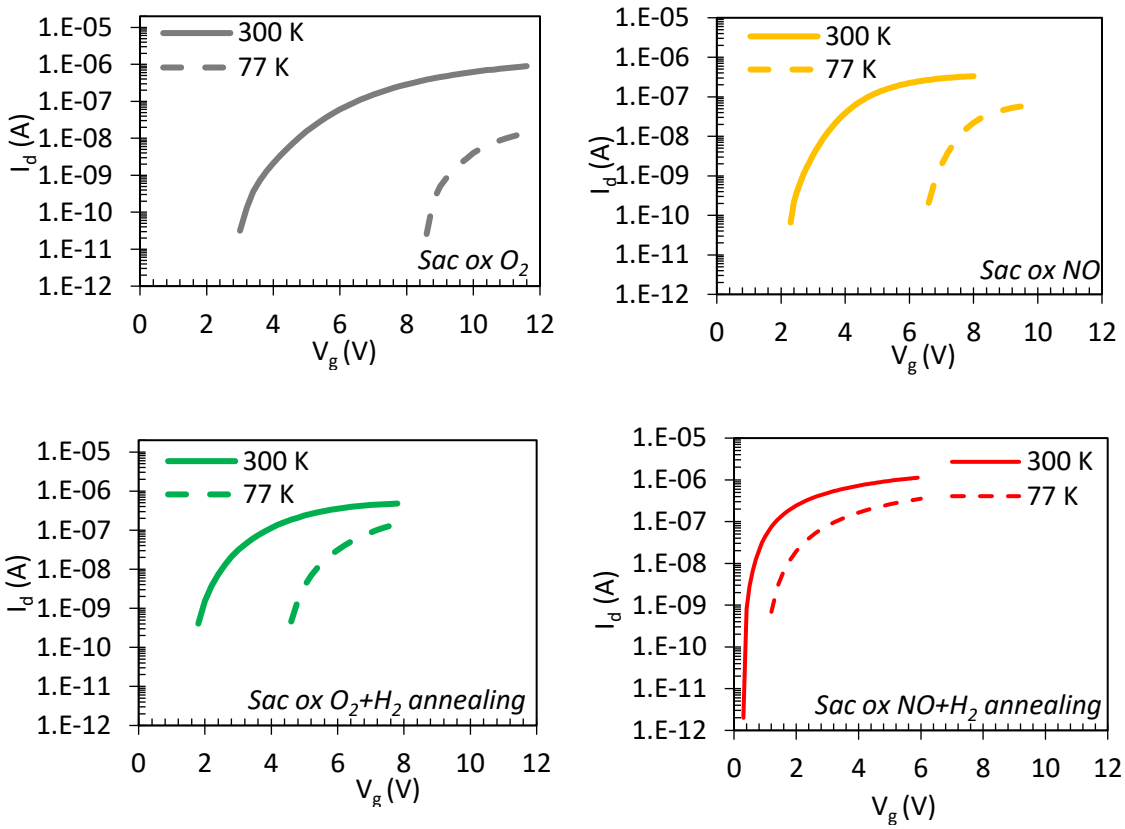

Figure 4.25: I_d-V_g for Al_2O_3/4H-SiC MOSFETs prepared with different surface treatments at 298 K (solid lines) and 77 K (dotted lines).

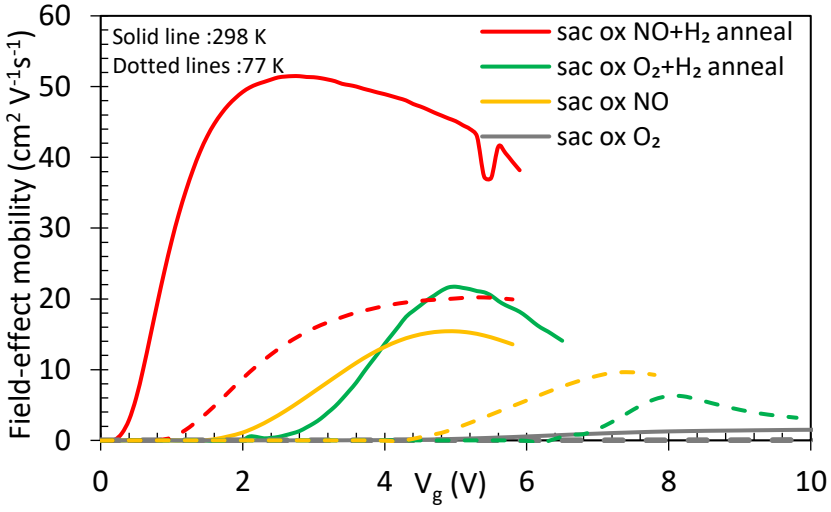

Figure 4.26: Field-effect mobilities for Al_2O_3/4H-SiC MOSFETs prepared with different surface treatments are compared at 298 K (solid lines) and 77 K (dotted lines).

Table 4.3: Peak field-effect mobilities and threshold voltages of Al_2O_3/4H-SiC MOSFETS prepared with different treatments measured at 298 K and 77 K

MOSFET sample	Peak field-effect mobilities (cm^2/Vs)		Threshold voltage (V_{th})	
	298 K	77 K	298 K	77 K
sac ox O_2	1.5	0.2	6.2	9.8
sac ox NO	12	6	3.6	7.2
sac ox O_2+H_2 anneal	26	10	3.1	5.7
sac ox NO+H_2 anneal	52	20	1.0	1.7

All SiO_2/4H-SiC MOSFETs (except PSG MOSFETs) show channel mobility reduction at a low temperature and the reason for this phenomenon can be very high interface trap densities close to the 4H-SiC conduction band edge [32], [33]. A similar trend is observed for our studied surface-treated 4H-SiC/Al_2O_3 MOSFETs as well.

Compared to MOS capacitors, in MOSFETs slightly higher ΔN_{it} was observed as in Figure 4.27. There could be several reasons behind this observation including different biasing voltages corresponding to different band bendings in capacitors and MOSFETs. This ΔN_{it} would lead to trapping and Coulomb scattering limited field-effect mobility in Al_2O_3/4H-SiC interfaces at room temperature as well as at low temperatures. Considering the MOS capacitors and MOSFETs, H_2 annealing makes a strong impact closer to the CB edge or ultra-shallow states according to the Gray-Brown method [34] results. In addition to that, incorporation of nitrogen to the 4H-SiC surface via sacrificial oxidation in NO also reduces ΔN_{it} and for both sacrificial oxidation surfaces (O_2 and NO) but the lowest ΔN_{it} value was observed for the combination of sacrificial oxidation in NO + H_2 annealing process. The impressive reduction of ΔN_{it} for this surface treatment is responding to an additive effect of reduction in near interface traps located closer to the conduction band edge due to the two steps in a combined manner.

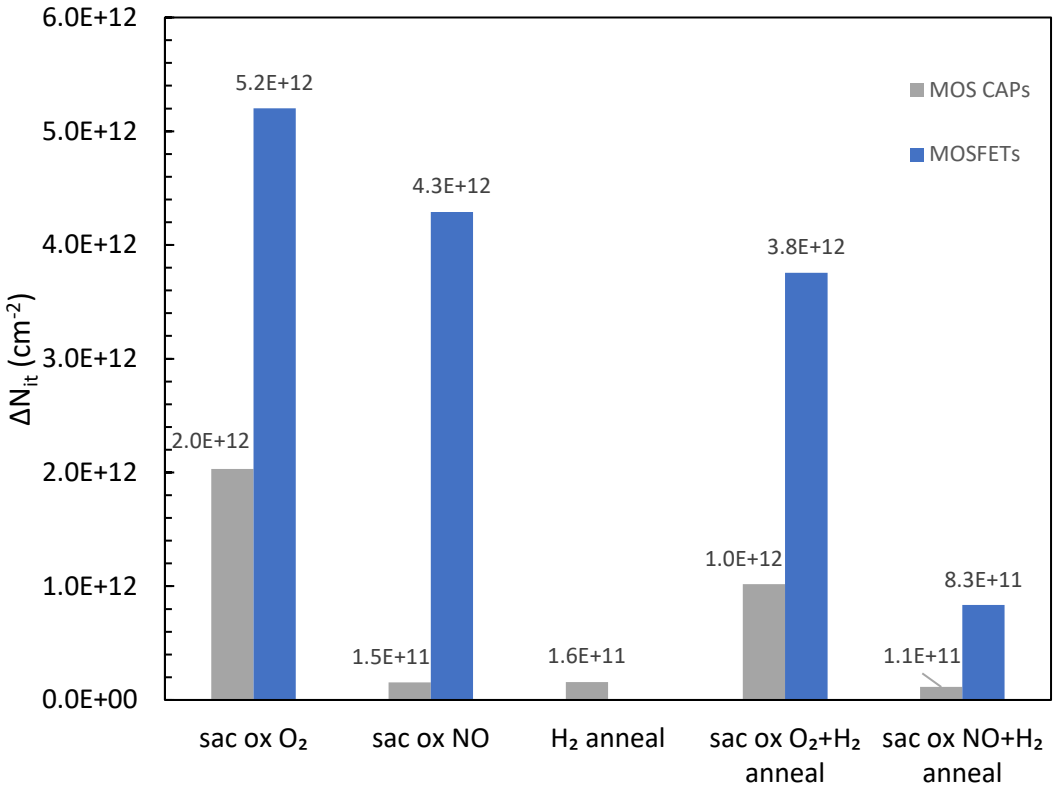

Figure 4.27: ΔN_{it} obtained from the Gray-Brown technique for Al_2O_3/4H-SiC MOSFETs and MOS capacitors fabricated under different surface treatments.

4.11. MOSFET Field-effect mobility versus interface trap densities relationship

Up to now in this chapter, we have discussed the Al_2O_3/4H-SiC MOS capacitors and MOSFETs fabricated with different surface treatments prior to ALD. Using capacitance-voltage measurements, interface trap densities, as well as effective charge densities in MOS capacitors, clear trap reductions were observed in the range of E_c-E~ 0.05 to 0.6 eV with the H_2 annealing as well as by incorporating nitrogen at the interface. In concurrence with this observation, we observed the highest channel mobility for the MOSFET prepared with the same surface treatment method.

By the Gray-Brown method, it was obvious that these surface treatments have resulted in passivating traps located closer to the conduction band edge of 4H-SiC, which have a significant

impact on channel conductance. Therefore, next we summarize the relationship between peak field-effect mobility measured at 298 K versus interface trap densities closer to the conduction band edge of 4H-SiC (ΔN_{it}), as in Figure 4.28. Here, peak μ_{FE} was extracted from lateral MOSFETs at room temperature and ΔN_{it} was obtained by Gray-Brown method (in range of E_c-E~0.05 to 0.2 eV) considering the threshold voltage shifts of MOSFETs. In the diagram, the blue dotted line is for the guidance for the eye only and does not have a physical meaning.

When ΔN_{it} obtained by Gray-Brown method was reduced either via H_2 annealing and/or sacrificial oxidation in NO, a channel conductance increase can be observed both at 298 K and 77 K. A distinct inversely proportional linear relationship between peak μ_{FE} vs N_{it} can be observed here for Al_2O_3/4H-SiC MOSFETs, according to our findings. This predicts that further reduction of Grey-Brown ΔN_{it} in Al_2O_3/4H-SiC MOS devices could result in better MOSFET channel mobility that is limited by a high density of ΔN_{it}. Here nitrided SiO_2/4H-SiC MOSFET mobility measured at 298 K and 77 K by Zheng et al. [33] and ΔN_{it} is included for reference purposes.

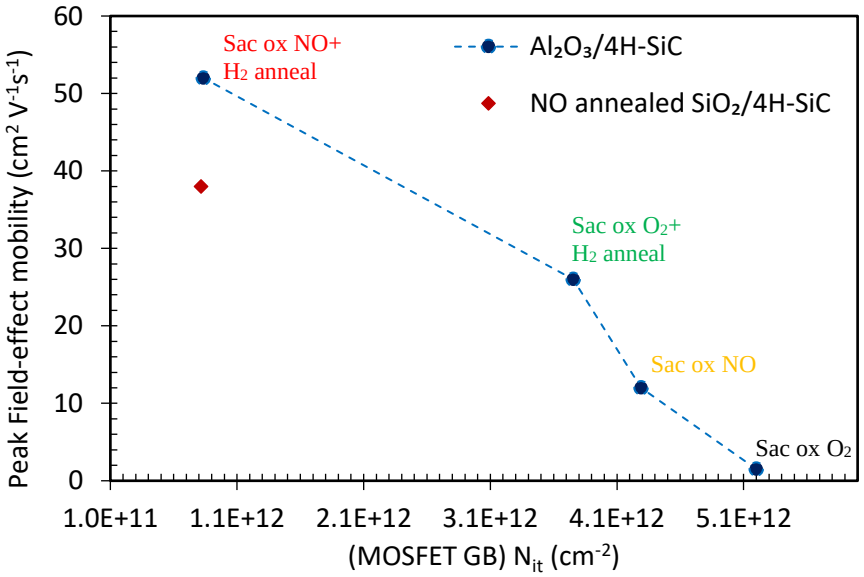

Figure 4.28: Peak field-effect mobility at 298 K as a function of ΔN_{it} for Al_2O_3/4H-SiC MOSFETs compared with 2 hr NO annealed SiO_2/4H-SiC MOSFET at different temperatures.

Previously, Rozen et al. [35] have proposed peak μ_{FE} as a function of D_{it} for nitrided SiO_2/4H-SiC and they have used n-channel lateral MOSFETs and MOS capacitors respectively to extract field-effect mobility μ_{FE} and D_{it} independently. They have concluded that channel mobility and D_{it} have an inverse relationship and assigned that D_{it} is responsible for the scattering mechanisms. According to our results, Al_2O_3/4H-SiC MOSFETs follows a similar trend in the relationship between peak μ_{FE} as a function of ΔN_{it}.

Another observation was the drop in peak channel mobilities of Al_2O_3/4H-SiC MOSFETs from 298 K to 77K was considerably higher compared to that of SiO_2/4H-SiC MOSFETs. The exact reason for this is unclear at the moment, but it is possible that the Al_2O_3/4H-SiC and SiO_2/4H-SiC interfaces related to scattering mechanisms resulted by scattering cross-sections/depth dependence or Coulomb potential screening of traps are different between the two of them.

4.12. Summary

In this chapter, the effect of 4H-SiC surface treatments prior to ALD of Al_2O_3 on Al_2O_3/4H-SiC MOS devices was investigated using electrical characterization methods. These surface treatments alter the 4H-SiC surface chemically, as shown in Figure 4.29. A clear correlation between surface preparation methods and resulting effective charge density, interface trap density, device stability, MOSFET field-effect mobility, and gate leakage currents were identified. A calibration curve for peak μ_{FE} and Grey-Brown N_{it} was proposed for Al_2O_3/4H-SiC MOS devices.

Among the studied surface treatments, H_2 annealing prior to ALD resulted in a lower interface density of traps energetically located near the conduction band edge of 4H-SiC. H_2 annealing results in a 4H-SiC substrate surface with uniform Si-H termination. These Si-H bonds can be easily converted into Si-OH bonds, which are the preferential surface bonding for ALD. This

results in uniform nucleation of ALD Al_2O_3 films and produces lower interface traps and improves oxide stability. Incorporation of nitrogen in the interface via sacrificial oxidation of SiC in NO results in further improvement of ALD Al_2O_3/4H-SiC MOS devices. This forms a sub-nm SiON layer on the SiC surface which was annealed in H_2 prior to Al_2O_3 deposition. Al_2O_3/4H-SiC MOSFETs fabricated with this process resulted in peak field-effect mobility of 52 cm^2/Vs, which has resulted in a 2x higher channel electron mobility compared to nitrided SiO_2/4H-SiC MOSFETs.

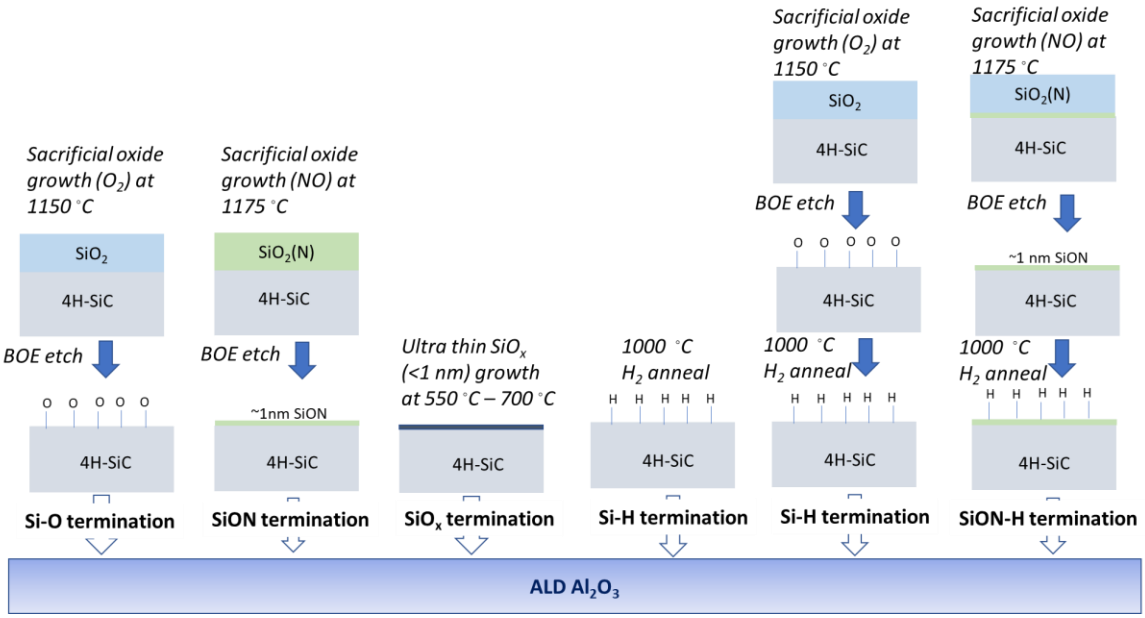

Figure 4.29: Studied 4H-SiC surface treatments prior to ALD Al_2O_3

The channel conduction is still limited by trapping, which suggests that further reduction of the D_{it} will lead to further improvements. At a low temperature, channel mobility reduction was observed for Al_2O_3/4H-SiC MOSFETs regardless of surface treatments; this is possibly due to trap limited or coulomb limited channel conductance. An inverse relationship was found between MOSFET peak channel mobility and Grey-Brown N_{it} for Al_2O_3/4H-SiC MOSFETs, both at room temperature and low temperature. However, the leakage currents associated with the Al_2O_3/4H-

SiC MOS devices remain the biggest challenge. In addition to that, exposing ALD Al_2O_3 to a high temperature above ~750 ˚C results in a phase change of Al_2O_3 from amorphous to crystalline phase, and this is a consideration to take into account during the MOSFET fabrication process.

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Chapter 5

Conclusions and Future work

5.1. Conclusions

4H-Silicon carbide is a promising wide band gap semiconductor, especially for the next generation high power, high-temperature device applications due to its outstanding material properties. Similar to Si, it has a native oxide SiO_2 which can be thermally grown to be used in MOS devices. Thermal oxidation of 4H-SiC introduces defects at the SiO_2/4H-SiC interface that yields high density of interface traps (D_{it}) which lowers the channel mobile carrier density and leads to a poor channel conductance. There are many trap passivation methods to overcome this challenge and among them, nitridation of the SiO_2/SiC interface is the most reliable method. But even with nitridation, channel mobility is much lower compared to SiC bulk electron mobility. Another approach to solve this issue is by replacing SiO_2 with alternative dielectrics. High-k dielectrics have added advantages over SiO_2 and among these, Al_2O_3 has shown promising results in the literature. In this work, a systematic study of 4H-SiC surface treatments was performed using Al_2O_3/4H-SiC MOS capacitors and MOSFETs to investigate the effect of 4H-SiC surface treatments on ALD Al_2O_3 MOS interface quality. The main findings of this work are summarized below:

- Using the CCDLTS technique, two signature near interface oxide traps named O1 and O2 can be detected for SiO_2/4H-SiC interfaces regardless of the trap passivation method, wafer orientation, and epitaxial layer concentration. ‘O1’ and ‘O2’ have emission activation energies of 0.15 ± 0.05 eV and 0.39 ± 0.1 eV below the 4H-SiC conduction band edge.

- The origin of these traps has been assigned in previous work to C-dimers on oxygen sites and Si- interstitials (Si_i) inside SiO_2 near the interface. In this work, it is shown that these traps are absent in Al_2O_3/4H-SiC MOS devices fabricated on H-terminated 4H-SiC surfaces. This presents very strong evidence that the O1 and O2 near interface oxide traps are inherent to the SiC/thermal SiO_2 interface and may play an important role in defining the MOSFET channel conductance. These experiments motivated the further study of surface treatments for ALD of Al_2O_3 on 4H-SiC and fabrication of Al_2O_3/4H-SiC MOSFETs to study channel electron mobility.
- Among the studied surface treatments, H_2 annealing prior to ALD yields lower interface trap density energetically located near the conduction band edge of 4H-SiC. The most likely reason for this is that H_2 annealing results in a 4H-SiC surface with uniform Si-H termination which can be easily converted to Si-OH bonds during ALD. This in turn leads to uniform nucleation of the Al_2O_3 films and produces lower interface traps and improves oxide stability.
- Incorporation of nitrogen at the interface causes further improvement of ALD Al_2O_3/4H-SiC MOS devices. Here, N was incorporated by performing sacrificial oxidation of SiC in nitric oxide (NO). This forms a sub-nm thick SiON layer on the SiC surface which was annealed in H_2 prior to Al_2O_3 deposition. Al_2O_3/4H-SiC MOSFETs fabricated with this process resulted in peak field-effect mobility of 52 cm^2/Vs which is 2x higher channel electron mobility compared to nitrided SiO_2/4H-SiC MOSFETs. The channel conduction is still limited by trapping which suggests that further reduction of the D_{it} will lead to better improvements.

- Insertion of ultra-thin oxide (~0.7 nm) between 4H-SiC and Al_2O_3 has been reported to improve MOSFET mobility in the literature. In contrary to these results, this work found that, the insertion of the ultra-thin oxide resulted in high D_{it} similar to an interface obtained by low-temperature thermal oxidation of 4H-SiC. This could be due to the difficulty in reproducing exact process conditions between different laboratories as well as the extremely tight SiO_2 thickness tolerance needed as suggested in the previous work.
- The channel mobility results in this work are very encouraging for the application of ALD Al_2O_3 on SiC from the point of view from channel conductance. However, the large leakage currents, most likely associated with defects in the bulk of the Al_2O_3 films were found to be the biggest challenge. In addition to that, exposing ALD Al_2O_3 to temperatures above ~750 ˚C results in a phase change of Al_2O_3 from amorphous to crystalline. This requires modified fabrication processes to be developed for practical MOSFET fabrication with Al_2O_3.

Overall, it can be concluded that 4H-SiC surface treatments are the key to MOS interface engineering for high channel conductance using deposited dielectrics. The Hydrogen and Nitrogen based surface treatments studied here could be used for other deposited dielectrics as well.

5.2. Future Work

4H-SiC MOS device performance improvements depend on rigorous research and understanding of the physics and engineering aspects of the related materials and devices. Considering the current need for improvements in microelectronics in high power and harsh environmental applications, SiC device improvements open up many possibilities. Considering the work presented in this thesis following future work is suggested.

- Studying the effect of ALD Al_2O_3 prepared under different conditions:

For improvement of gate dielectric leakage, it is worth investigating using other precursors such as Ozone during thermal ALD of Al_2O_3 and also optimizing the Al_2O_3 deposition temperature. Plasma ALD is another approach that has been reported to improve dielectric leakage. The H and N incorporated 4H-SiC surface developed in this work may also result in better channel mobility by plasma ALD.

- Hall mobility characterization of Al_2O_3/4H-SiC MOSFETs:

In this work, field-effect mobilities of MOSFET have been measured and discussed. But the dominating mobility limiting mechanisms for Al_2O_3/4H-SiC MOSFETs seems to be different compared to nitrided SiO_2 according to the results obtained. The scattering mechanisms and effect of surface treatments on free carrier concentrations can be investigated further through Hall mobility measurements.

- CCDLTS analysis of ALD Al_2O_3/4H-SiC MOS devices prepared under different surface treatments:

CCDLTS can be used to study trap types and their densities on Al_2O_3/4H-SiC MOS interfaces fabricated with different 4H-SiC surface treatments. This could help to understand the difference in each trap type associated with each surface and their contributions to channel mobility limitation. In addition, CCDLTS analysis could be used to understand the depth profile of the interface trap density distribution by changing the pulse voltage (V_p) during CCDDLTS measurements. However, relevant mathematical derivations need to be done before that.

- Investigating MOS interfaces prepared under different surface terminations with surface chemistry analysis methods and theoretical modeling:

FTIR, XPS, and EELS analysis can be used to understand the interface chemistry. Proposed 4H-SiC surface treatments in this work change the MOS interface chemistry and modeling this

interface with the incorporation of H and N would be extremely useful. The effect of N and H on the interface can be optimized through a systematic study to further improvements. Also, the effect of H_2 annealing on reducing O in the surface and investigating if Hydrogen stays or leaves from the interface after ALD are important facts to be investigated. Answering these questions would help understand the interface chemistry, defects and stress/strain in the interface.

- Application of 4H-SiC surface treatments with other dielectrics:

The 4H-SiC surface treatments were found to be the key behind the MOSFET channel conductance for deposited dielectrics. Thus, these surface treatments can be extended to other ALD based high-k dielectrics.

- Application of 4H-SiC surface treatments on other 4H-SiC wafer orientations and p-type 4H-SiC:

In this study (0001) Si-face n-4H-SiC surface was investigated to prepare differently surface terminated devices. But, imposing these treatments on other wafer orientations such as C- and a-face may yield improved channel mobilities as well as helping to understand atomistic surface chemistry to model the 4H-SiC/dielectric interface. Investigating the effects of 4H-SiC surface treatments on p-type MOS devices will open the opportunity for improving SiC CMOS technology using Al_2O_3

Appendix A: Sample cleaning

1. Label the backside of samples if necessary.
2. Use a cotton swab and acetone to remove the glue on the sample surface.
3. The next set of steps is to remove organic compounds on the sample surface. Place the sample in a sample holder.
    3.1. Place it in acetone beaker in the ultrasonic cleaner for 5 min
    3.2. Remove and place in trichloroethylene (TCE) beaker in the ultrasonic cleaner for 5 min.
    3.3. Remove and place in acetone beaker in the ultrasonic cleaner for 5 min.
    3.4. Remove and place in methanol beaker in the ultrasonic cleaner for 5 min.
    3.5. Remove and place in methanol beaker in the ultrasonic cleaner for 5 min.
    3.6. Remove and place in deionized water (DI water) beaker in the ultrasonic cleaner for 5 min.
    3.7. Remove and place in buffered oxide etch (BOE) for 5 min
    3.8. Remove and place in deionized water (DI water) beaker in the ultrasonic cleaner for 5 min.
4. To remove inorganic compounds of the sample surface
    4.1. Mix H_2SO_4:H_2O_2 (1:1) and place sample in the solution for 15 min. (warning: the reaction is exothermic)
    4.2. Rinse sample in DI water for 30 seconds, then place the sample in BOE for 1min. Rinse sample in DI water 30 seconds.
    4.3. Mix DI water: H_2O_2:NH_4OH (3:1:1) and heat sample to 100-115°C for 15 min.
    4.4. Rinse sample in DI water for 30 seconds, then place the sample in BOE for 1min. Rinse sample in DI water 30 seconds

4.5. Mix DI water: H_2O_2: HCl (3:1:1) and heat sample to 100-115°C for 15 min.

4.6. Rinse sample in DI water for 30 seconds, then place the sample in BOE for 1min. Rinse sample in DI water 30 seconds

5. Rinse sample and dry with N_2 air.

Appendix B: Thermal Oxidation and NO annealing

1. Vacuum oxidation furnace tube until base pressure is less than 1 torr.
2. Flush oxidation furnace tube with 500 sccm argon for 15 min to remove residual gases.
3. Load samples into the oxidation furnace tube.
4. Vacuum oxidation furnace tube for 10-15 min.
5. When pressure is less than 1 torr, fill and flush with argon for 10-15 min.
6. Set oxidation furnace temperature to 1150°C and the ramp rate to 5 °C/min.
7. When the temperature is at 1150 °C, stop argon flow and begin oxygen flow at 500 sccm.
8. Record the start time.
9. Let oxidation run for the desired time.
10. Record the finish time.
11. Stop oxygen flow and flow argon for 30 min.

Steps 12-18 are for NO passivation. If no NO passivation necessary, skip to step 19.

12. Increase temperature to 1175 °C.
13. Flow 500 sccm argon through NO lines.
14. Begin NO flow and turn off argon flow.
15. Set NO regulator to 15 psi. and flow NO at 575 sccm and anneal for 2 hrs.
16. After annealing is finished close the NO bottle cap and let NO pressure drop to zero.
17. Open argon and flush NO lines with argon
18. Set oxidation furnace temperature ramp rate to 10 °C/min and ramp temperature down to oxidation furnace base temperature.
19. Ground yourself and remove samples from the oxidation furnace tube.
20. Vacuum the furnace tube and fill it with Ar.

Appendix C: Photolithography

1. Ground yourself if the sample has gate oxide.
2. Clean Si wafer (use H_2O_2 to remove metals or organic cleaning) and dry with N_2 gas.
3. Get a small amount of 5214 photoresist using a pipet tip and attach the sample in the middle of Si wafer. Attach extra edge pieces to avoid edge beads especially for MOSFETs.
4. Bake in an oven at 105 °C for 15 min.
5. Expose to HMDS vapor for 10 min.
6. Turn on the spinner, vacuum switch and open N_2 gas valve.
7. Place the Si wafer on spinner and center the sample. (by checking at 1000 rpm trial rotation)
8. Use a new pipet tip to get the desired photoresist depending on the mask type and cover the sample avoiding creating air bubbles.
9. Select the proper rotation speed and time (5000 rpm for NLOF 2070(positive) or 4000 rpm for 5214(negative) – 30 sec)
10. Run spinner with the selected program.
11. Soft bake at 105 °C (90 sec for NLOF 2070 or 60 sec for 5214) and remove edge pieces.
12. Turn on MJB3 Karl Suss mask aligner and open N_2 gas.
13. Get the relevant mask and align patterns of the sample while checking under the microscope.
14. Set UV exposure time depending on the photoresist. (1 min for NLOF 2070 or 30 sec for 5214) and expose the sample.
15. Do a second soft bake at 105 °C for 90 sec only if NLOF 2070 was used.
16. Develop the exposed sample using AZ 726 MIF for 40 sec and wash with running DI water.
17. Dry with N_2 and check under the microscope for visibility of sharp pattern lines.

Appendix D: DC Sputtering

1. Open sputter chamber
   1.1. Turn off the vacuum.
   1.2. Close gate valve
   1.3. Open N_2 and air inlet to fill in the chamber until pressure increase up to atmospheric pressure.
   1.4. Close N_2 when the chamber jumps up
   1.5. Open the chamber and change the sputter target as necessary.
2. Place sample facing downward (ground yourself if the sample has oxide).
3. Close chamber manually by lifting it down.
4. Pump out air from the chamber
   4.1. Close for-line
   4.2. Open the roughing pump slowly and wait until the pressure gets down to 30 mtorr.
   4.3. Close roughing pump.
   4.4. open fore-line.
   4.5. Slowly open the high vacuum valve (gate valve) without letting pressure exceeding 100 mtorr.
   4.6. Turn on vacuum
5. Let chamber pressure reduce until ~ 3×10^{-7} torr (usually take about 6 hours)
6. Sputtering
   6.1. Close the high turbopump partial valve.
   6.2. Open Ar (95 sccm, 17 mtorr) and wait until turbopump power settles down.
   6.3. Check power line for target and cooling water is open.

6.4. Focus dummy sample on target

6.5. Turn on the power and slowly increase voltage for plasma ignition.

6.6. Once the plasma is on maintain the fixed current (depending on the sputter target) by adjusting the voltage knob.

6.7. Pre-sputter for 2 min and rotate the sample focusing target

6.8. Sputter the sample to obtain the desired film thickness by changing sputter time.

6.9. Turn down voltage and power off, close Ar, wait until pressure drops and open turbopump partial valve.

7. Open the sputter chamber following step 1.
8. Take samples out while wearing grounding wire.
9. Close chamber and pump out the air from chamber following step 4 for steady-state of the system.

Appendix E: Al evaporation

1. Open sample chamber
    1.1. Turn off the ion gauge.
    1.2. Close the high vacuum (gate valve) and check if the roughing pump and fore-line are closed.
    1.3. Open N_2 and air inlet to fill in the chamber until pressure increase up to atmospheric pressure and chamber jump up.
    1.4. Close N_2 and air inlet.
    1.5. Open the chamber manually.
2. load Al pellets (number of pellets used depend on the desired metal thickness) into the bridge holder.
3. Place sample facing downward (ground yourself if the sample has oxide). If lithography was not done on samples use the shadow mask for gate patterning.
4. Close chamber manually by lifting it down.
5. Pump out air from the chamber.
    5.1. Close fore-line while holding the chamber closed.
    5.2. Open the roughing pump slowly and wait until the pressure gets down to 30 mtorr.
    5.3. Close the roughing pump
    5.4. Open fore-line
    5.5. Open high- vacuum slowly without letting pressure rise more than 100 mtorr.
    5.6. Turn on ion-gauge
    5.7. Wait until the pressure drops ~1×10^{-7} torr. (usually about 6 hrs)
6. Evaporation

6.1. Turn on the filament, voltmeter and ammeter.

6.2. Turn on AC power (60%) and pre evaporate Al for 20 sec.

6.3. Remove the cover plate and expose samples for 4 min.

6.4. Turn off AC power.

7. Open chamber following step 1.
8. Take samples out and close chamber.
9. Pump out chamber following step 5.

Appendix F: Reactive Ion etching (RIE)

1. After the suitable photolithography, attach the sample to clean 2-inch Si wafer.
2. Open glass window to etcher.
3. Place wafer on electrode and try to center the sample.
4. Close the glass window and tighten until snug
5. Open nitrogen for 1 min and check air flow from the chamber to outside.
6. Vacuum system for 30 min until system reaches the base pressure10 mtorr. (before the first etch, pump out the gas lines too)
7. Open all gas line valves and turn on the appropriate switches on the flow controller.
8. Flush the gas line for 5 min and become stable.
9. Turn on RF power supply.
10. Adjust power setting about 3 W higher than the desired power.
11. Turn ON power and start timing.
12. If necessary, adjust power to appropriate level and adjust matching network to obtain the lowest possible reflected power
13. After desired etch time, turn off power.
14. Turn off the etchant gas and allow system to vacuum to base pressure.
15. Fill chamber with nitrogen for 1 minute and vacuum again. Repeat this step at least two times. (etch gases are toxic gases)
16. Close vacuum valve and fill chamber with nitrogen to get to atmospheric pressure.
17. Open the chamber and remove the wafer with the sample.
18. If no other etching is required, close all valves and turn off system and vacuum pump.
19. Fill chamber with nitrogen for 1 minute. Close all the gas tanks and turn off the

Appendix G: Ohmic contact anneal

1. Flow argon (10-12 L/min) through ohmic anneal finance tube until atmospheric pressure is reached.
2. Reduce Ar flow rate to 4 L/min
3. Open loading area and load samples and close the loading area (ground yourself)
4. Move the sample paddle close to the tube entrance.
5. Flush ohmic anneal system with Ar flow rate to 12 L/min for 5 min
6. Stop argon flow and pump out ohmic anneal furnace tube until 10^{-7} torr. At the same time let temperature reach 800 ˚C (take about 1 hr)
7. Stop vacuuming and flush system with argon for 5 min at 12 L/min
8. Reduce Ar flow rate to 4 L/min
9. Insert sample paddle completely into the furnace and start timing for 30 seconds once sample temperature reaches 800 ˚C.
10. After 30 s annealing is finished, transfer samples from furnace to loading area stepwise
11. Close Ar completely and remove samples from system (ground yourself)
12. Take relevant steps to return the ohmic anneal system to standby mode.